Letters

Low-Cost HVdc Circuit Breaker With High Current Breaking Capability Based on IGCTs

Qiang Yi, Yifei Wu, *Member, IEEE*, Zhihui Zhang, Fei Yang, *Senior Member, IEEE*, Yi Wu, *Senior Member, IEEE*, Chong Gao, Chunping Niu, *Member, IEEE*, and Mingzhe Rong, *Senior Member, IEEE*

***Abstract*—DC circuit breaker plays an important role in the reliability of HVdc system, but the large number of expensive press-pack insulated-gate bipolar transistors (IGBTs) is used at present, which is a serious impediment to HVdc development. Thus, the low-price integrated gate commutated thyristor (IGCT) becomes a promising alternative device. This letter presents a low-cost HVdc circuit breaker with high current breaking capability based on IGCTs. The topology and principle of the proposed HVdc circuit breaker are introduced at first. Then, the parameter design is analyzed. A scaled-down test successfully demonstrates the high current breaking capability of 15 kA. In the end, the cost comparison shows that this scheme can achieve 61.8% cost reduction of the commutation branch.**

***Index Terms*—DC circuit breaker, integrated gate commutated thyristor (IGCT).**

I. Introduction

DC GRIDS provide many advantages over ac systems due to the low transmission losses, no phase or frequency control, thus becoming a research hotspot [1]. However, dc fault current rises very quickly because of the small system impedance; thus, the dc fault current clearance remains a tough problem and dc circuit breakers are indispensable to achieve dc grid protection [2].

In 2011, ABB proposed the hybrid dc circuit breaker [3]. It contains two branches: The main branch composed of the ultra-fast disconnector (UFD) and load commutated switch (LCS), commutation branch made up of series main breakers (MBs), which integrates the advantages of low conduction losses, arcless interruption, and fast current breaking [4]. Hence, the hybrid scheme becomes a promising solution. In the normal operation, the main branch carries all the nominal current. When breaking fault currents, LCS turns OFF at first, and the fault current commutates to the commutation branch. When the current commutation is completed, UFD is controlled to open without arc and MBs are turned OFF to achieve the current interruption afterward.

To achieve fault current interruption of MBs, press-pack insulated gate bipolar transistors (IGBTs) are usually used due to their advantages such as high voltage, large capacity, short-circuit failure mode, and series-connected redundancy. However, IGBTs are very expensive, leading to high cost of circuit breaker, especially in HVdc applications. Therefore, many researchers are seeking for cheap alternative power devices. In recent years, integrated gate commutated thyristors (IGCTs) have been increasingly applied in dc circuit breakers, as IGCT only costs about half as much as IGBT, and it has high surge withstand capability and gate driver reliability [5]. In [6] and [7], various dc circuit breakers based on IGCTs are developed, but the current breaking ability is very low due to which IGCT has low controllable cutoff ability (I_{cutoff}). The authors in [8] propose a circuit breaker with high current breaking capability using IGCTs, but expensive IGBTs are still not avoided. In summary, it seems to be very hard to realize both cost-efficiency and high current breaking ability by using IGCTs.

To solve the problems above, this letter proposes a low-cost HVdc circuit breaker using IGCT. It has the advantages of low cost, high current breaking, and surge capability. Section II introduces the principles and operation. In Section III, the parameter design regarding current commutation and interruption is analyzed. In section IV, a scaled-down test is successfully carried out, verifying the effectiveness. In section V, the cost comparisons and application discussions are made. Finally, Section V concludes the letter.

II. Fundamental Principle

A. Configuration

Fig. 1 shows the configuration of the proposed HVdc circuit breaker based on IGCTs. Es, Rs, and Ls are the system source, resistance, and inductance, respectively. It consists of

Manuscript received July 21, 2020; revised August 23, 2020 and September 23, 2020; accepted October 6, 2020. Date of publication October 13, 2020; date of current version January 22, 2021. This work was supported in part by the National Key R&D Program of China under Grant 2018YFB0904700, in part by the National Natural Science Foundation of China under Grant 51707145 and Grant U1966602, and in part by the Shaanxi Province "Sanqin Scholar" Innovation Team Project (Innovation team of Xi'an Jiaotong University for the key technology of advance DC power equipment and its industrialization). *(Corresponding authors: Yifei Wu; Fei Yang; Mingzhe Rong.)*

The authors are with the Xi'an Jiaotong University, Xi'an 710049, China (e-mail: angeloyq@qq.com; yifei208@xjtu.edu.cn; zhang-zhihui@foxmail.com; yfei2007@mail.xjtu.edu.cn; wuyic51@mail.xjtu.edu.cn; gaochong_1995@qq.com; niuyue@xjtu.edu.cn; mzrong@xjtu.edu.cn).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3030255

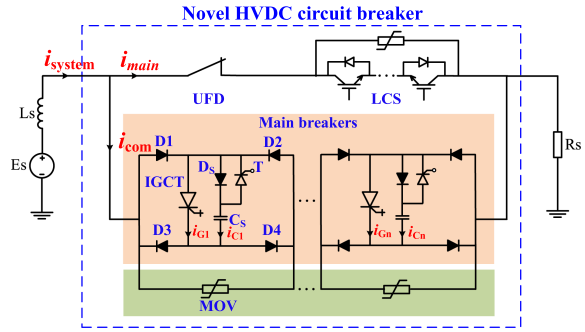

Fig. 1. Configuration of the novel hybrid dc circuit breaker.

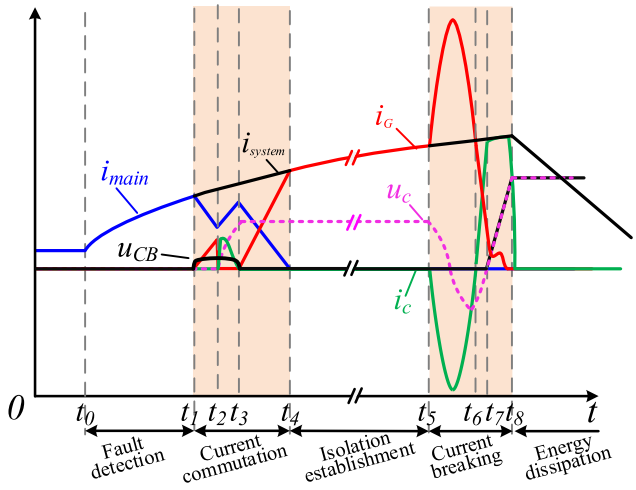

Fig. 2. The schematic waveforms of proposed HVdc circuit breaker.

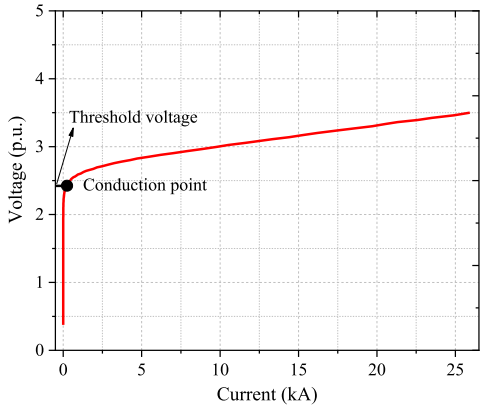

Fig. 3. Typical V-I characteristics of MOV.

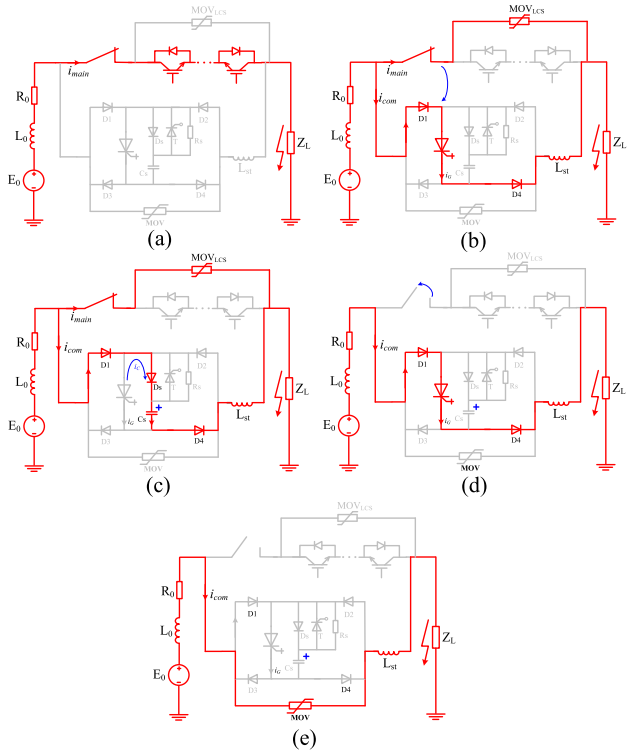

Fig. 4. Equivalent circuits of the proposed hybrid dc circuit breaker during (a)–(d) current commutation and (e) energy dissipation.

two branches: the main branch and the commutation branch. The number of parallel and series connected power devices in LCS is small and acceptable compared with commutation branch; therefore, the main branch is the same as the traditional dc circuit breaker in [3]. The commutation branch is composed of MBs in series, which are quite different from the traditional hybrid dc circuit breaker. The MB is an IGCT-based diode-bridge, and paralleled with the metal oxide varistor (MOV). A novel snubber circuit is paralleled to the IGCT, which contains snubber diode (D_S) and capacitor (C_S), and thyristor T.

Remarkably, the capacitor (C_S) has two purposes in the dc circuit breaker: 1) to construct a snubber circuit during IGCT's switch-OFF to help lower down the turn-OFF du/dt and suppress voltage spikes; 2) to store energy during current commutation process and discharge oscillating current to achieve high current breaking capability.

B. Principle and Transient Analysis

Fig. 2 presents the schematic current breaking waveforms, which can be divided into four stages. The i_{system}, i_{main}, i_G and i_C are system current, the current in the LCS, IGCT, and C_S, respectively. u_C is the voltage across C_S. Fig. 4 presents the equivalent circuits during current commutation. In normal operation, all the system current flows through the UFD and LCS. When a short-circuit occurs, the fault current breaking processes are as follows.

Stage 1. Current Commutation: At t_1, LCS turns OFF and IGCT turns ON. Then, the fault current starts commutating from main branch to IGCT [Fig. 4(b)]. Note that the LCS voltage (u_{LCS}) is equal to the voltage across MOV_{LCS} paralleled with LCS, which is a highly voltage-sensitive resistor. After LCS is turned OFF and the voltage over MOV_{LCS} exceeds the threshold value, MOV_{LCS} becomes conductive. The typical volt-ampere characteristics curve of MOV_{LCS} is shown in Fig. 3, which is very flat after conduction, indicating that u_{LCS} is basically constant during the current commutation process.

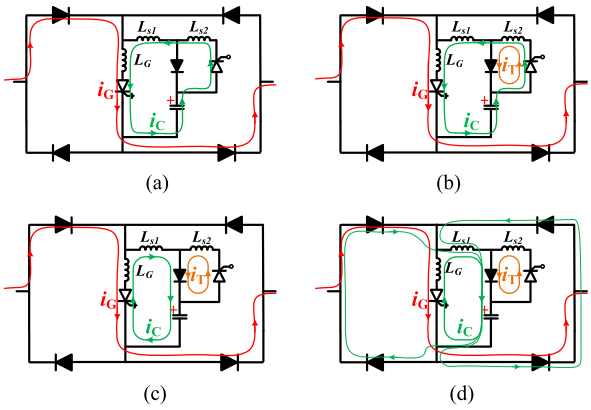

Fig. 5. Detailed current paths during the snubber oscillation.(a) Oscillation starts. (b) Thyristor freewheeling. (c) Current conteract. (d) Diode freewheeling.

Therefore, considering that the initial current in IGCT before current commutation is zero, the cutoff current during current commutation process at t_2 can be determined by

$$I_{t_2} = \frac{di_{\mathrm{G}}}{dt} \cdot (t_2 - t_1) = \frac{u_{\mathrm{LCS}}}{L_{\mathrm{st}}} \cdot (t_2 - t_1). \tag{1}$$

At t_2, the IGCT is turned OFF. The time duration between t_2 and t_3 is determined on the criteria that IGCT blocks before its maximum cutoff current and is calculated using (1). Then, the current in the commutation branch all flows through C_{S} [Fig. 4(c)], which can also be expressed by the product of capacitance and the voltage changing rate as shown in (2). By taking the left port of the dc circuit breaker as the reference node, the voltage across C_{S} can be obtained by solving (3). At t_3, IGCT turns ON again. Then, the current commutation continues and finishes at t_4 [Fig. 4(d)] as follows:

$$i_{\mathrm{com}} = C_{\mathrm{s}} \frac{du_{\mathrm{c}}}{dt} \tag{2}$$

$$u_{\mathrm{c}} + L_{\mathrm{st}} \frac{di_{\mathrm{com}}}{dt} = u_{\mathrm{LCS}} \tag{3}$$

wherein i_{com} is the commutation branch current, L_{st} is the stray inductance of the current commutation loop, and u_{IGCT} is the voltage across IGCT. The initial conditions of the voltage across C_{S} (u_{c}) are: $u_{\mathrm{c}}(0) = 0$ and $C_{\mathrm{s}} u_{\mathrm{c}}{}'(0) = I_{\mathrm{cutoff}}$. By solving the equations, we can obtain (4) as follows:

$$u_{\mathrm{c}} = u_{\mathrm{LCS}} \left(1 - \cos \frac{t}{\sqrt{C_{\mathrm{s}} L_{\mathrm{st}}}}\right) + I_{\mathrm{cutoff}} \sqrt{\frac{L_{\mathrm{st}}}{C_{\mathrm{s}}}} \left(1 + \sin \frac{t}{\sqrt{C_{\mathrm{s}} L_{\mathrm{st}}}}\right). \tag{4}$$

Stage 2. Isolation Establishment: Thus, UFD can open without arc and the insulation strength is built up from t_4 to t_5. The fault current flows through IGCT.

Stage 3. Current Interruption: The detailed current paths of snubber oscillation process are depicted in Fig. 5, including two major stray inductors: L_{S1} and L_{S2}, which are the stray inductance of IGCT-D_S-C_S loop and the connection line of the thyristor, respectively.

1) The thyristor T is triggered and C_{S} begins to discharge, and the discharging current has the same polarity with i_G, which refers to the waveforms before the peak of i_{G} in Fig. 2 during t_5–t_6.
2) D_S becomes forward biased as the oscillating current falls, leading to L_{S2} freewheeling through D_{S}, which refers to the waveforms after the peak of i_{G} in Fig. 2 during t_5–t_6. This indicates that part of the energy released by capacitor will not return.
3) The discharging current polarity is reversed, and IGCT current is thus commutated to *Ds*. This is the detailed process of period during t_6–t_7.
4) As the current flowing through IGCT keeps decreasing, the reverse bridge-diode conducts due to the stray inductance voltage. Hence, part of the oscillating current is bypassed, which can avoid reverse voltage across IGCT when the oscillating current exceeds the fault current too much, for example, in small current breaking.

Considering the device conduction loss and current bypass, the forward ($i_{c\_\max 1}$) and reverse ($i_{c\_\max 2}$) maximum value of i_{C} in the first oscillation period can be expressed by (5) and (6), where Q_{C} is the energy stored in the snubber capacitor. And, (7) and (8) express the maximum and minimum current in IGCT, which must be smaller than the surge capacity (I_{surge}) and the cutoff ability (I_{cutoff}) of IGCT, respectively. Therefore, the upper and lower limit of the stray inductance can be derived as shown in (9)

$$Q_{\mathrm{C}} \geq \frac{1}{2} (L_{\mathrm{s1}} + L_{\mathrm{s2}}) i^2_{\mathrm{C\_max1}} \tag{5}$$

$$\frac{L_{\mathrm{s1}}}{L_{\mathrm{s1}} + L_{\mathrm{s2}}} Q_{\mathrm{C}} \geq \frac{1}{2} L_{\mathrm{s1}} i^2_{\mathrm{C\_max2}} \tag{6}$$

$$i_{\mathrm{G\_max}} = I_0 + i_{\mathrm{C\_max1}} \leq I_0 + \sqrt{\frac{2Q_{\mathrm{C}}}{L_{\mathrm{s1}} + L_{\mathrm{s2}}}} \leq I_{\mathrm{surge}} \tag{7}$$

$$I_{\mathrm{cutoff}} \geq i_{\mathrm{G\_min}} = I_0 - i_{\mathrm{C\_max2}} \geq I_0 - \sqrt{\frac{2Q_{\mathrm{C}}}{L_{\mathrm{s1}} + L_{\mathrm{s2}}}} \tag{8}$$

$$\frac{2Q_{\mathrm{C}}}{(I_{\mathrm{surge}} - I_0)^2} < L_{s1} + L_{s2} < \frac{2Q_{\mathrm{C}}}{(I_0 - I_{\mathrm{cutof}f})^2}. \tag{9}$$

At t_7, IGCT is turned OFF within cutoff ability. Then, all the current flows though C_{S}, and MOV gets conducted when u_{C} exceeds MOV's threshold voltage. Remarkably, the interval (t_6–t_7) is fixed because the oscillation is only determined by C_{s} and stray inductance, independent of current amplitudes.

Stage 4. Energy Dissipation: Finally, all the current flows through MOV as shown in Fig. 4(e) and the whole current breaking is complete when the current in MOV drops to zero.

III. Parameter Design

The most important issue in parameter design is to ensure that the energy stored in snubber capacitor can generate sufficient snubber oscillation during the current interruption. A 500 kV/15 kA HVdc circuit breaker simulation model is built up and the simulated waveforms are shown in Fig. 6. The typical

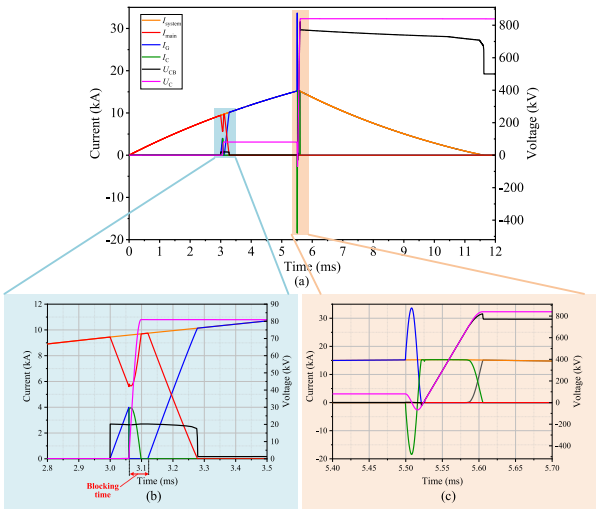

Fig. 6. Simulated breaking waveforms of the proposed HVdc circuit breaker. (a) Whole waveforms. (b) Current commutation. (c) Current interruption.

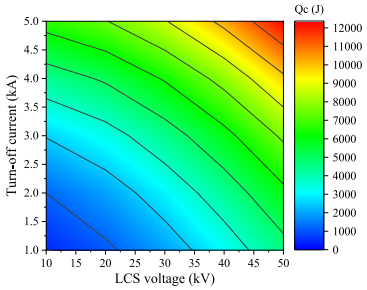

Fig. 7. Simulation results of Q_{C} under different LCS voltages and IGCT cutoff current.

values of the current commutation loop inductance and u_{LCS} are 0.3 mH and 20 kV, respectively [9].

A. Current Commutation Process

According to (4), the snubber charging process is determined by u_{LCS}, L_{st}, Cs, and blocking time of IGCT. First of all, the simulations result of Q_{C} under different values of u_{LCS} and L_{st} are presented in Fig. 7. As seen from the figure, Q_{C} increases greatly with both parameters, and we continue to use the typical values of the existing HVdc circuit breaker to maximize the technical adaptability.

Then, the simulations of Q_{C} under different Cs and blocking time are carried out and the relationship is presented in Fig. 8. The blocking time and capacitance C_{S} have different effects on the energy stored in C_{S}. An optimal matching curve between C_{S} and blocking time can be drawn, from which the maximum energy can be obtained with minimum C_{S} and blocking time. According to this curve, as long as Q_{C} is determined, the capacitance can be selected.

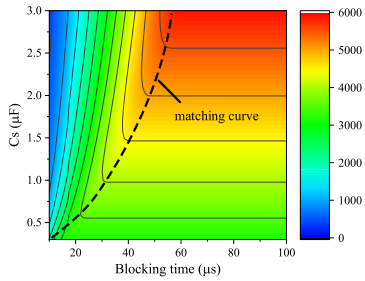

Fig. 8. Simulation results of Q_{C} under different snubber capacitances and blocking time.

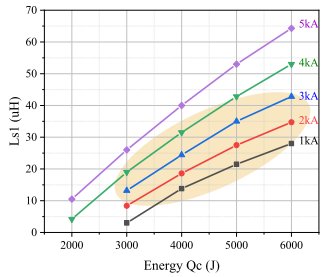

Fig. 9. Lowest IGCT currents during the snubber oscillation under different Q_{C} and LS1.

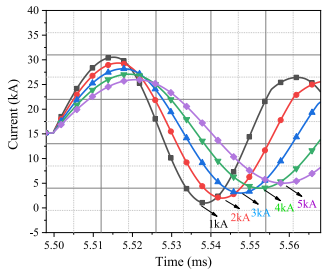

Fig. 10. Simulated IGCT currents during the snubber oscillation under different LS1corresponding to Fig. 9 (4500 J).

B. Current Interruption Process

When Q_{C} in the capacitor discharges during the current interruption process, the stray inductance is significantly important to the oscillation. Since D_{S} and T are tightly connected, L_{S2} is treated as unchanged. Fig. 9 shows the lowest IGCT current under different stray inductance (L_{S1}) and Q_{C} when the dc circuit breaker interrupts 15 kA. Considering IGCT cutoff stress and difficulty in structural design, a preferred parameter selection area is marked.

To achieve 15 kA current breaking, as seen from Fig. 9, $Q_{\mathrm{C}} = 4500$ J is suitable because it can meet a large range of stray inductance (15–35 uH), and also ensure reliable turn-OFF of IGCT ($\leq$4 kA). Then, the minimum capacitance for the energy of 4500 J on the optimal matching curve is 1.33 μF. The IGCT current waveforms during current interruption under different stray inductances are simulated as shown in Fig. 10.

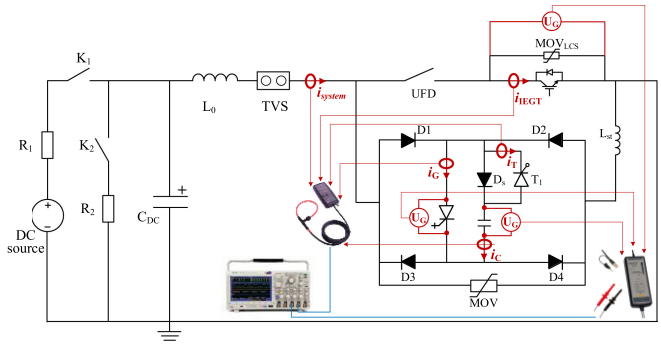

Fig. 11. Test circuit of the current breaking experiment.

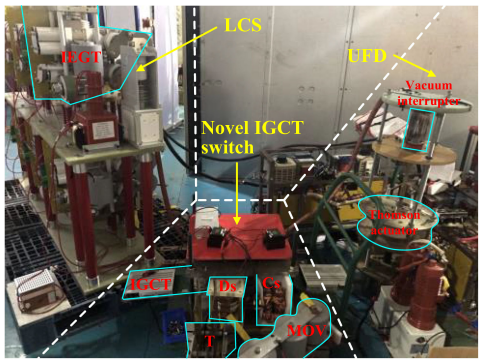

Fig. 12. Test setup of the proposed dc circuit breaker.

TABLE I
TEST PARAMETERS

parameters	Simulation (500 kV)	Experiment
L_{st}	300 μH	10 μH
U_{LCS}	20 kV	0.7 kV
Equivalent C_S	1.33 μF	40 μF

IV. EXPERIMENTAL RESULTS

A. Experiment Test

A scaled-down test is designed as presented in Fig. 11, and the test platform is shown in Fig. 12. C_{dc} and L_0 construct a current source to simulate the fault current. Before the test, K_1 is closed and C_{dc} is charged to a certain value by the dc source. To start the test, triggered vacuum switch (TVS) is triggered to conduct the circuit and the simulated fault current generates. The test parameters of the dc circuit breaker are listed in Table I. The specification models of IGCT, thyristor, and diode are CA_C 4000-45 [9], KKC 3500-60 [10], and FY_B 2000-45 [11], respectively.

The rated voltage and current of the power devices are 4.5 kV/4 kA, 6 kV/3.5 kA, and 4.5 kV/2 kA, respectively. Especially, IGCT's maximum turn-OFF ability is 5 kA, and its surge ability provided by the manufacturer is a sine current wave with 35 kA peak and 10 ms half-cycle. The LCS is designed using single injection-enhanced gate transistor (IEGT, ST3000GXH24A) [12]. The conduction and residual voltages of MOV is 2.8 and 4 kV. The currents and voltages are measured by PEM-CWT 300 and TESTEC 9010, respectively.

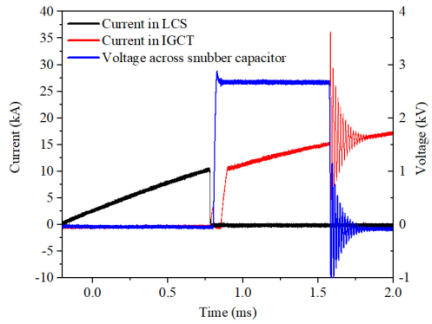

Fig. 13. Test waveforms of current commutation and snubber oscillation.

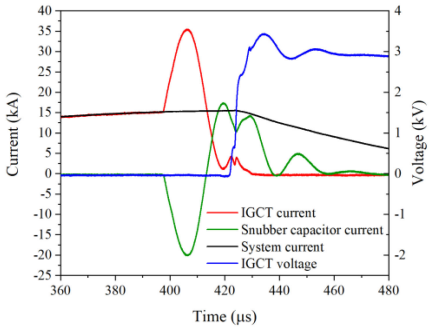

Fig. 14. Waveforms of the final current breaking.

TABLE II
COST PERFORMANCE COMPARISON

Field		Ref [13]	Ref [14]	Proposed scheme
Breaking current		25 kA	15 kA	15/25 kA[1]
Series MBs		350	350	350
MB	**Power Device**	IGBT×2 Diode×5	IGBT×4	IGCT×1/Diode×5/ Thyristor×1
		100,000	160,000	39,000
	Gate Driver [2]	driver×2	driver×4	thyristor trigger×1
		10,000	20,000	3,000
Total cost		38,500,000	63,000,000	14,700,000

[1]As demonstrated, the proposed breaker can break 15 kA, and the current breaking capability can reach over 25 kA with certain structural improvement.
[2]The gate drivers of [13] and [14] are the drivers of IGBTs. The gate driver for the proposed scheme is the thyristor trigger, since the gate of IGCT is integrated and included in the cost of IGCT device.

B. Test Results

The test is carried out by two steps. First, the current commutation test is carried out. As shown in Fig. 13, LCS is turned OFF at 10 kA, and when the current in IGCT rises to 3.6 kA, IGCT is turned OFF and maintain blocking state for 60 μs, which charges the snubber capacitor to 2.7 kV. When i_G reaches 15 kA, T is triggered ON. A high frequency oscillation occurs, and the lowest IGCT current arrives at around 1.5 kA.

When the first step succeeds, the whole current breaking is tested. According to the test waveforms, the oscillation period is 32 μs, and the stray inductance ($L_{S1} + L_{S2}$) is calculated to be 0.649 μH, which matches the stray inductance calculation in Section II. As shown in Fig. 14, IGCT is successfully turned OFF at 3.97 kA, and the system current of 15 kA begins to drop, which means the success of current breaking.

V. Application Discussions

This letter shows a 15-kA breaking demonstration. In fact, many measures can improve the breaking capability, such as increasing the LCS voltage. Besides, laboratory tests prove that IGCT can withstand over 60 kA under such pulse; hence, for the future improvement, laminated busbar will be used to reduce the stray inductance and further increase the breaking capacity.

The cost comparisons are made between the proposed and the existing schemes under the 500 kV as presented in Table II (the currency is Chinese Yuan). The cost of the proposed scheme is greatly reduced, which attributes to the price of IGCT. To be specific, compared with the scheme in [13] and the scheme in [14] based on press-pack IGBTs, the cost is reduced by 61.8% and 76.7%, respectively. It should be pointed out that the power supply for the proposed HVdc circuit breaker would be higher than conventional IGBT schemes because the current-controlled IGCT consumes more power than the voltage-controlled IGBT.

VI. Conclusion

This letter presents a novel low-cost HVdc circuit breaker with high current breaking capability based on IGCTs. Detailed current breaking process and parameter design are analyzed. A scaled-down experimental test successfully proves the effectiveness of the proposed scheme. This HVdc circuit breaker has the following advantages.

1) Hybrid dc circuit breaker is technically mature, and the new control is independent of current and reliable.
2) The current breaking capability based on IGCT is up to 15 kA and can reach even higher with integrated structural design.
3) The current commutation branch cost is reduced by 61.8%.

References

[1] Y. Wang, W. Wen, C. Wang, H. Liu, X. Zhan, and X. Xiao, "Adaptive voltage droop method of multiterminal VSC-HVDC systems for DC voltage deviation and power sharing," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 169–176, Feb. 2019.

[2] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[3] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.

[4] W. Wen, Y. Huang, Y. Sun, J. Wu, M. Al-Dweikat, and W. Liu, "Research on current commutation measures for hybrid DC circuit breakers," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1456–1463, Aug. 2016.

[5] B. Zhao *et al.*, "A more prospective look at IGCT: Uncovering a promising choice for dc grids," *IEEE Ind. Electron. Mag.*, vol. 12, no. 3, pp. 6–18, Sep. 2018.

[6] Q. Lu *et al.*, "Design and analysis of a 375V/5kA solid state DC circuit breaker based on IGCT," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–5.

[7] J. Meyer and A. Rufer, "A DC hybrid circuit breaker with ultra-fast contact opening and integrated gate-commutated thyristors (IGCTs)," *IEEE Trans. Power Del.*, vol. 21, no. 2, pp. 646–651, Apr. 2006.

[8] X. Zhang *et al.*, "A novel mixture solid-state switch based on IGCT with high capacity and IGBT with high turn-off ability for hybrid DC breakers," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4485–4495, Jun. 2020.

[9] "Asymmetric IGCT Device: CAC 4000-45-02" in *CRRC Group*, Zhuzhou, China: Product Datasheet, Nov. 2016.

[10] "Fast Thyristor: KKC 3000-60" *CRRC Group,* Zhuzhou, China: Product Datasheet, Nov. 2016.

[11] "Fast Recovery Diode: FYB 2000-45-02" *CRRC Group*, Zhuzhou, China: Product Datasheet, Nov. 2016.

[12] Toshiba, "Toshiba silicon N-channel IEGT ST3000GXH24A," in *Proc. Toshiba*, Tokyo, Japan, Datasheet, Dec. 8, 2016.

[13] H. Pang and X. Wei, "Research on key technology and equipment for zhangbei 500kV DC grid," in *Proc. Int. Power Electron. Conf. (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 2343–2351.

[14] W. Zhou *et al.*, "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *Proc. 17th European Conf. Power Electron. Appl. (EPE'15 ECCE-Europe)*, 2015, pp. 1–7.