Letters

Equal Loss Distribution in Duty-Cycle Controlled H-Bridge LLC Resonant Converters

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***Abstract*—The duty-cycle control is a popular option for current limiting in LLC resonant converters. Such current limiting is required to protect the converter either during the start-up or during an overload. Although this method proved to be effective, the switching and conduction losses of the converter are increased because of the modified current waveforms in the resonant tank. Hence, for the safe operation, it is vital to distribute the losses between the switches symmetrically. However, the conventional duty-cycle or phase-shift modulation methods do not provide this naturally. This letter elaborates on a method that was proposed for a different soft-switching topology more than a decade ago to solve this problem, and is adaptable for the emerging dc transformers. Furthermore, a simple implementation of the method is shown and the equal distribution of losses is validated experimentally. The VHDL code with the implementation of the modulator is attached to this letter available openly for reuse.**

***Index Terms*—Duty cycle, equal losses, H bridge, LLC converter.**

I. Introduction

DESPITE the nonlinear properties of the duty-cycle modulation in LLC converters [1]–[3], this method has become a popular and well-established solution for several specific tasks. In variable-voltage applications, the duty-cycle modulation was proposed several times for light-load efficiency optimization [4]–[6]. In dc transformer applications of LLC converter (DCX applications), where the voltage transfer ratio is fixed, the duty-cycle modulation can be utilized as a protection method. While these converters are usually operated in open-loop operation near resonant frequency with a constant duty cycle of $\delta = 0.5$, the duty-cycle modulation is an effective measure to limit the transferred currents either during start-up of the converter [2], [3], [7] or during overload conditions [7]–[9]. Compared to the hardware-based methods for current limiting, such as application of clamping diodes [10], [11] or an additional resistor in the resonant tank [9], the duty-cycle modulation does not require any modification of the converter, which results in reduced costs and converter size. The frequency modulation [10] is not well-suited for current limiting in DCX applications, since the typical parameters of resonant tank would require the increase of the switching frequency multiple times, which is likely unfeasible with the utilized semiconductor switches. Case studies, that compare the current limiting methods, can be found, e.g., in [9] and [10].

In the literature, two modulation techniques were proposed for the H-bridge LLC converters: duty-cycle method that uses only one zero-voltage state [3], and the phase-shift modulation [2]–[4], [6]–[8]. While they generate the same three-level voltage waveforms at the resonant tank, the distribution of the losses between the switches is not only different (due to the different utilization of zero states) but also unequal in both cases. This is especially critical during the current-limiting operation of the LLC-converter-based dc transformers, since the duty-cycle modulation increases both the switching and the conduction losses due to the modified waveforms of the currents in the resonant tank. As a consequence, if the losses are not equalized, the operation might be limited. A heavy-load start-up might be thermally unfeasible for given devices and only a lower current can be delivered for a shorter time period during overload conditions.

Hence, in order to improve the start-up and overload capabilities of the LLC-converter-based dc transformers, it is vital to limit overloading of single switches by an equal redistribution of the losses. This letter demonstrates the effectiveness of the asymmetric loss-equalizing modulation method utilized for a different converter topology in [12]. By modifying the switching pattern, the method is capable of complete loss equalization without affecting the total losses.

This letter elaborates on the available modulation methods and demonstrates the causes of unequal loss distribution in the H-bridge of an LLC converter. It shows the derivation and implementation of the loss-equalizing modulation, and validates the effectiveness of this method experimentally.

II. Topology Description

The studied H-bridge LLC converter is displayed in Fig. 1. It consists of the H-bridge inverter stage, the diode rectifier stage,

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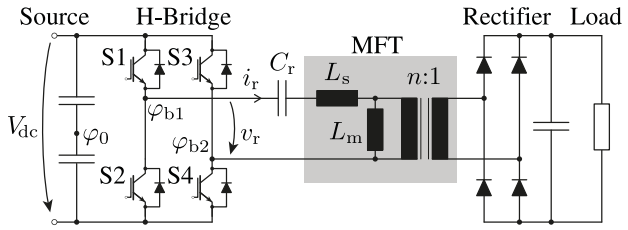

Fig. 1. Studied H-bridge LLC converter topology.

TABLE I
SWITCHING STATES OF AN H-BRIDGE

	Switching State			
	P	N	0^+	0^-
Switch S1	ON	OFF	ON	OFF
Switch S3	OFF	ON	ON	OFF

and the LLC resonant tank comprising the resonant capacitor C_r and two inductors L_s and L_m that are usually integrated as a part of a medium-frequency transformer (MFT).

The H bridge consists of four switches (in this case IGBTs) S1–S4 with four antiparallel diodes D1–D4, respectively. This converter stage is capable of generating four switching states: *P* for positive output voltage $v_r = V_{\rm dc}$, *N* for negative output voltage $v_r = -V_{\rm dc}$, and two redundant zero states 0^+ and 0^- to generate zero voltage $v_r = 0$. The switching states are listed in Table I. The switches S2 and S4 are switched complementary to switches S1 and S3, respectively.

III. Modulation Methods and Their Properties

During the normal open-loop operation with duty cycle of $\delta = 0.5$, all modulation methods generate the same switching signals that lead to perfectly equalized losses. Only during the current-limiting operation, when duty cycle is decreased, differences are observable. While all modulation methods generate the same three-level voltage waveforms in the resonant tank, the main difference is how they select the zero states in the switching pattern.

A. Duty-Cycle Modulation With Single Zero State

A straight-forward method is to use exclusively one zero state 0^- (or 0^+). This modulation method is demonstrated over two switching periods in Fig. 2(a).

As the figure shows, utilizing only one zero state leads to an unequal distribution of the current between the upper switches (S1 and S3) and the lower switches (S2 and S4). In this case, the most of the current is conducted by the lower switches and diodes (S2, D2, S4, and D4), while the upper switches and diodes (S1, D1, S3, and D3) conduct only for a short period of time. Hence, the conduction losses will be higher in the lower switches.

Taking a look at the switching instants, it can be seen that all switches experience zero-voltage turn ON. However, the upper switches (S1 and S3) turn OFF significantly higher currents than the lower switches (S2 and S4). Hence, the switching losses will be significantly higher in the upper switches.

As a consequence, it is expected that in the modulation techniques that only use the 0^- zero state (or only use the 0^+ zero state), the losses will be split unequally between the upper and lower switches. Which switches will experience higher losses depends on the ratio between the turn-OFF loss energy and the conduction losses.

B. Phase-Shift Modulation

Although there are several options how to implement the phase-shift modulation, it is characteristic that the zero states 0^+ and 0^- are alternated each time when a zero state is necessary. The resulting modulation pattern is shown in Fig. 2(b).

As can be recognized, this method leads to unequal losses between the switches of the left half bridge (S1 and S2) and the right half bridge (S3 and S4). Compared to the previous modulation method, the conduction losses are expected to be more equalized, since the switch-diode combination S1/D1 (and S2/D2) conducts the same rms currents as the switch-diode combination S3/D3 (and S4/D4). While the zero-voltage turn ON is still maintained, the switches of the left half bridge will experience significantly higher turn-OFF losses than those of the right half bridge.

In summary, when phase-shift modulation is applied, the losses in one of the half bridges are expected to be significantly higher than in the other one, due to the nonequivalent distribution of the switching losses.

C. Loss-Equalizing Modulation

As demonstrated in Fig. 2(c), the loss-equalizing modulation alternates between the zero states in pairs: 0^+, 0^+, 0^-, 0^-, 0^+, 0^+, 0^-, 0^-... This can be viewed either as a cycling of the utilized zero state in duty-cycle modulation after each switching period (from 0^+ to 0^-) or as toggling between the leading and lagging half bridge in phase-shift modulation (from 0^+, 0^- to 0^-, 0^+).

Observing Fig. 2(c), it can be recognized that while the total losses are unaffected, they are distributed equally between the switches. Similarly to the other two modulation methods, the current is conducted via two semiconductor devices at each time and the same currents are turned OFF within a switching period. However, with the loss-equalizing mehod, all four conduction current waveforms of diodes and of switches become identical, only with a certain phase shift in between. This guarantees equally distributed conduction losses.

Furthermore, the turn-OFF current is one time high and one time low within each two periods for all switches and thus, the switching losses are equalized as well. The zero-voltage turn ON remains unaffected, since the antiparallel diode is conducting during the switch being turned ON.

Note that since the diode is supposed to conduct after each switching, there is no impact of the dead times on the waveforms (as long as the dead times are short enough). Nonetheless, this applies for all presented modulation techniques.

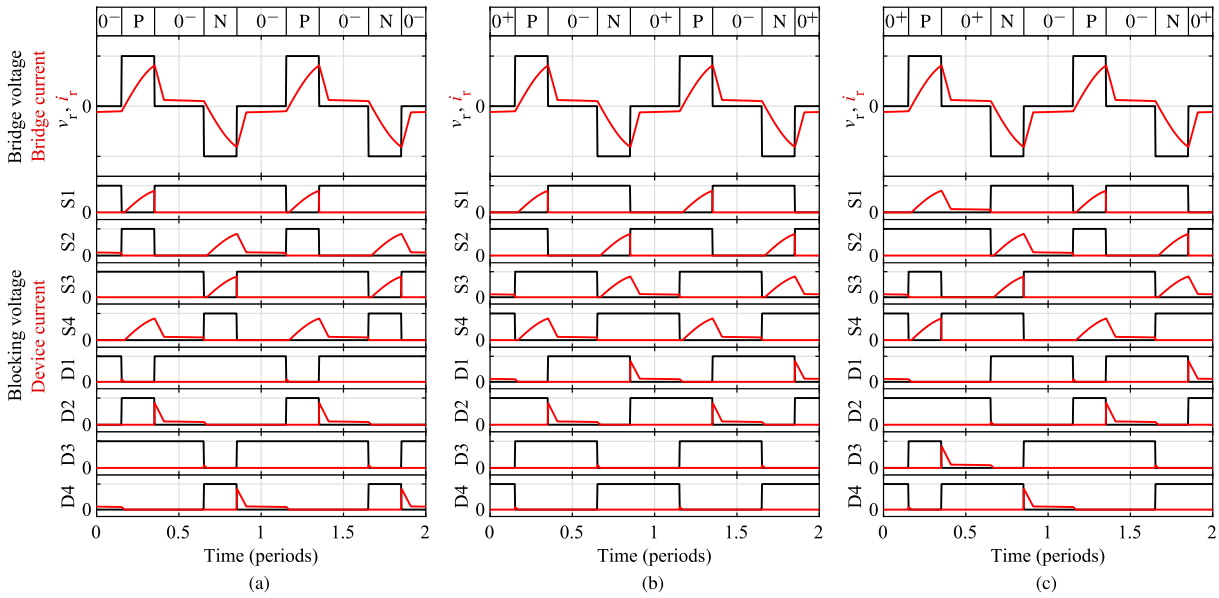

Fig. 2. Waveforms demonstrating the principle and the properties of different modulation techniques. (a) Duty-cycle modulation using only state 0^-. (b) Phase-shift modulation. (c) Loss-equalizing modulation. The duty cycle in the example is $\delta = 0.2$.

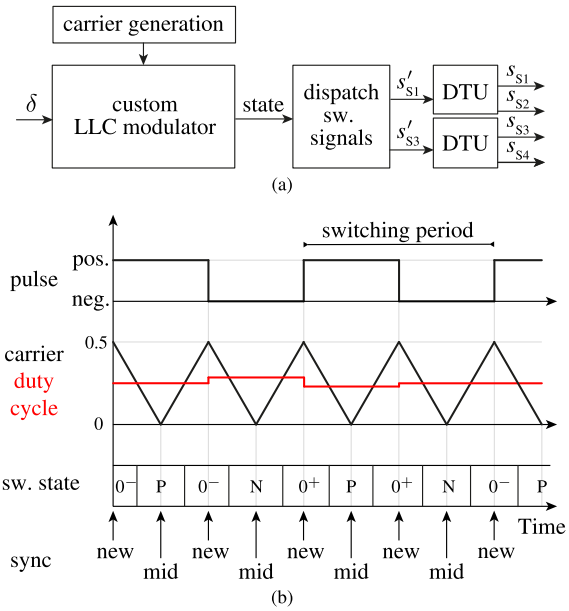

Fig. 3. Implementation of the loss-equalizing method. (a) Overall scheme of the modulator. (b) Demonstration of the principles. DTU stands for dead-time unit.

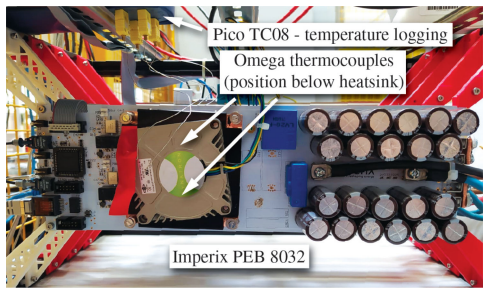

Fig. 4. Imperix half bridge module and the position of thermal couples.

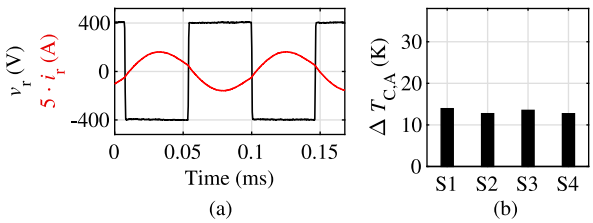

Fig. 5. Rated operating point of the dc transformer with duty cycle $\delta = 0.5$: (a) H-bridge output waveforms, (b) steady-state case-to-ambient temperature of the discrete switches.

In summary, the loss-equalizing modulation method is expected to equalize the losses without any obvious drawbacks.

IV. Implementation

The proposed implementation of the loss-equalizing modulation can be explained using Fig. 3. Note that this also represents the implementation in the attached VHDL code.

As the overview in Fig. 3(a) shows, the implemented loss-equalizing modulator unit consists of a carrier generation block, custom LLC modulator that determines the switching state (P, N, 0^+ or 0^-), block that dispatches the switching signals for the particular switches, and two dead-time generation units (DTUs).

In Fig. 3(b), the function of the custom LLC modulator block is demonstrated. The inputs for this block are the setpoint duty cycle δ and the carrier signal generated in the carrier generation block together with the synchronization signals marking the beginning and the end of switching period. The custom LLC modulator uses a triangular carrier with a frequency double of the switching frequency with values ranging from 0 to 0.5

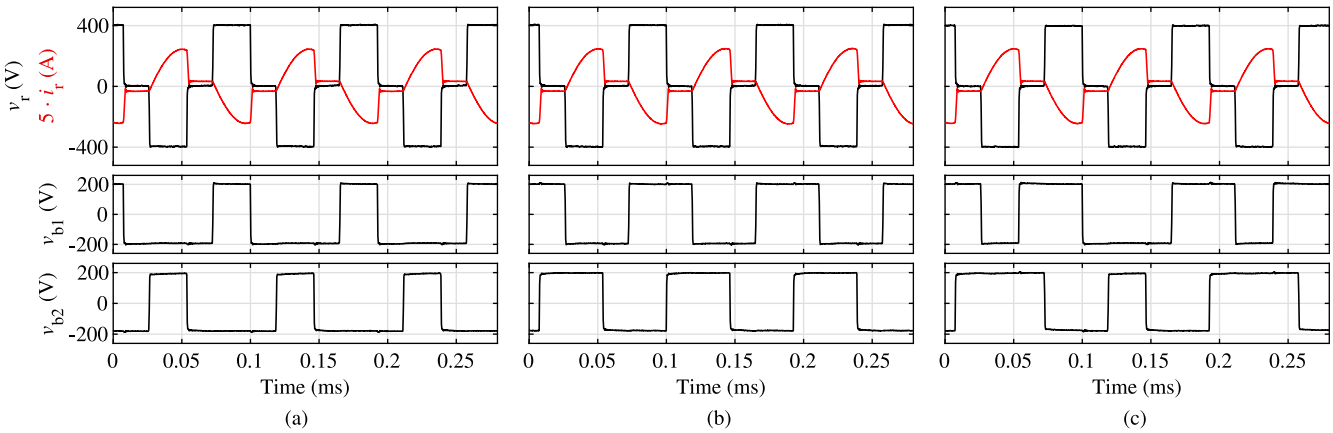

Fig. 6. Waveforms captured at duty cycle $\delta = 0.3$ and rated current with different modulation methods. (a) Duty-cycle modulation using only state 0^-. (b) Phase-shift modulation. (c) Loss-equalizing modulation.

to generate the patterns. At the beginning of each half-period (marked with synchronization signal labeled as "new"), the duty-cycle values are updated in the modulator block and the internal pulse polarity signal (labeled as "pulse") is toggled between positive and negative state.

When the duty cycle is higher than the carrier signal, the active switching states are assigned depending on the pulse polarity signal: When pulse polarity signal is positive, the switching state is P. When it is negative, the switching state is N. The zero switching states are assigned in the loss-equalizing pattern (0^+, 0^+, 0^-, 0^-, 0^+, 0^+, 0^-, 0^-...). The next preferred zero state is updated from the list always in the middle of the half-period (marked with synchronization signal labeled as "mid").

Once the switching state is assigned in the custom LLC modulator, the particular complementary switching signals s'_{S1} and s'_{S3} are determined according to Table I in the dispatching block, and the switching dead times are added in dedicated dead-time units to prevent a shoot through, generating the gate signals $s_{\mathrm{S1..S4}}$ for the switches.

V. Experimental Validation

To validate the performance of the studied modulation methods, a set of experiments was conducted using an LLC converter prototype.

The H-bridge stage consists of two Imperix PEB 8032 half bridges [see Fig. 4]. These half bridges were modified for temperature measurement by milling a groove into the heatsink and placing the thermocouples Omega SCASS-020U-12 centrally on the top of the respective IGBT modules. The resonant tank comprises a 1:1 MFT that integrates the inductances ($L_m =$ 750 µH, $L_s = 11.6$ µH including the cabling inductance) and a split resonant capacitor with an equivalent value of $C_r =$ 18.75 µF. The details on the MFT can be found in [13].

The LLC converter is rated at 400 V and 20 A with an efficiency of 97%. In the normal operation, the duty cycle is constant: $\delta = 0.5$. The switching frequency is equal to the resonant frequency at $f_s = 10.8$ kHz. The characteristic waveforms of the H bridge of the dc transformer under the rated conditions are displayed in Fig. 5(a). Since no zero states are applied, all modulation techniques lead to identical results. Furthermore, the steady-state temperature distribution (as well as loss distribution) between the switches is naturally equalized as demonstrated in Fig. 5(b).

Fig. 6 shows the key waveforms captured during the experiments with reduced duty cycle of $\delta = 0.3$ (current-limiting operation). It demonstrates clearly that regardless of the applied modulation, the output voltage v_r and the output current i_r of the H-bridge are the same. Nonetheless, the half-bridge output voltages

$$v_{\mathrm{b1}} = \varphi_{\mathrm{b1}} - \varphi_0 \tag{1}$$

$$v_{\mathrm{b2}} = \varphi_{\mathrm{b2}} - \varphi_0 \tag{2}$$

measured between the phase output (potentials φ_{b1} and φ_{b2}) and the midpoint of the dc-link capacitor (potential φ_0) show that completely different switching patterns were utilized in each case. As discussed before, these switching patterns are expected to impact the distribution of the losses between the devices.

To validate the loss distribution, the temperatures of the IGBT cases were measured during a 10 minute experiments, which guaranteed a steady-state thermal condition [see Fig. 7]. The resulting steady-state case-to-ambient temperatures for each device and modulation method are shown graphically in Fig. 8 for duty cycle $\delta = 0.3$ and in Fig. 9 for $\delta = 0.2$.

Figs. 8(a) and 9(a) show that there is a significant inequality between the losses in the upper switches (S1 and S3) and the lower switches (S2 and S4) in the single-zero-state duty-cycle modulation. Since the upper switches have higher losses than the lower, it can be concluded that in the given operating point, the increased conduction losses in the lower switches are less impactful than the increased switching losses in the upper switches. Please note that this distribution depends on the applied operating point. Furthermore, the temperature differences might be even higher when discrete heatsinks would be applied for each IGBT (in contrast to the test setup).

Figs. 8(b) and 9(b) demonstrate that the phase-shift modulation leads to significant inequality between the switches of the

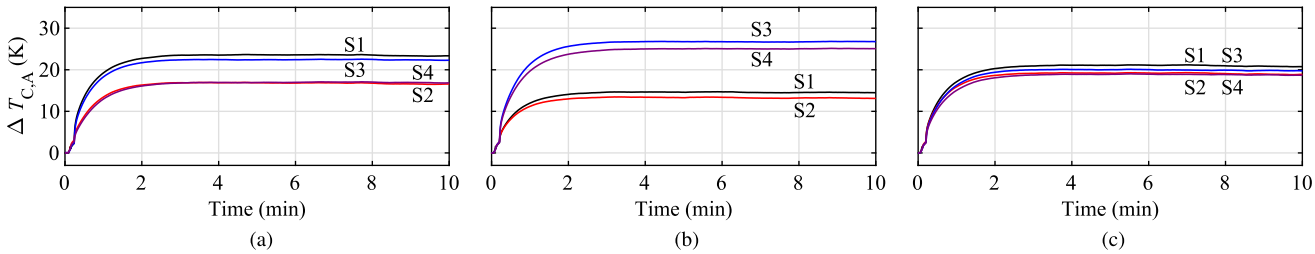

Fig. 7. Case-to-ambient temperature waveforms captured at duty cycle $\delta = 0.3$ and rated current with different modulation methods. (a) Duty-cycle modulation using only state 0^-. (b) Phase-shift modulation. (c) Loss-equalizing modulation.

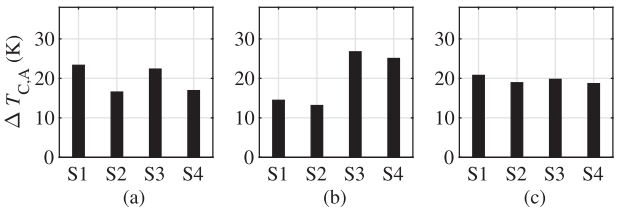

Fig. 8. Case-to-ambient temperature distribution captured in steady state at duty cycle $\delta = 0.3$ and rated current with different modulation methods. (a) Duty-cycle modulation using only state 0^-. (b) Phase-shift modulation. (c) Loss-equalizing modulation.

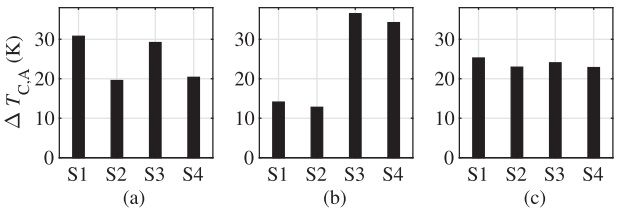

Fig. 9. Case-to-ambient temperature distribution captured in steady state at duty cycle $\delta = 0.2$ and rated current with different modulation methods. (a) Duty-cycle modulation using only state 0^-. (b) Phase-shift modulation. (c) Loss-equalizing modulation.

left half bridge (S1 and S2) and the losses of the right half bridge (S3 and S4), as expected.

Finally, Figs. 8(c) and 9(c) clearly show that the loss-equalizing modulation leads to the best power loss distribution. Moreover, it can be observed that in the same operating point, the loss-equalizing method leads to the lowest maximum temperature. Consequently, with this method, the dc transformer is capable of delivering higher currents for a longer period of time during overload conditions and during the start-up. This is especially important because the H-bridge losses are increased during current-limiting operation and thus, such operation is likely thermally limited. While the total H-bridge losses at the rated operation point are only $\approx$120 W, they increase to $\approx$185 W at $\delta = 0.3$ and $\approx$250 W at $\delta = 0.2$, regardless of the applied modulation technique.

VI. Conclusion

This letter has clearly demonstrated that the conventional modulation techniques lead to unequal distribution of losses in LLC resonant converters. Since this occurrence negatively impacts their performance during current limiting tasks, such as the converter start-up or overload limiting, a loss-equalizing method proposed for other topology was adapted. This method provides a perfect loss equalization without any significant drawbacks, beside a slightly more complex implementation. To address this single disadvantage, a possible implementation was explained and the utilized VHDL code is attached to this letter.

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