Design a 400 V–12 V 6 kW Bidirectional Auxiliary Power Module for Electric or Autonomous Vehicles With Fast Precharge Dynamics and Zero DC-Bias Current

Liyan Zhu, *Student Member, IEEE*, Hua Bai, *Senior Member, IEEE*, Alan Brown, and Matt McAmmond

***Abstract*—An auxiliary power module in electric vehicles is a dc/dc converter bridging the high-voltage propulsion battery with a low-voltage auxiliary system. In the coming era of connected and autonomous vehicles, the power rating of such dc/dc converters is expected to surge from 2.5 to 6 kW. In addition, there is the challenge of a wide operating voltage range, e.g., 250–450 V required by the high-voltage propulsion battery and 10–16 V at the low-voltage auxiliary battery. To meet these voltage and power challenges, this article proposes a two-stage bidirectional design, i.e., interleaved buck + dc transformer (DCX) that offers full voltage range coverage, 3.5 kW rated power, and peak power of >6 kW. Experimental results indicated >96% efficiency, owing to the zero-switching loss of DCX. Furthermore, the precharge mode that charges the input dc-bus capacitor with the low-voltage battery is accomplished using the inner phase shift control of the DCX stage. DC-bias blocking capacitors on the low-voltage side are replaced with a simple, unique dc-bias detection circuit that samples and eliminates the dc-current offset of the transformer. Simulation and test results confirm that the proposed method effectively detects and eliminates the dc-bias current.**

***Index Terms*—Auxiliary power module, dc-bias detection, dc transformer, dc–dc converter, electric vehicles (EVs).**

I. Introduction

AN ISOLATED, high-step-down dc/dc converter is a requirement for electric vehicles (EVs) where an alternator is not available to power 12-V auxiliary loads. Such a dc/dc converter is shown in Fig. 1. It is also known as an auxiliary power module (APM). In EVs, the APM bridges the high-voltage (HV) on-board propulsion battery with the low-voltage (LV) battery. For nowadays application, an exemplary design using Si CoolMOS and a phase-shift full-bridge (PSFB) yields >93% efficiency and has a power density of 1.5 kW/L with 2 kW peak output power [1]. A current-fed, dual-active-bridge is considered as an excellent candidate for a high-step-down dc/dc converter [2], [3]. However, hard switch OFF large currents at the LV side creates challenges, such as high switching losses and electromagnetic interference (EMI) [4], [5]. Another approach employs an *LLC* resonant converter [6]–[8]. These are typical one-stage designs, while simple and cost-effective, typically have limited output power and hard to cover wide input and output voltage range requirements.

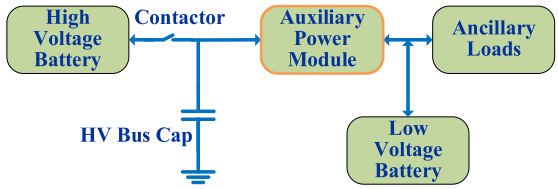

Fig. 1 APM in EV.

Facing future autonomous and connected EVs, there are three primary challenges related to the proposed APM design, i.e., high output current/power rating, a wide input and output voltage range, and bidirectional power flow.

First, the high output current/power rating. As a historical reference point, the first generation 2005 Toyota Prius is considered. The Prius required 108 A current out of a 14 V battery [9]. Then, the auxiliary load consisted of basic applications, such as the control unit, wiper, and headlights. Today, additional equipment, such as speakers, screens, and electric steering systems, increases the load on the 12 V system. The average power has significantly risen from 2 to 3.5 kW in EVs [10]. Given the trend of EV swapping out hydraulic systems with the electric ones, the short-period overload situation, e.g., 6 kW, creates a considerable challenge. The thermal stress induced by high conduction loss and switching current must be addressed.

The next consideration is the wide input and output voltage range. For a 400 V HV battery, the APM needs to accept the input from 250 to 450 V [11] and provide an output voltage that varies from 10 to 16 V [12], [13], subject to the HV and LV battery state of charge. Aiming at high-power applications in future autonomous and connected EVs, the APM needs to

Manuscript received June 4, 2020; revised August 17, 2020; accepted September 29, 2020. Date of publication October 1, 2020; date of current version January 22, 2021. Recommended for publication by Associate Editor K. Sun. *(Corresponding author: Hua Bai.)*

Liyan Zhu and Hua Bai are with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996 USA (e-mail: lzhu21@vols.utk.edu; kevinbai@icloud.com).

Alan Brown and Matt McAmmond are with the HELLA Electronics Corporation, Northville, MI 48168 USA (e-mail: alan.brown@hella.com; matt.mcammond@hella.com).

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Digital Object Identifier 10.1109/TPEL.2020.3028361

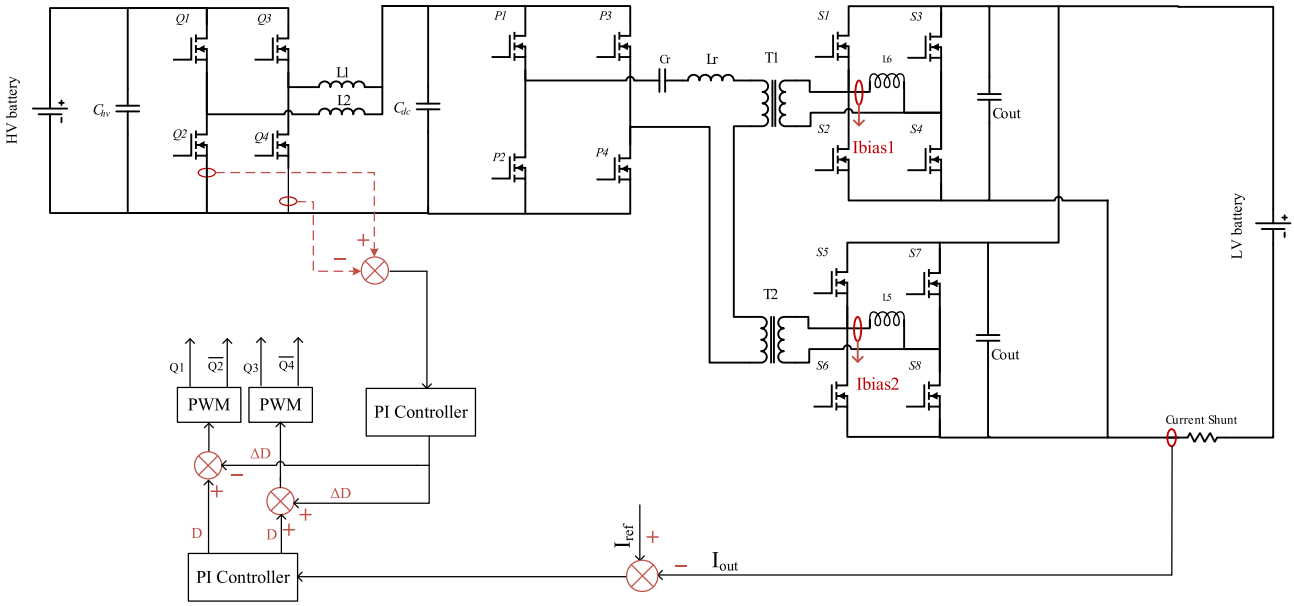


Fig. 2. Proposed topology for a 6 kW bidirectional EV APM.

output full power at all voltage scenarios, for example, 250 V/16 V or 450 V/10 V. This requires a wide range of voltage gain that excludes the most commonly used dc/dc topologies. For instance, the *LLC* circuit has a limited voltage gain and the dual-active bridge (DAB) topology has a high switching OFF current.

Last but not the least, the bidirectional power capability is also a desired feature to precharge the HV bus capacitors. To avoid the in-rush current when turning ON the contactor to the HV battery, the HV bus capacitor needs to be precharged to a voltage matching the HV battery voltage. Usually, this function is done by a dedicated circuit. For example, the most commonly used method is adopting two relays [14]–[16]. One precharge relay in series with a current-limiting resistor turns ON first. When the capacitor is charged, the main relay turns ON. Such a method requires two additional relays and one power resistor. Therefore, the extra cost is needed and the mechanical relay also presents a reliability issue. To extend the lifetime of the relay, Ozguc *et al*. [17] use the semiconductor devices with gate-drive circuits to replace relays. However, the additional cost is still needed. Some other methods, such as using a dedicated dc–dc converter, are also proposed [18], which controls the precharging current. However, the cost is still a common issue. If the APM is bidirectional, it will be easy to charge the HV capacitor without any additional cost.

Facing the challenges of such a high-power wide voltage range and bidirectional application, the single-stage APMs from previous research works show the limitations. A GaN devices based single-stage *LLC* converter for APM is proposed in [19], where two paralleled *LLC* converter modules deliver 2 kW power with a peak efficiency of 95%. If 6 kW power is needed, six such *LLC* modules are needed and the total switches numbers are unendurably high. No mention such an *LLC* converter is just unidirectional. The improved single-*LLC* converters are studied in [6] and [8] but common issues are still low power (<2.5 kW) and derated operation under extreme input/output voltages. The phase-shift-based converters, such as DAB and PSFBs, are popular topologies as well. Both voltage-fed and current-fed phase-shift converters are proposed in [20]–[23] ranging from 1.5 to 3 kW. However, their peak efficiencies are only 87%–93%. Higher output power yields a lower efficiency because of the high switching-OFF current.

The limitation of single-stage design has led to the consideration of a two-stage design using SiC devices, as shown in Fig. 2. The front-end adopts interleaved buck converters to step-down the HV battery to an intermediate dc-bus voltage, which is then converted to the LV side through a resonance-based dc transformer (DCX). The buck converters (Q_1–Q_4 made of SiC MOSFETs) determine the power level and direction of flow. The DCX isolation stage (P_1–P_4 using SiC MOSFETs and S_1–S_8 using LV Si MOSFETs) is always operated at the resonant frequency, providing a unit voltage gain and close to zero switching losses. With two matrix transformers, it is expected that each transformer will take half of the load. Overall, the front-stage addresses the wide voltage range and relies on the DCX stage to avoid the high switching-OFF current, thereby providing high efficiency. Another merit of this design is its bidirectional feature, allowing for symmetric HV to LV (defined as the buck mode) and LV to HV (defined as the boost mode) power capabilities. The goal is a device with a >2 kW/L power density and >96% efficiency, with a peak output power of 6 kW, in contrast to an in-market device with a ∼1 kW/L density, 94% efficiency, and 2.5 kW at the peak power.

The rest of this article is organized as follows. Section II of this article compares a two-stage design with the conventional one-stage design. It demonstrates that the proposed topology can cover the whole voltage and power ranges at high-efficiency levels. Section III discusses the zero-voltage switching (ZVS) operation for both the buck stage and the DCX stage. In Section IV, a dc-bias current detection and elimination method is proposed to remove the dc-bias current. It removes the need for

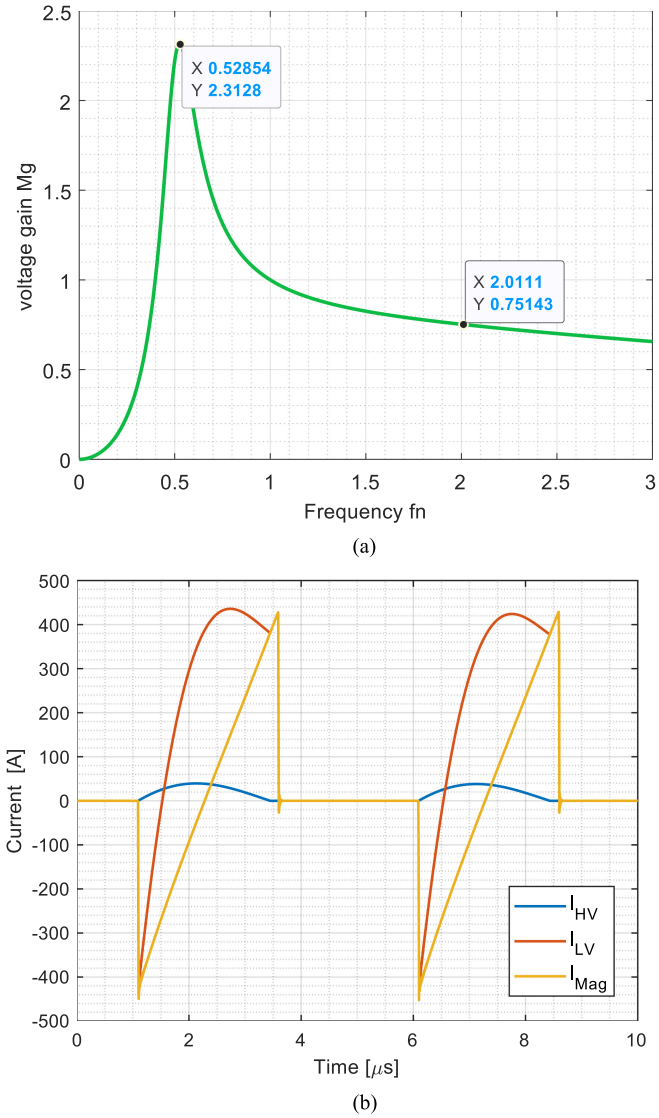


Fig. 3. (a) Voltage gain of the one-stage *LLC* converter. (b) Current of the secondary-side switches at the boost mode.

installing the dc-blocking cap on the LV side. Section V focuses on the bidirectional power capability of the topology with an emphasis on the transient process when using the LV battery to precharge the HVdc capacitor before closing the contactor between the HV battery and input capacitor. A novel control, combining phase shift with DCX, is proposed to secure ZVS throughout the entire precharge process. Section VI details the experimental results. Finally, Section VII provides the conclusion.

II. Two-Stage Versus One-Stage Design

A two-stage design typically comes at a higher cost and lower efficiency than the equivalent single-stage design. Therefore, it is critical to evaluate the pros and cons of the single-stage design (*LLC*, DAB, etc.) and two-stage design, respectively.

To cover the wide input and output voltage range, an *LLC* design is shown in Fig. 3(a). Here the gain is defined as

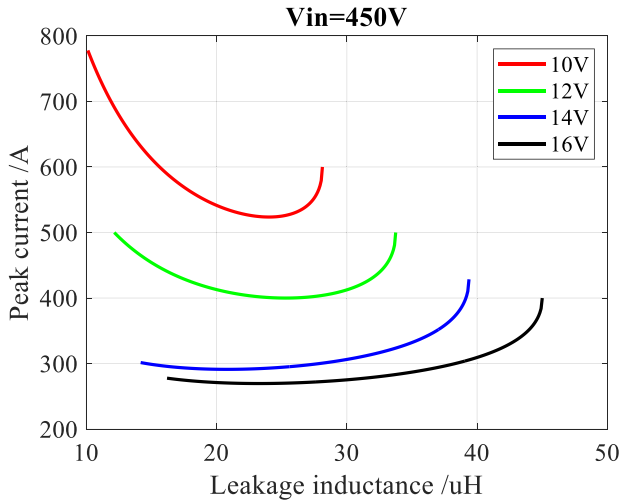


Fig. 4. Peak current of DAB LV side for the APM application.

$n_t * V_o / V_{\text{in}}$, where n_t is the transformer turn ratio, e.g., 10 for each transformer and 20 for the overall matrix transformers. When $C_r = 517$ nF, the resonant frequency is approximately 200 kHz. Given the *LLC* design is a well-understood topology [24], [25], this article will not go through the details of its design. This design struggles to perform over the entire voltage range. It creates a challenge where the mutual inductance L_m reflected the LV side is only 36.7 nH, resulting in a large current when the secondary-side switches are enabled to power the HV side. Shown as I_{Mag} in Fig. 3(b), the peak of excitation current can go beyond 400 A, creating a large current stress on the secondary-side switches.

The DAB converter has the advantages of a wider voltage gain and the securing of ZVS turn-ON is well studied [26], [27]. However, the DAB always presents a considerable switching-OFF current no matter the power flow direction. For the same specifications, the peak current is highly related to the leakage inductance. The worst-case LV-switch current stress is depicted in Fig. 4. The peak switching-OFF current is >500 A, even worse than *LLC*.

Concluded from the literature review and single-stage *LLC*/DAB design mentioned above, the single-stage design usually delivers a power less than 3 kW with the efficiency lower than 95%. Very few of APMs have the bidirectional capability (<15% [28]) or the precharge mode. Even we managed to design a single-stage 6 kW DAB or *LLC*, the current stress is extremely high or the parameters are impractical for manufacturing. Facing the 6 kW output power, bidirectional operation, and full-voltage ranges, the proposed two-stage design relieves the design stress and presents superiorities. Therefore, a two-stage design composed of an interleaved buck stage and matrix DCX stage is considered in this article, as shown in Fig. 2.

For the DCX stage, by setting its switching frequency exactly to the resonant frequency of the L_r and C_r tank, the circuit always runs at the resonant point and presents a unit voltage gain. As a result, the current and voltage will be in phase, as shown in Fig. 5. It shows near-zero switching stress. Note both V_{pri} and V_{sec} (primary and secondary *H*-bridge output voltage) switch

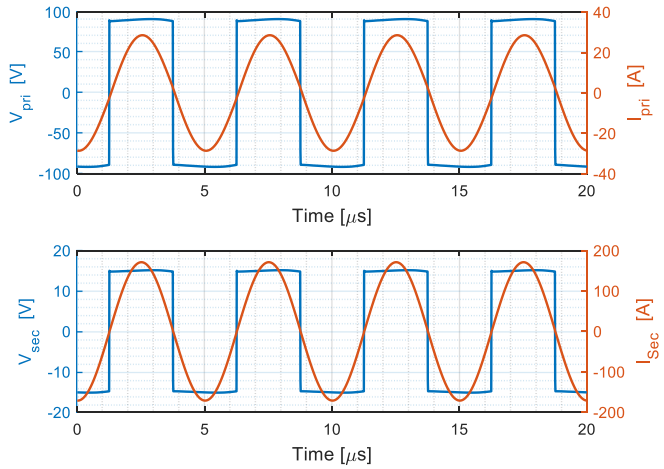


Fig. 5. Waveform of DCX showing ZCS stress.

the polarity right at the current zero-crossing point (red curves). Therefore, the switching loss is negligible, which is essential to providing a high output current or a high switching frequency. The resonant design is frequency selective, requiring its input across C_{DC} to perfectly match its output. This is accomplished with the front-end buck stage.

For instance, if the LV battery is V_o, the C_{DC} will undertake the voltage of $V_o{*}n_t{*}2$. Here n_t is the single-transformer turn ratio. Now, if the HV battery is V_{in}, we need the duty cycle for the buck converter as $D^* = V_o{*}n_t{*}2/V_{\mathrm{in}}$. Of course, at this point, it will not deliver any power. If we need the power to flow from HV to LV, the duty cycle $D > D^*$, otherwise, $D < D^*$. So the power demand determines the increment or decrement of the duty cycle around this reference value.

Although the two-stage dc/dc converter looks more complex, it has the advantage of nearly zero switching stress, low EMI radiation, and simpler and more practical transformer design. Also, fewer paralleled switches are needed on the secondary side, given no high-switching current. Furthermore, the design will be less sensitive to the parasitic inductance of the layout because of low *di/dt* and the high frequency allows for the use of a smaller output filter.

III. ZVS for Two Stages

SiC MOSFETs have higher switching-ON losses as compared with their switching-OFF losses. Therefore, it is necessary to achieve ZVS turn-ON in the buck stage. As for the DCX stage, theoretically, it has natural ZVS. However, when considering the impact of the transformer's mutual inductance and the parasitics of the switches and the printed circuit board (PCB), we might not take ZVS for granted, which is covered in this section.

A. ZVS for Interleaved Bucks

Although securing zero-current turn-OFF is impossible, it is very likely that the interleaved buck stage can still achieve ZVS turn-ON when running in the critical conduction mode [29]. Given that the input and output voltage ranges are wide, the switching frequency f_s of the buck stage needs to be varied to secure ZVS at any voltage and power level.

Assuming the overall power is P, each inductor current has the maximum value as $I_{\max}$ and the minimum value as $I_{\min}$. We will have

$$L\,\frac{I_{\max}-I_{\min}}{DTs} = V_{\mathrm{in}} - V_{\mathrm{DC}} \tag{1}$$

$$\frac{V_{\mathrm{DC}}\,(I_{\max}+I_{\min})}{2} = \frac{P}{2} \tag{2}$$

$$DV_{\mathrm{in}} = V_{\mathrm{DC}} \tag{3}$$

$$I_{\min} < -I_z. \tag{4}$$

Here, I_z is the minimum current to secure ZVS turn-ON of the switch. It is mainly determined by the switch output capacitance C_{oss}. V_{in} is the input battery voltage and V_{DC} is the dc-bus voltage. D is the duty cycle, L is the inductor inductance, and T_s is the switching period. Given the nature of the DCX

$$2\,n_{\mathrm{t}}\mathrm{V_o} = \mathrm{V_{DC}} \tag{5}$$

where n_t is the transformer turn ratio. V_o is the LV battery voltage. From (1) to (5), we have

$$\frac{1}{2}\left(\frac{P}{2n_tV_o} - \frac{V_{\mathrm{in}}-2n_tV_o}{Lf_s}\,\frac{2n_tV_o}{V_{\mathrm{in}}}\right) < -I_z. \tag{6}$$

The boundary ZVS current can be calculated in the following equation, where $t_{\mathrm{bd\_bk}}$ is the deadband at the buck stage:

$$I_Z = \frac{2\cdot C_{\mathrm{oss}}}{t_{\mathrm{db\_bk}}}. \tag{7}$$

From (6) and (7), the desired switching frequency for the buck stage to realize ZVS is

$$f_s < \frac{n_tV_o\,(V_{in}-2n_tV_o)}{V_{\mathrm{in}}L\left(\frac{2C\mathrm{oss}}{t_{\mathrm{db\_bk}}}+\frac{P}{4n_tV_o}\right)} \tag{8}$$

With the calculated frequency, the buck stage operated at different voltages is simulated in Fig. 6, where the minimum current is always negative in order to secure ZVS.

To implement the variable frequency control, (8) needs to be calculated online. Note that the equation involves n_t, C_{oss} of the switches, and output inductance L, which are constants predefined in DSP based on the datasheet and design parameters. Other variables in the equation, such as voltages and power, are sampled and calculated in real time. Because the equation is relatively simple, there is no need to build the lookup table. All the calculation is done with DSP TMS32028379D in real time.

B. ZVS for the DCX

An *LLC*-based DCX usually uses the diode rectifier [30] or synchronous rectifier [7], [31] to control (SRC) the secondary side and to reduce the conduction losses. However, SRC requires the use of specialized chips or complicated auxiliary synchronous circuits to determine the turn-ON and turn-OFF time [32], [33]. To obtain high efficiency and maintain the simplicity of the system, this article proposed a novel digital pulsewidth modulations (PWMs) for both the primary side and secondary

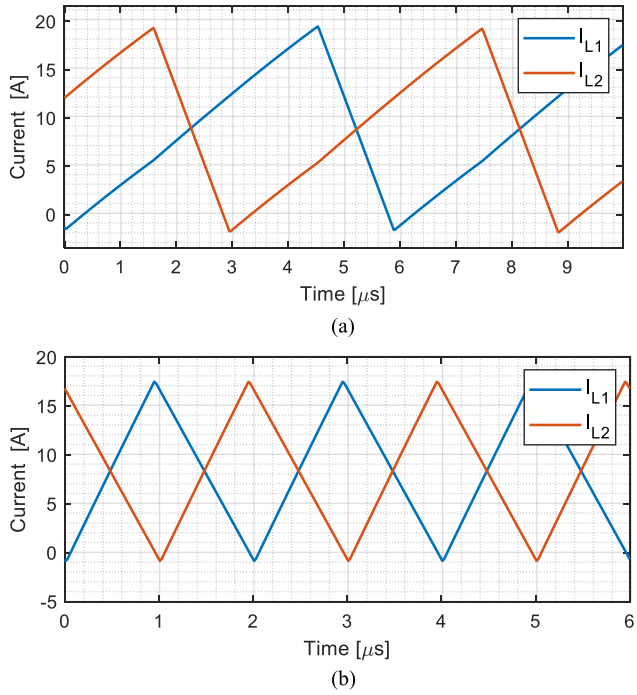


Fig. 6. (a) f_s = 170 kHz for 250 V_{in}/10V_{out}. (b) f_s = 500 kHz for 450V_{in}/16V_{out}.

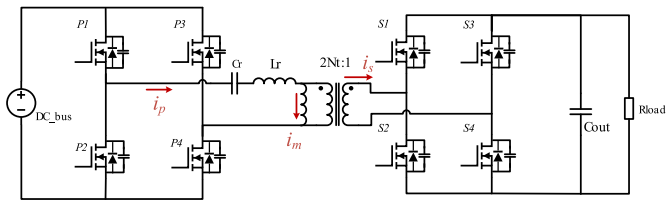


Fig. 7. Simplified ideal DCX model.

side of the DCX without any need for an auxiliary circuit. The PWMs for the two sides cannot simply be the same because of the parasitics of the switches and the PCBs.

A simplified DCX model in the buck mode is shown in Fig. 7, where the matrix transformer is now replaced with a single transformer with a turn ratio of $2{*}n_t$, operated at the resonant frequency. The ideal waveforms of the DCX are given in Fig. 8.

With the primary and secondary-side gate signals aligned, it is clear that ZVS is easy to achieve on the primary side of the *LLC* converter due to the magnetizing current. But on the secondary side, it is zero-current-switching (ZCS) rather than ZVS. Although ZCS is also lossless ideally, when all the parasitics are taken into consideration, it is no longer true. Fig. 9 shows that during the deadband, there is no power delivered to the secondary and all the switches are turned OFF. C_{oss} of all four switches is charged to the half of the output voltage V_{out}. When the switches begin to turn-ON because of the zero load current, the energy stored in C_{oss} cannot be discharged before the switches turning ON.

The zero load current and large C_{oss} of the LV high-current Si devices raise two concerns: first, the energy stored in C_{oss} will

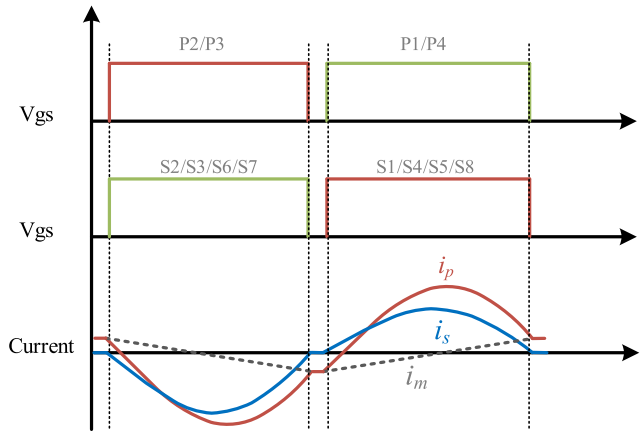


Fig. 8. Ideal waveforms of the DCX.

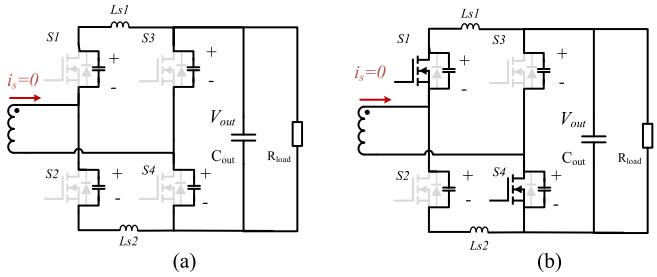


Fig. 9. Switching transient of the secondary side. (a) During deadband. (b) Turn-ON transient.

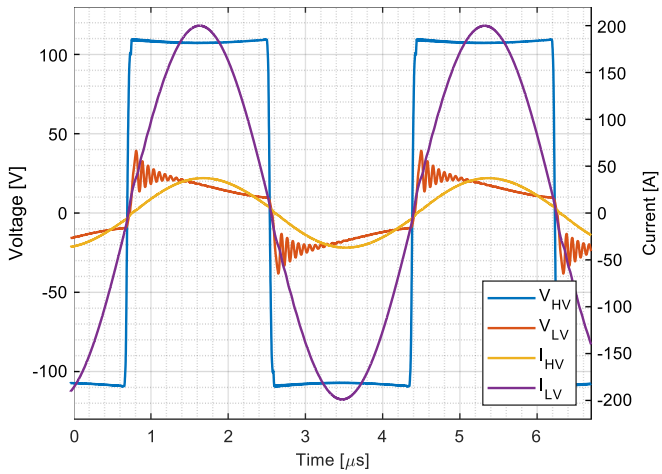


Fig. 10. Simulation results showing the spike of partial ZVS.

be dissipated in the channel as a loss; second, when the channel is turned ON, the voltage of upper C_{oss} will decrease sharply and the complementary side C_{oss} will be charged by the output capacitor, which induces a relatively high *di*/*dt* creating a potential oscillation and overvoltage scenario, as shown in Fig. 10. The spike is particularly dangerous for the LV-side switches because of their low voltage rating.

As a solution, this article proposes a simple control strategy to achieve ZVS, i.e., imposing extra time delay, as illustrated in

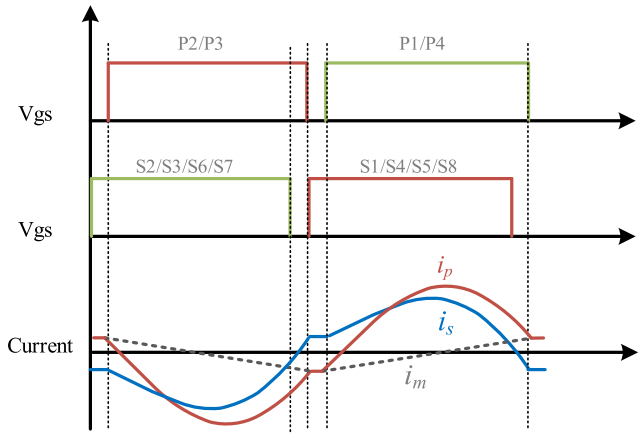


Fig. 11. Typical waveforms when the time delay is inserted.

Fig. 11. When operated in the buck mode, the primary-side gate signals are delayed for a certain time interval. The deadband of the secondary side occurs before the primary side, and a phase difference between the primary and the secondary side current is created. During the secondary-side deadband, the current is no longer zero and there is a certain amount of load current delivered to the secondary side to discharge the $C_{\rm oss}$ before the switches turn-ON. ZVS turn-ON for both sides is then realized.

The relationship between the discharge time and all parallel $Q_{\rm oss}$ is given as follows:

$$\int_0^{t_d} I_{\rm peak} \sin\left(\frac{t_d}{T_s}\cdot 2\pi t\right) dt \;=\; 4Q_{\rm oss} \tag{9}$$

where $I_{\rm peak}$ is the peak current on the transformer secondary side. When ignoring the impact of the deadband and losses, $I_{\rm peak}$ can be expressed when the loss is ignored as

$$I_{\rm peak} = \frac{\sqrt{2}P_{\rm out}}{2\times V_{\rm out}}. \tag{10}$$

To calculate the needed delay time t_d, the sinusoidal current wave can be regarded as a linearly increasing one, as long as the phase angle is small enough, $\theta \approx \sin(\theta)$. Then, the charging process of $C_{\rm oss}$ can be simplified as

$$\frac{1}{2}\times t_d \times \frac{t_d}{Ts}\times 2\pi \times \; I_{\rm peak} = \; 4Q_{\rm oss}. \tag{11}$$

Together with (10), the delay time t_d is calculated in the following equation, where $t_{d\rm on}$ is the switch's turn-ON delay:

$$t_d = \; 2\sqrt{\frac{\sqrt{2}T_s Q_{\rm oss} V_{\rm out}}{\pi P_{\rm out}}} + t_{d\rm on}. \tag{12}$$

In the boost mode, the principle is the same but the delay will be on the secondary side.

IV. DC-Bias Current Detection and Elimination

For a low power and unidirectional resonant type converter, the dc-bias current of the transformer is usually not a critical issue because the resonant capacitor naturally blocks the dc offset. However, in the proposed bidirectional high-power converter, the secondary-side *H*-bridge has to actively switch to push the energy back in the boost mode. It is difficult to equip the dc-blocking capacitor at the LV side because the ac current is >500 A. However, without capacitors, any small variation in the device parameters or a control error can result in an unbalanced square voltage at the LV side, yielding a large dc current offset.

For example, the proposed converter has a transformer with a winding resistance of 0.4 $\rm m\Omega$. A 10 mV unbalanced voltage can generate a 25 A dc-bias current. Two major concerns are exposed when such a dc bias exists. First, the large dc bias makes the peak magnetizing current increased by 25 A, potentially saturating the transformer core. Second, with the dc bias, the magnetizing current becomes a unipolar waveform, potentially resulting in no negative magnetizing current to discharge $C_{\rm oss}$ before the switch turns ON. ZVS will be lost and higher switching loss occurs. Therefore, the dc bias active control at such a power level needs to be considered.

The dc-bias detection methods proposed in the previous research can be categorized into two types, i.e., direct flux measurement and indirect measurement. In the first scenario, the most straightforward method is the use of a Hall sensor to measure the flux in the airgap [34]. A specialized core structure can also measure the flux. For instance, Patel [35] and Klopper and Ferreira [36] proposed to use an external core parallelled with the main core to sense the core's saturation. But in cases where dc bias exists without saturating the core, these methods will not work. Adding an external winding instead of the core is another option studied in [37] and [38] but these windings add extra cost and are subject to high current levels. Ortiz *et al.* [39] proposed a "magnetic ear" method, where the external core is not only a passive sensor but also excited by an external source. It is capable of detecting the dc bias even when the core is not saturated. However, this approach is complicated.

The second type of detection does not measure the flux itself. Instead, related electric signals are measured and processed to estimate real bias. Dutta and Bhattacharya [40] proposed a method of measuring the primary-side and secondary-side current to calculate the dc bias. In the case of the APM, it is difficult to measure the high-frequency transformer current with hundreds of ampere peak. Since the dc bias is induced by the unbalanced voltage, Wilson [41] proposed to measure the voltage across the transformer. As already noted, this voltage unbalance is typically tiny and it is hard to measure accurately.

A novel and simple dc current detection and elimination method is proposed in this article. As shown in Fig. 12, one extra sampling inductor is paralleled with the secondary-side winding of the transformer. The equivalent circuit is shown in Fig. 13.

The unbalanced voltage source can cause a dc-bias current in the secondary-side winding. So, it can also affect the external detecting inductor. Here $L_d >> L_{\rm sec}$ and $R_{LD} >> R_{\rm sec}$, meaning the current flowing through such detecting inductor is much smaller and yielding such an inductor is easy to manufacture. Meanwhile, the large L_d filters out the high-frequency current ripple and provides a smoother dc current for the current sensor. The large R_{LD} attenuates the peak current through the detecting inductor, resulting in a small, cost-effective current sensor on the LV side.

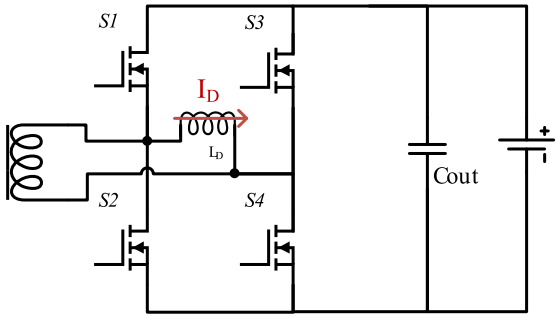


Fig. 12. Proposed dc-bias detecting method.

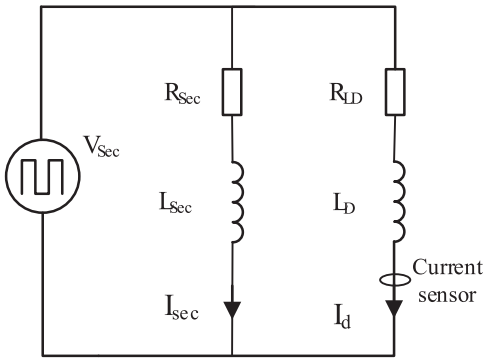


Fig. 13. Model of dc-bias detection circuit.

The steady-state average value of the dc-bias current flowing through the detecting inductor I_d is

$$I_{d\_\mathrm{avg}} = \frac{R_{\mathrm{sec}}}{R_{LD}} \cdot I_{\mathrm{sec}_{\mathrm{avg}}}. \tag{13}$$

The peak-to-peak current ripple in the L_d is solely determined by the inductance, i.e.,

$$I_{d_{p-p}} = \frac{V_{\mathrm{sec}_{p-p}}}{2\pi f_{sw} L_d}. \tag{14}$$

To best track the secondary-side current, the time constants of L_d/R_{LD} and $L_{\mathrm{sec}}/R_{\mathrm{sec}}$ need to be designed equal, i.e.,

$$\tau = \frac{L_{\mathrm{sec}}}{R_{\mathrm{sec}}} = \frac{L_d}{R_{Ld}}. \tag{15}$$

The dc–bias control algorithm in the transformer is then proposed in Fig. 14.

The detected current I_{bias} in Fig. 14 can either be a positive or negative value. With no dc bias being detected, the switches are always run at a duty cycle of 0.5. When there is a positive dc bias, the controller will reduce the duty cycle of *S*1/*S*4 and increase the duty cycle of *S*2/*S*3 to compensate for the unbalanced voltage applied to the winding. When there is a negative dc bias, the controller will reduce the duty cycle of *S*2/*S*3 and increase the duty cycle of *S*1/*S*4.

The simulation results are shown in Fig. 15. The detected current perfectly tracks the trend of the actual current on the secondary side. Once the dc-bias control is enabled, the dc-bias current disappears.

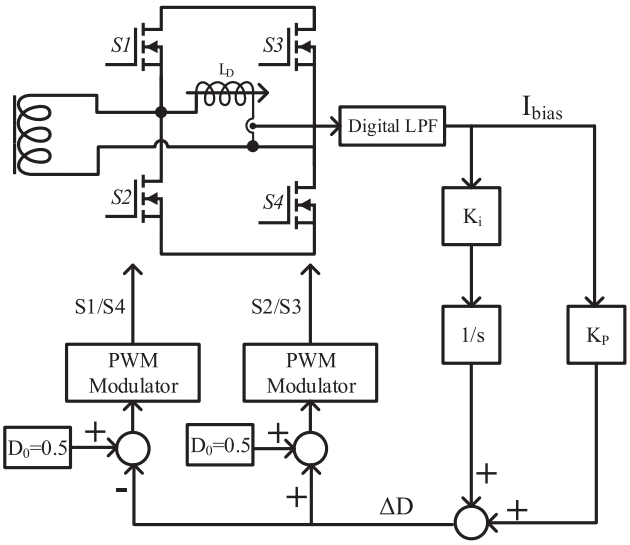


Fig. 14. DC-bias elimination diagram.

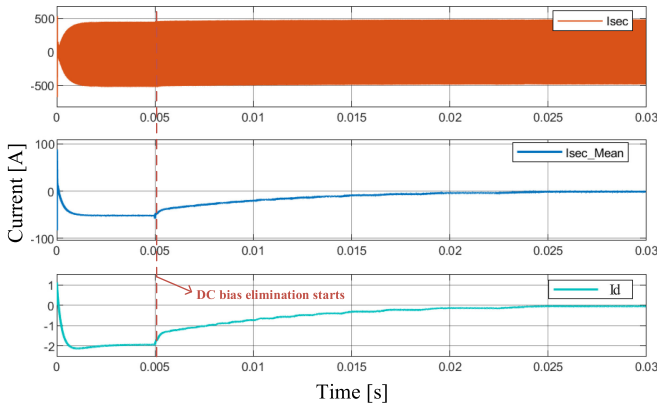


Fig. 15. Simulation results of the proposed dc-bias elimination.

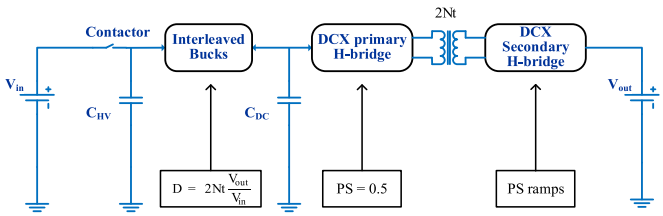


Fig. 16. Simplified model for the precharge mode.

With the proposed method, an off-the-shelf low rating and low-cost current sensor can be easily found to detect the dc bias. For example, if the current of the secondary-side winding contains 25 A dc bias, and the selected detecting inductor has a scale ratio of 12.5:1, the sensor will only see a 2 A dc bias. Finding a commercial sensor to sample a 2 A dc current is easy.

V. Precharging Mode Control

When the EV is not in the drive mode, a contactor ensures the propulsion HV battery is disconnected from the HVdc bus

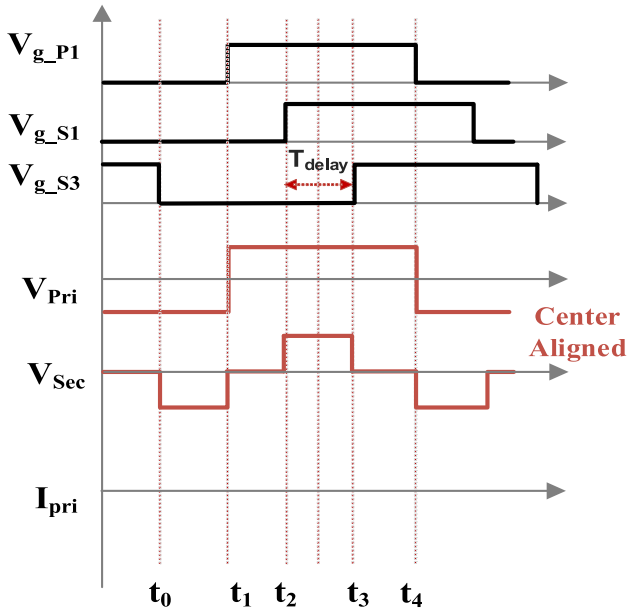


Fig. 17. Typical waveforms of the precharge mode.

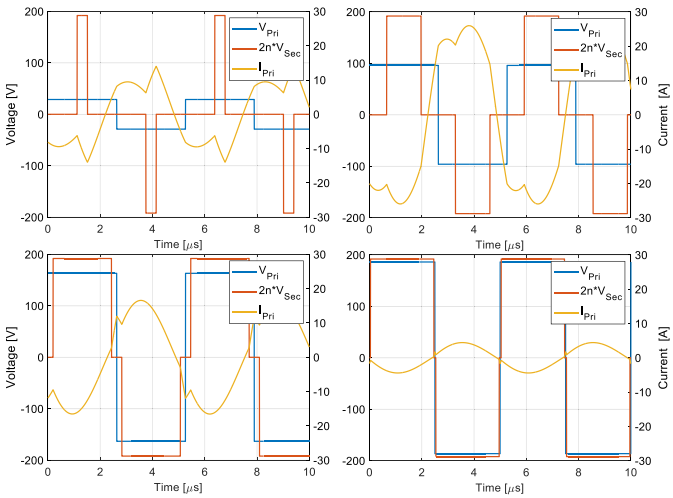


Fig. 18. Simulated waveform when the phase shift ramps up.

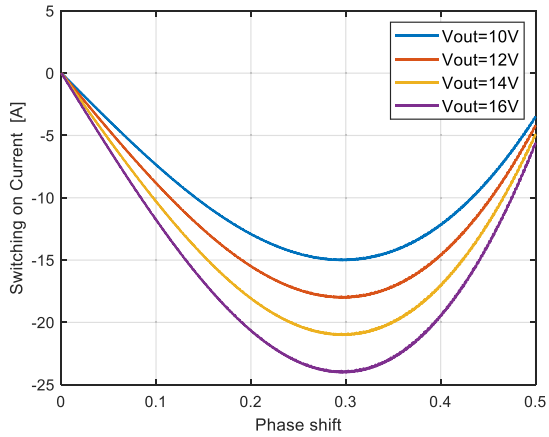
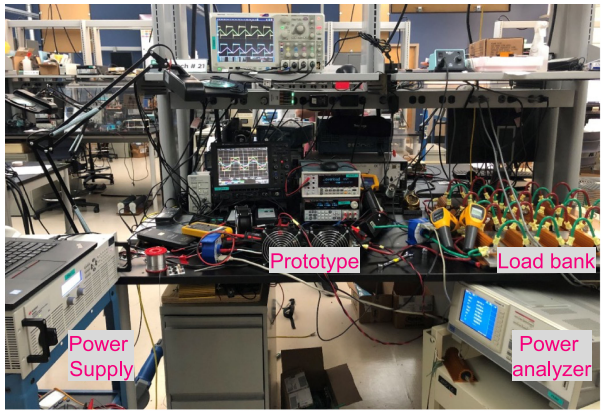


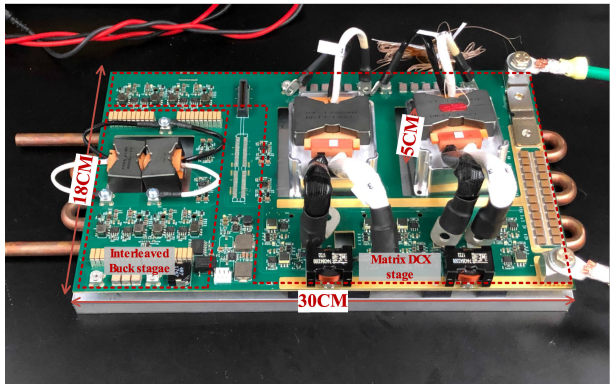
Fig. 19. Turn-ON current versus phase shift.

TABLE I
PROTOTYPE AND TEST PARAMETERS

HV-side switches	C3M0065090J
LV-side switches	IPLU300N04S4
fs (Buck stage)	100kHz~500kHz
fs (DCX stage)	200kHz
Resonant inductance Lr	2.1μH
Resonant capacitance Cr	302nF
Transformer turn ratio n_t (single)	6:1
Transformer magnetizing Lm (single)	30μH
Transformers and inductors core material	DMR96A
Transformer core	PQ-50/35
Inductors core	PQ-32/20
DC link capacitor Cdc	20μF
Buck output inductors L1 and L2	12μH
DC bias detecting Ld	33μH
LV output capacitor Cout	22μF×24pcs



(a)



(b)

Fig. 20. (a) Test setup. (b) APM prototype.

capacitor. When starting up, the HV capacitor is required to be precharged before the contactor is turned ON.

Given that the proposed converter is bidirectional, there is an option to simply use the converter itself to precharge the HVdc bus capacitors. In this case, the voltage across C_{DC} is close to zero in the beginning so a different control is needed to avoid the high short-circuit-like inrush current. Furthermore, even at

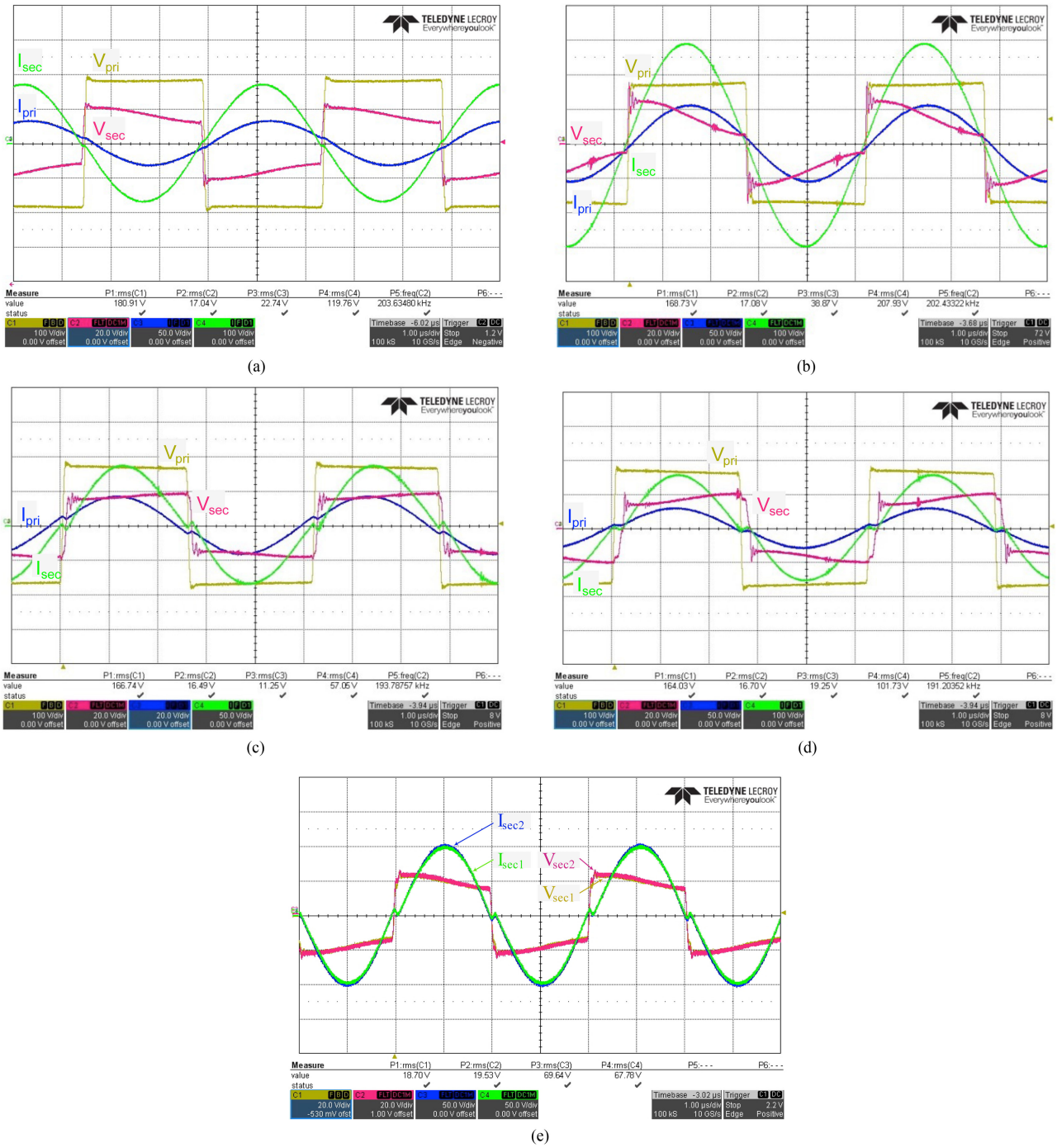


Fig. 21. (a) Buck mode: 16 V/220 A/3.5 kW. (b) Buck mode: 16 V/440 A/7 kW. (c) Boost mode: 16 to 350 V/1.5 kW. (d) Boost mode: 16 to 350 V/3 kW. (e) Current and voltage balancing of matrix transformers.

such transient mode, it is essential that ZVS be maintained for all switches, for the sake of EMI and reliability.

This article proposes a soft starting control strategy for the DCX stage in order to limit the precharging current, which introduces an inner phase shift PS to the secondary side of the DCX. Here, the PS is shown in Fig. 17 and is defined as

$$PS = \frac{T_{\text{delay}}}{T_s}. \tag{16}$$

Note we still have $\mathrm{V_{sec}}$ and $\mathrm{V_{pri}}$ center aligned, although it is different from the conventional two-level output voltage. The inner phase shift of the secondary *H*-bridge generates a three-level output voltage on the LV side. As shown in Fig. 16, the duty cycle of the BUCK stage is kept as a constant value $\mathrm{D} = 2\mathrm{Nt}\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}}$. The dc-bus capacitor $\mathrm{C_{DC}}$ and HV-side capacitor $\mathrm{C_{HV}}$ will be precharged simultaneously.

For the DCX stage, the secondary-side phase shift will gradually increase from 0 to 0.5. It generates an equivalent voltage

starting from zero on the LV side, which matches the voltage of empty HVdc bus capacitors. Thus, the charging current can be effectively limited.

The detailed switching modes and typical waveforms are given in Figs. 17 and 18. In the precharging process, the relatively higher current stress drive a recommendation to maintain ZVS for the switches. To verify the ZVS condition, the switching-ON current on the HV side for different LV-side voltages is plotted in Fig. 19. Note all such currents are negative, indicating that the ZVS is secured under all voltages.

VI. Experimental Results

To verify the proposed two-stage design, a prototype is built and tested with the system parameters given in Table I.

The prototype is shown in Fig. 20(a) and (b). It is assembled with multiple PCBs. The main PCB on the top is for the signals and gate drivers. All power switches are soldered on the metal core PCB, which helps dissipate the heat. The overall size of the converter is $30\times18\times5$ cm^3 with a volume of 2.7 L. The peak power achieved is 7 kW, then the power density is calculated as 2.6 kW/L. This test bench will be used to verify the 3.5 kW rated power output and >6 kW peak output along with the precharge-mode operation and the dc-bias current elimination control.

The power test results in the buck mode are given in Fig. 21(a) and (b) at the rated 3.5 and peak 7 kW, respectively, where $V_{\rm pri}$ and $V_{\rm sec}$ are the primary and secondary-side voltages of the single transformer, and $I_{\rm pri}$ and $I_{\rm sec}$ are the primary and secondary-side currents of the single transformer, respectively. Here $V_{\rm DC} = 12\times16$ V $= 192$ V. The unexpected voltage slope on the LV side is due to the parasitic inductance of the PCB layout. However, this slope does not significantly affect the efficiency, given that the switching actions still occur around the zero current. The test results in the boost mode are given in Fig. 21(c) and (d), where the maximum output power is tested up to 3 kW, boosting from 16 to 350 V. Again, both the switching-ON and switching-OFF currents are close to zero.

To evaluate the balancing of matrix transformers, the voltage and current waveforms of two transformers are tested, as shown in Fig. 21(e). No obvious difference was detected. The reasons include: first, the secondary winding is only one turn, which is easy to control the length and keep the resistance equal; second, even when the unbalance happens, the winding carrying higher current will have a higher temperature than another winding. Due to the MOSFET's positive thermal coefficient, i.e., the higher the temperature, the higher the resistance, the current will then naturally shift to the other side, vice versa. This self-balance mechanism also guarantees a balanced current sharing.

In addition, the matrix transformer is already well studied by the previous work [42]–[45], a similar input-series-output-parallel configuration is adopted and there is no unbalance issue reported either. Therefore, in this article, how to balance the matrix transformer is not the focus.

The proposed method of the dc-bias detection and elimination is also tested. The converter was operated in the boost mode, and the dc bias was intentionally added by introducing an extra 100

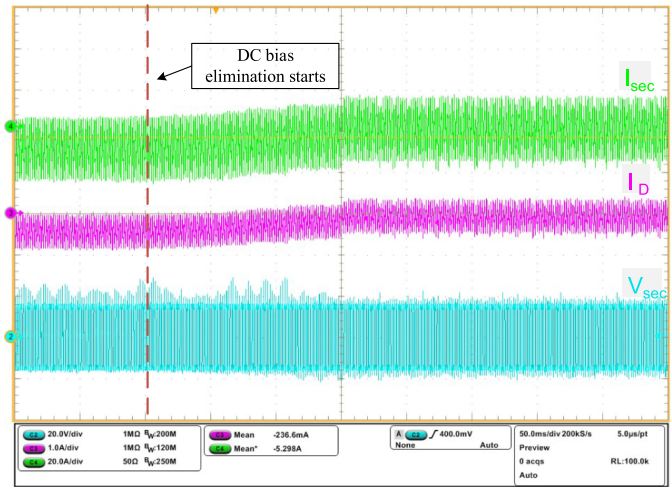
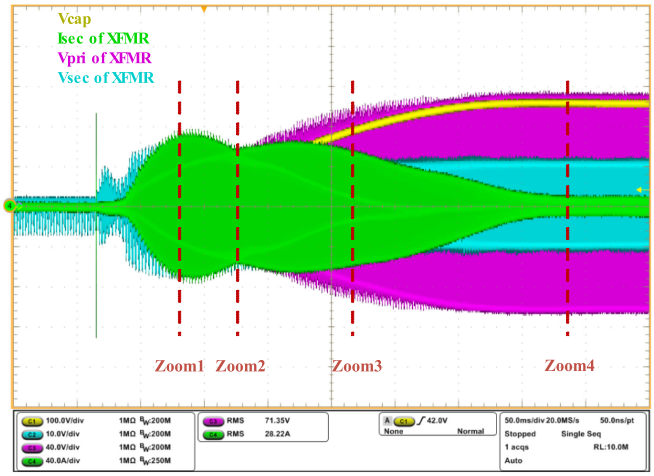
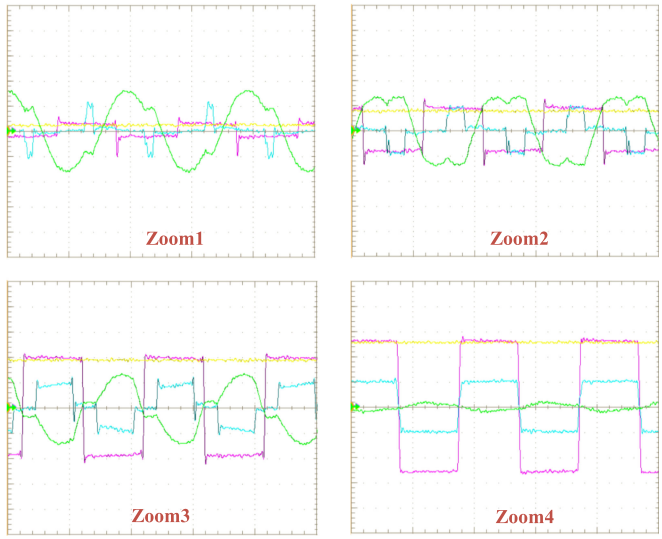


Fig. 22. DC bias elimination.



(a)



(b)

Fig. 23. (a) Precharge process. (b) Zoom-in waveform showing full range ZVS.

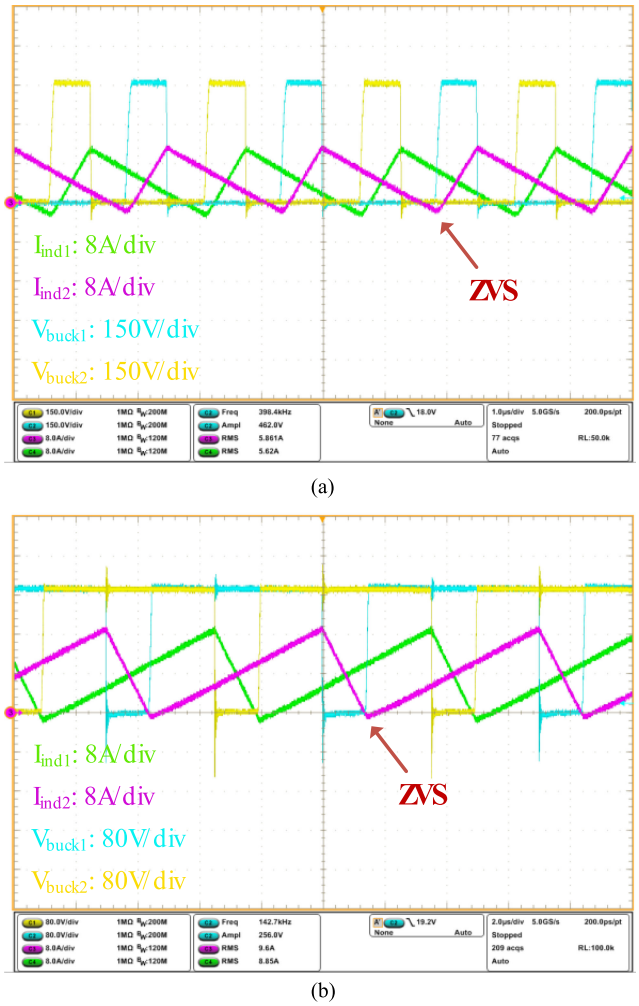


Fig. 24. (a) Buck stage ZVS: $V_{\text{in}} = 450$ V, $V_{\text{out}} = 10$ V, $P_{\text{out}} = 1.2$ kW, and $f_{sw} = 400$ kHz. (b) Buck stage ZVS: $V_{\text{in}} = 250$ V, $V_{\text{out}} = 16$ V, $P_{\text{out}} = 3.5$ kW, and $f_{sw} = 140$ kHz.

ns deadband error for $S3$ and $S4$, compared with $S1$ and $S2$. The tested waveform is shown in Fig. 22, where V_{sec} and I_{sec} are the secondary-side winding voltage and current, respectively, and I_D is the current of the external detecting inductor. Before the dc elimination control starts, both I_{sec} and I_{D} have certain dc bias. After the elimination control starts, the dc component in I_D is gradually attenuated and the dc bias in the transformer windings is also reduced. This test validated the proposed control.

Fig. 23(a) shows the precharging process waveform. The converter is powered by a 14 V voltage source to charge a 2.5 mF capacitor. The capacitor was charged to 400 V within 400 ms with the peak charging current being 80 A. The charging current was successfully suppressed with the inner phase shift control. The zoomed waveforms of the whole process are given in Fig. 23(b). The results show that when the inner phase shift is applied, the ZVS can still be secured in the whole precharging process.

The interleaved buck converters were also tested, as shown in Fig. 24. With the variable frequency control, the soft turn-ON is secured under all the operation scenarios.

Finally, the measured efficiency of the buck mode is shown in Fig. 25(a). The peak efficiency is >96%. The dashed line is

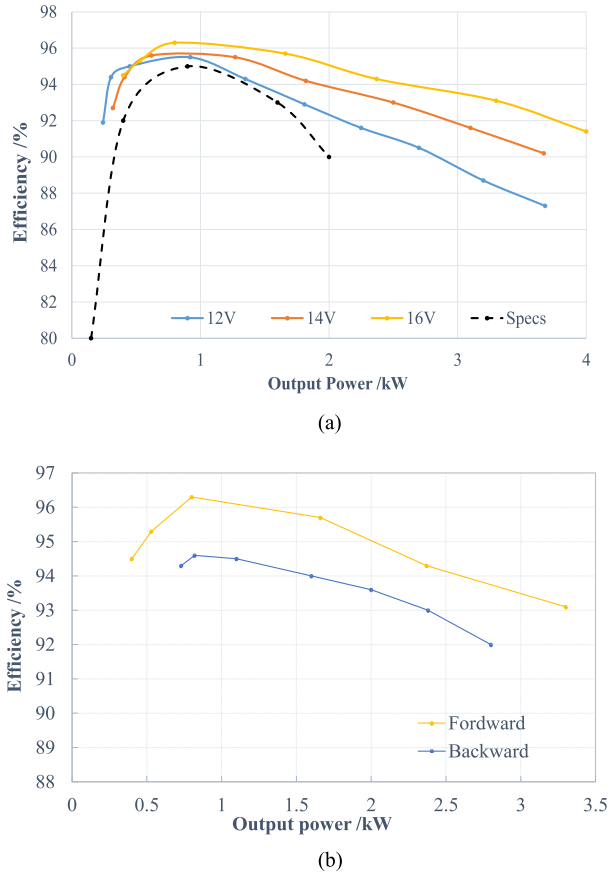


Fig. 25. (a) Forward-mode efficiency. (b) Efficiency comparison: buck mode versus boost mode.

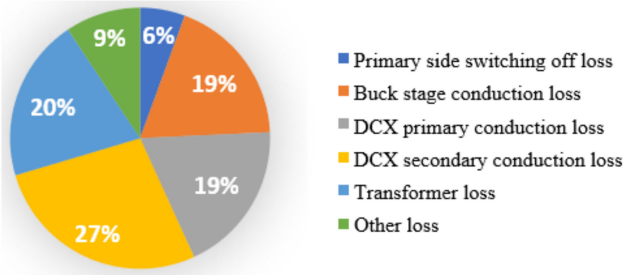


Fig. 26. Loss breakdown at 3.5 kW rated output.

the design specs, which show the experimental result is better than the target. The efficiency of the buck and boost modes are compared in Fig. 25(b). The peak efficiency of the boost mode is higher than 94%. Overall, the boost mode has a lower efficiency than the buck mode. The main reason is that in the boost mode, the secondary-side H-bridge has to switch OFF at a relatively higher current, yielding extra switching losses.

The loss breakdown is shown in Fig. 26. Although the proposed design has two stages, because the DCX stage is always operated at the resonant frequency, there are almost no switching losses from this stage. The majority of the losses are the conduction loss instead of the switching losses. This explains why the converter can still maintain a higher efficiency as compared with a single-stage design.

TABLE II
SPECIFICATIONS AND PERFORMANCE COMPARISON

Production/prototype	Peak Power	PEAK EFFICIENCY	POWER DENSITY
Martek Power [46]	2 kW	90%	0.26 kW/L
TDI Power [47]	3 kW	94%	0.526 kW/L
Brusa [48]	3.5 kW	93.5%	1.11 kW/L
Bel Power [49]	4 kW	93%	0.38 kW/L
Aegis [50]	2.4 kW	82%	0.6 kW/L
CRRC [23]	3.5 kW	87%	2 kW/L
ETH [51]	2 kW	90%	1.63 kW/L
Proposed design	6~7 kW	96%	2.6 kW/L

VII. CONCLUSION

This article presented a design and respective test results for a high-power dc/dc converter for APM applications in EVs. The two main challenges were the wide voltage range and high current capability. The challenge was met by using two stages, i.e., the buck stage to handle the wide voltage range and DCX stage to cope with the high current. The low current stress of the DCX stage allowed the designed converter to achieve >6 kW power capability and >96% peak efficiency. High efficiency also means there is no need to parallel a massive amount of switches, which further benefits the size. As a result, even it is a two-stage design, it still exhibits superiorities compared with most of the products and related research, as given in Table II.

In addition, to further extend the versatility, a novel and simple dc-bias detection and elimination method, along with a precharge control using the inner-phase shift, is proposed in the article as well. The test results show the converter can effectively eliminate the dc bias and precharge the capacitor with a controllable current. More importantly, the ZVS turn-ON can still be secured in the precharging process.

As shown in the experimental waveforms, the secondary-side voltage still has some slope, caused by the parasitics inductance in the PCB loop. Future work will focus on the minimization of the parasitic inductances.

REFERENCES

[1] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[2] X. Pan and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated dc/dc converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[3] I.-O. Lee and G.-W. Moon, "Analysis and design of phase-shifted dual H-bridge converter with a wide ZVS range and reduced output filter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4415–4426, Oct. 2013.

[4] R. T. Naayagi, "Electromagnetic compatibility issues of dual active bridge DC-DC converter," in *Proc. Int. Conf. on Energy Efficient Technol. Sustain.*, 2013, pp. 699–703.

[5] H. Nie, Y. Bai, Q. Cheng, and M. J. Scott, "Evaluation of conducted EMI in GaN and Si based isolated DC/DC converters," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl.*, 2019, pp. 251–254.

[6] Y. Jang, M. M. Jovanovic, M. Kumar, J. M. Ruiz, R. Lu, and T. Wei, "Isolated, bi-directional dc-dc converter for fuel cellelectric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 1674–1681.

[7] C. Duan *et al.*, "Design of a 2.5kW 400V→M2V high-efficiency dc/dc converter using a novel synchronous rectification control for electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1082–1086.

[8] Z. Nie, W. D. Williams, C. Duan, W. Guo, and K. H. Bai, "System optimization of a high-power and high-step-down accessory power module for electric vehicles," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1926–1931.

[9] A. Kawahashi, "A new-generation hybrid electric vehicle and its supporting power semiconductor devices," in *Proc. 16th Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 23–29.

[10] A. Emadi, *Advanced Electric Drive Vehicles*. Boca Raton, FL, USA: CRC Press, 2014.

[11] R. Hou and A. Emadi, "Evaluation of integrated active filter auxiliary power modules in electrified vehicle applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 6314–6319.

[12] C. L. Zhu, M. Shen, and M. Obrigkeit, "A high power DC/DC converter designed for single coolant loop hybrid electric vehicle application," SAE Tech. Papers, 2010, doi: 10.4271/2010-01-1254.

[13] O. García, L. A. Flores, J. A. Oliver, J. A. Cobos, and J. de la Peña, "Bi-directional dc/dc converter for hybrid vehicles," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, 2005, pp. 1881–1886.

[14] E. Honey, I.-S. Suh, and S. R. Ryu, "Practical considerations on the electrical safety of the high power system in a prototype EV," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2013, pp. 250–255.

[15] C. K. Gowda, V. G. Khedekar, N. Anandh, L. R. S. Paragond, and P. Kulkarni, "Bidirectional on-board EV battery charger with V2H application," in *Proc. Innov. Power Adv. Comput. Technol.*, 2019, pp. 1–5, doi: 10.1109/i-PACT44901.2019.8960126.

[16] H. Sakata, T. Oosawa, and A. Matsumoto, "Car power source apparatus," U.S. Patent No. 8,063,506. Nov. 22, 2011.

[17] M. K. Ozguc, E. Ipek, K. Aras, and K. Erhan, "Comprehensive analysis of pre-charge sequence in automotive battery systems," *Trans. Environ. Elect. Eng.*, vol. 4, no. 1, pp. 1–6, 2019, doi: 10.22149/teee.v4i1.136.

[18] M. R. Vemparala, S. R. SomaSundaram, S. M. Anandkrishnan, B. Ashok, and C. Kavitha, "Implementation of real time low voltage system for enhancement of safety in an electric vehicle," in *Proc. Int. Conf. Inf. Commun. Embedded Syst.*, 2016, pp. 1–6.

[19] Z. Pang, X. Ren, J. Xiang, Q. Chen, X. Ruan, and W. Chen, "High-frequency DC-DC converter in electric vehicle based on GaN transistors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7.

[20] F. Beg, "A novel design methodology for a 1.5 KW dc/dc converter in EV and hybrid EV applications," *Int. J. Elect. Comput. Eng.*, vol. 8, pp. 1497–1500, 2014.

[21] P. Xuewei and A. K. Rathore, "Comparison of bi-directional voltage-fed and current-fed dual active bridge isolated dc/dc converters low voltage high current applications," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, 2014, pp. 2566–2571.

[22] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC-DC converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.

[23] M. R. Ahmed and Y. Li, "A low-cost, high-power-density DC-DC converter for hybrid and electric vehicle applications," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. 1–8.

[24] Z. Hu, L. Wang, Y. Qiu, Y.-F. Liu, and P. C. Sen, "An accurate design algorithm for LLC resonant converters—Part II," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5448–5460, Aug. 2016.

[25] Z. Li, H. Lin, W. Mao, C. Cai, X. Guo, and Z. Shu, "Optimized parameter design of an improved LLC resonant converter," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6, doi: 10.1109/PEAC.2018.8590343.

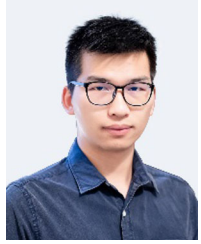
[26] Y. Yan, H. Bai, A. Foote, and W. Wang, "Securing full-power-range zero-voltage switching in both steady-state and transient operations for a dual-active-bridge-based bidirectional electric vehicle charger," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7506–7519, Jul. 2020.

[27] K. Shi, D. Zhang, Z. Zhou, M. Zhang, D. Zhang, and Y. Gu, "A novel phase-shift dual full-bridge converter with full soft-switching range and wide conversion range," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7747–7760, Nov. 2016.

[28] D. Murthy-Bellur, B. Palmer, K. Iyer, M. Cai, and H. Yang, "Commercial DC-DC converters: A survey of isolated low-voltage very-high-current systems for transportation electrification," in *Proc. IEEE Power Energy Conf. Illinois (PECI)*, Champaign, IL, 2017, pp. 1–8, doi: 10.1109/PECI.2017.7935745.

[29] J.-H. Park and B.-H. Cho, "The zero voltage switching (ZVS) critical conduction mode (CRM) buck converter with tapped-inductor," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 762–774, Jul. 2005.

[30] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. 7th Annu. IEEE Appl. Power Electron. Conf. Expo.*, vol. 2, 2002, pp. 1108–1112.
[31] Q. Qian, S. Xu, J. Yu, W. Sun, and H. Li, "A digital detecting method for synchronous rectification based on dual-verification for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2091–2097.
[32] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012.
[33] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driven synchronous rectifier for series–parallel resonant (LLC) DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 289–297, Jan. 2011.
[34] R. Nalepa, F. Grecki, M. Ostrogorska, P. Aloszko, and J. Duc, "DC-bias current measurement in high power AC grids," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013.
[35] R. Patel, "Detecting impending core saturation in switched-mode power converters," in *Proc. Powercon*, 1980, vol. 7, pp. 1–11.
[36] S. Klopper and J. A. Ferreira, "A sensor for balancing flux in converters with a high-frequency transformer link," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 774–779, May/Jun. 1997.
[37] A. Gertsman and S. Ben-Yaakov, "Zeroing transformer's DC current in resonant converters with no series capacitors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 4028–4034.
[38] P. Ripka, "Review of fluxgate sensors," *Sensors Actuators A, Phys.*, vol. 33, no. 3, pp. 129–141, Jun. 1992, doi: 10.1016/0924-4247(92)80159-Z.
[39] G. Ortiz, L. Fassler, J. W. Kolar, and O. Apeldoorn, "Flux balancing of isolation transformers and application of 'the magnetic ear' for closed-loop volt–second compensation," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4078–4090, Aug. 2014.
[40] S. Dutta and S. Bhattacharya, "A method to measure the DC bias in high frequency isolation transformer of the dual active bridge DC to DC converter and its removal using current injection and PWM switching," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 1134–1139.
[41] D. Wilson, "A new pulsewidth modulation method inherently maintains output transformer flux balance," in *Proc. Powercon*, 1981, vol. 8, pp. 1–15.
[42] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High efficiency two-stage 48V VRM with PCB winding matrix transformer," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.
[43] D. Huang, S. Ji, and F. C. Lee, "Matrix transformer for LLC resonant converters," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2078–2083.
[44] D. Huang, S. Ji, and F. C. Lee, "LLC resonant converter with matrix transformer," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4339–4347, Aug. 2014.
[45] C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density LLC converter with an integrated planar matrix transformer for high-output current applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9072–9082, Nov. 2017.
[46] PS2450, Martek Power Inc., 2014. [Online]. Available: http://www.martekpower.com/files/pdf/PS2450__440.pdf
[47] LSM3k0-400-12, TDI Power Inc., Hackettstown, NJ, USA, 2014. [Online]. Available: http://ep-power.com/wp-content/uploads/2018/05/LSM3k.pdf, Accessed: Aug. 1, 2020.
[48] BSC624-12V-B, BRUSA Elektronik, Sennwald, Switzerland, 2012. [Online]. Available: https://www.brusa.biz/_files/bsc/BSC6/Customer_data/1_Manuals/BSC623-12V_Manual_EN(UK).pdf, Accessed: Aug. 1, 2020.
[49] 350DNC40-12, Bel Power Solutions Inc., Jersey City, NJ, USA, 2017. [Online]. Available: https://belfuse.com/resources/datasheets/powersolutions/ds-bps-350dnc40-12-series.pdf, Accessed: Aug. 1, 2020.
[50] AEGIS, "HEV2400," 2015. [Online]. Available: https://www.aegispower.com/images/product-spec-sheets/HEV2400_Spec_Sheet.pdf, Accessed: Aug. 1, 2020.
[51] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," in *Proc. 14th Annu. Meeting Conf. Rec. Ind. Appl. Conf.*, 2005, vol. 1, pp. 599–606.

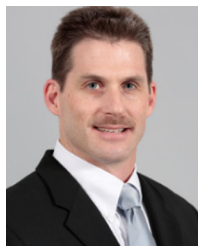


Liyan Zhu (Student Member, IEEE) received the B.S. degree from the Department of Electrical Engineering, Kunming University of Science and Technology, Kunming, China, in 2017. He is currently working toward the Ph.D. degree with the Center for Ultrawide-Area Resilient Electric Energy Transmission Networks, University of Tennessee, Knoxville, TN, USA.

His research interests include WBG device-based dc/dc converters, magnetic components, fast chargers, and auxiliary power modules in EV.

Hua Bai (Senior Member, IEEE) received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2002 and 2007, respectively.

He was a Postdoctoral Fellow and Research Scientist with the University of Michigan-Dearborn, Dearborn, MI, USA, in 2007 and 2009, respectively. From 2010 to 2016, he was an Assistant Professor with the Department of Electrical and Computer Engineering, Kettering University, Flint, MI, USA. From 2017 to 2018, he was an Associate Professor with the University of Michigan-Dearborn. He is currently an Associate Professor in the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville. His research interests include power electronic modeling, control and integration, including variable frequency motor drive system, HV and high-power dc/dc converter, electric vehicle battery chargers, and various wide-bandgap device applications.



Alan Brown received the B.Sc. degree in electrical engineering from the Michigan State University, East Lansing, MI, USA, in 1992.

He is currently a Senior Power Electronics Engineer for HELLA Electronics Corporation, Plymouth, MI, USA. His responsibilities include the development of high-power dc/dc converters, ac/dc onboard chargers, and fuel-saving technologies for micro and mild hybrids.

Matt McAmmond received the B.S. degree in electrical engineering from Kettering University, Flint, MI, USA, in 1993, and the M.B.A. degree from Oakland University, Rochester, MI, USA, in 1996.

He is an Advanced Engineering Manager with HELLA Electronics Corporation, Plymouth, MI, USA. He manages a team that designs power electronics with a focus on chargers and driver assistance systems with a focus on LiDAR. Prior to joining HELLA, he was part of the founding team with Pixel Velocity, a startup producing high-resolution video cameras and advanced algorithms for wide-area surveillance applications.