Bidirectional Synchronous Rectification ON-Line Calculation Control for High Voltage Applications in SiC Bidirectional LLC Portable Chargers

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***Abstract*—With 700 V bus voltage in the SiC bidirectional *LLC* converters, high *dv/dt* is up to 35 kV/μs with 20 ns switching speed, which causes high common mode noise and poses serious challenge for synchronous rectification (SRs) control. A digital bidirectional SR online calculation control is proposed for 700 V high voltage at 300 kHz. It not only achieves bidirectional operation with high efficiency, but also applies to high voltage since it owns high immunity to the switching noise without any detection circuits. The mathematical model is built to calculate the SR conduction time online in the forward and reverse modes, and determine the SR turn OFF instant considering the switching frequency and load. The transformer dc bias is analyzed in the reverse mode. A 6.6-kW SiC bidirectional portable charger was built. The *LLC* efficiency of forward and reverse modes is improved by 0.3% and 0.2% over the conventional SR control at full load, respectively.**

***Index Terms*—Bidirectional, charger, electric vehicle, high voltage, LLC, SiC, synchronous rectification.**

I. Introduction

NOWADAYS, the onboard chargers or portable off-board chargers combined with vehicle-to-grid, vehicle-to-vehicle, and vehicle-to-home have been attractive because they can feed the battery energy back to the grid or support standalone loads such as the urgent rescue or outdoor lighting [1]–[3]. Moreover, combining the SiC MOSFETs and soft-switching capability, the *LLC* converters are promising for bidirectional chargers [4]–[7].

Compared to the onboard chargers, the portable chargers can be replaced conveniently with low after-service cost. However, to meet different electric vehicle (EV) battery voltage levels, the output voltage of portable charger needs to be wider. High efficiency and compact size are extremely important.

In our previous work [8], a bidirectional SiC *LLC* onboard charger was built as shown in Fig. 1. The interleaved totem-pole bridgeless power factor correction (PFC) can achieve bidirectional function and high efficiency. It is beneficial to use SiC MOSFETs to realize high bus voltage from 380 to 700 V. The *LLC* converter with 900-V SiC MOSFETs achieves compact size and high efficiency at 300 kHz.

However, two important issues should be further analyzed. One thing is that the bidirectional synchronous rectification (SR) scheme only considers the switching frequency and neglects the load variations. The SR ON-time is obtained roughly from the primary-side driving signals with the margin of dead time. There is no mathematical model to help quantitative analysis considering the different out voltage and current.

The other important thing is that since there are no blocking capacitors at the *LLC* transformer input in the reverse mode, the unmatched conduction time may cause nonzero voltage-second area generating the dc bias current, which may cause the transformer saturation. Therefore, this should be analyzed clearly.

Recently, digital SR driving schemes have been adopted for the bidirectional chargers [9]–[11]. Normally, the reported digital SR driving schemes are categorized as the drain-source voltage sensing methods and model-based methods.

The first category is sensing the SR drain-source voltage (v_{ds_SR}) by an SR integrated circuit (IC), which communicates with a digital controller to turn ON/OFF the SR MOSFETs. As the SR body diode conducts, the IC sends a pulse to the digital controller and the SR duty cycle will be increased or decreased by the digital controller [12]–[14]. The method is effective at low out voltage as tens of volts, but it can be hardly applied at high voltage (up to 700 V). Moreover, the SR IC is also not transparent to designers. Due to high *dv/dt* and series noise in the high voltage and high power application, if the ICs functions improperly, it is difficult for the engineers to debug the circuit and locate the problem.

The secondary category is the model-based approach, which is based on the *LLC* model without sensing v_{ds_SR}. By using the *LLC* simulation model, the turn ON/OFF delay times of SRs are simulated and preset in two look-up tables in [15]. However, it only considers the output current and neglects the battery voltage variations, so that it can hardly reflect the actual output power

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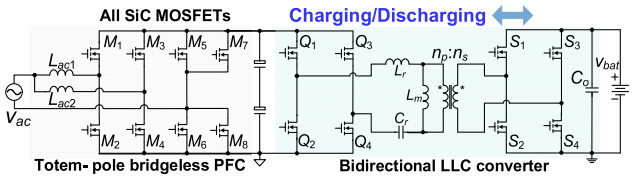


Fig. 1. Bidirectional *LLC* charger.

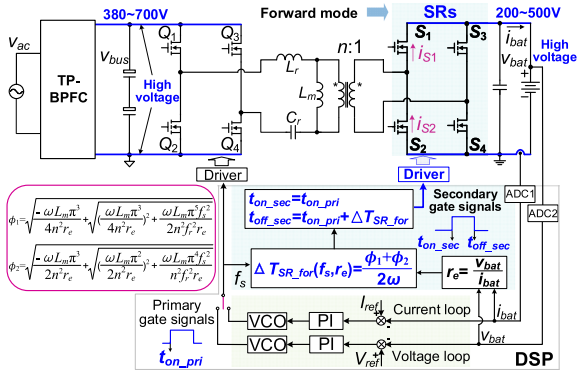


Fig. 2. Proposed bidirectional online calculation control in forward mode.

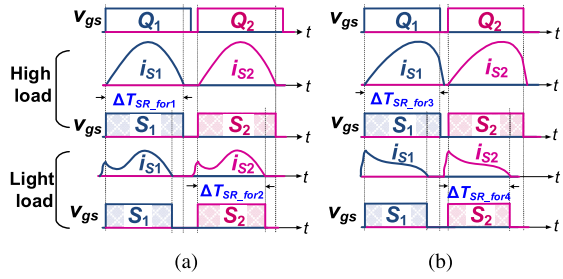


Fig. 3. Waveforms for proposed SR control in forward mode. (a) Below the resonance. (b) Above the resonance.

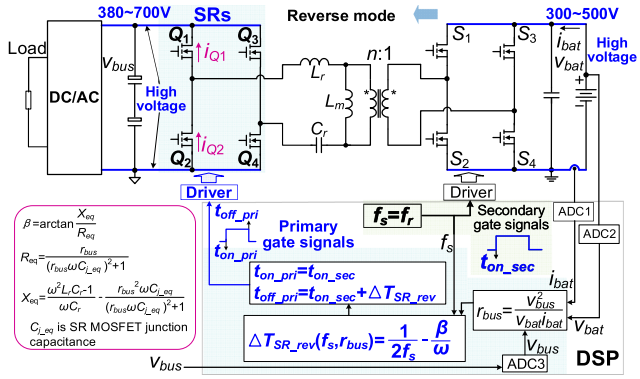


Fig. 4. Proposed bidirectional online calculation control in reverse mode.

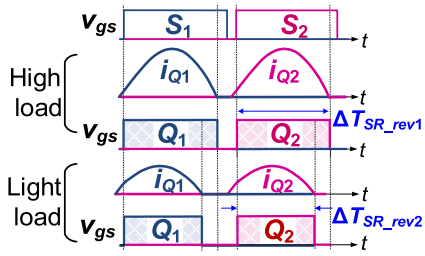


Fig. 5. Waveforms for proposed SR control in reverse mode.

and the SR driving signals are inaccurate. Two similar SR driving schemes are also proposed in [16] and [17] with optimal fixed SR ON-time. It is unsuitable for the bidirectional *LLC* because it neglects the load variations and loses a large SR duty cycle, which results in higher ON-time of SR body diode causing higher conduction loss.

In the reverse mode, the magnetizing inductance is in parallel with the input voltage and the *LLC* operation is similar to the *LC* resonant converter. Bidirectional *LLC* converters in [18]–[20] mainly focus on the implementation or seamless transition of bidirectional operation, while the dc bias issue for the *LLC* in the reverse mode is not addressed.

The contribution of this article is to propose a bidirectional SR control by building mathematical models to calculate the SR ON-time online and achieve high efficiency for the bidirectional *LLC* converter with 700 V bus voltage at 300 kHz. The transformer dc bias is analyzed for the *LLC* in the reverse mode.

II. Proposed Digital Bidirectional SR Online Calculation Control and DC Bias Analysis

A. Proposed Bidirectional SR Online Calculation Control

In the forward mode, the proposed SR control is shown in Fig. 2 and the waveforms are shown in Fig. 3. The mathematical model $\Delta T_{\mathrm{SR\_for}}$ (f_s, r_e) is built to calculate the SR conduction time online, which considers the variations of switching frequency f_s and load r_e. The SR turn-on instant $t_{\mathrm{on\_sec}}$ is identical to the primary-side driving signal and the turn-OFF instant $t_{\mathrm{off\_sec}}$ is equal to $t_{\mathrm{on\_sec}}$ plus the calculated conduction time $\Delta T_{\mathrm{SR\_for}}$. The calculation process is finished in the digital signal process (DSP).

The battery voltage ranges from 200 to 500 V and the bus voltage is regulated from 380–700 V to track the battery voltage. From Fig. 3, as the load and the switching frequency vary, the proposed SR control adapts to the variations to reduce the conduction loss and optimize the efficiency.

Compared to the conventional SR methods used in the unidirectional application of 400 V bus voltage and low output voltage/ high output current [12]–[14], the proposed SR control is applied in the bidirectional *LLC* operation with 700 V bus voltage and 500 V battery voltage.

In the reverse mode, the SR control is proposed in Fig. 4 and the waveforms are shown in Fig. 5. The *LLC* operation in the reverse mode is similar to the *LC* resonant converter. The proposed SR control tracks the load variations by building the mathematical model $\Delta T_{\mathrm{SR\_rev}}$ (f_s, r_{bus}). The SR turn-ON instant $t_{\mathrm{on\_pri}}$ is identical to the secondary-side gate signal and the turn-OFF instant $t_{\mathrm{off\_pri}}$ is equal to $t_{\mathrm{on\_pri}}$ plus the calculated ON-time $\Delta T_{\mathrm{SR\_rev}}$.

From Fig. 5, the proposed SR control is adaptive to the load variations to reduce the conduction loss and increase the efficiency.

The advantages of the proposed SR control include the following.

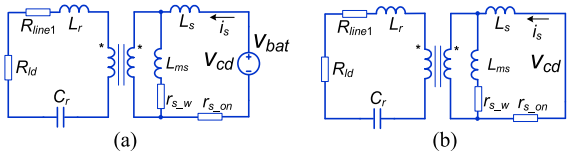


Fig. 6. *LLC* equivalent circuits in reverse mode. (a) Mode 1: $[t_0, t_1]$. (b) Mode 2: $[t_1, t_2]$.

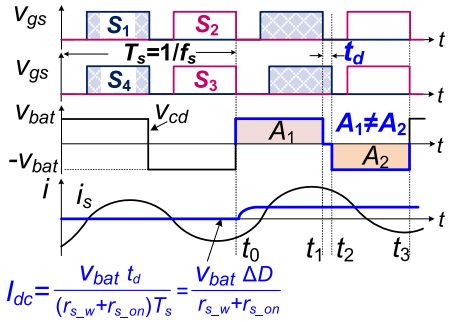


Fig. 7. DC bias current for the *LLC* converter in reverse mode.

1) It achieves bidirectional *LLC* function and is adaptive to the variations of switching frequency and load. The efficiency is improved by decreasing the ON-time of SR body diode and reducing the conduction loss.
2) It is based on the mathematical model without sensing any high frequency current/ voltage. It has high immunity to the switching noise and is suitable for 700 V high voltage at 300 kHz applications.
3) The sampled signals of dc current and voltage that have been used in the closed-loop control, are reused in the proposed control. Therefore, the control is achieved without adding any costs.

B. Proposed DC Bias Analysis for LLC *in Reverse Mode*

The dc bias analysis for *LLC* in the reverse mode is presented to calculate the dc bias current and evaluate the transformer saturation or not. The *LLC* equivalent circuits in the reverse mode are shown in Fig. 6. $R_{\rm ld}$ and $R_{\rm line1}$ are the equivalent resistances of load and power loop. r_{s_w} and r_{s_on} are the equivalent resistances of transformer winding and MOSFETs. The dc bias current is shown in Fig. 7 considering the driver delay. A_1 and A_2 are the voltage-second areas.

During $t_0 \sim t_1$ from Fig. 6(a), v_{cd} is equal to $v_{\rm bat}$ and A_1 is $v_{\rm bat}T_{\rm s}/2$. During $t_1 \sim t_2$ from Fig. 6(b), v_{cd} is equal to zero. During $t_2 \sim t_3$, the equivalent circuit is similar to Fig. 6(a) and v_{cd} is $-v_{\rm bat}$, so that A_2 is $v_{\rm bat}(T_{\rm s}/2 - t_d)$.

Therefore, the unequal voltage-second areas in the positive and negative half cycles generate the dc bias current, which is determined by the input voltage, the net duty cycle and the equivalent resistance of power loop.

III. Modeling of Proposed Digital Bidirectional SR Online Calculation Control

The SR conduction times in the forward and reverse modes are calculated online by the mathematical models. The proposed control is suitable for high voltage/ frequency applications and will not be affected by the circuit oscillations caused by high *dv/dt* since the control does not sense any high frequency current/ voltage.

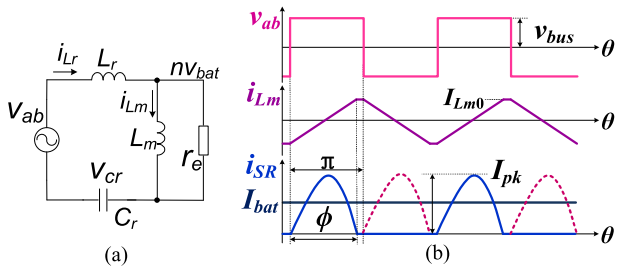


Fig. 8. Forward *LLC* converter. (a) Equivalent circuit. (b) Key waveforms.

A. Calculation of SR Conduction Time in Forward Mode

In order to facilitate the modeling, the rectifier current is assumed as a sinusoidal waveform in the half cycle. The power devices and passive elements are considered as ideal. Fig. 8 shows the *LLC* equivalent circuit and waveforms, which are used to derive the mathematical model of SR conduction time.

From Fig. 8(b), the rectifier current $i_{\rm SR}$ is

$$i_{\rm SR}(\theta) = I_{\rm pk}\sin\left(\frac{\pi}{\phi}\theta\right) \quad 0 \le \theta \le \phi \tag{1}$$

where θ is equal to ωt, ω is the angular switching frequency and t is the real time. ϕ is the SR conduction time angle. $I_{\rm pk}$ is the peak value of rectifier current. $I_{\rm pk}$ can be deduced as

$$\int_0^{\phi} i_{\rm SR}(\theta)d\theta = I_{\rm bat}\phi \tag{2}$$

$$I_{\rm pk} = \frac{\pi^2 I_{\rm bat}}{2\phi} = \frac{\pi^2 v_{\rm bat}}{2\phi r_e} \tag{3}$$

where $I_{\rm bat}$ is the battery current and $v_{\rm bat}$ is the battery voltage. r_e is the equivalent resistance of load. When the SR conducts, the magnetizing inductance current increases or decreases linearly. The magnetizing inductance current i_{Lm} is

$$i_{Lm} = I_{Lm0} + \frac{nv_{\rm bat}}{L_m}t = I_{Lm0} + \frac{nv_{\rm bat}\phi}{\omega L_m}\frac{\theta}{\phi} \tag{4}$$

Where L_m is the magnetizing inductance and I_{Lm0} is the initial current of L_m. n is the transformer ratio. Substituting (3) into (4), it can be rearranged as

$$i_{Lm} = I_{Lm0} + \frac{2nI_{\rm pk}r_e}{\omega L_m}\left(\frac{\phi}{\pi}\right)^2 \tag{5}$$

From Fig. 8(b), v_{ab} denotes the transformer input voltage on the primary side. From Kirchhoff's Law, v_{ab} is

$$v_{ab} = v_{cr} + \omega L_r\frac{di_{Lr}}{d\theta} + \omega L_m\frac{di_{Lm}}{d\theta}. \tag{6}$$

It can be rearranged as

$$v_{ab} = V_{cr0} + \frac{\int (i_{Lm} + i_{\rm SR}/n)d\theta}{\omega C_r} + \omega L_m\frac{di_{Lm}}{d\theta} + \frac{\omega L_r d((i_{\rm SR}/n) + i_{Lm})}{d\theta} \tag{7}$$

Fig. 9. Comparisons of ON-time in forward mode: $v_{\rm bat} = 360$ V and $f_s = 270$ kHz.

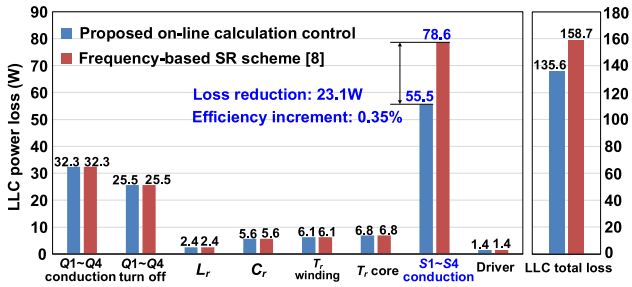


Fig. 10. *LLC* loss comparisons in forward mode: $v_{\rm bat} = 370$ V and $P_{\rm charge} = 6.6$ kW.

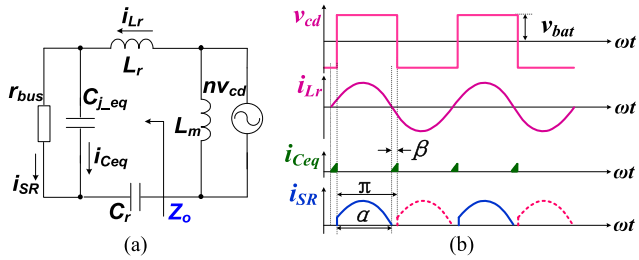


Fig. 11. Reverse *LLC* converter. (a) Equivalent circuit. (b) Waveforms.

where V_{cr0} is the initial value of resonant capacitor voltage. v_{ab} is equal to the bus voltage $v_{\rm bus}$ in the positive half cycle or the negative half cycle. Equation (7) is rearranged as

$$v_{\rm bus} = V_{cr0} + \frac{\int (i_{Lm} + \frac{i_{\rm SR}}{n}) d\theta}{\omega C_r} + \left(1 + \frac{L_r}{L_m}\right) n v_{\rm bat} + \frac{\omega L_r d(i_{\rm SR}/n)}{d\theta}. \quad (8)$$

The derivative of (8) is

$$0 = \left[1 - f_n^2 \left(\frac{\pi}{\phi}\right)^2\right] \sin\left(\frac{\pi}{\phi}\theta\right) + \frac{2n^2 r_e \phi}{\omega L_m \pi^2}\theta + \frac{n I_{Lm0}}{I_{pk}}. \quad (9)$$

Equation (9) has no analytical solutions and it is supposing that $|nI_{Lm0}| << I_{pk}$. When θ<0.1ϕ, $\sin(\pi\theta/\phi) \approx \pi\theta/\phi$, ϕ_1 can be derived based on (9)

$$\phi_1 = \sqrt{-\frac{\omega L_m \pi^3}{4n^2 r_e} + \sqrt{\left(\frac{\omega L_m \pi^3}{4n^2 r_e}\right)^2 + \frac{\omega L_m \pi^5}{2n^2 r_e} f_n^2}} \quad (10)$$

where f_n is the normalized switching frequency. ϕ_2 can be derived when θ is equal to 0.5ϕ

$$\phi_2 = \sqrt{-\frac{\omega L_m \pi^3}{2n^2 r_e} + \sqrt{\left(\frac{\omega L_m \pi^2}{2n^2 r_e}\right)^2 + \frac{\omega L_m \pi^4}{n^2 r_e} f_n^2}}. \quad (11)$$

The SR conduction time angle is

$$\phi = \frac{\phi_1 + \phi_2}{2}. \quad (12)$$

The SR conduction time in the time domain is

$$\Delta T_{\rm SR\_for} = \frac{\phi}{\omega}. \quad (13)$$

Based on (13), the conduction time can be calculated online in the DSP. Fig. 9 demonstrates the conduction time comparisons at 360 V battery voltage and 270 kHz. The magnetizing inductance is 49.9 μH, the resonant inductance is 12.8 μH and the resonant capacitance is 22 nF.

From Fig. 9, the calculated SR conduction time is close to the simulation results and the tolerance is less than 2.5%. But the frequency-based SR scheme is as high as 11.9% because it neglects the load variations.

Fig. 10 demonstrates the *LLC* loss comparisons at 300 kHz. Compared to the frequency-based SR, the loss reduction for the SRs is as high as 23.1 W and the efficiency improves 0.35% by using the proposed control.

B. Calculation of SR Conduction Time in Reverse Mode

The *LLC* operation in the reverse mode is similar to the *LC* resonant converter, which is different from the forward mode. Fig. 11 demonstrates the *LLC* equivalent circuit and waveforms in the reverse mode. $C_{j\_\rm eq}$ is the equivalent junction capacitance of MOSFETs.

The equivalent output impedance Z_o is

$$Z_o(j\omega) = \frac{R_{\rm eq} \cdot X_{\rm eq}^2 + j R_{\rm eq}^2 \cdot X_{\rm eq}}{R_{\rm eq}^2 + X_{\rm eq}^2}. \quad (14)$$

The imaginary part $X_{\rm eq}$ is

$$X_{\rm eq} = \omega L_r - \frac{1}{\omega C_r} - \frac{r_{\rm bus}^2 \cdot X_{j\_\rm eq}}{r_{\rm bus}^2 + X_{j\_\rm eq}^2}. \quad (15)$$

The real part $R_{\rm eq}$ is

$$R_{\rm eq} = \frac{r_{\rm bus} \cdot X_{j\_\rm eq}^2}{r_{\rm bus}^2 + X_{j\_\rm eq}^2}. \quad (16)$$

Based on (15) and (16), the time interval β is

$$\beta = \arctan\left(\frac{X_{\rm eq}}{R_{\rm eq}}\right). \quad (17)$$

The SR conduction time is calculated as

$$\alpha = \pi - \beta. \quad (18)$$

The SR conduction time in time domain is

$$\Delta T_{\rm SR\_rev} = \frac{\alpha}{\omega} = \frac{T_s}{2} - \frac{\beta}{\omega}. \quad (19)$$

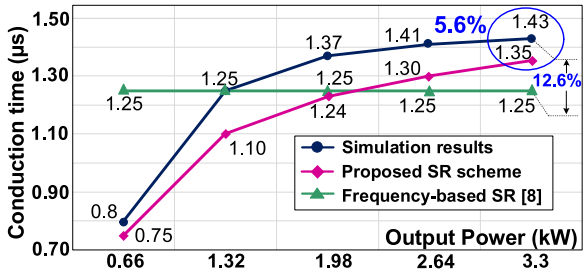


Fig. 12. Comparisons of conduction time in reverse mode: $v_{\rm bat} = 330$ V.

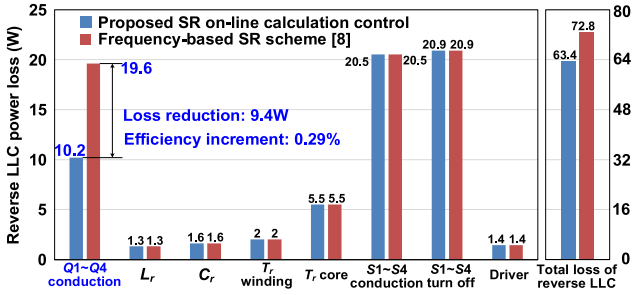


Fig. 13. Reverse *LLC* loss comparisons: $v_{\rm bat} = 320$ V and $P_{\rm discharge} = 3.3$ kW.

From (19), the conduction time in the reverse mode can be calculated online in the DSP. Fig. 12 shows the conduction time comparisons. In the reverse mode, the *LLC* converter operates at 310 kHz and the rated power is 3.3 kW. From Fig. 12, the tolerance is 5.6% at full load based on the proposed control, while the tolerance in [8] is up to 12.6%.

Fig. 13 shows the loss comparisons of reverse *LLC* at 310 kHz. Compared to the frequency-based SR scheme, the power loss reduction is 9.4 W and the efficiency improves 0.29%, which indicates that the proposed SR control is effective.

IV. Tolerance Effects Analysis for Proposed Bidirectional Online Calculation Control

By analyzing the tolerances effects of the magnetizing inductance, resonant frequency, equivalent output resistance, and driving loop delay, they almost have no effect on the proposed control.

A. Effects Analysis of Resonant Parameters and Load

In the actual application, the magnetizing inductance L_m, the resonant frequency f_r and the equivalent output resistance r_e may have tolerances due to the manufacturing and components tolerances. Moreover, the driver ICs also has delay time in the driving loop. Consequently, the tolerance effects should be evaluated carefully.

Fig. 14 demonstrates the SR conduction time when L_m, r_e, and f_r have 5% tolerance in the forward mode. From Fig. 14(a), when L_m has 5% tolerance, the maximum tolerance is only 9 ns and accounts for 0.73%. Therefore, the proposed SR control will not be affected due to the low tolerance.

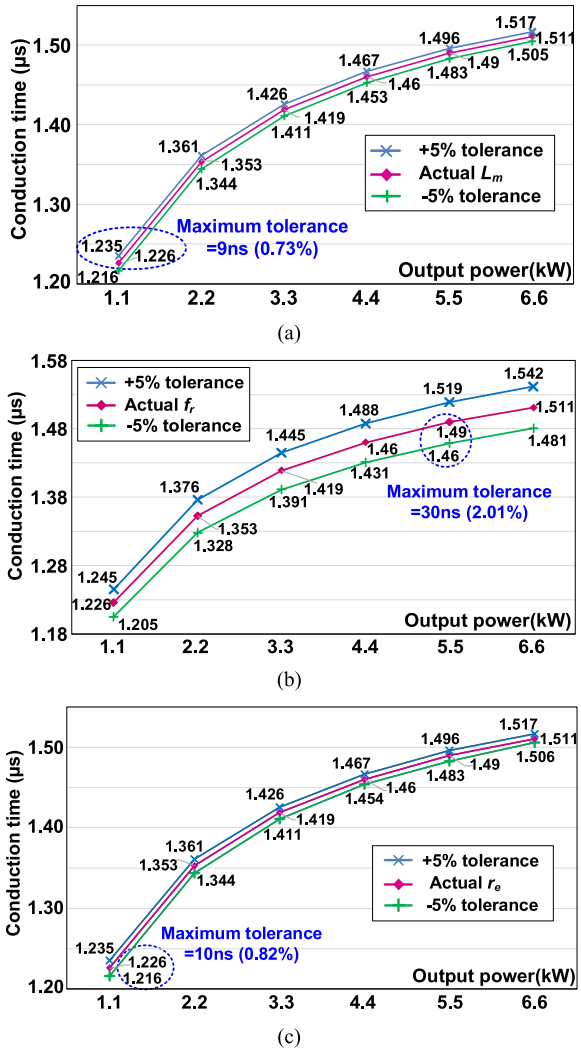


Fig. 14. Parameters tolerance in forward mode: $v_{\rm bat} = 320$ V and $f_s = 300$ kHz. (a) Tolerance of magnetizing inductance. (b) Tolerance of resonant frequency. (c) Tolerance of equivalent output resistance.

From Fig. 14(b), the maximum tolerance is 30 ns and accounts for 2.01% when the resonant frequency (300 kHz) has 5% tolerance. In Fig. 14(c), when there is 5% tolerance for the equivalent resistance of load, the maximum tolerance is only 10 ns and accounts for 0.82%. Therefore, the tolerance will not affect the implementation of the proposed SR control.

In the reverse mode, Fig. 15 shows the equivalent output resistance $r_{\rm bus}$ has 5% tolerance. The maximum tolerance of conduction time is 12 ns and accounts for 1.24%, which is low and will not affect the proposed control.

B. Effects Analysis of Driving Loop Delay

The gate-drive circuit consists of a buffer SN74ABT541B and a driver IC SI8271 and the maximum delay in the driving loop is 53 ns. Fig. 16 shows the SR gate signals considering the delay time in the forward mode. The dead time is 160 ns and the actual SR conduction time is equal to $\Delta T_{\rm SR\_for}$ minus the dead time.

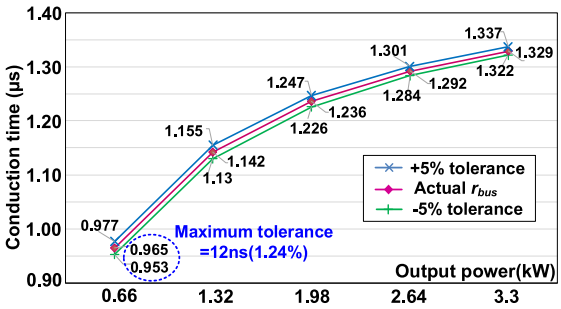


Fig. 15. Conduction time tolerance of equivalent output resistance in reverse mode: $v_{\rm bat} = 350$ V and $f_s = 310$ kHz.

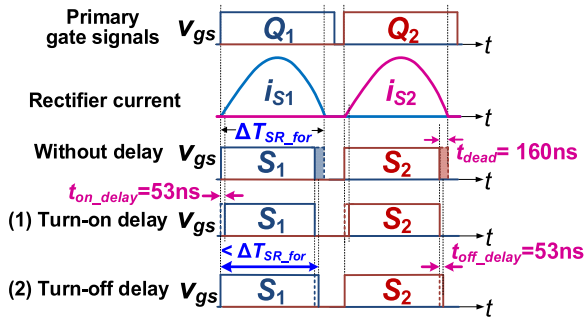


Fig. 16. Delays analysis of SR driving signals in forward mode.

In the forward mode, when the driver delay happens at the turn-ON instant, the rectifier current and forward voltage of body diode are low so that the efficiency will not hurt in the short delay time and the SR control performance can be maintained.

When the driver delay happens at the turn-OFF instant, the delay time is much lower than the dead time so that the practical conduction time is lower than the calculated $\Delta T_{\rm SR\_for}$ and the SR control function can also be achieved. Therefore, the proposed SR control is applicable considering the driving loop delay in the forward mode.

In the reverse mode, the driver delays also have no effect on the proposed control in the reverse mode and will not be discussed in detail.

V. Digital Implementation and Transient Analysis for Proposed Online Calculation Control

The SR is closed in the soft start process, while it operates in the closed-loop control. The transient performance of proposed SR control in the reverse mode is analyzed and the shoot through for the SRs can be prevented when the load steps up or down.

A. Digital Implementation for the Proposed SR Control

TMS320F280049C from Texas Instruments (TI) is adopted. The generation for the proposed SR gate signals in the forward mode is shown in Fig. 17. The clock of enhanced pulsewidth modulation (ePWM) $f_{\rm clk}$ is 100 MHz and the up-down-count mode is used.

In Fig. 17, *PRD* is equal to $f_{\rm clk}/(2f_s)$. $A_{\rm CMP}$ and $B_{\rm CMP}$ are obtained from the calculated SR conduction time. $A_{\rm CMP}$ is

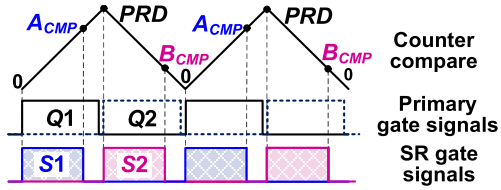


Fig. 17. Generation of SR driving signals in forward mode.

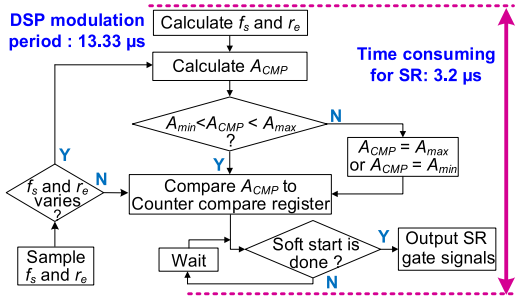


Fig. 18. Flowchart of the proposed control in forward mode.

calculated as

$$A_{\rm CMP} = f_{\rm clk} \cdot \Delta T_{\rm SR\_for}. \tag{20}$$

$B_{\rm CMP}$ is

$$B_{\rm CMP} = PRD - f_{\rm clk} \cdot \Delta T_{\rm SR\_for}. \tag{21}$$

When the value in the counter-compare register equals to $A_{\rm CMP}$ or $B_{\rm CMP}$, the ePWM digital signals will toggle to generate the SR driving signals. Fig. 18 demonstrates the flow chart of proposed SR control.

From Fig. 18, the total calculated time for the proposed SR control is 3.2 μs. The sampling frequency of the output voltage and current is 75 kHz, which is equal to the modulation frequency. Consequently, the DSP modulation period is 13.33 μs so that there is plenty of time to finish the proposed SR calculation with 76% margin.

The soft start strategy adopts the phase shift and burst mode control and there is no load in the start process of charger. It is noted that the SR gate signals are closed in the soft start process. When the soft start is done, the DSP outputs the SR gate signals to tune the output current or voltage. The implementation of proposed SR control in the reverse mode is similar to the forward mode and will not be discussed in detail.

B. Transient Analysis of LLC in Reverse Mode

It is important to ensure safe operation for the SRs in the transient. When the load steps down in the reverse mode, the SR ON-time decreases so that the SRs are always turned OFF earlier than the secondary-side switches and the shoot through will not happen.

Fig. 19 shows the gate signals when the load steps up and $T_{\rm ons}$ is the ON-time of secondary gate signals. As the load steps up without limitation, $\Delta T_{\rm SR\_rev}$ is calculated to increase and it may be higher than $T_{\rm ons}$, which may result in the shoot through.

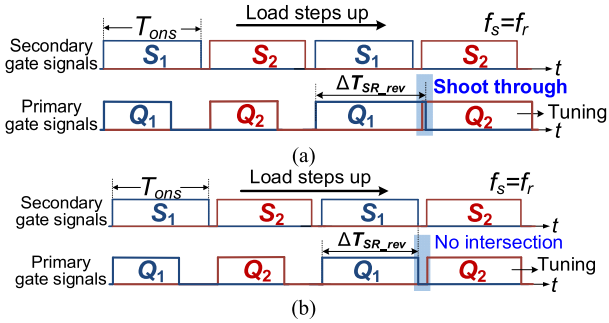


Fig. 19. Gate signals when load steps up in reverse mode. (a) SR ON-time increases without limit. (b) SR ON-time increases with limit.

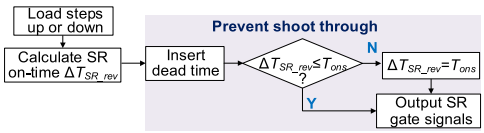


Fig. 20. Flowchart of tuning process in the transient in reverse mode.

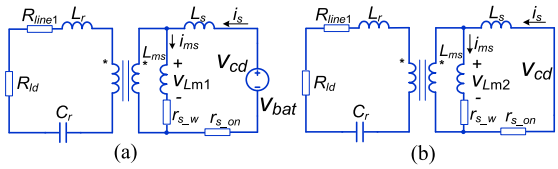


Fig. 21. *LLC* equivalent circuits in reverse mode. (a) Mode 1: $[t_0, t_1]$. (b) Mode 2: $[t_1, t_2]$.

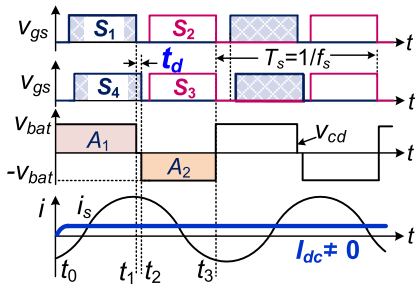


Fig. 22. DC bias current with driving loop delay.

When the limit is given as

$$\Delta T_{\mathrm{SR\_rev}} \le T_{\mathrm{ons}} \tag{22}$$

Therefore, when the load steps up, the SRs shoot through will be prevented because the turn-OFF instant of Q_1 is always earlier than the turn-ON instant of Q_2. Fig. 20 shows the flowchart of tuning process in the transient.

VI. Proposed DC Bias Analysis for Bidirectional *LLC*

The transformer dc bias is analyzed and the maximum *LLC* dc bias current is calculated, which is lower than the allowed saturation current of transformer so that the transformer will not saturate.

A. Proposed DC Bias Current Analysis in Reverse Mode

There are several factors that may cause the nonzero voltage-second area generating the dc bias current, which includes unequal conduction time due to the delay time difference of gate-drive circuit, unequal ON-state resistance of MOSFETs, unequal turn ON and turn OFF time for MOSFETs.

In the bidirectional *LLC* charger, the gate-drive resistances are selected identically and the SiC MOSFETs are obtained from the batches produced by the same manufacturer. Their values may vary slightly, but it is difficult to evaluate. Therefore, the driver loop delay is the main consideration to analyze the dc bias current in the reverse mode.

Fig. 21 shows the *LLC* equivalent circuits in the reverse mode. R_{line1} and R_{ld} are the equivalent resistances of power loop and load. L_s is the leakage inductance, r_{s_w} is the transformer winding resistance, and r_{s_on} is the MOSFETs ON-resistance. The line resistance of printed circuit board is neglected to facilitate the analysis. The dc bias current is shown in Fig. 22. A_1 and A_2 are the voltage-second areas.

During $t_0 \sim t_1$, the magnetizing inductance voltage v_{Lm1} is

$$v_{Lm1} = v_{\mathrm{bat}} - i_s r_{s\_\mathrm{on}} - i_{ms} r_{s\_w} - L_s \frac{di_s}{dt} \tag{23}$$

where i_{ms} is the magnetizing inductance current. During $t_1 \sim t_2$, v_{Lm2} is

$$v_{Lm2} = -i_s r_{s\_\mathrm{on}} - i_{ms} r_{s\_w} - L_s \frac{di_s}{dt}. \tag{24}$$

During $t_2 \sim t_3$, v_{Lm3} is

$$v_{Lm3} = -v_{\mathrm{bat}} - i_s r_{s\_\mathrm{on}} - i_{ms} r_{s\_w} - L_s \frac{di_s}{dt}. \tag{25}$$

In one switching cycle, (26) is established as

$$\int_{t_0}^{t_1} v_{Lm1} dt + \int_{t_1}^{t_2} v_{Lm2} dt + \int_{t_2}^{t_3} v_{Lm3} dt = 0 \tag{26}$$

where $t_3 - t_0$ is equal to T_s. In a complete cycle, the current integration of L_s is zero, so that dc bias current I_{dc} is

$$I_{\mathrm{dc}} = \frac{v_{\mathrm{bat}} t_d}{R_{\mathrm{line2}} T_s} = \frac{v_{\mathrm{bat}} \Delta D}{R_{\mathrm{line2}}} \tag{27}$$

where R_{line2} is the equivalent resistance of power loop that is r_{s_on} plus r_{s_w}. Based on (27), the dc bias current is determined by the input voltage, the net duty cycle and the equivalent resistance of power loop.

B. Transformer Unsaturation Evaluation in Reverse Mode

In order to ensure stable operation, the proposed dc bias analysis is used to evaluate the transformer saturation or not.

The transformer type is EE70 and the material is DMR96 selected from Dongyang Magnetics Enterprise Group Company. The magnetic path length l_{m} and cross-sectional area A_e are 134.1 mm and 686 mm^2, respectively. The core permeability μ_r is 3800.

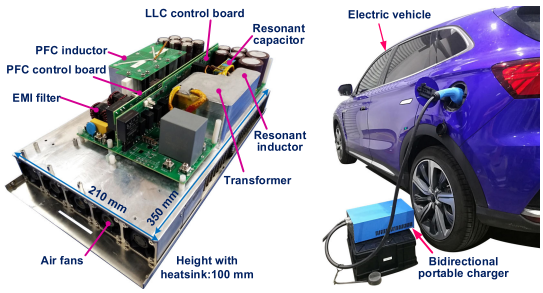


Fig. 23. Bidirectional portable charger. (a) Charger prototype. (b) EV is charged by portable charger.

TABLE I
SPECIFICATIONS OF BIDIRECTIONAL CHARGER

Symbol	Values	Symbol	Values
P_{charge}	6.6 kW	n_p: n_s	10:7
$P_{discharge}$	3.3 kW	f_r	300 kHz
v_{ac}	220 VAC±15%	f_{s_LLC}	270 kHz~400 kHz
v_{bus}	380 V~700 V	L_m	49.9 μH
C_{bus}	1145 μF	L_r	12.8 μH
f_{sw_pfc}	66.7 kHz	C_r	22 nF
L_{ac1}/ L_{ac2}	500 μH	v_{bat}	200 V~500 V

The maximum AC flux density is

$$B_{\mathrm{ac\_max}} = v_{\mathrm{bat\_max}}/(4n_s A_e f_s) = 84mT \tag{28}$$

where $v_{\mathrm{bat\_max}}$ is 500 V and f_s is 310 kHz. The saturation flux density is 415 mT at 100°C from the transformer datasheet. The allowed maximum dc flux density $B_{\mathrm{dc\_max}}$ is 331 mT. The allowed saturation current $I_{\mathrm{dc\_sat}}$ is

$$I_{\mathrm{dc\_sat}} = \left(l_{g\_\mathrm{for}} + \frac{l_m}{\mu_r}\right)\frac{B_{\mathrm{dc\_max}}}{n_s \cdot \mu_0} = 66.4\mathrm{A} \tag{29}$$

where μ_0 is the air permeability that is $4\pi\times10^{-7}$ H/m. 900-V 36-A SiC MOSFETs (C3M0065090D) from Wolfspeed are used and the ON-resistance is 72 mΩ at 70°C. As r_{s_w} and r_{s_on} are 8.3 mΩ and 144 mΩ, so that R_{line2} is 152.3 mΩ. The maximum driver delay t_d is 53 ns, so the maximum dc bias current $I_{\mathrm{dc\_max}}$ is

$$I_{\mathrm{dc\_max}} = V_{\mathrm{bat}} t_d/(R_{\mathrm{line2}} T_s) = 53.9\mathrm{A}. \tag{30}$$

The maximum dc bias current is 53.9 A, which is lower than the allowed saturation current of 66.4 A, so that the *LLC* transformer will not saturate in the reverse mode.

VII. EXPERIMENTAL VERIFICATION AND DISCUSSION

A. Experimental Prototype

A bidirectional 300-kHz full-SiC *LLC* portable charger was built in Fig. 23. 900-V 36-A SiC MOSFETs (C3M0065090D) from Wolfspeed are used. The EV is ROEWE Marvel X from SAIC Motor Corporation Limited and the EV battery is ternary lithium battery with 52.5 kWh capacity. The rated charging power is 6.6 kW and the discharging power is 3.3 kW. The bus voltage is from 380–700 V and the output voltage ranges from 200 to 500 V. The detailed parameters are given in Table I.

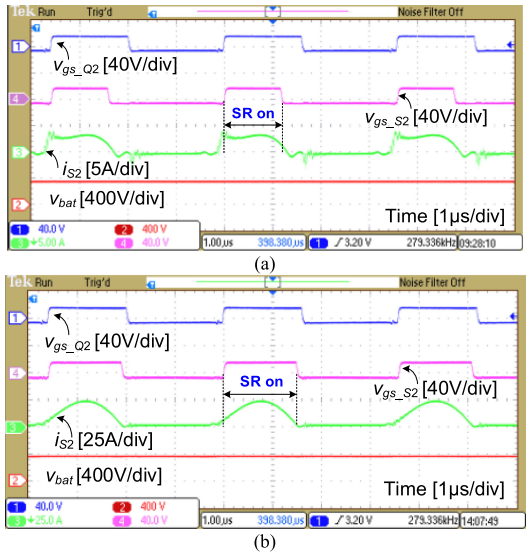


Fig. 24. SR waveforms in forward mode: $v_{\mathrm{bat}} = 350$ V and $f_s = 280$ kHz. (a) 10% of full load (660 W). (b) Full load (6.6 kW).

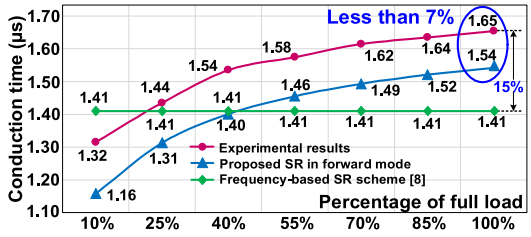


Fig. 25. ON-time comparisons in forward mode: $v_{\mathrm{bat}} = 350$ V and $f_s = 280$ kHz.

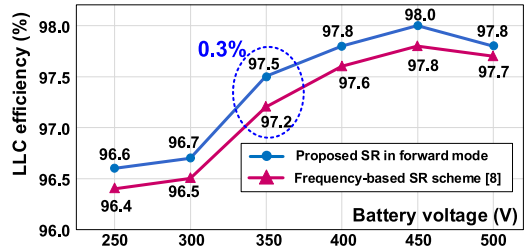


Fig. 26. Efficiency comparisons in forward mode: $f_s = 300$ kHz.

B. Proposed Online Calculation Control in Forward Mode

Fig. 24 shows the SR waveforms in the forward mode. When the loads increase from 10% of full load to full load, the SR conduction time increases adaptively to track the load variations. It indicates that the proposed SR control achieves expected control at different load conditions.

Fig. 25 shows the SR ON-time comparisons. The tolerance is less than 7% at 6.6 kW between the experiments and calculations, which verifies the effectiveness of proposed control. But the tolerance in [8] is as high as 15%.

Fig. 26 shows the efficiency comparisons. Based on the charging profile, the maximum charging power is 4.6 kW at 250 V. As the output voltage ranges from 300–500 V, the charging power

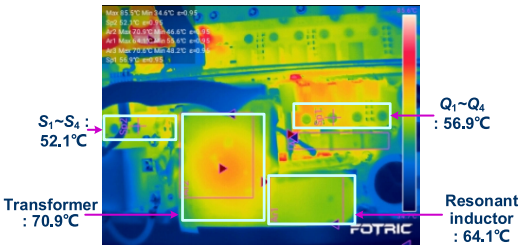
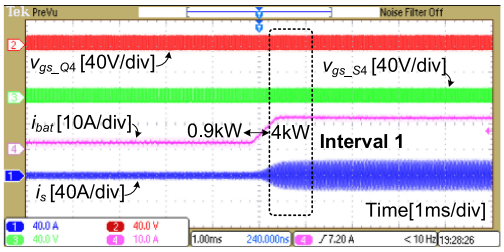
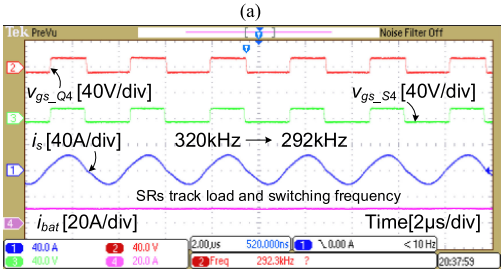


Fig. 27. Charger thermal image in forward mode: $v_{\rm bat} = 320$ V and $P_{\rm charge} = 6.6$ kW.



(a)



(b)

Fig. 28. Loads step up in forward mode: $v_{\rm bat} = 310$ V. (a) Loads step up from 0.9 to 4 kW. (b) Interval 1 is zoomed in.

is 6.6 kW. The efficiency improves 0.3% at 6.6 kW, so that the proposed control has better performance.

Fig. 27 shows the charger thermal image. Air cooling is used and the temperatures are from the charger operation with one hour. The transformer temperature is 70.9C and the resonant inductor temperature is 64.1 °C. The temperatures of $Q_1 \sim Q_4$ and $S_1 \sim S_4$ are 56.9°C and 52.1°C, respectively.

Fig. 28 shows that the loads step up from 0.9 to 4 kW in the forward mode. The switching frequency ranges from 292 to 320 kHz. It indicates that the proposed ON-line calculation control is effective in the transient.

C. Proposed Online Calculation Control in Reverse Mode

In the reverse mode, Fig. 29 shows the SR waveforms at 500 V battery voltage and 700 V output bus voltage. It is observed that the proposed SR control is effective.

Fig. 30 shows the SR conduction time comparisons. The tolerance between the proposed control and experiments is as low as 0.7%, but the tolerance of [8] is up to 10.7%. It indicates that the proposed control has better performance.

The LLC efficiency comparisons at 3.3 kW in the reverse mode are demonstrated in Fig. 31. Compared to the frequency-based SR scheme, the efficiency improves 0.2% at full load by using the proposed SR control.

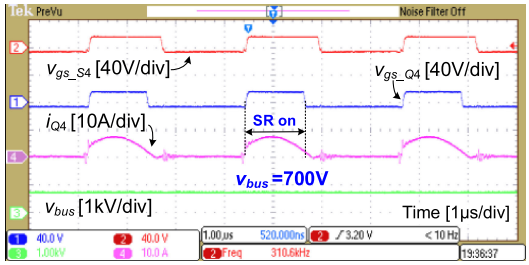


Fig. 29. SR waveforms in reverse mode: $v_{\rm bat} = 500$ V and $P_{\rm discharge} = 3.3$ kW.

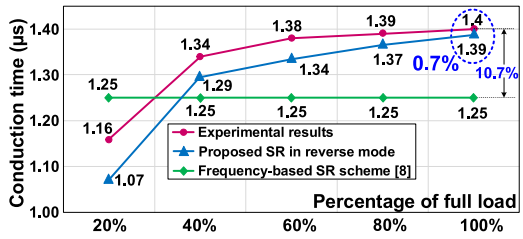


Fig. 30. ON-time comparisons in reverse mode: $v_{\rm bat} = 300$ V and $f_s = 310$ kHz.

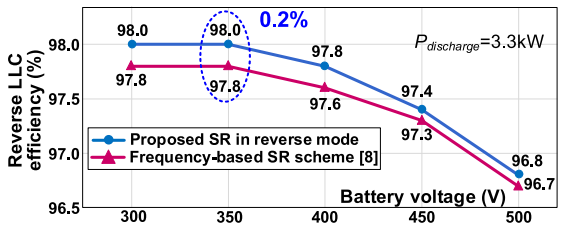


Fig. 31. *LLC* efficiency comparisons in reverse mode: $f_s = 310$ kHz.

The loads step down from 3.3 to 0.6 kW is shown in Fig. 32. In the dynamic change, the SR conduction time decreases to track the load variations, which verifies that the proposed SR control is valid.

D. Measured Efficiency

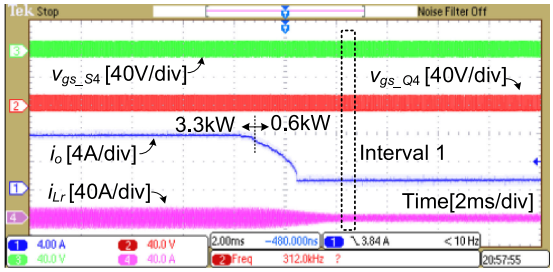
Fig. 33 gives the forward efficiency measured by Yokogawa WT500 power analyzer. At 250 V battery voltage, the maximum charging power is 4.6 kW (70% of full load) based on the charging profile. The peak overall charging efficiency is 95.5% at 6.6 kW.

In the reverse mode, the efficiency is shown in Fig. 34. The peak overall discharging efficiency is 96.6% at 3.3 kW.

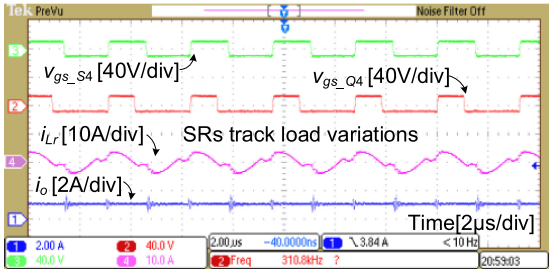
Table II gives the efficiency and power density comparisons of bidirectional chargers. The *LLC* efficiency in the proposed charger is 97.8%, which is higher than the *CLLC* charger in [1]. The power density of proposed charger is 36.3 W/in^3, which is slightly higher than Wolfspeed charger in [4].

E. Proposed Control With Different Power Devices

In order to further verify the proposed online calculation control, different power devices from Wolfspeed are also used and given in Table III.

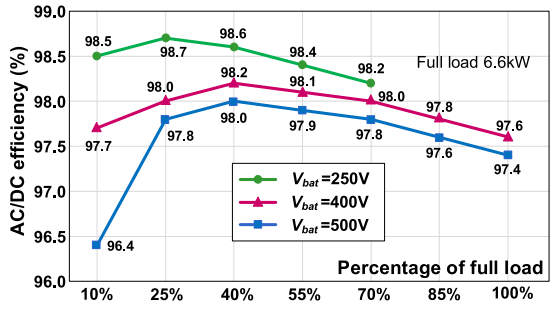


(a)

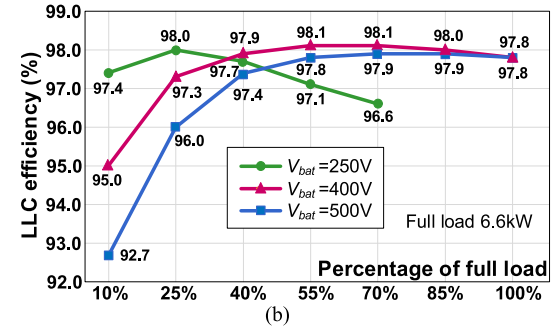


(b)

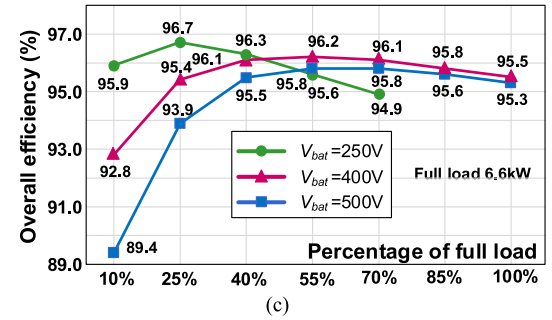
Fig. 32. Loads step down in reverse mode: $v_{bat} = 300$ V and $f_s = 310$ kHz. (a) Loads step down from 3.3 kW to 0.6 kW. (b) Interval 1 is zoomed in.



(a)

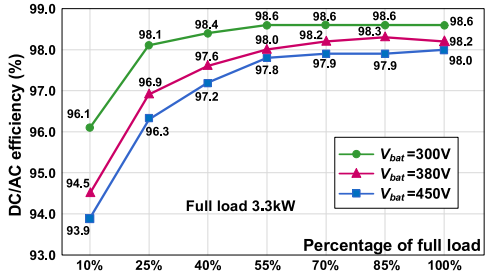


(b)

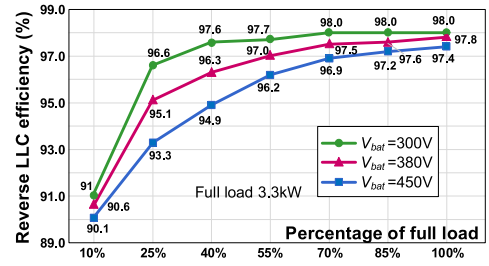


(c)

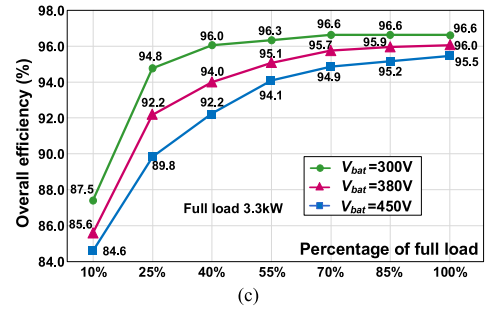
Fig. 33. Charging efficiency in forward mode. (a) AC/DC efficiency. (b) *LLC* efficiency. (c) Overall efficiency.



(a)



(b)



(c)

Fig. 34. Discharging efficiency in reverse mode. (a) DC–AC efficiency. (b) Reverse *LLC* efficiency. (c) Overall efficiency.

TABLE II
COMPARISONS OF BIDIRECTIONAL CHARGERS

	DC-DC topology	DC-DC efficiency	Power density without heatsink
Wolfspeed Charger [4]	CLLLC converter	97.8%@ 6.6 kW	36 W/in^3
CLLLC charger [10]	CLLLC with matrix transformer	97.8%@ 6.6 kW	37 W/in^3
CLLC charger [1]	CLLC converter	97%@ 3.5 kW	10 W/in^3
Proposed charger	LLC converter	97.8%@ 6.6 kW	36.3 W/in^3

TABLE III
DIFFERENT POWER DEVICES FOR *LLC* CONVERTER

	Part number	V_{DSS}, I_D @70 °C	$R_{DS(on)}$ @70 °C
Test #1	C3M0065090D	900 V 29 A	72 mΩ
	C2M0120090D	1200 V 19 A	132 mΩ
Test #2	C2M0080120D	1200 V 30 A	92 mΩ
	C2M0025120D	1200 V 78 A	30 mΩ

Fig. 35 shows the SR waveforms with the power devices of C3M0065090D in the primary side and C2M0080120D in the secondary side. The proposed control is effective with different power devices in the forward and reverse modes. As the SR waveforms of test #2 are same to Fig. 35, they will be not given repeatedly.

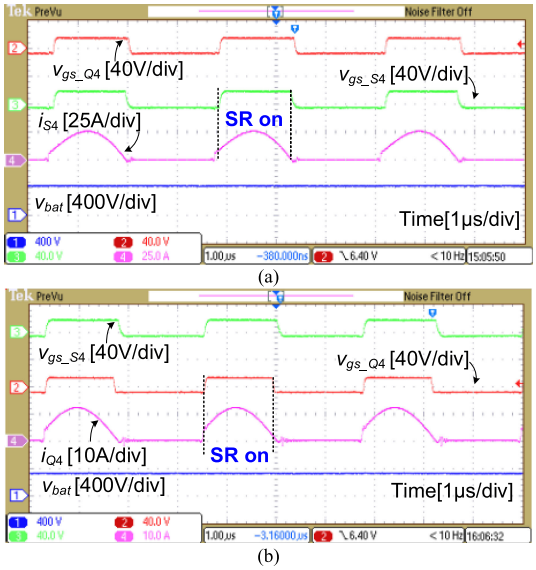


Fig. 35. SR waveforms of test #1. (a) Forward mode: $v_{\rm bat} = 400$ V, $f_s = 300$ kHz, and $P_{\rm charge} = 6.6$ kW. (b) Reverse mode: $v_{\rm bat} = 300$ V, $f_s = 310$ kHz, and $P_{\rm discharge} = 3.3$ kW.

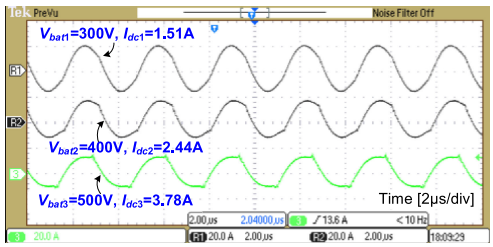


Fig. 36. *LLC* transformer input current in reverse mode: $P_{\rm discharge} = 3.3$ kW.

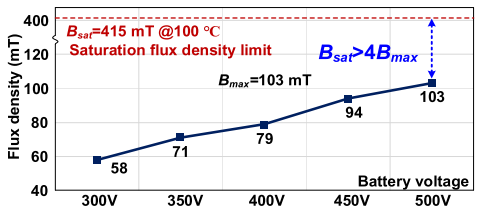


Fig. 37. Flux density at different battery voltages: $P_{\rm discharge} = 3.3$ kW.

F. DC Bias Current in Reverse Mode

Fig. 36 shows the transformer input current with the power devices of C3M0065090D in the primary side and secondary side. The maximum dc bias current is 3.78 A, which is much lower than the allowed saturation current of transformer that is 66.4 A. The safe margin is as high as 94.3%, which guarantees the *LLC* transformer unsaturation in the reverse mode considering the component tolerances and the temperature variations.

Fig. 37 shows the flux density. The maximum flux density is 103 mT, which is much lower than the saturation limit of 415 mT, so that the reverse *LLC* transformer will not saturate.

VIII. Conclusion

This article proposed a digital bidirectional SR online calculation control for high voltage applications in the SiC bidirectional *LLC* portable charger. Based on the mathematical models, the SR conduction time is calculated online considering the switching frequency and load. The turn-ON instants of the primary-side and secondary-side gate signals are identical and the SR turn-OFF instants are determined by the calculated conduction time. It not only achieves the bidirectional *LLC* function, but also improves the efficiency over wide load range significantly. Compared to the conventional SR methods used in the unidirectional applications such as 400 V bus voltage and low output voltage/ high output current [12]–[14], the proposed control can be applied to 700 V bus voltage and 500 V battery voltage.

Compared to the frequency-based SR scheme at full load, the *LLC* efficiency with the proposed control is improved by 0.3% and 0.2% in the forward and reverse modes, respectively. The peak overall charging efficiency and discharging efficiency are 95.5% and 96.6% at full load.

The transformer dc bias is analyzed to calculate the dc bias current. The *LLC* transformer in the reverse mode is guaranteed without saturation since the maximum experimental dc bias current is 3.78 A, which is much lower than the allowed saturation current of 66.4 A and the safe margin is as high as 94.3%.

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