Analytic–Adaptive *LLC* Resonant Converter Synchronous Rectifier Control

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***Abstract*—Synchronous rectification (SR) is the key to achieve high efficiency for high output current *LLC* resonant converters. Recently proposed methods for SR control do not offer a complete solution for industrial applications. The drain-to-source voltage sensing based methods cannot utilize the full benefits of SR due to the field-effect transistor (FET) package stray inductance. The adaptive SR control methods suffer from the variable ON time and cannot reach the minimum power loss. This research aims for a high-performance SR control strategy that not only has good steady-state performance but also works reliably during transients. This article introduces an analytic–adaptive method for SR control that delivers accurate adjustment for both turn ON and turn OFF moments of SR FETs below and above resonance. The proposed method takes into account the stray inductance of SR FETs; hence, it enables full efficiency gain of SR. The feasibility of implementation for the proposed method integrated with closed-loop control is experimentally validated on a 300 W 390/12 V half-bridge *LLC* resonant converter with 93.66% peak efficiency.**

***Index Terms*—Adaptive control, digital control, *LLC* resonant converter, synchronous rectification (SR).**

I. INTRODUCTION

LLC resonant converter is widely used in the dc front end of power supplies for data centers and in industrial chargers for light electric vehicles [1]–[5]. Integrated magnetics and low switching loss contribute to high power density and efficiency in industrial designs [6]–[8]. Additionally, zero-voltage switching for the primary side and zero-current switching for the secondary side result in reduced electromagnetic interference.

The rapid development of information technology has increased the need for low-voltage and high-current power supplies. The conventional converters use diode rectifiers that result in large voltage drops in the conduction path and poor efficiency. SR, the technique of replacing rectifier diodes with field-effect transistors (FETs), significantly reduces the voltage drop across rectifying devices and improves the efficiency. Fig. 1 shows an *LLC* resonant converter with SR. Due to the presence of the magnetizing current i_{mag} in the resonant tank, the secondary-side currents ($i_{\text{QSR}\,1}$ and $i_{\text{QSR}\,2}$) are not in phase with the resonant tank current i_{tank}. As a result, the gate signals of SR FETs ($Q_{\text{SR}\,1}$ and $Q_{\text{SR}\,2}$) cannot be produced based on the gate signals of the primary-side FETs (Q_{HS} and Q_{LS}).

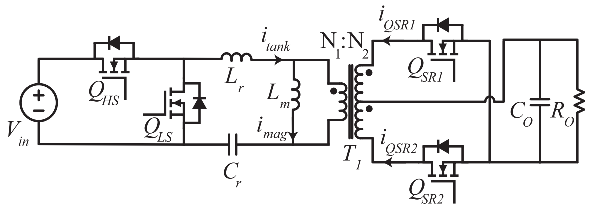
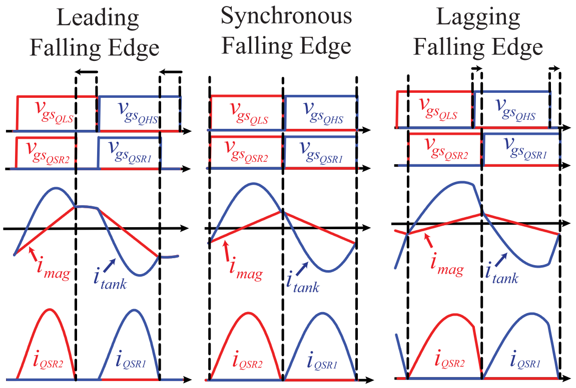


Fig. 1. Half-bridge *LLC* resonant converter with SR.



(a) (b) (c)

Fig. 2. SR optimum gate drive signals. (a) Below resonance. (b) At resonance. (c) Above resonance.

An *LLC* resonant converter demonstrates a multiresonant characteristic. The two resonant frequencies of the converter are defined as follows:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)\, C_r}}. \tag{2}$$

L_r, L_m, and C_r represent the resonant inductance, the magnetizing inductance of the transformer, and the resonant capacitance, respectively. The SR FETs are usually controlled based on the converter's switching frequency f_{sw}. For below resonance region ($f_{r2} < f_{\text{sw}} < f_{r1}$), as shown in Fig. 2(a), the SR FET

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should be turned ON as soon as the current flows through the body diode of the FET. The current in $Q_{\mathrm{SR}\,2}$ ($Q_{\mathrm{SR}\,1}$) goes to zero before the turn OFF for Q_{HS} (Q_{LS}). As a result, the SR FETs should be turned OFF prior to the primary-side FET. At the resonance frequency ($f_{\mathrm{sw}} = f_{r1}$), as shown in Fig. 2(b), the turn ON and OFF for the SR FETs are synchronous with their corresponding primary-side FETs. In the above resonance region ($f_{\mathrm{sw}} > f_{r1}$), as shown in Fig. 2(c), when Q_{HS} (Q_{LS}) is turned OFF the current in $Q_{\mathrm{SR}\,2}$ ($Q_{\mathrm{SR}\,1}$) is still nonzero. After a short period of deadtime (t_d), Q_{LS} (Q_{HS}) is turned ON and the current in $Q_{\mathrm{SR}\,2}$ ($Q_{\mathrm{SR}\,1}$) is forced to zero. As a result, $Q_{\mathrm{SR}\,1}$ and $Q_{\mathrm{SR}\,2}$ should be turned OFF with a delay after Q_{LS} and Q_{HS}, respectively. To avoid reverse current, the turn ON for the SR FETs also should happen with the same amount of delay with reference to the primary-side FETs. This delay allows enough time for the converter to force the current in the other SR FET to zero.

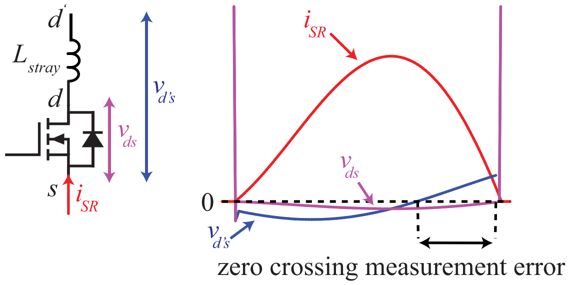
The demand for high power density has resulted in an increasing trend in switching frequency in recent years. With rapid improvements in wideband gap semiconductors and planar magnetics, the trend to push the switching frequency higher will continue in *LLC* resonant converter, which adds to the complexity of SR control [9]–[11]. Over the past few years, various SR control techniques for *LLC* resonant converters have been proposed, which are categorized into three groups.

A. Current Sensing Based Methods

Sensing the secondary-side current is the most accurate method for controlling SR FETs. Sensing the current is usually performed by a current transducer (CT), which introduces additional losses and offsets the benefit of SR [12]. An energy recovering SR scheme based on sensing the secondary-side current was proposed in [13]. However, the method was designed for pulsewidth modulation converters with square-shape current and not for resonant rectifiers. Reducing the number of CTs was the focus of research in [14] and yet, with an increased number of windings, the introduced conduction loss is the same. The number of CTs used in voltage doubler and full-wave rectifier structures was optimized in other works [15]–[17]. The use of a saturable current transformer to implement a self-contained gate driver for SR FETs was described in [18]. However, it involves a custom design for a CT. The integration of CT with a transformer was proposed in [19] to reduce weight and volume. Utilizing the transformer's primary-side current for SR control results in reduced CT conduction loss. However, it is only possible using a *CLL* resonant tank structure and it will result in the use of separate magnetics in the *LLC* structure [20]. Separate magnetic parts were avoided in other works by compensating the effect of magnetizing inductance [21]–[24]. However, these methods require either a complicated circuitry to offset the effect of magnetizing current and/or a custom-designed CT.

B. Drain-to-Source Voltage Sensing Based Methods

Sensing the drain-to-source voltage v_{ds} of the SR FETs eliminates the use of additional CTs and forms the basis for a number of commercially implemented solutions for SR control in an *LLC* resonant converter [25]–[28]. Ideally, the voltage drop across the drain-to-source of the secondary-side FETs can be a good reference for driving the SR FETs. In this method, as soon as v_{ds} falls below the body diode conduction threshold, typically −0.7 V, the SR FET is turned ON and the current will flow through the channel of the FET. When the current decreases back to zero, the resistive voltage drop across the FET also decreases to zero and the FET is turned OFF at zero crossing of v_{ds}. However, due to the presence of FET's package stray inductance L_{stray}, the drain-to-source voltage leads the drain-to-source current, which results in early turn OFF for the SR FET [29]. The combination of SR FET package inductance and printed circuit board (PCB) stray inductance typically ranges between 6.5 and 17 nH for different packages and layouts [30]. The high-frequency *LLC* resonant converters are affected the most by the stray inductance of SR FETs.



(a) (b)

Fig. 3. (a) Lumped model of the stray inductance of a FET. (b) Leading drain-to-source voltage due to the stray inductance and the resulting zero-crossing measurement error ($f_{\mathrm{sw}} = 150$ kHz, $L_{\mathrm{stray}} = 5$ nH, and $R_{\mathrm{ds,on}} = 2.5$ mΩ).

Fig. 3(a) shows the lumped equivalent model for the stray inductance of a FET. Fig. 3(b) shows the effect of this stray inductance on sensed drain-to-source voltage $v_{d's}$, which is leading the current through the FET i_{SR} during the ON time. In order to compensate the effect of stray inductance, the use of active low-pass filters was recommended in [31] and [32]. However, these methods of compensation require information on the value of stray inductance that varies widely with the FET package and PCB layout design. The accuracy of the compensating network is also dependent on the value of $R_{\mathrm{ds,on}}$, which changes significantly with the FET junction temperature.

A passive compensation network for compensating the leading effect of stray inductance was proposed in [33]. This method increased the dependability and decreased the complexity of the design compared with the active methods. However, it introduces a delay in turn ON and still suffers from the lack of accurate information on L_{stray} and $R_{\mathrm{ds,on}}$.

C. Adaptive Methods

The adaptive control for SR in *LLC* resonant converter was introduced in [34]. In this method, the SR ON time is increased cycle-by-cycle until no body diode conduction is detected at the falling edge of the gate signal. Then, the ON time of the SR FET will be reduced for the next switching cycle. After a few cycles, the ON time will be adjusted to the optimum value. However, in this reference, the SR FET ON time is limited to the primary-side FET ON time. As a result, in the above resonance operation, the SR ON time is always smaller than the optimum value.

The digital implementation of the adaptive method for the control of SR FETs has drawn significant attention during the past few years. Researchers in [35]–[37] improved either the accuracy and/or the speed of adaptive SR control. The use of adaptive methods resulted in reduced conduction loss in SR FETs. However, the average power loss caused by the variable ON time is still half of the worst case [38].

Amouzandeh *et al.* [36] and Sato *et al.* [37] implemented the adaptive turn ON adjustment in order to increase efficiency at light loading. Wang *et al.* [39], Fei *et al.* [40], and Qian *et al.* [41] either focused on the integration of SR driving schemes with a closed-loop voltage control or investigated the feasibility of implementing the adaptive method for very high frequency *LLC* resonant converters using low-cost controllers. Nowadays, the adaptive method is available commercially in the analog and digital forms for industrial use [42]–[44].

A few other control methods were introduced in recent years that do not fit in any of the described categories. An open-loop fixed ON time was proposed in [45]. Although simplicity is an advantage in this method, the operating range of the method is limited and the efficiency advantage is not fully gained for all operating points. The feasibility of the adaptive driving of SR FETs based on the output voltage information was demonstrated in [46] for below resonance operation within a limited range. Choi [47] proposed an ON-time prediction method for SR control based on dual edge tracking, aiming at improved transient performance. Although the transient performance above resonance is improved, the additional tracking scheme is not utilized below resonance. An analog SR control based on the resonant capacitor voltage demonstrates the noise-resistant operation below and above resonance [38]. However, the implementation of the method integrated with closed-loop control is challenging due to the need for continuous monitoring of various signals.

Although the performance of an SR control strategy during transients is of minor importance from the efficiency point of view, designing an SR control scheme that performs well in steady state and is able to provide a reliable operation during transients is valuable in practical applications and, therefore, is the motivation of this article. In this article, a novel digital analytic–adaptive method for SR control is proposed, which accurately controls both turn ON and turn OFF time for SR FETs. This method does not require a secondary-side CT. It analytically calculates the optimum turn OFF moment of the SR FET based on the zero crossing of the FET drain-to-source voltage and compensates for the effect of stray inductance. Additionally, the method is able to adapt itself to manufacturing tolerances in package stray inductance or variation of $R_{\mathrm{ds,on}}$ of SR FETs. Section II of this article presents the theory of the control scheme. Section III provides the simulation results for different operating modes in the battery charging application. Section IV reports the experimental results of the proposed method using a 130 kHz, 300 W, and 390/12 V half-bridge *LLC* resonant converter. Section V forms the conclusion part of the article.

II. PROPOSED ANALYTIC–ADAPTIVE SR CONTROL METHOD

The proposed method uses different schemes for driving the SR FETs below and above resonance.

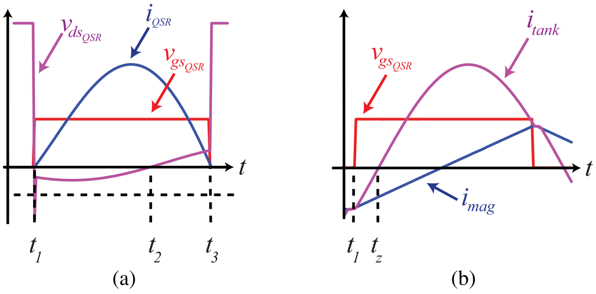


Fig. 4. Visualization of the time intervals used for the implementation of the proposed method for below resonance operation. (a) t_1, t_2, and t_3. (b) t_1 and t_z.

A. Below Resonance

For the below resonance operation, the SR FET is turned ON as soon as the body diode conduction is detected. In order to explain the adjustment of the turn OFF time, we first define different time instants marked in Fig. 4.

T_1 is the ideal turn ON moment for SR FET. At this moment, the sensed drain-to-source voltage of FET falls below the body diode conduction threshold V_{th}. At t_2, the drain-to-source voltage of SR FET reduces back to zero, which happens before the zero crossing of FET current due to the presence of stray inductance. t_3 is the ideal turn OFF moment for the SR FET. The control method aims to calculate t_3 and turn OFF the SR FET right at this moment. At t_z, the resonant tank current crosses zero, as shown in Fig. 4(b).

Based on the defined moments, the secondary-side current ($i_{Q\mathrm{SR}}$) is derived as a scaled-up version of the magnetizing current subtracted from the resonant tank current. During the SR FET conduction time, the voltage across magnetizing inductance L_m is the output voltage times the transformer turns ratio. Therefore, L_m does not participate in the resonance and the resonant tank is effectively an *LC* series circuit so the response of the circuit is a sinusoidal current. As a result, the resonant tank current is a sinusoidal current, while the magnetizing current is a linear current.

$$i_{Q\mathrm{SR}}\ (t) = n\left(I_p \sin\left(\omega_{\mathrm{SR}}\left(t-t_1\right)-\varphi\right)\right.$$
$$\left.-\frac{nV_o}{L_m}\left(t-\frac{t_1+t_3}{2}\right)\right) \tag{3}$$

where, $n = N_1/N_2$ is the turn ratio of the high-frequency transformer, I_p is the peak value of the sinusoidal resonant tank current i_{tank}, and V_o is the output voltage of the converter.

From t_1 to t_3, the resonant tank current has a sinusoidal shape and one of the SR FETs is conducting. Therefore, ω_{SR}, named SR angular frequency here, is not necessarily the same as switching frequency and it is defined in (4). φ in (5) is the phase difference between the primary-side and secondary-side currents

$$\omega_{\mathrm{SR}} = \frac{\pi}{t_3-t_1} \tag{4}$$

$$\varphi = \pi\frac{t_z-t_1}{t_3-t_1}. \tag{5}$$

When the SR FET is turned ON, the actual drain-to-source voltage v_{ds} is the voltage drop across $R_{\mathrm{ds,on}}$

$$v_{\mathrm{ds}}\,(t) = R_{\mathrm{ds,on}}\, i_{\mathrm{SR}}\,(t)\,. \tag{6}$$

However, the sensed drain-to-source voltage of the SR FET $v_{\mathrm{d's}}$ is the sum of the voltage drops across $R_{\mathrm{ds,on}}$ and L_{stray}

$$v_{\mathrm{d's}}\left(t\right) = R_{\mathrm{ds,on}}\, i_{\mathrm{SR}}\left(t\right) + L_{\mathrm{stray}}\frac{di_{\mathrm{SR}}\left(t\right)}{dt}. \tag{7}$$

At t_2, $v_{\mathrm{d's}}$ becomes zero, which shows that the voltage drops across $R_{\mathrm{ds,on}}$ and L_{stray} are opposite in polarity with the same magnitude

$$-L_{\mathrm{stray}}\frac{di_{\mathrm{SR}}\left(t_2\right)}{dt} = R_{\mathrm{ds,on}}\, i_{\mathrm{SR}}\left(t_2\right). \tag{8}$$

By substituting (3) into (8) and assuming t_1 as the reference for time measurement ($t_1 = 0$), we have

$$\frac{-L_{\mathrm{stray}}}{R_{\mathrm{ds,on}}} = \frac{\sin\left(\omega_{\mathrm{SR}} t_2 - \varphi\right) - k\left(t_2 - \frac{t_3}{2}\right)}{\omega_{\mathrm{SR}}\cos\left(\omega_{\mathrm{SR}} t_2 - \varphi\right) - k}. \tag{9}$$

In the above equation, k is defined as

$$k \triangleq \frac{\frac{nV_o}{L_m}}{I_p}. \tag{10}$$

In order to simplify the calculations, we expand the sinusoidal terms in (9)

$$\frac{-L_{\mathrm{stray}}}{R_{\mathrm{ds,on}}} = \frac{\sin\left(\omega_{\mathrm{SR}} t_2\right)\cos\left(\varphi\right) - \cos\left(\omega_{\mathrm{SR}} t_2\right)\sin\left(\varphi\right) - k\left(t_2 - \frac{t_3}{2}\right)}{\omega_{\mathrm{SR}}\cos\left(\omega_{\mathrm{SR}} t_2\right)\cos\left(\varphi\right) + \omega_{\mathrm{SR}}\sin\left(\omega_{\mathrm{SR}} t_2\right)\sin\left(\varphi\right) - k}. \tag{11}$$

By evaluating (3) at t_1, we can determine Sin (φ) and Cos (φ) using the sensed value for I_p, expressed as follows:

$$\sin\left(\varphi\right) = \frac{t_3\frac{nV_o}{L_m}}{2I_p} \tag{12}$$

$$\cos\left(\varphi\right) = \sqrt{1 - \left(\frac{t_3\frac{nV_o}{L_m}}{2I_p}\right)^2}. \tag{13}$$

By using (10)–(13) together with measuring I_p and t_2, the ideal turn OFF time for SR FETs (t_3) can be calculated and used instantly. Due to the presence of trigonometric functions, the direct expression cannot be derived without the loss of accuracy. Hence, a numerically calculated lookup table should be used to calculate t_3 from which $t_{\mathrm{ext}} = t_3$ - t_2 is calculated.

Fig. 5 shows the key operating waveform for below resonance. In this mode, the SR FET is turned ON as soon as $v_{\mathrm{d's}}$ falls below the body diode conduction threshold $V_{\mathrm{th,BDC}}$. The falling edge of the SR gate signal is delayed after the zero crossing of v_{ds} with the calculated t_{ext}. t_{ext} is the difference between the actual conduction time t_{cond} and the measured conduction time $t_{\mathrm{cond,m}}$ and it is calculated by using (10)–(13) together with measuring I_p and t_2. Hence, full efficiency gain is achieved with the proposed control method.

B. Above Resonance

Fig. 6 shows the key operating waveform above resonance. Similar to the below resonance region, the SR FET is turned ON as soon as the body diode conduction is detected. The falling edge of the SR gate signal is extended with t_{ext}. t_{ext} should be long enough to let the current in the SR FET to be reduced to zero.

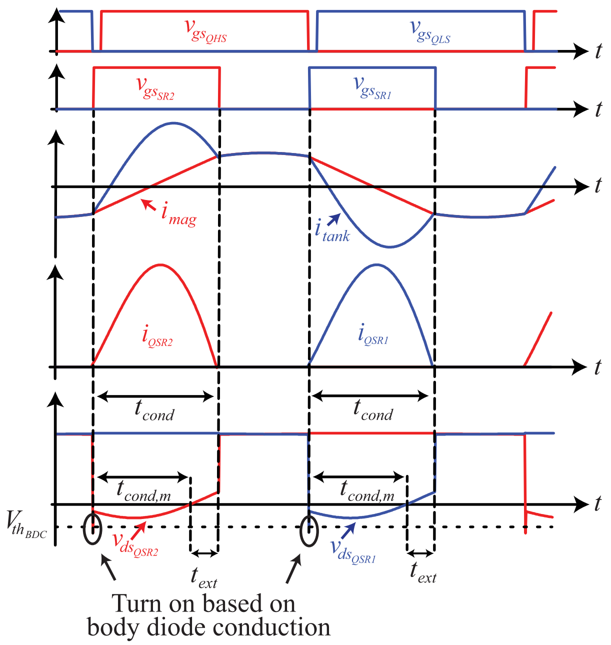


Fig. 5. Key operating waveform for below resonance operation.

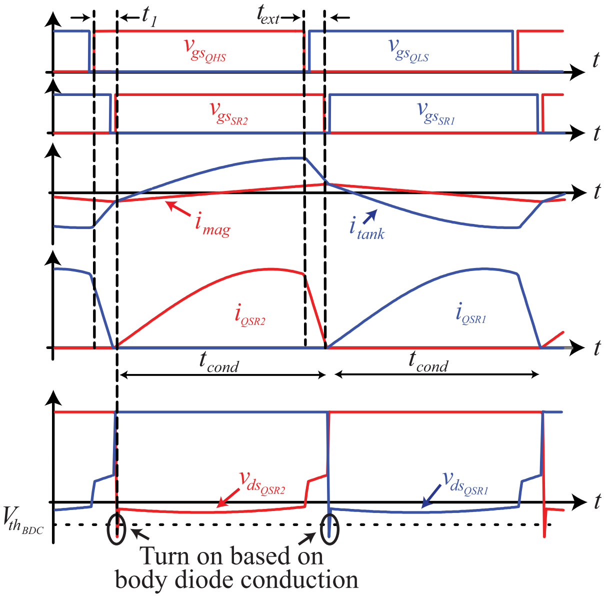


Fig. 6. Key operating waveform for above resonance operation.

In order to achieve the highest efficiency and prevent reliability degradation, the center-tapped transformer in an *LLC* resonant converter is designed in a way that currents at the secondary side are symmetrical [48]. As a result, the period of time that it takes for $i_{\mathrm{QSR}\,1}$ to be forced to zero (t_1) is very close to the one for i_{QSR2} (t_{ext}). In the proposed method, t_1, which is the period between the rising edge of the corresponding

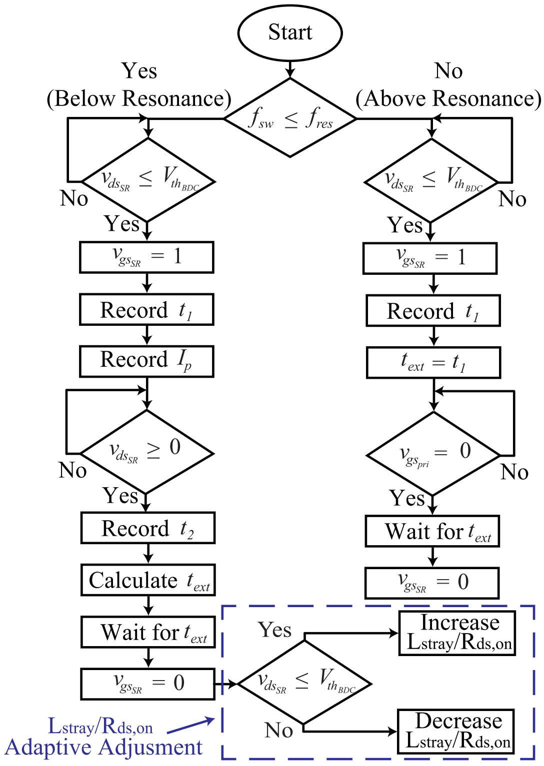


Fig. 7. Flowchart for the implementation of the proposed method.

primary-side gate signal (e.g., $v_{\mathrm{gs},QHS}$) and the rising edge of the SR FET gate signal (e.g., $v_{\mathrm{gs},\mathrm{SR}2}$), is detected with body diode conduction detection. Therefore, t_1 is measured at the rising edge of the SR gate signal and it is used to extend the falling edge of the SR gate signal past the falling edge of the primary-side gate signal.

Fig. 7 shows the control flowchart of the proposed method. In the first step, below or above resonance operation is chosen based on the switching frequency, which is determined by the voltage control loop. For the below resonance operation, the SR FET is turned ON as soon as a body diode conduction is detected. Next, the peak value of the resonant tank current I_p is measured. In the final step, after zero-crossing time of the sensed $v_{\mathrm{d's}}$ is detected and t_2 is recorded, t_3 is calculated based on (10)–(13) and the SR FET is turned OFF at t_3.

In this mode of operation, the $L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$ is adaptively adjusted, as shown in the dashed box in Fig. 7. If the estimated $L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$ is smaller than the actual value, the calculated t_{ext} will be less than enough for compensating the effect of the stray inductance. As a result, there will be a period of body diode conduction right after the SR FET is turned OFF. On the other hand, if the estimated $L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$ is bigger than its actual value, there will be a short period of reverse current in the SR FET and no body diode conduction will be detected at the falling edge of the SR gate signal. Therefore, the presence or absence of the body diode conduction right after the turn OFF of SR FET is used to adaptively adjust the estimated value for $L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$. The adaptive adjustment of this ratio helps to compensate for the variations of $R_{\mathrm{ds,on}}$ as a result of temperature change in the junction of the FET as well as L_{Stray} manufacturing tolerances.

For the above resonance operation, the SR FET is turned ON as soon as a body diode conduction is detected. The delay for turn ON of the SR FET with respect to the rising edge of $v_{\mathrm{gs,pri}}$ of the corresponding primary-side FET is recorded using an internal counter in the microcontroller and applied to t_{ext}. t_{ext} is then used to delay turn OFF for the SR FET after the falling edge of $v_{\mathrm{gs,pri}}$ of the corresponding primary FET.

Adaptive-based methods demonstrate a promising performance in steady state. However, unlike the proposed method, they change the ON time of SR FETs adaptively. Due to potential sharp changes in the switching frequency and as a result in the ON time of SR FETs, these adaptive methods are susceptible to transients. Therefore, additional protective measures are needed to protect the converter from shoot through in case of a sharp frequency increase. On the other hand, the proposed method in this article considers the switching frequency and zero crossing of $v_{\mathrm{d's}}$ in determining the ON-time for SR FETs and only adaptively adjusts the slowly changing parameter ($L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$). Hence, it has a more reliable performance during transients.

Although the calculations in the proposed method are more complex compared with the adaptive method, implementation techniques employed in this article (more detail in Section IV) enable the designers to implement the proposed method with a low-cost controller.

Table I compares different SR control strategies. The proposed method takes advantage of the benefits of v_{ds} sensing method and employs an adaptive mechanism for the adjustment of $L_{\mathrm{stray}}/R_{\mathrm{ds,on}}$; therefore, it demonstrates promising performance both in steady state and during transients.

III. SIMULATION RESULTS

This section shows simulation results carried out in PSIM for three operating modes in battery charging, i.e., constant current (CC), constant power (CP), and constant voltage (CV). The simulation parameters are listed in Table II.

Fig. 8 shows simulation results at the beginning of the charging profile that the converter works at maximum CC. The voltage of the battery is below the rated value and it will be increased as the battery is charged. As a result, the converter works in the above resonance mode. t_{ext} is measured from the delay between the turn ON of the primary FET and the turn ON of the SR FET. The simulation results show that the proposed method emulates ideal rectification at different output voltages.

When the voltage of the battery pack is increased above the rated voltage, the output power of the converter will be limited to its maximum level and the converter will enter CP mode operating below resonance. Fig. 9 shows the simulation results at CP for different voltage levels. Equations (10)–(13) are used to calculate text and use it to control the SR FETs. The results show that the falling edge of the SR gate occurs when the current is reduced to zero and the maximum efficiency gain is achieved at different voltage levels.

At the end of the charging process, the voltage of the battery pack is approximately constant; hence, the converter works below resonance. The charging current declines as the battery gets close to full charge. The simulation results in Fig. 10 show

TABLE I
COMPARISON OF *LLC* SR CONTROL STRATEGIES

Control category	Current sensing based		V_{ds} sensing based			Adaptive based
Sub-category	Primary side	Secondary side	Without compensation	With compensation	Proposed method	-
References	[21-24]	[12-19]	[25-28]	[29-33]	-	[34-37], [39-44]
Extra power loss	Low	High	Low	Low	Low	Low
Feasibility with integrated magnetics	No	Yes	Yes	Yes	Yes	Yes
Steady state performance	High	High	Low	High	High	High
Transient handling capability	Strong	Strong	Strong	Strong	Strong	Poor
Complexity	Low	Low	Low	Medium	Medium	Medium
Robust to Variation of $R_{ds,on}/L_{stray}$	Yes	Yes	No	No	Yes	Yes

TABLE II
SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
Rated output power	300 W	Resonant inductor	55 μH
Input voltage	390 VDC	Magnetizing inductor	280 μH
Rated output voltage	12 VDC	Resonant capacitor	24 nF
Switching frequency	70~200 kHz	Transformer turns ratio	17

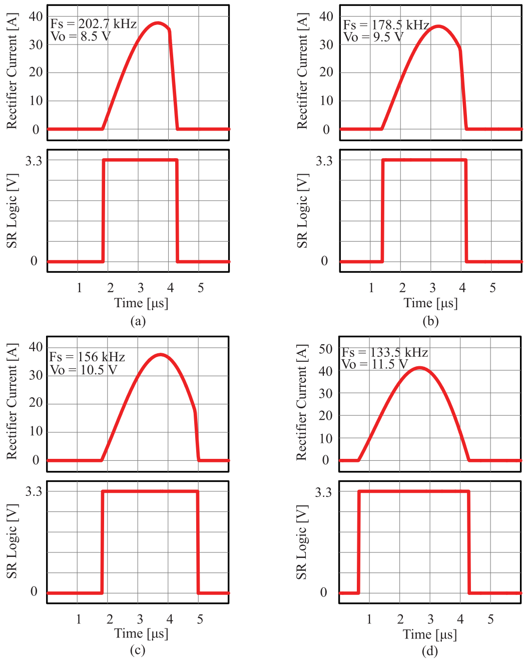


Fig. 8. Simulation results for CC operation mode ($I_o = 25$ A). (a) 8.5 V. (b) 9.5 V. (c) 10.5 V. (d) 11.5 V.

that the SR FET is turned OFF as soon as the current goes to zero and maximum efficiency gain is achieved at different current levels.

Fig. 11 shows the performance of $L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$ adaptive adjustment routine. At the beginning of this simulation, incorrect values for L_{Stray} are used for determining the ON time for SR FETs. In other words, the estimated value of $L_{\mathrm{SR,est}\,1}$ is used instead of the actual value of L_{sr} for L_{Stray} in the calculation of ON time for Q_{SR1}. Fig. 11(d) shows that this error results in late turn OFF and reverse current for Q_{SR1}. In the same manner, Fig. 11(e) shows that using a smaller estimated value ($L_{\mathrm{SR,est}\,2}$) instead of L_{SR} results in early turn OFF and body diode conduction for the Q_{SR2}. Using the adaptive adjustment routine for $L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$, the values for L_{Stray} are adjusted in very small steps and converge to the actual value (L_{sr}). When the correct value for L_{Stray} is found, the body diode conduction is minimized, as shown in Fig. 11(f) and (g).

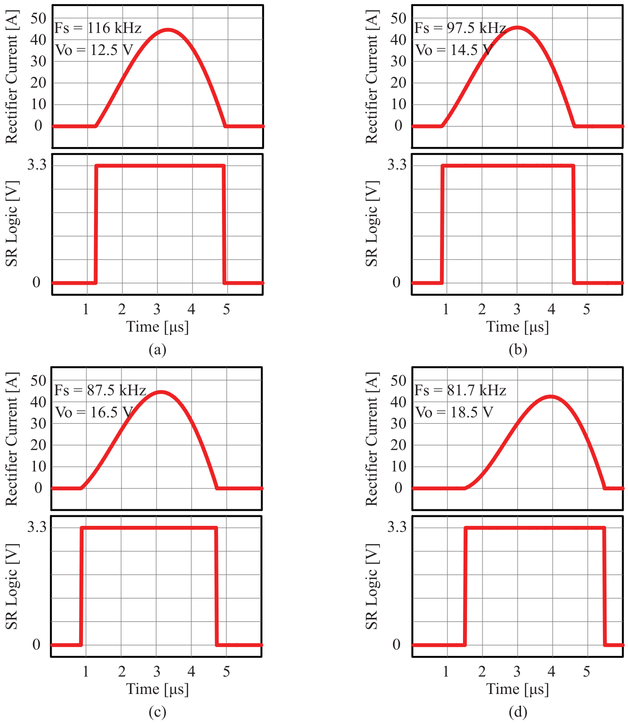
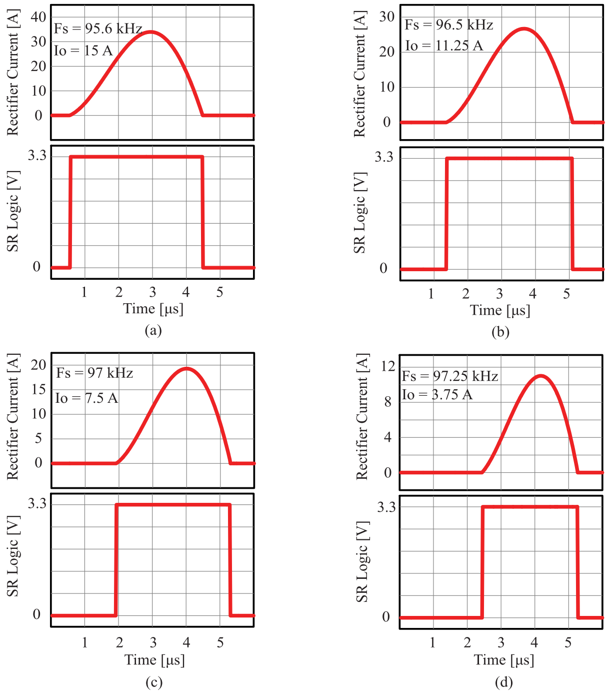


Fig. 9. Simulation results for CP mode ($P_o = 300$ W). (a) 12.5 V. (b) 14.5 V. (c) 16.5 V. (d) 18.5 V.



(a) (b) (c) (d)

Fig. 10. Simulation results for CV mode ($V_o = 15$ V). (a) 15 A. (b) 11.25 A. (c) 7.5 A. (d) 3.75 A.

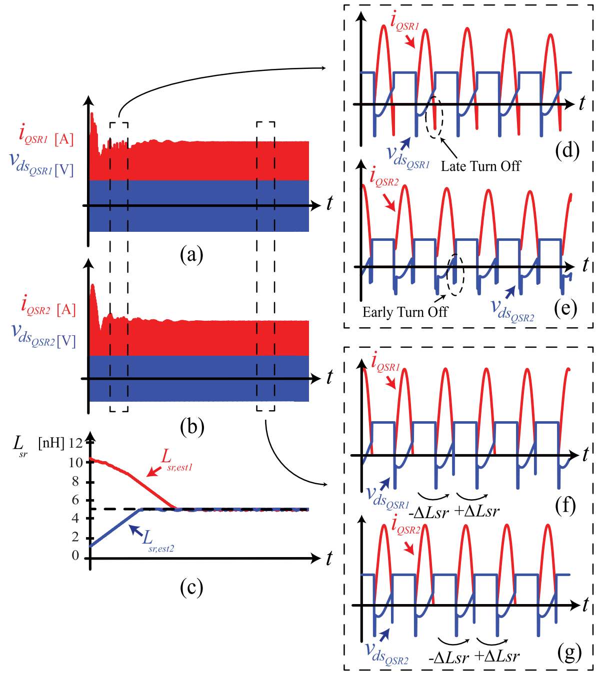


Fig. 11. Simulation of convergence of L_{Stray} to the actual value with the implementation of $L_{\text{Stray}}/R_{\text{ds,on}}$ adaptive adjustment.

Unlike other adaptive methods, the proposed method considers the switching frequency and zero crossing of $v_{\text{d's}}$ in determining the ON time. Hence, it is intrinsically robust to sharp frequency transients and does not require an additional protective scheme for avoiding shoot through during sharp frequency increases.

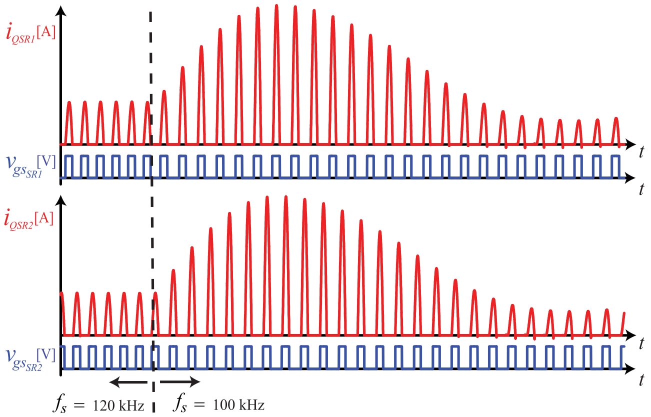


Fig. 12. Frequency step-down (120–100 kHz) transient.

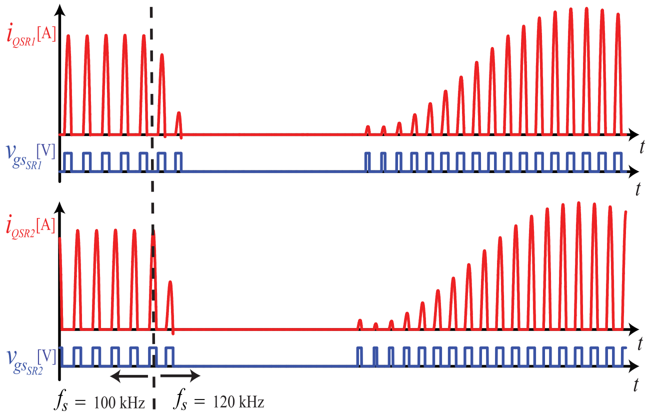


Fig. 13. Frequency step-up (100–120 kHz) transient.

Fig. 12 shows a step-down frequency change from 120 to 100 kHz in which the ON time is accurately adjusted during the transient and no reverse current is observed during this sharp transient. Fig. 13 shows a seamless step-up frequency transient from 100 to 120 kHz. In this severe transient, the SR currents are reduced to zero for a short period and the gate signals are stopped, accordingly. As soon as the SR currents grow, the proposed method accurately tunes the ON time for SR FETs.

Fig. 14 shows a seamless transition from below resonance (12.5 V and 25 A output at 116 kHz) to above resonance (9.5 V and 25 A output at 178 kHz). The dashed line shows the moment when the reference for the voltage control loop is changed. As illustrated in Fig. 14, the controller continuously monitors the mode of operation and controls the SR FETs accordingly. As a result, we see a clean transition from below resonance to above resonance.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The proposed method is validated on a half-bridge *LLC* resonant converter evaluation board from Texas Instruments. The specifications are listed in Table III. In the following paragraphs, the implementation techniques employed to validate the proposed method on a low-cost controller are outlined.

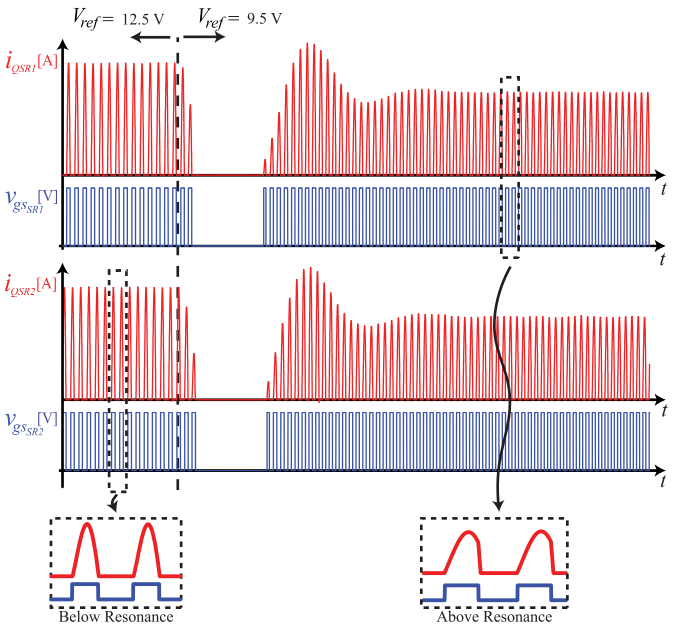


Fig. 14. Transition from below resonance (12.5 V and 25 A) to above resonance (9.5 V and 25 A).

TABLE III
PROTOTYPE SPECIFICATIONS

Parameter	Value	Parameter	Value
Rated output power	300 W	Resonant inductor	55 µH
Input voltage	375 ~ 405 VDC	Magnetizing inductor	280 µH
Output voltage	12 VDC	Resonant capacitor	24 nF
Switching frequency	80 ~ 150 kHz	Output capacitor	1.32 mF
Resonant frequency	130 kHz	Control card	TI F28027

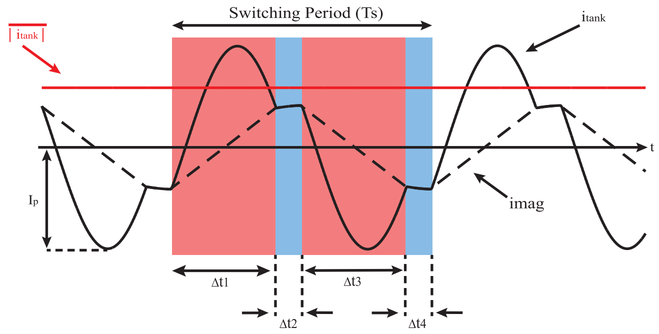


Fig. 15. Illustration of the resonant tank peak current estimation method.

A. I$_p$ Measurement

Unlike measuring the peak value of resonant tank current I_p, measuring the average value of rectified resonant tank current ($\overline{|i_{\text{tank}}|}$) is feasible with a limited analog-to-digital conversion (ADC) rate. As a result, a method for the estimation of I_p based on $\overline{|i_{\text{tank}}|}$ is employed. The method of estimation, which was verified by simulation, is illustrated in Fig. 15. Every switching cycle of resonant tank current is divided into the sinusoidal part (red) and an almost constant part (blue). As a result, $\overline{|i_{\text{tank}}|}$ is derived based on the average value for these two parts

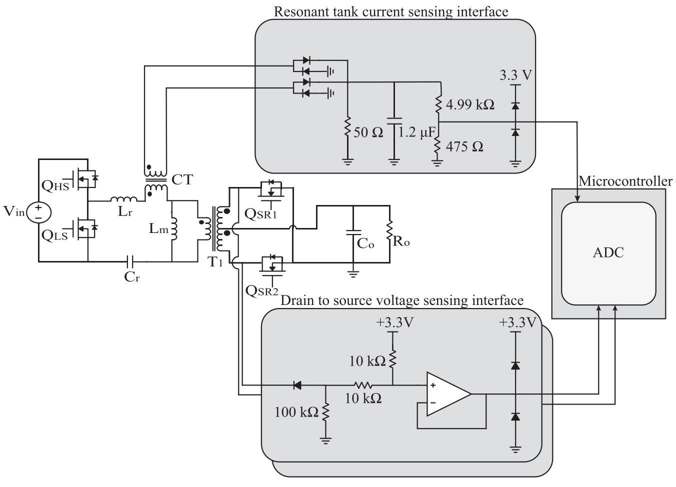


Fig. 16. Interface circuits between the power stage and the controller.

$$\overline{|i_{\text{tank}}|} = \frac{1}{T_s}\left(\overline{|i_{\text{tank}}|}_{\text{sin}}(\Delta t_1 + \Delta t_3) + \overline{|i_{\text{tank}}|}_{cte}(\Delta t_2 + \Delta t_4)\right). \tag{14}$$

In (14), T_s is the switching period, $\overline{|i_{\text{tank}}|}_{\text{sin}}$ is the average value of the sinusoidal part of the rectified resonant tank current, and $\overline{|i_{\text{tank}}|}_{cte}$ is the average value of the constant part of the rectified resonant tank current. $\triangle t_1$, $\triangle t_2$, $\triangle t_3$, and $\triangle t_4$ are shown in Fig. 15. The period in which the resonant tank current has a sinusoidal shape can be approximated by the resonant period (T_r). Therefore, $\overline{|i_{\text{tank}}|}_{\text{sin}}$ is a function of I_p and T_r. As a result, (14) is simplified as follows:

$$\overline{|i_{\text{tank}}|} = \frac{1}{T_s}\left(\frac{2I_p}{\pi}T_r + \frac{nv_o}{L_m}\frac{T_r}{4}(T_s - T_r)\right). \tag{15}$$

Therefore, I_p is estimated by measuring $\overline{|i_{\text{tank}}|}$ using (16). $\overline{|i_{\text{tank}}|}$ is measured using the interface circuit in Fig. 16

$$I_p = \frac{\pi}{2}\left(\frac{T_s}{T_r}\overline{|i_{\text{tank}}|} - \frac{nv_o}{4L_m}(T_s - T_r)\right). \tag{16}$$

B. Body Diode and v$_{ds}$ Zero-Crossing Detection

The detection of body diode and v_{ds} zero crossing is achieved through built-in comparators in the TI Piccolo F28027 control card and the interface circuit, as shown in Fig. 16. The outputs of these circuits are connected to ADC pins that also functions as pins of the built-in comparators. The comparator reference level is configured using a built-in digital-to-analog converter to detect the body diode conduction as well as v_{ds} zero crossing.

C. Calculation of t$_{ext}$

To avoid heavy online calculations for determining t_3 using (10)–(13), a precalculated lookup table is used to calculate α, which is defined in (17). In every calculation cycle, the

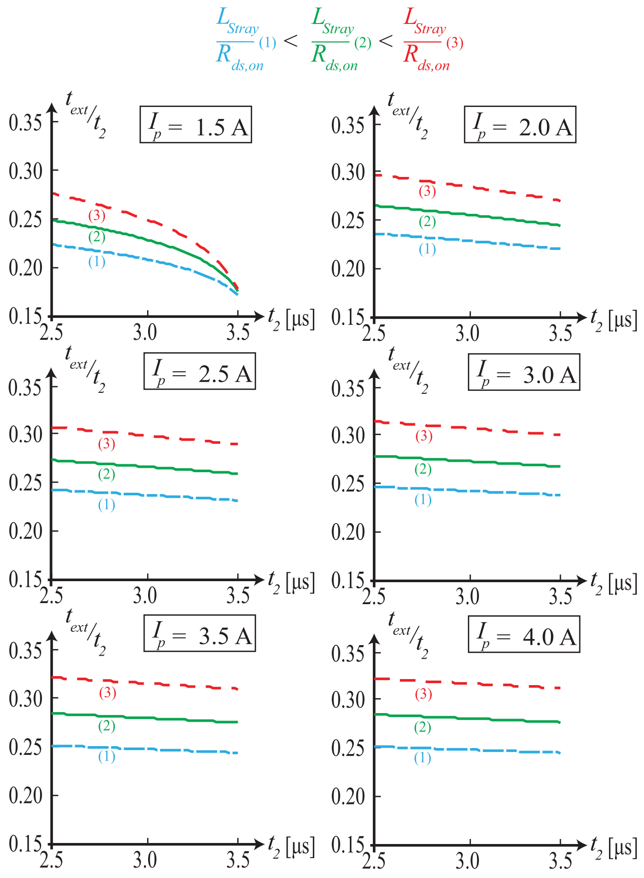


Fig. 17. Graph representation of t_{ext} lookup table.

appropriate value for α is looked up for given $L_{\text{stray}}/R_{\text{ds,on}}$, I_p, and t_2 values and it is used to calculate t_3

$$\alpha = \frac{t_3 - t_2}{t_2}. \tag{17}$$

Fig. 17 shows various graphs extracted from the lookup table. This figure shows that, in heavy loadings (higher I_p), α does not change significantly with changes in t_2, which makes the proposed method less sensitive to t_2 measurement errors. Although changes in $L_{\text{stray}}/R_{\text{ds,on}}$ result in a considerable change in α, the slow nature of this change together with the adaptive adjustment of $L_{\text{stray}}/R_{\text{ds,on}}$ work in favor of the robustness of the proposed method.

SR control strategy based on v_{ds} sensing provides a reliable performance and it is considered an industry standard that has been implemented in the form of industrial integrated circuit controllers [25]–[28]. It has also been the benchmark for recent publications in this field [38]. Therefore, this conventional method has been used as the benchmark in this article. Figs. 18 and 19 compare the above resonance performance of the v_{ds} sensing method and the proposed method, respectively. Due to SR FET stray inductance, the v_{ds} sensing method in Fig. 18 fails to gain the full advantage of SR and results in significant periods of body diode conduction and large turn OFF currents. In contrast, for the proposed method, as shown in Fig. 19, the time interval between the rising edge of the primary-side gate signal ($v_{\text{g,pri}}$) and the rising edge of the secondary gate signal ($v_{\text{g,SR}}$) is stored in the controller. This time is later used to delay the falling edge of $v_{\text{g,SR}}$ with respect to the falling edge of $v_{\text{g,pri}}$. The time measurement is performed using the microcontroller's built-in counter. The resolution of this counter (16.67 ns) is 0.25% of the minimum switching period (6.67 μs), which provides a very good resolution for the ON-time measurement. With the proposed method, the body diode conduction is minimized and the SR FET is turned OFF at approximately zero current.

In order to plot the current waveforms, two 10 mΩ shunt resistors were placed in the source of the SR FETs; as a result, the

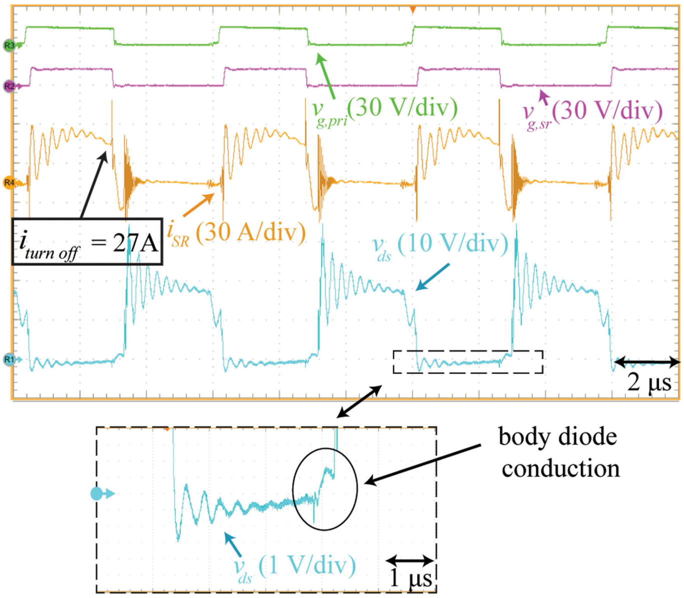


Fig. 18. v_{ds} sensing method performance above resonance 8.5 V–25 A. Green: primary gate signal ($V_{\text{gs,pri}}$). Purple: SR gate signal ($V_{\text{gs,sr}}$). Orange: SR current (i_{SR}). Blue: SR drain-to-source voltage (V_{ds}).

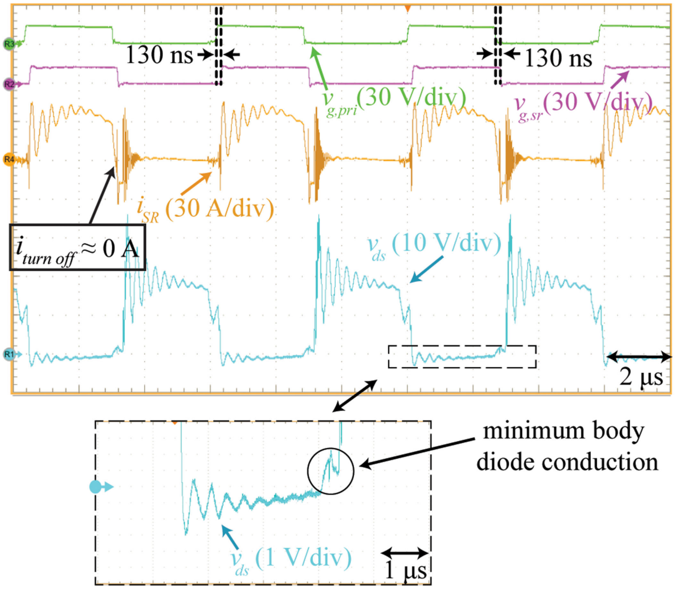


Fig. 19. Proposed method performance above resonance 8.5 V–25 A. Green: Primary gate signal ($V_{\text{gs,pri}}$). Purple: SR gate signal ($V_{\text{gs,sr}}$). Orange: SR current (i_{SR}). Blue: SR drain-to-source voltage (V_{ds}).

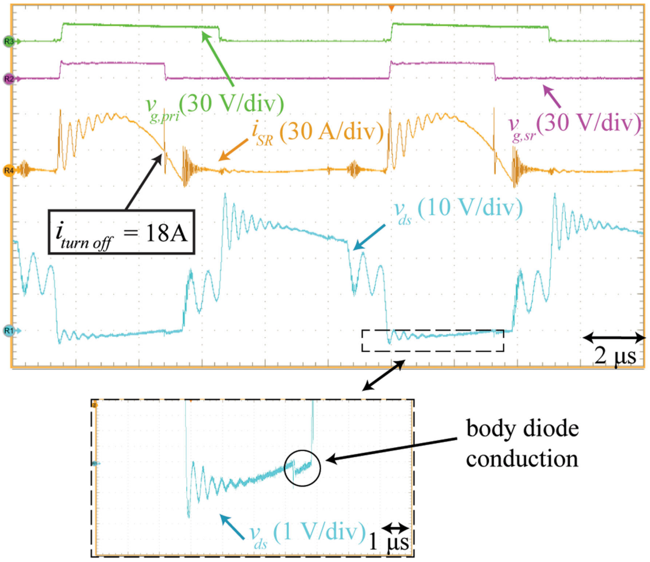


Fig. 20. v_{ds} sensing method performance below resonance 13.5 V–22.5 A. Green: primary gate signal ($V_{\mathrm{gs,pri}}$). Purple: SR gate signal ($V_{\mathrm{gs,sr}}$). Orange: SR current (i_{SR}). Blue: SR drain-to-source voltage (V_{ds}).

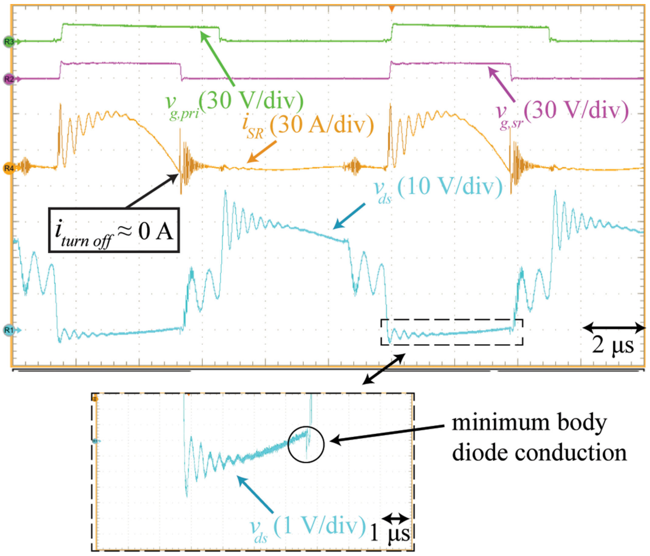


Fig. 21. Proposed method performance below resonance 13.5 V–22.5 A. Green: primary gate signal ($V_{\mathrm{gs,pri}}$). Purple: SR gate signal ($V_{\mathrm{gs,sr}}$). Orange: SR current (i_{SR}). Blue: SR drain-to-source voltage (V_{ds}).

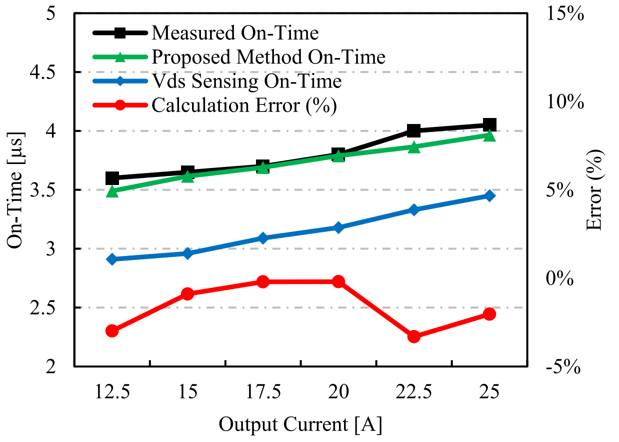


Fig. 22. ON-time calculation improvement compared with V_{ds} sensing method and calculation error analysis at $V_o = 12$ V.

$L_{\mathrm{Stray}}/R_{\mathrm{ds,on}}$ is artificially small, which explains the relatively small difference between the waveforms for the v_{ds} sensing method and the proposed method. However, the efficiency measurements in the following section, which are recorded without the shunt resistor, show the efficiency gain achieved by the proposed method.

Figs. 20 and 21 demonstrate the below resonance performance of the v_{ds} sensing method and the proposed method, respectively. In both cases, current ringing caused by the interaction of the SR FET junction capacitance and transformer secondary-side leakage inductance is visible. The v_{ds} sensing method, as shown in Fig. 20, results in large periods of body diode conduction and large turn OFF current due to the presence of package stray inductance. The stray inductance was measured to be about 15 nH with the TO-220 package of the SR FETs as the dominant source. On the other hand, the proposed method, as shown in Fig. 21, estimates the ON time of the SR FET accurately and turns OFF the FET approximately at zero current.

The calculated ON time by the proposed method shows a significant improvement compared with the v_{ds} sensing method. Fig. 22 shows the ON-time calculation accuracy improvement at 12 V output for various loading conditions. Fig. 22 also shows that the calculated ON-time closely tracks the measured ideal ON-time with a maximum of 3.3% error.

Fig. 23 shows that the proposed method facilitates a flawless step-down load transient from 25 to 12.5 A at 12 V output. The integrated implementation of the proposed method with closed-loop voltage control determines the ON time accurately before, after, and during the transient while the output voltage is being regulated. It is shown that there exist neither reverse current nor shoot through during this step-down load transient.

Fig. 24 shows a seamless step-down voltage transient from 10 to 8.5 V at 25 A output. The proposed method determines ON time accurately before, after, and during the transient while providing a CC.

Figs. 18–24 show that the proposed method compensates the effect of stray inductance and demonstrates an acceptable accuracy for operation below and above resonance. Additionally, the effectiveness of the proposed method during a load transient is experimentally verified. Due to the reliable operation of the proposed method in different operating modes, the body diode conduction is minimized. As a result, using the proposed method yields a higher efficiency compared with the v_{ds} sensing method.

Figs. 25 and 26 show the experimental efficiency comparison between the proposed and v_{ds} sensing based SR control methods for below and above resonance operation, respectively. These results were measured using the Yokogawa WT500 power analyzer. The proposed method can increase the efficiency of the converter up to 1.63% points and save up to 4.75 W of power from being dissipated within the synchronous FETs. With a smaller amount of heat dissipated through the synchronous

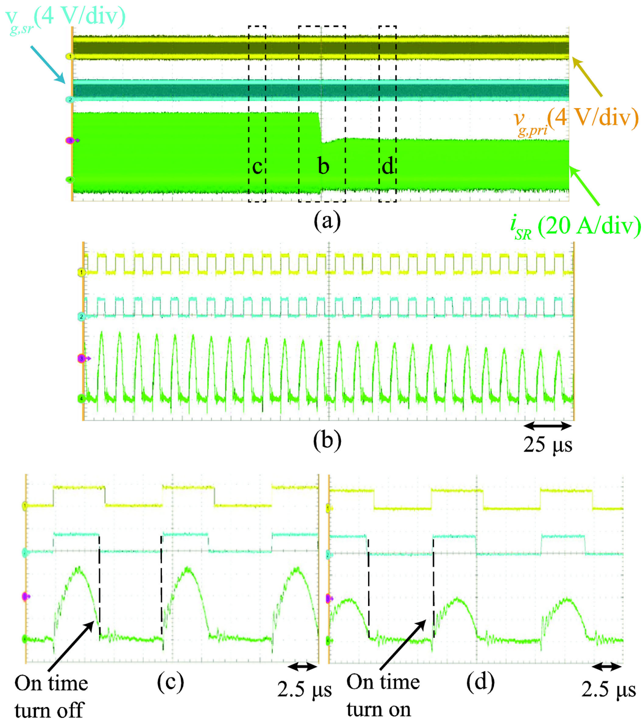


Fig. 23. Below resonance, load step-down (25–12.5 A) transient at 12 V output voltage. Yellow: primary gate signal ($V_{\mathrm{gs,pri}}$). Blue: synchronous rectifier gate signal ($V_{\mathrm{gs,sr}}$). Green: Synchronous rectifier current (i_{sr}). (a) Whole transient process: (b) during the transient; (c) before the transient; and (d) after the transient.

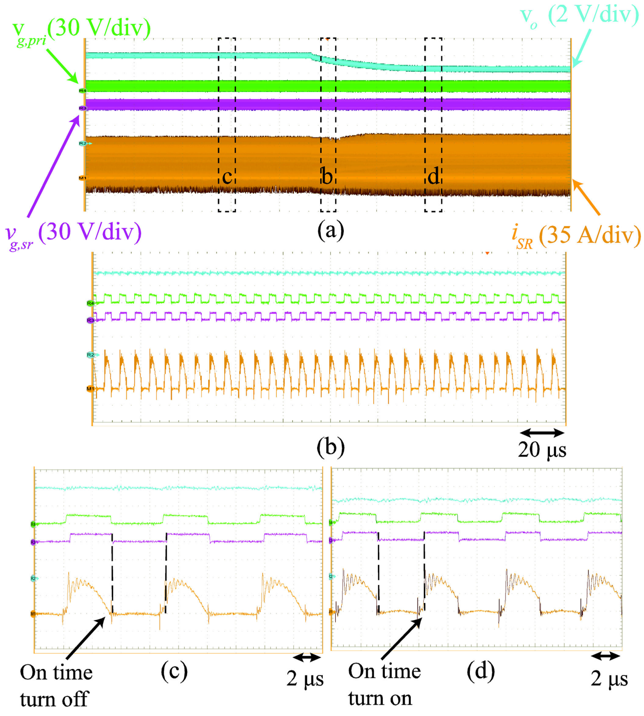


Fig. 24. Above resonance, voltage step-down (10–8.5 V) transient at 25 A output current. Green: Primary gate signal ($V_{\mathrm{gs,pri}}$), Purple: synchronous rectifier gate signal ($V_{\mathrm{gs,sr}}$). Blue: output voltage (*Vo*). Orange: synchronous rectifier current (i_{sr}). (a) Whole transient process: (b) during the transient; (c) before the transient; and (d) after the transient.

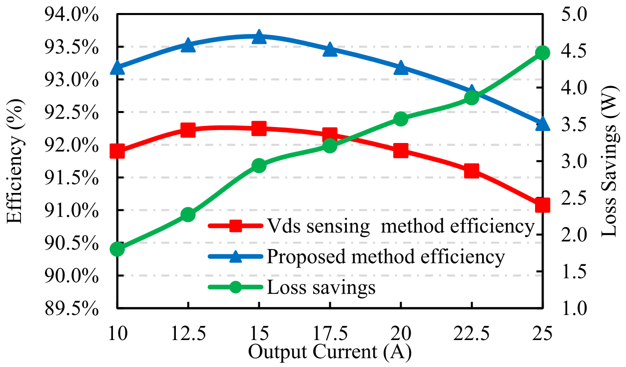


Fig. 25. Below resonance efficiency comparison between the proposed and v_{ds} sensing based methods ($V_{\mathrm{in}} = 390$ V and $V_o = 12$ V).

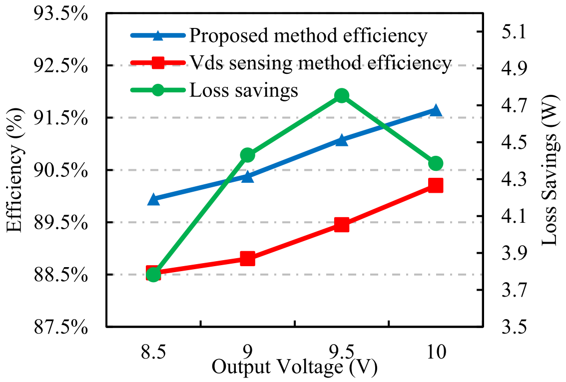


Fig. 26. Above resonance efficiency comparison between the proposed and v_{ds} sensing based methods ($V_{\mathrm{in}} = 390$ V and $I_o = 25$ A).

FETs, the volume and weight of the heatsink for the *LLC* resonant converter can be reduced significantly.

V. Conclusion

A novel analytic–adaptive method for SR for *LLC* resonant converters was proposed. The method utilizes two different schemes in order to control the turn OFF moment of each SR FET below and above resonance. For below resonance, the method uses the zero crossing of the drain-to-source voltage and the peak value of the rectified resonant tank current to estimate the ON time of the SR FET. For the above resonance, the time interval between the rising edge of the primary-side gate signal and the rising edge of the secondary gate signal is stored in the controller and used to delay the falling edge of the secondary-side gate signal with respect to the falling edge of the primary-side gate signal. The performance of the proposed method during transients as well as the accuracy of control below and above resonance was verified using the simulation and experimental results

The feasibility of the implementation of the proposed method integrated with the voltage control loop is experimentally verified using a low-cost microcontroller. The measurements of a 300 W 390/12 V *LLC* resonant converter showed that the proposed method increases the efficiency by 1.63% point at full load compared with v_{ds} sensing method. The efficiency boost saves up to 4.75 W loss ON SR FETs, which results in a heatsink with a smaller footprint.

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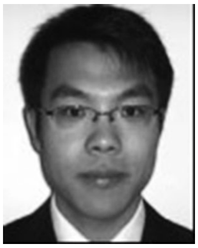

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