An S-CLC Compensated Load-Independent Inductive Power Relay System With Constant Voltage Outputs

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***Abstract*—This article proposes an S-CLC compensation network to achieve a relay system to power multiple gate drivers of series modules. There are three major contributions. First, it achieves the constant voltage (CV) and load-independent property, meaning the induced voltage on each receiver is immune to load variations. Second, the S-CLC circuit topology is compact to be constructed, and an integrated coil structure is proposed to limit the system size. Third, the efficiency of the power relay system is analyzed, including parasitic resistances of resonant components and coils, which reveal the load regulation phenomenon in practical applications. In order to validate the proposed topology, the parameter design methodology to achieve the highest efficiency is proposed, and a single-input-four-output prototype is implemented. The coil size is 180 mm × 175 mm, the transfer distance between receivers is 50 mm, and the switching frequency is 200 kHz. When the input dc voltage is 18 V, the induced voltage of each receiver is around 15 V, and the voltage difference between receivers is within 2 V. When the load resistances vary in a wide range from 15 to 100 Ω, the output voltage regulation rate is within 17.01%. The maximum power of the receiver can reach 13.53 W, and the maximum efficiency can reach 89.79%, showing that the proposed system can be used in practical applications. Besides, the prototype is exploited to power gate drivers with a total power consumption of 2.75 W, further verifying the practical application value.**

***Index Terms*—Constant voltage (CV) outputs, dc grid, load independent, power relay.**

I. Introduction

THE medium voltage and high voltage (HV) dc grids are attracting more research attention. Moreover, the modular multilevel converters (MMCs) [1]–[3] and dc circuit breakers (DCCBs) [4], [5] are widely studied. To handle the HV, MMCs and DCCBs usually have multiple series-connected IGBT modules. Due to the voltage isolation requirement, it is challenging to supply power to the gate drivers of series modules [6]. A solution for the MMC is to use a fly-back converter with a high-voltage transformer to supply power from internal capacitors to the power module [7], [8]. For the DCCB, a cascade transformer structure with multiple series magnetic rings can also be used to supply power [9], but the differential mode interference in the power supply system might cause the fault action of the DCCB [10].

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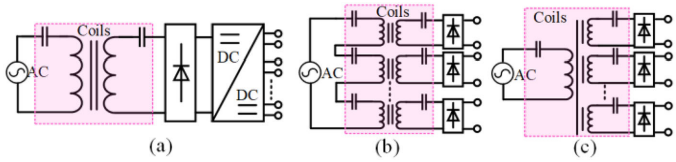

Fig. 1. IPT system structures with multiple output loads. (a) 1-to-1 IPT. (b) *N*-to-*N* IPT. (c) 1-to-*N* IPT.

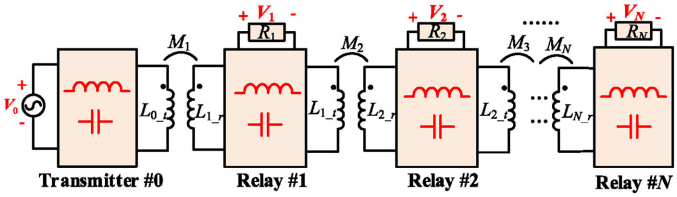

Fig. 2. Topology of the magnetic field repeater system.

An alternative option is the inductive power transfer (IPT) technology for long-distance applications [11], [12]. There are three system structures, as shown in Fig. 1.

First, the 1-to-1 structure in Fig. 1(a) usually adopts one coil structure to provide the high-voltage insulation, and a multiple-port dc/dc converter to distribute to multiple loads [13]. Second, the *N*-to-*N* structure in Fig. 1(b) is used to power directly multiple loads[14]. Compared to the previous case, the isolation voltage between coils is significantly reduced. Third, the 1-to-*N* structure in Fig. 1(c) could simplify the transmitter coil and compensation circuit structure [15]–[17]. But the cross-coupling among receiver coils could not be vanished, resulting in inference among different loads.

Recently, the magnetic field repeater system with one transmitter and multiple power relay units has also been studied, as shown in Fig. 2. Each power relay unit receives power from the former unit and distributes it to the next one by coupled flux. A prototype to power multiple loads over various distances is developed in [18]. The design methodology of circuit parameters is provided in [19].

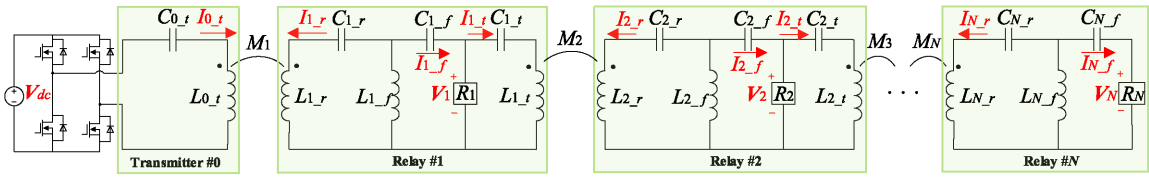

Fig. 3. The proposed power relay system with S-CLC compensation network.

However, in the above IPT systems with multiple loads, the output characteristics are not only determined by its load but also affected by other loads. To solve this problem, Mastri *et al*. [20] has pointed out that the IPT system with double-side series compensation could obtain load-independent constant output power. Pantic *et al*. [21]–[23] have exploited the multifrequency technology, in which the receivers resonate at different frequencies to achieve the load-independent property. Meanwhile, the individual controller could be applied to different receivers to control the transferred power, making a magnetic field relay system work in a load-independent mode [24]. In addition, Class E and Class EF inverters and rectifiers have been equipped with inherent output regulation to be load-independent across a wide load range [25], [26].

The compensation circuit topology has been studied to achieve constant current (CC) outputs [27]–[29]. However, the gate driver loads usually prefer constant voltage (CV) outputs. For example, the LCC compensation network can achieve CV property [30]. It could be further simplified to eliminate the extra inductor [31], but the asymmetrical coil structure is challenging to achieve in practical applications. Moreover, Costanzo *et al*. [32] and Pacini *et al*. [33] have proposed a design methodology to achieve CC or CV by applying odd or even numbers of immittance inverters. This methodology also could be used to analyze the IPT topology proposed by this article.

This article proposes a novel power relay system with S-CLC compensation network, where each relay adopts a series-compensated capacitance on the transmitter side and cascaded-compensated CLC network on the receiver side to achieve the CV property to supply power to multiple gate drivers. In addition, the electrical insulation among different outputs is easy to be achieved for the relayed power transfer structure. Compared to previous publications, the original contributions mainly lie in three aspects.

First, the S-CLC network simplifies the compensation circuit topology, and the compensated inductor is integrated into the magnetic coupler to achieve a compact structure. The developed layout of magnetic couplers could eliminate unnecessary coupling among coils.

Second, the mathematical relationship between the output voltage and the circuit parameters is provided, and the impact of the parasitic resistances is included, showing the efficiency and the design way to tune parameters to achieve equal power distribution. It reveals that the ratio of the mutual inductance and the compensated inductance is the critical parameter.

Third, the parameter design methodology to achieve the highest efficiency of the IPT system is proposed, and a prototype is implemented. The experiments show that CV property would be achieved for four independent loads in a wide range, and the system efficiency reaches 89.8%. Moreover, the prototype is used to power gate drivers, which further validates the proposed S-CLC compensated power relay system.

II. Working Principle of S-CLC Compensated System

A. System Description

Fig. 3 shows the circuit topology of the proposed inductive power relay system with one transmitter and N relay units (Relay #1–Relay #N). The input voltage is $V_{\rm dc}$. For each relay, it has a receiver coil L_{n_r} ($n = 1, 2, \ldots, N$), a transmitter coil L_{n-1_t}, the load resistance R_n. The transmitter coil L_{n-1_t} is series (S) with the capacitance C_{n-1_t}, and the receiver coil is cascaded with a T-type C_{n_r}-L_{n_f}-C_{n_f} (CLC) compensation network. Therefore, this new topology is defined as the S-CLC compensation network. Moreover, the coupling coefficient k_n and the mutual inductance M_n are given by

$$k_n = M_n \Big/ \sqrt{L_{n\_r} L_{n-1\_t}}, \quad n = 1, 2, \ldots, N. \tag{1}$$

B. System Modeling

Using the fundamental harmonics approximation, the equivalent circuit is depicted in Fig. 4. For simplicity, the influence of the parasitic resistances is neglected here.

In Fig. 4, the definitions of the output voltage $\boldsymbol{V}_n$ and critical currents $\boldsymbol{I}_{n\_r}$, $\boldsymbol{I}_{n\_t}$, and $\boldsymbol{I}_{n\_f}$ are provided. The input voltage V_0 is expressed as follows:

$$V_0 = 2\sqrt{2} V_{\rm dc} \Big/ \pi. \tag{2}$$

Based on KVL, the Loop$_{n_t}$ (violet dashed line) and Loop$_{n_f}$ (blue dotted line) in Fig. 4 are expressed by

$$\begin{cases} \boldsymbol{V}_{n-1} = \left(j\omega L_{n-1\_t} + \frac{1}{j\omega C_{n-1\_t}} + \right) \boldsymbol{I}_{n-1\_t} \\ \qquad\qquad + j\omega M_n \boldsymbol{I}_{n\_r}, n = 1, 2, \ldots, N \\ 0 = \frac{\boldsymbol{I}_{n\_f}}{j\omega C_{n\_f}} + \boldsymbol{V}_n + j\omega L_{n\_f} \left(\boldsymbol{I}_{n\_r} + \boldsymbol{I}_{n\_f}\right), n = 1, 2, \ldots, N. \end{cases} \tag{3}$$

The angular frequency is defined as ω, and the resonant relationship is expressed as

$$\begin{aligned} \omega &= \frac{1}{\sqrt{L_{n-1\_t} C_{n-1\_t}}} = \frac{1}{\sqrt{L_{n\_f} C_{n\_f}}} \\ &= \frac{1}{\sqrt{\left(L_{n\_f} + L_{n\_r}\right) C_{n\_r}}}, n = 1, 2, \ldots, N. \end{aligned} \tag{4}$$

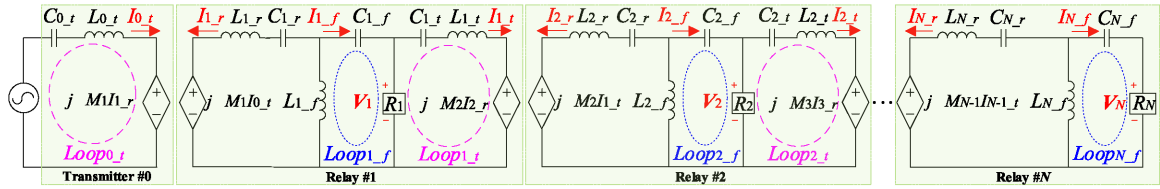

Fig. 4. Equivalent circuit of the proposed power relay system.

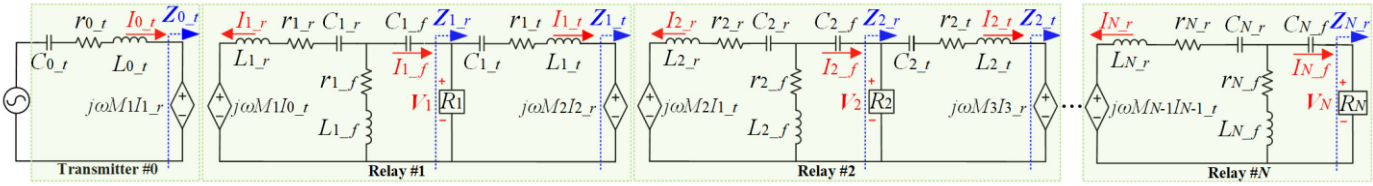

Fig. 5. Equivalent circuit considering the parasitic resistances of coils and circuit components.

Substituting (4) to (3), we can get

$$\boldsymbol{V}_{n-1} = j\omega M_n \boldsymbol{I}_{n\_r}, \boldsymbol{I}_{n\_r} = -\frac{\boldsymbol{V}_n}{j\omega L_{n\_f}}, n = 1, 2, \ldots, N. \tag{5}$$

Then, the relationship among voltages is given by:

$$\begin{cases} \boldsymbol{V}_1 = -\frac{L_{1\_f}}{M_1}\boldsymbol{V}_0, \boldsymbol{V}_2 = -\frac{L_{2\_f}}{M_2}\boldsymbol{V}_1, \boldsymbol{V}_3 = -\frac{L_{3\_f}}{M_3}\boldsymbol{V}_2, \ldots \\ \boldsymbol{V}_n = -\frac{L_{n\_f}}{M_n}\boldsymbol{V}_{n-1} = (-1)^n \boldsymbol{V}_0 \prod_{m=1}^{n} \frac{L_{m\_f}}{M_m}, n = 1, 2, \ldots, N. \end{cases} \tag{6}$$

It clearly shows that the output voltage $\boldsymbol{V}_n$ is independent of the load resistance R_n. It is only determined by the mutual inductance M_n, the inductance L_{n_f}, and the voltage $\boldsymbol{V}_{n\text{-}1}$. It means the load-independent property is achieved, and the voltage can be tuned by the circuit parameters M_n and L_{n_f}.

If we assume $M_n = L_{n\_f}$, the equal voltage distribution is achieved, which is expressed as

$$\boldsymbol{V}_0 = -\boldsymbol{V}_1 = \cdots = (-1)^n \boldsymbol{V}_n, n = 1, 2, \ldots, N. \tag{7}$$

It needs to be paid attention that the adjacent voltages have the same amplitude, but they are 180° out of phase. Therefore, in the practical application, this proposed design can be used to provide CV output to power multiple identical gate drivers.

III. Transfer Capacity Analysis

A. Impact of Parasitic Resistances on the Output Voltage

Fig. 5 considers the parasitic resistances of coils and circuit components, which affect the system power and efficiency. Then, the definitions of the quality factors and the resistances are shown as

$$\begin{cases} r_{n-1\_t} = \omega L_{n-1\_t}/Q_{n-1\_t}, \\ r_{n\_r} = \omega L_{n\_r}/Q_{n\_r} \\ r_{n\_f} = \omega L_{n\_f}/Q_{n\_f}. \end{cases}, n = 1, 2, \ldots, N \tag{8}$$

According to Fig. 5, the receiving reflection impedances are defined as $\boldsymbol{Z}_{n\_r}$ and expressed as

$$\boldsymbol{Z}_{n\_r} = \begin{cases} \frac{(\boldsymbol{Z}_{n\_t}+r_{n\_t})R_n}{\boldsymbol{Z}_{n\_t}+r_{n\_t}+R_n}, n = 1, 2, \ldots, N-1 \\ R_N, n = N. \end{cases} \tag{9}$$

Similarly, according to Fig. 5, the transmitting reflection impedances $\boldsymbol{Z}_{n-1\_t}$ is given as

$$\boldsymbol{Z}_{n-1\_t} = \frac{(\omega M_n)^2}{r_{n\_r}+j\omega L_{n\_r}+\frac{1}{j\omega C_{n\_r}}+\frac{(Z_{n\_r}+1/j\omega C_{n\_f})(r_{n\_f}+j\omega L_{n\_f})}{r_{n\_f}+Z_{n\_r}+1/j\omega C_{n\_f}+j\omega L_{n\_f}}}. \tag{10}$$

In practice, the parasitic resistances of coils are usually smaller than load resistances R_n. And, L_{n_f} is much smaller than $L_{n\text{-}1\_t}$ and L_{n_r}, which means a smaller parasitic resistance based on (8). Therefore, r_{n_f} could be neglected (more illustration could be seen from Appendix). So, (10) could be simplified as

$$\boldsymbol{Z}_{n-1\_t} \approx \frac{(\omega M_n)^2}{r_{n\_r}+\frac{(\omega L_{n\_f})^2}{Z_{n\_r}}}, n = 1, 2, \ldots, N. \tag{11}$$

From (9) and (11), it could be concluded that the reflection impedances are both resistive, showing that the zero phase angle (ZPA) is achieved. Furthermore, ZPA could help to minimize the inverter VA rating.

Based on the impedances, the currents in Transmitter #0 and Relay #*n* ($n = 1, 2, \ldots, N$) are calculated as

$$\begin{cases} \boldsymbol{I}_{0\_t} = \frac{\boldsymbol{V}_0}{r_{0\_t}+Z_{0\_t}}, \ldots, \boldsymbol{I}_{n-1\_t} = \frac{\boldsymbol{V}_{n-1}}{r_{n-1\_t}+Z_{n-1\_t}} \\ \boldsymbol{I}_{1\_r} = \frac{Z_{0\_t}\boldsymbol{I}_{0\_t}}{j\omega M_1}, \ldots, \boldsymbol{I}_{n\_r} = \frac{Z_{n-1\_t}\boldsymbol{I}_{n-1\_t}}{j\omega M_n} \\ \boldsymbol{I}_{1\_f} = \boldsymbol{I}_{1\_r}\frac{-j\omega L_{1\_f}}{Z_{1\_r}}, \ldots, \boldsymbol{I}_{n\_f} = \boldsymbol{I}_{n\_r}\frac{-j\omega L_{n\_f}}{Z_{n\_r}}. \end{cases} \tag{12}$$

According to Fig. 5, the output voltage is expressed as

$$\boldsymbol{V}_n = Z_{n\_r}\boldsymbol{I}_{n\_f}, n = 1, 2, \ldots, N. \tag{13}$$

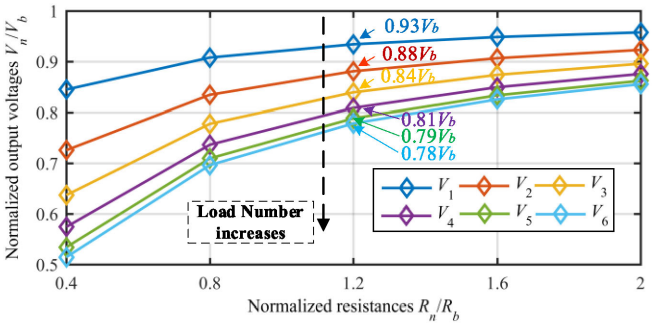

Fig. 6. Output voltages versus load resistances ($k = 0.2$, $Q = 400$, $N = 6$).

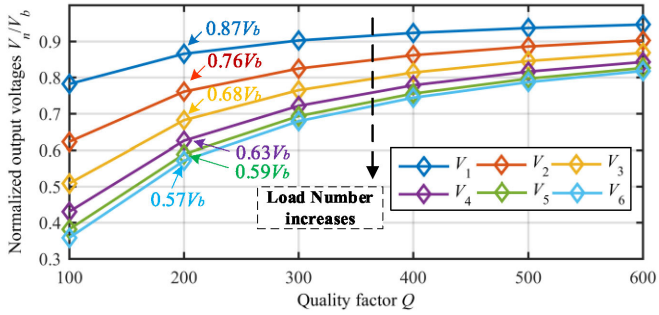

Fig. 7. Output voltages versus quality factors Q ($k = 0.2$, $R = R_b$, $N = 6$).

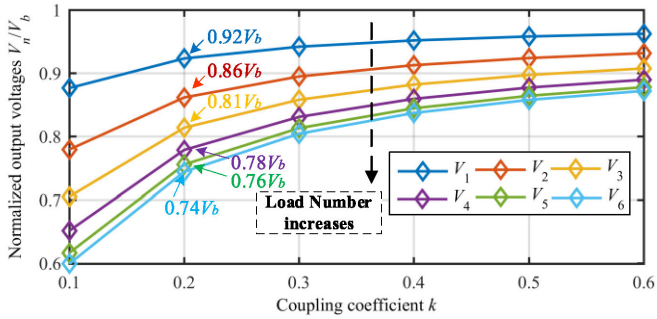

Fig. 8. Output voltages versus coupling coefficient k ($Q = 400$, $R = R_b$, $N = 6$).

By substituting (12) into (13), it is calculated as follows:

$$V_1 = -\frac{L_{1\_f}}{M_1}\frac{Z_{0\_t}}{(r_{0\_t}+Z_{0\_t})}V_0$$
$$V_2 = -\frac{L_{2\_f}}{M_2}\frac{Z_{1\_t}}{(r_{1\_t}+Z_{1\_t})}V_1, \ldots$$
$$V_n = -\frac{L_{n\_f}}{M_n}\frac{Z_{n-1\_t}}{(r_{n-1\_t}+Z_{n-1\_t})}V_{n-1}. \quad (14)$$

Therefore, the output voltage $\boldsymbol{V}_n$ can be obtained from the input voltage $\boldsymbol{V}_0$, shown as

$$\boldsymbol{V}_n = (-1)^n \boldsymbol{V}_0 \prod_{m=1}^{n}\left(\frac{L_{m\_f}}{M_m}\frac{Z_{m-1\_t}}{(r_{m-1\_t}+Z_{m-1\_t})}\right). \quad (15)$$

It clearly shows that the output voltage is reduced by the parasitic resistances. Then, the input power $\boldsymbol{P}_{\text{in}}$, the total load lower $\boldsymbol{P}_l$, and efficiency η are further calculated as

$$P_{\text{in}} = V_0 I_{0\_t}, P_l = \sum_{n=1}^{N} V_n^2/R_n, \eta = P_l/P_{\text{in}}. \quad (16)$$

B. Numerical Analysis of Voltage and Efficiency

To simplify the analysis, assumptions are made as follows: $L_{0\_t} = L_{1\_r} = L_{1\_t} = L_{2\_r} \ldots = L_{N\_r}$, $L_{1\_f} = L_{2\_f} = \ldots = L_{N\_f}$, $k = k_1 = k_2 = \ldots = k_N$, $R = R_1 = R_2 = \ldots R_N$, $Q = Q_{n-1\_r} = Q_{n-1\_t} = Q_{n\_f}$, and $L_{n\_f} = M$. In addition, the frequency f is equal to 200 kHz.

According to (16), the output voltage V_n is a function of k, Q, N, and R. In the analysis process, the resistance, voltage, and power need to be normalized, and the based values are defined as

$$V_b = V_0, R_b = \omega M, P_b = V_b^2/R_b. \quad (17)$$

Fig. 6 shows the relationship between the output voltage V_n and the load resistance R. For example, when $k = 0.2$, $Q = 400$, and $N = 6$, the voltage V_n decreases with a decreased value of R, which is consistent with the designed CV output property. As the load resistance R decreases, the output current increases and the corresponding voltage drop on the parasitic resistance increases, so the output voltage V_n decreases. In addition, for the load far from the transmitter, the voltage drop is more significant. For example, when the normalized load $R/R_b = 1.2$, Fig. 6 clearly shows a decreased voltage sequence $[V_1\ V_2\ V_3\ V_4\ V_5\ V_6] = [0.93V_b\ 0.88V_b\ 0.84V_b\ 0.81V_b\ 0.79V_b\ 0.78V_b]$.

Fig. 7 shows the relationship between the output voltage V_n and the quality factor Q. For example, when $k = 0.2$, $N = 6$, and $R = R_b$, the voltage V_n decreases with a decreased value of Q. It is because that a reduced Q means the parasitic resistance is increased, so the voltage drop is also increased. For example, when $Q = 200$, Fig. 7 clearly shows that the output voltage sequence reduces rapidly as the parasitic resistance increases.

Fig. 8 shows the relationship between the output voltage V_n and the coupling coefficient k. It agrees with common sense that the voltage V_n decreases with a decreased value of k. When $k = 0.2$, $Q = 400$, and $N = 6$, and $R = R_b$, the output voltage sequence is also shown in Fig. 8.

Besides, the impact of the parasitic resistances on the system efficiency is analyzed. Here, the efficiency is calculated based on the ratio between the total output power of all power relays and the input power. Fig. 9 shows the relationship between the efficiency and coupling coefficient k. It shows that increasing k and Q both contribute to improving efficiency. For example, when $Q = 400$, $R = R_b$, and $N = 6$, it clearly shows that the overall system efficiency can reach 60% as long as k and Q are large enough ($k > 0.2$, $Q > 200$).

Fig. 10 shows the relationship between the efficiency and the load resistance R. For example, when $k = 0.2$ and $Q = 400$, it clearly shows that there is an optimal load resistance that can maximize the system efficiency. An enlarged figure is used to provide the efficiency details, showing that the maximum achievable efficiency reduces with an increasing number of N. It is because when the number of power relays increases, the power loss also increases, and the efficiency is reduced. For example,

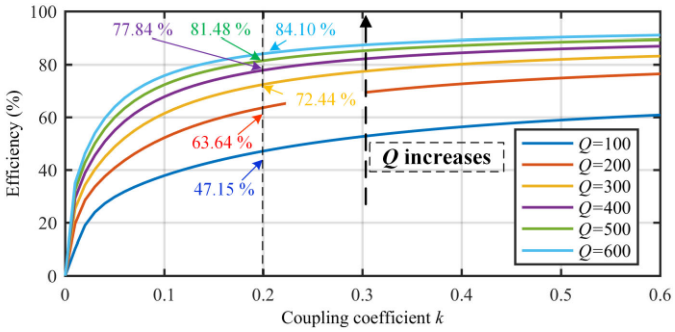

Fig. 9. Efficiency versus coupling coefficient k under multiple Q ($R = R_b$, $N = 6$).

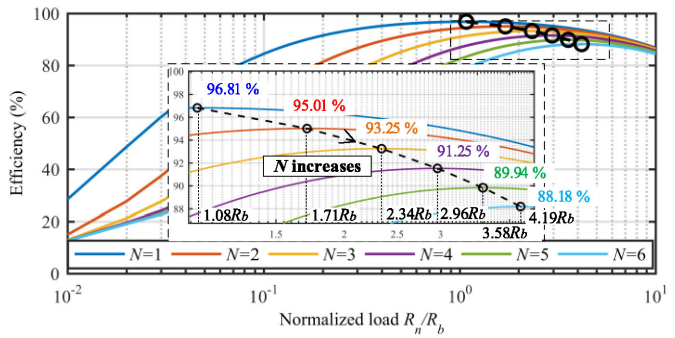

Fig. 10. Efficiency versus normalized load R_n/R_b ($k = 0.2$, $Q = 400$).

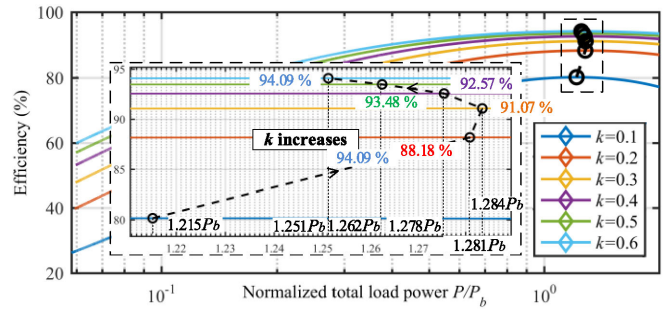

Fig. 11. Efficiency versus load power at various k ($N = 6$, $Q = 400$).

when $k = 0.2$, $Q = 400$, $N = 6$, the optimal load condition is $R_{\text{best}} = 4.19R_b$, and the maximum efficiency is 88.18%.

Fig. 11 shows the relationship between the efficiency and the total output power. For example, when $Q = 400$ and $N = 6$, it shows that there is an optimal power value that can maximize system efficiency. Also, an enlarged figure is provided to show the details. In this case, when k increases, the maximum efficiency also increases. Meanwhile, it also shows that the optimal power condition P_{best} is around $1.25P_b$.

Fig. 12 summaries the maximum achievable efficiency at different k, Q, and N. In this analysis, it is assumed that the load resistances have been tuned to maximize efficiency. It clearly shows the power transfer capability of a power relay system, and it also provides the guideline to design a practical system. For example, if we need to achieve an efficiency above 88.16% for a six-power-relay system with quality factor $Q = 400$, we have to optimize the coils and circuit components to ensure that the coupling coefficient k is higher than 0.2.

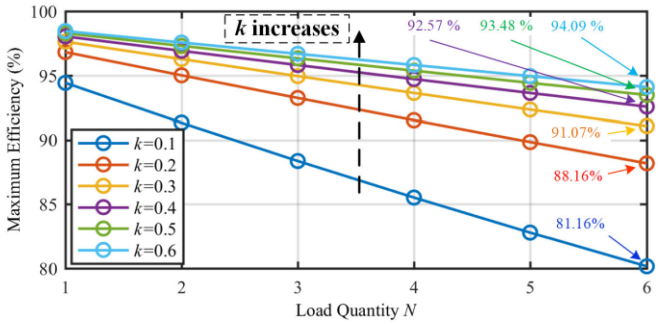

Fig. 12. Maximum efficiency at different load quantity ($Q = 400$).

C. Tune Inductance to Achieve Equal Voltage Distribution

The previous analyses in Figs. 6–8 have shown the voltage difference among different receivers. For the receiver far from the transmitter, the voltage is significantly reduced. However, in the practical application to power multiple gate drivers, we need to maintain equal voltage distribution for all the gate drivers. Therefore, we propose to tune the circuit parameters in order to achieve equal voltage distribution.

Based on (15), in order to achieve equal voltages, circuit parameters should satisfy the following equation:

$$1 = \frac{L_{1\_f}}{M_1}\frac{Z_{0\_t}}{(r_{0\_t}+Z_{0\_t})} = \frac{L_{2\_f}}{M_2}\frac{Z_{1\_t}}{(r_{1\_t}+Z_{1\_t})} = \cdots = \frac{L_{n\_f}}{M_n}\frac{Z_{n-1\_t}}{(r_{n-1\_t}+Z_{n-1\_t})}. \tag{18}$$

By substituting the impedance in (11) into (18), the inductance ratio is calculated as

$$\frac{L_{n\_f}}{M_n} = 1 + \frac{r_{n\_r} + (\omega L_{n\_f})^2 \Big/ Z_{n\_r}}{(\omega M_n)^2} r_{n-1\_t}. \tag{19}$$

According to Appendix, $\omega M_n >> r_{n\_r}$. Then, the parameter relationship could be expressed as

$$(r_{n-1\_t}/Z_{n\_r})\,(L_{n\_f}/M_n)^2 - L_{n\_f}/M_n + 1 = 0. \tag{20}$$

Therefore, according to (9), (12), and (20), the inductance ratio L_{n_f}/M_n can be calculated. It means that the equal voltage distribution performance would be achieved through tuning either the compensation inductance L_{n_f} or the mutual inductance M_n. In this design, L_{n_f} could be tuned because it is more convenient to reach.

Fig. 13 shows the output voltage distribution in four power relays with $k = 0.2$, $Q = 400$, and $N = 4$. For example, the voltages in two cases (with and without inductance tuning) are also compared as follows.

1) When there is no tuning, the inductances satisfy $L_{1\_f} = L_{2\_f} = \ldots = L_{N\_f}$, and the output voltages follow the dashed lines in Fig. 13. Especially for the $R = R_b$ condition, it shows that the first voltage V_1 is 91.11% of the base voltage, but the fourth voltage V_4 is only 78.47% of the base voltage.
2) However, when there is tuning, the inductances satisfy (22), and the output voltages follow the solid lines in

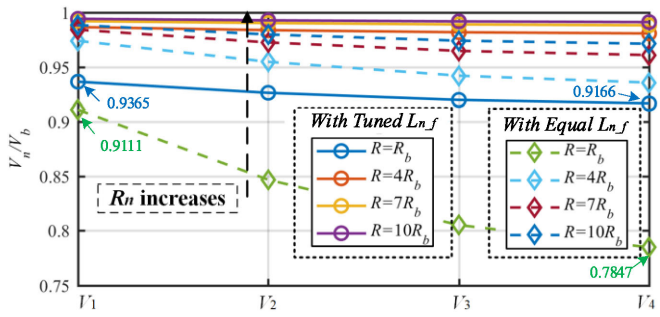

Fig. 13. Output voltages at various load resistances ($k = 0.2$, $N = 4$, $Q = 400$).

TABLE I
INITIALIZED PARAMETERS

Parameters	Values	Parameters	Values
Load number N	4	*Working frequency f*	200 kHz
Output voltages V_n	18 V	*Coupling coefficient k*	0.2
Output power P_n	10 W	*Quality factor Q*	300

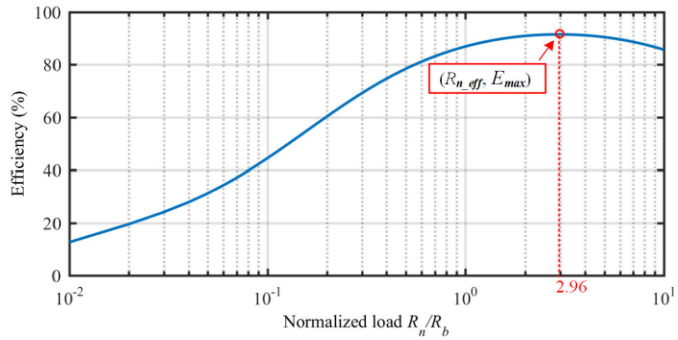

Fig. 14. Efficiency versus normalized load R_n/R_b ($Q = 300$, $k = 0.2$, $N = 4$).

Fig. 13. It clearly shows that the voltage differences among different power relays are significantly reduced. When $R = R_b$, it shows that the first voltage V_1 is 93.65% of the base voltage, and the fourth voltage V_4 is still maintained at 91.66% of the base voltage. Therefore, it is effective to achieve equal voltage distribution among different power relays.

IV. Experimental Validation

A. Parameter Design

In this article, the parameter design is aimed at achieving the highest efficiency of the IPT system, and the procedure is expressed as follows.

1) Initialized parameters of the IPT system with four outputs are shown in Table I, where each output has identical voltage and power. The equivalent load resistance R_n could be calculated by $R_n = V^2{}_n/P_n = 32.4\ \Omega$.
2) Same as the analysis method in Section III-B, efficiency versus normalized load R_n/R_b ($R_b = \omega M$) could be obtained, as shown in Fig. 14. The efficiency reaches peak value when $R_n = 2.96R_b$. Therefore, the mutual inductance M could be calculated by $M = R_b/\omega = R_n/2.96\omega = 8.7\ \mu$H. Moreover, based on (6), $L_{n_f} = M = 8.7\ \mu$H to get identical output voltages of the IPT system.

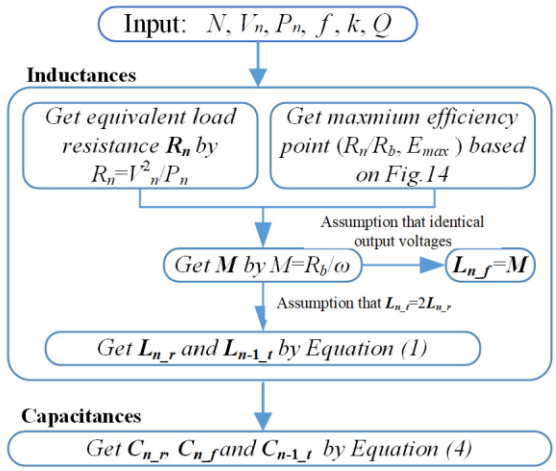

Fig. 15. Flowchart of parameter design.

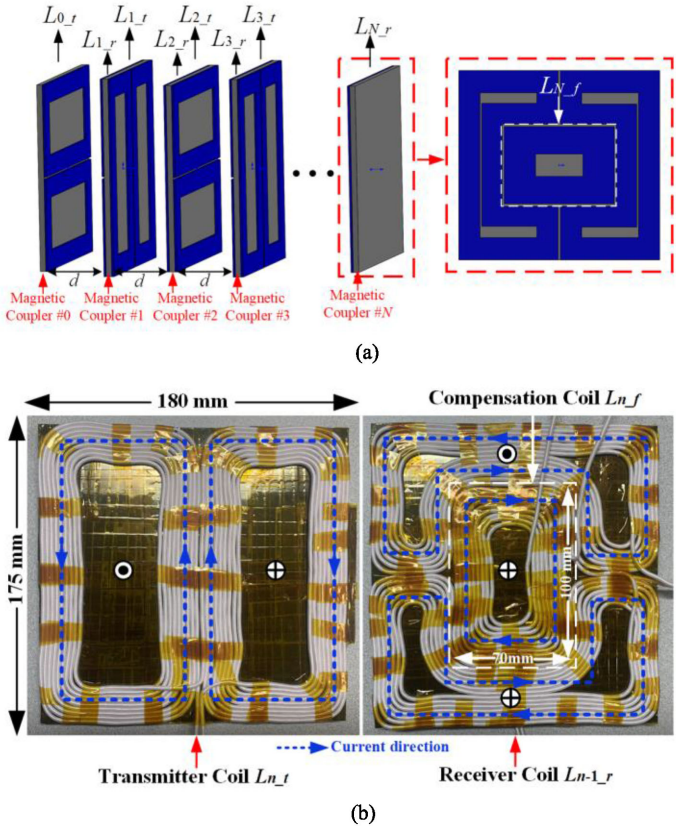

Fig. 16. Proposed integrated magnetic coupler of the power relay system. (a) Three-dimensional model of the proposed magnetic coupler. (b) Prototype of the developed magnetic coupler.

According to the magnetic coupler in the following section, the receiver coil L_{n_r} should be smaller than L_{n_t} because of the smaller occupied area, as shown in Fig. 16. Assuming that $L_{n-1\_t} = 2L_{n\_r}$, L_{n-1_t}, and L_{n_r} could be calculated by (1). L_{n-1_t} and L_{n_r} are 61.6 and 30.8 μH, respectively.

1) Capacitances in the IPT system could be obtained from resonance relationships in (4)

TABLE II
REFERENCE DESIGN VALUES OF A POWER RELAY SYSTEM WITH FOUR LOADS

Parameter	Design Value	Parameter	Design Value
L_{0_f}~L_{4_t}	61.6 μH	C_{0_f}~C_{3_t}	10.3 nF
L_{1_r}~L_{4_r}	30.8 μH	C_{1_r}~C_{4_r}	16.0 nF
L_{1_f}~L_{4_f}	8.7 μH	C_{1_f}~C_{4_f}	72.8 nF

TABLE III
COUPLING COEFFICIENTS SIMULATED BY MAXWELL™

k_{0t_1r}	k_{0t_1f}	k_{0t_1t}	k_{1r_1f}	k_{1r_1t}	k_{1f_1t}
0.20	1.39e-5	6.20e-5	2.50e-3	8.48e-5	2.20e-4
k_{1r_2r}	k_{1r_2t}	k_{1r_2f}	k_{1f_2r}	k_{1f_2f}	k_{1f_2t}
1.88e-5	6.80e-4	3.26e-5	1.20e-3	6.01e-3	4.02e-6
k_{0t_2t}	k_{0t_2r}	k_{0t_2f}	k_{1r_3r}	k_{1r_3f}	k_{1f_3f}
9.66e-4	6.40e-5	7.84e-6	7.50e-4	3.26e-5	1.60e-3

Table II shows the calculated reference design values obtained from the above procedure. Fig. 15 illustrates the flowchart of parameter design.

B. Integrated Magnetic Coupler Design With L_{n_f}

According to Fig. 3, the coupling between adjacent coils should be maximized to transfer power, but other nonadjacent couplings should be minimized to simplify the circuit model. Then, the proposed integrated magnetic coupler structure is shown in Fig. 16.

Fig. 16(a) shows the 3-D structure of the magnetic couplers in the power relay system. Receiver coils and transmitter coils are designed in the bipolar DD structure, while compensation coils are designed in the unipolar structure. For each power relay, there are two coils: one as the receiver and the other one as the transmitter. It could be observed that the first unit only has a transmitter coil and the last unit only has a receiver coil. The transmitter coil is coaxially placed with a 90-degree rotation on the other side of the ferrite plate, to eliminate the coupling between the transmitter coil and receiver coil in a magnetic coupler. Furthermore, there is a ferrite layer in each power relay to reduce the coupling between the receiver and transfer, and it can also reduce the magnetic field emission to the surrounding environment [34], [35].

The compensation coil is put symmetrically in the middle of the ferrite plate and tightly rests to the receiver coils. According to the current direction flowing through coils in Fig. 16(b), DD coils have two magnetic flux groups with the same magnitude and opposite directions, while the unipolar coil has magnetic flux in only one direction. So, the coupling effect among DD coils and the unipolar coil could be negligible.

The 3-D model in Fig. 16(a) is used to simulate the coupling coefficient among coils in the Maxwell software. In the simulation, the magnetic coupler size is 180 mm $\times$ 175 mm, the thickness of the ferrite is 8 mm, and the thickness of the coil is 1 mm. The coils are designed on the surface of the ferrite to make full use of the area. The distance between the adjacent coils is $d = 50$ mm, and the switching frequency is 200 kHz. The simulated results of coupling coefficients among magnetic coupler #0, #1, and #2 are shown in Table III.

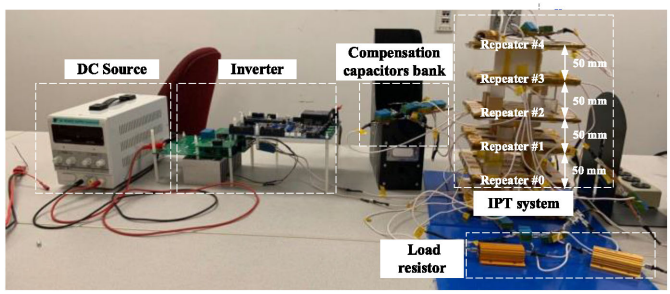

Fig. 17. Experimental setup of a four-load power relay system.

It could be seen from Table III that the desired coupling coefficient k_{0t_1r} between the transmitter and the receiver is maintained as 0.20. The other unnecessary couplings are minimized to extremely small values, which achieves the decoupling among coils.

Fig. 16(b) shows the designed prototype of the magnetic coupler. The 320-strand AWG 40 Litz-wire is used to implement the coils and inductors to reduce the skin-effect and proximity-effect power loss. The ferrite material PC 40 is used to reduce the magnetic loss at 200 kHz. In the coil design, the insulation between adjacent turns is paid extra attention. It clearly shows that the transmitter coil is stand alone as a DD coil, and the receiver coil is integrated with the compensation coils to save space and achieve a compact structure. Since the main coils are all in the DD structure, the inductor L_{n_f} is designed to be a unipolar coil to mitigate all the unnecessary couplings. In the prototype, the main coil size follows the 3-D simulation as 180 mm $\times$ 175 mm, and the compensation inductor size is only 100 mm $\times$ 70 mm.

C. Implementation of the Experimental Setup

According to the resonant relationship in (4) and the magnetic coupler in Fig. 16(a), an experimental setup is implemented to achieve the load-independent and CV property for the gate driver powering the application. The reference design parameters have been provided in Table II. In this example, the input dc voltage 18 V, the coupling coefficient is 0.20, which is consistent with the Maxwell simulation results.

Using the Table II parameters as the guideline, a prototype is implemented, as shown in Fig. 17.

Five layers of magnetic couplers are assembled as a tower: the bottom layer is the transmitter, and the top layer is the last receiver. The distance between the adjacent layer is 50 mm. All the couplers are placed in the well-aligned positions to eliminate unnecessary couplings. High-frequency film capacitors are used to reduce the power loss, and the silicon carbide device based inverter is used at the input side to provide the 200 kHz switching ability. Besides, four resistors are connected with the power relay to work as the loads.

Table IV shows the actual measured values of parameters. Since the coils are manually wound, there are unavoidable differences from the designed values. Through comparing the values in Tables II and IV, it shows that all the parameters are consistent with the desired values. The capacitance values

TABLE IV
MEASURED PARAMETERS OF THE EXPERIMENTAL SETUP IN Fig. 17

Parameter	Value	Parameter	Value	Parameter	Value
L_{0_t}	60.46 μH	L_{3_f}	8.55 μH	C_{1_f}	75.40 nF
L_{1_t}	61.02 μH	L_{4_f}	8.56 μH	C_{2_f}	72.82 nF
L_{2_t}	62.03 μH	C_{0_t}	10.29 nF	C_{3_f}	74.44 nF
L_{3_t}	61.87 μH	C_{1_t}	10.40 nF	C_{4_f}	73.63 nF
L_{1_r}	32.57 μH	C_{2_t}	9.98 nF	k_1	0.195
L_{2_r}	35.52 μH	C_{3_t}	10.02 nF	k_2	0.191
L_{3_r}	32.96 μH	C_{1_r}	15.00 nF	k_3	0.202
L_{4_r}	32.78 μH	C_{2_r}	14.48 nF	k_4	0.201
L_{1_f}	8.80 μH	C_{3_r}	15.10 nF	Q	320
L_{2_f}	8.82 μH	C_{4_r}	14.84 nF	L_s	4.6 μH

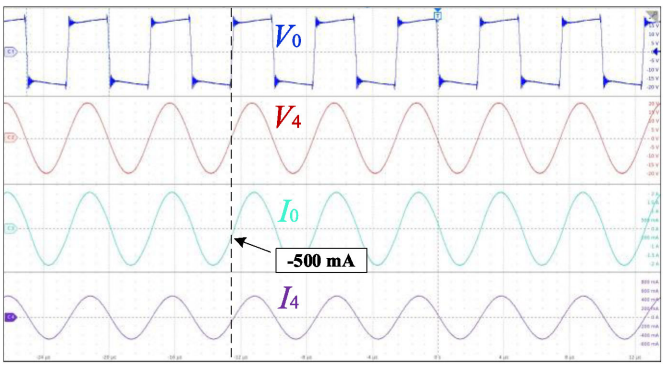

Fig. 18. Experimental waveforms when the load resistance is 40 Ω.

are tuned through (4) to achieve resonances in the circuit. In addition, the parasitic inductance L_s of the load resistor is also measured, showing a value of 4.6 μH, which is also considered in the circuit.

D. Experimental Results of Output Voltages

Experiments are conducted to evaluate the performance of the prototype. When the input voltage is 18 V, and each power relay is connected with a 40 Ω resistive load, the measured waveforms are shown in Fig. 18.

In Fig. 18, the square-wave inverter voltage $\boldsymbol{V}_0$ is used as the excitation, and the inverter current $\boldsymbol{I}_0$ is in phase with $\boldsymbol{V}_0$, showing that the ZPA condition is achieved at the input side. At the switching transient, the current magnitude is 500 mA, which contributes to achieving soft-switching for the MOSFETs in the inverter. Fig. 16 also shows the voltage and current waveforms of the fourth receiver, validating effective power transfer has been achieved. In addition, according to (7), V_4 should be in phase with the input voltage V_0, which is also validated in this experiment.

Fig. 19 shows the output voltages $\boldsymbol{V}_1$–$\boldsymbol{V}_4$ waveforms when all the load resistances change to 60 Ω. In the experiments, all the voltage waveform data is recorded by the oscilloscope and replot in MATLAB for comparison. There are two phenomena that should be paid attention to.

1) The phase difference between adjacent voltages is 180°, which is consistent with (7).
2) The amplitudes of voltages $\boldsymbol{V}_1$–$\boldsymbol{V}_4$ are close to each other. With the load number increases, there is a slight voltage drop from $\boldsymbol{V}_1$ to $\boldsymbol{V}_4$ due to parasitic resistances, but the difference is not significant. It validates that the implemented power relay system has a relatively high-quality factor Q, which is consistent with the voltage analysis in Figs. 6–8.

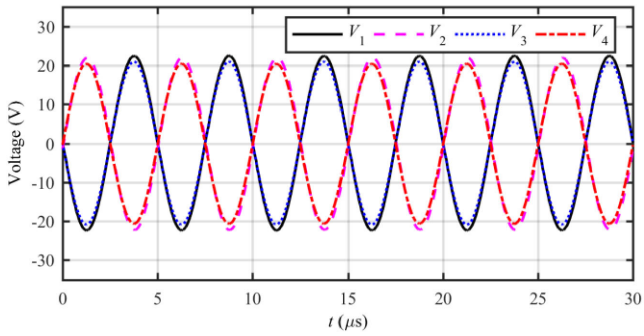

Fig. 19. Measured waveforms of output voltages at the load resistor of 60 Ω.

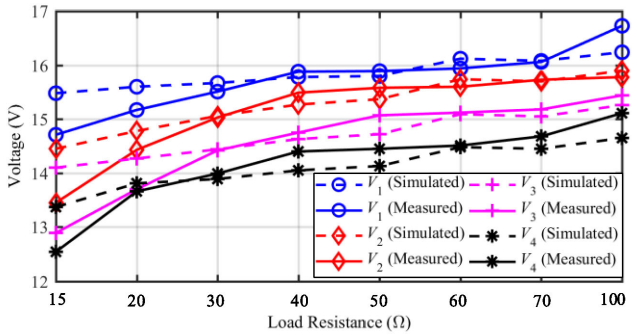

Fig. 20. Measured and simulated output voltages at different load resistance.

TABLE V
OUTPUT VOLTAGE REGULATION RATE FROM MEASUREMENTS IN Fig. 20

	V_1	V_2	V_3	V_4
Simulated Results	0.26	9.12%	7.62%	8.73%
Measured Results	12.07%	14.77%	16.52%	17.01%

Fig. 20 shows the measured rms values of the output voltages when the load resistance R varies in a wide range from 15 to 100 Ω. There are also two phenomena that should be emphasized.

1) The output voltage $\boldsymbol{V}_n$ reduces with a decreased value of load resistance. In order to quantify the voltage variation at different load conditions, a concept of output voltage regulation rate α_n as defined as

$$\alpha_n = \frac{V_{n|R_n=100\Omega} - V_{n|R_n=15\Omega}}{V_{n|R_n=100\Omega}} \times 100, n = 1, 2, 3, 4. \tag{21}$$

For each power relay, the output voltage at $R_n = 100$ Ω is selected as the reference value, and the load regulation rate is calculated, as shown in Table V. It clearly shows that the load regulation rate for the first voltage $\boldsymbol{V}_1$ is 12.07% and the rate for the fourth voltage $\boldsymbol{V}_4$ is 17.01%. With a change of the load resistance in the range between 15 and 100 Ω, the output voltage of the power relay is maintained around 18 V, which is load-independent CV output.

1) The experimental results are also compared with the simulation results. The simulation is built in LTspice, and

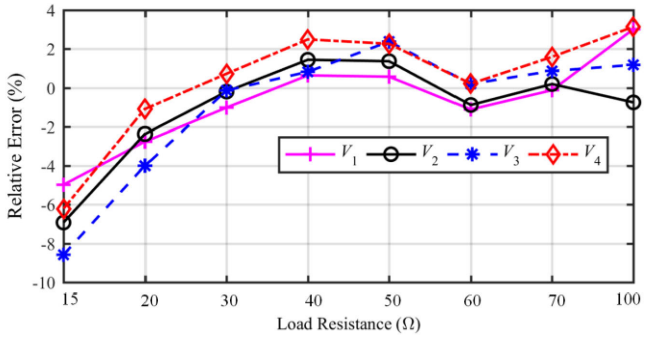

Fig. 21. Relative errors between measured and simulated voltages in Fig. 20.

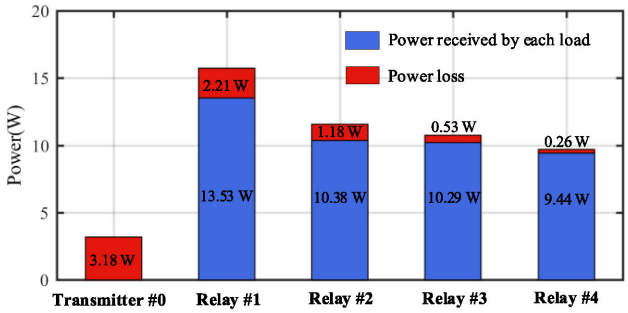

Fig. 22. Power distribution among receivers with the load resistance of 15 Ω.

the simulated component models follow the parameters in Table IV. Fig. 20 clearly shows that the simulation agrees well with the experiment.

Fig. 21 compares the relative error between the experiment and simulation for different output voltages V_1–V_4. It shows that the relative error is within $\pm 10\%$.

E. Experimental Results of Efficiency and Power Loss

Fig. 22 shows the power distribution among relays when the load resistance is 15 Ω. In this case, the system achieves maximum power. It shows that the output power is almost equally distributed among relays. The first relay receives 13.53 W and the fourth relay receives 9.44 W. The difference in power is mainly induced by the voltage difference presented in the previous section. The power loss analysis shows that the first transmitter generates the highest power loss, which is because the circulating current in the transmitter is relatively large.

Fig. 23 shows the relationship between system efficiency and load resistance R_n. When the load varies from 15 to 100 Ω, there is an optimal load resistance that can maximize the efficiency, which is consistent with the analysis in Fig. 10. In this design, the maximum efficiency is 89.79% when the load is 40 Ω. In addition, the system is also simulated in LTspice, and the simulated efficiency aligns well with the experiments.

Fig. 24 shows the relationship between system efficiency and output power. There is an optimal value that can maximize efficiency, which is consistent with the analysis in Fig. 11. In this design, when the output power is 22 W, the system efficiency reaches the maximum value. In addition, the simulation results also agree well with the experiments.

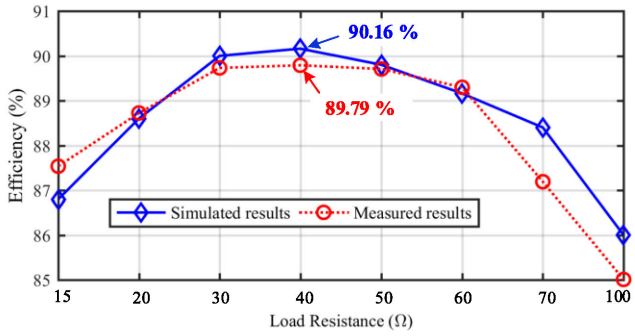

Fig. 23. Comparison of the measured and simulated efficiency at different load resistance from 15 to 100 Ω.

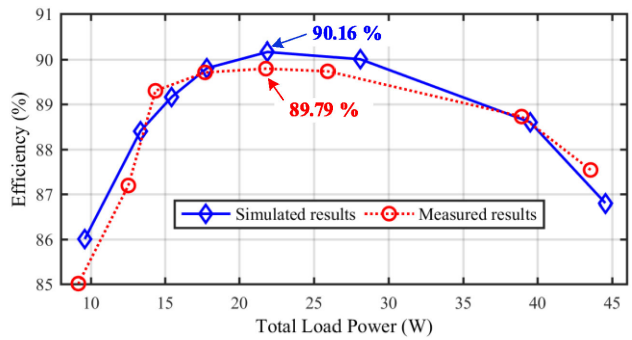

Fig. 24. Comparison of the measured and simulated output power at different load resistance from 15 to 100 Ω.

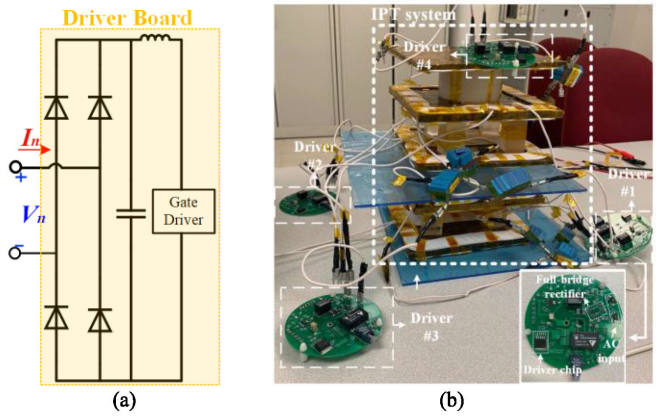

Fig. 25. Experiments when the IPT system powering gate drivers. (a) Schematics of driver boards. (b) Photograph of the experiment.

F. Experimental Results When Powering Gate Drivers

In order to further verify the application values of the proposed IPT system, experiments are conducted in this article. The IPT system is powering four identical gate drivers (Driver #1–#4), as shown in Fig. 25. The applied gate driver has been integrated with a diode full-bridge rectifier. Fig. 26 shows the experimental waveforms. V_0, I_0, and P_0 represent the input voltage, input current, and input power, respectively. V_1 and I_1 represent the voltage and current of driver #1, respectively.

Four output voltages are identical, as shown in Table VI. Table VII reveals that power losses of each gate driver are less than 1 W, and the total output power of the IPT prototype is 2.75 W.

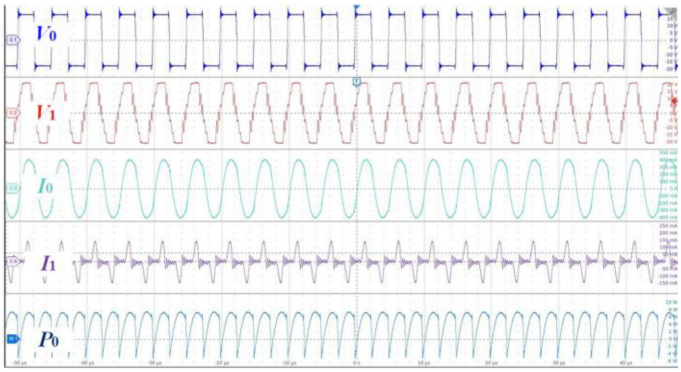

Fig. 26. Experimental waveforms when the load is gate driver.

TABLE VI
MEASURED RMS VALUES OF INPUT AND OUTPUT VOLTAGES

$r_{n\text{-}1\_t}$	r_{n_r}	r_{n_f}
0.26	0.13	0.036

TABLE VII
MEASURED INPUT AND OUTPUT POWER

V_0	V_1	V_2	V_3	V_4
17.69 V	17.25 V	16.73 V	16.33 V	16.13 V

In addition, the calculated efficiency is 65%. The relatively low efficiency is the result of the low power consumption of the gate driver, as shown in Fig. 24. It is expected that the IPT system could achieve higher efficiency with a higher output power.

V. CONCLUSION

This article proposed an S-CLC compensated inductive power relay system to achieve the load-independent CV property. The circuit working principle and the output voltage expressions were derived. This article showed that the CV property could be achieved with proper parameter design. Moreover, the system efficiency was analyzed by considering the parasitic resistances of coils in the circuit. A design methodology was also proposed to maintain the output voltage through tuning the compensation inductance L_{n_f} and the mutual inductance M_n.

Besides, the parameter design methodology to achieve the highest efficiency of the IPT system was proposed as a guideline. A prototype was implemented to transfer power to four power relays. The output voltage was around 15 V, and the load regulation rate was within 17.01% when the load resistance varied from 15 to 100 Ω. Therefore, this result further validated the proposed CV design. The maximum power could reach 13.53 W, and the maximum efficiency was 89.79%. In addition, the prototype was used to power gate drivers with a total power of 2.75 W, validating the proposed IPT topology.

APPENDIX

The parasitic resistances of coils could be calculated by

$$\begin{cases} r_{n-1\_t} = \omega L_{n-1\_t}/Q_{n-1\_t}, \\ r_{n\_r} = \omega L_{n\_r}/Q_{n\_r} \end{cases}, n = 1, 2, \ldots, N \tag{A1}$$

TABLE VIII
CALCULATED RESULTS OF PARASITIC RESISTANCES

P_0	P_1	P_2	P_3	P_4
4.3 W	720.6 mW	700.1 mW	686.7 mW	638.1 mW

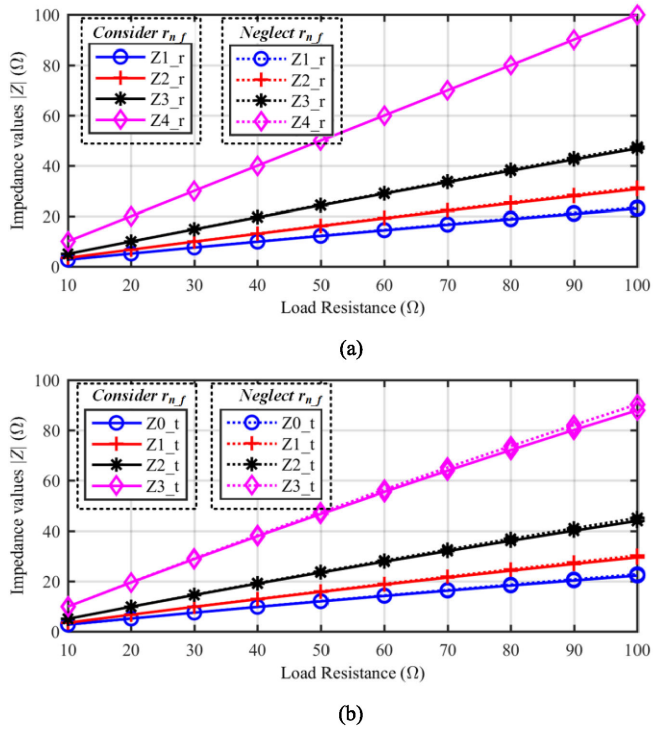

Fig. 27. Calculated results of reflection impedances. (a) Z_{n_r} ($n = 1, 2, 3, 4$). (b) Z_{n-1_t} ($n = 1, 2, 3, 4$).

Table VIII shows the calculated results. The base value $R_b = \omega M = 10.9\ \Omega$. It could be noticed that $R_b >> r_{n-1\_t} > r_{n\_r} > r_{n\_f}$.

Reflection impedances could be expressed by

$$\boldsymbol{Z}_{n\_r} = \begin{cases} \frac{(\boldsymbol{Z}_{n\_t}+r_{n\_t})R_n}{\boldsymbol{Z}_{n\_t}+r_{n\_t}+R_n}, n = 1, 2, \ldots, N-1 \\ R_N, n = N \end{cases} \tag{A2}$$

$$\boldsymbol{Z}_{n-1\_t} = \frac{(\omega M_n)^2}{r_{n\_r} + j\omega L_{n\_r} + \frac{1}{j\omega C_{n\_r}} + \frac{(Z_{n\_r}+1/j\omega C_{n\_f})(r_{n\_f}+j\omega L_{n\_f})}{r_{n\_f}+Z_{n\_r}+1/j\omega C_{n\_f}+j\omega L_{n\_f}}}. \tag{A3}$$

Assuming that r_{n_f} could be neglected, (A3) could be simplified as

$$\boldsymbol{Z}_{n-1\_t} \approx \frac{(\omega M_n)^2}{r_{n\_r} + \frac{(\omega L_{n\_f})^2}{Z_{n\_r}}}, n = 1, 2, \ldots, N. \tag{A4}$$

Based on reference parameter values shown in Tables I and II, Fig. 27 shows that calculated reflection impedances increase as the load resistance varies from 10 to 100 Ω. Calculated results considering r_{n_f} are consistent with these neglecting r_{n_f}. So, r_{n_f} could be negligible in calculating reflection impedances.

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