Aging Detection and State of Health Estimation of Live Power Semiconductor Devices Using SSTDR Embedded PWM Sequence

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***Abstract*—Power semiconductor switches undergo degradation due to environmental and electro-thermal stresses resulting in an impedance variation within the device. This impedance variation can be characterized using reflectometry, which is a well-known technique in electromagnetics. A condition monitoring algorithm for power devices in a live power converter using spread spectrum time domain reflectometry (SSTDR) method has been introduced in this article. SSTDR has been successfully used for locating transmission line faults and detecting device degradation in power converters while running at static condition. However, the rapid variation in impedance throughout the entire live converter circuit caused by fast switching makes condition monitoring more challenging while using SSTDR. This article addresses these shortcomings by proposing a novel solution that can be successfully used to identify the aging of the power devices in a live converter. SSTDR test signal was applied at various test nodes in three different circuits: a single-phase H-bridge photovoltaic inverter, a dc–dc buck converter, and a three-phase inverter. The experimental results demonstrate that the SSTDR test data are consistent with the aging of the power devices and do not affect the switching performance of the modulation process even the test signal is applied across the gate-source interface of the power MOSFET. This implies that the SSTDR technique can be integrated with the gate driver module, thereby creating a new platform for an intelligent gate-driver architecture that enables real-time health monitoring of power devices while performing features offered by a commercially available driver.**

***Index Terms*—Accelerated aging, dc–dc converter, degradation, *in situ* condition monitoring, intelligent gate driver, power MOSFET, photovoltaic (PV) inverter, reliability, spread spectrum time-domain reflectometry (SSTDR), three-phase power inverter.**

I. Introduction

A POWER converter is an integral part of most consumer and industrial products needing electric power. Various segments such as upcoming all-electric aircraft industry, existing motor drive market, space mission, electric automotive, health sector, renewable energy market, high voltage direct current substation, and many others require the use of power converters. Power semiconductor switching devices are indispensable elements in any power conversion system, especially where heavy but critical power is required. Unfortunately, these power semiconductor devices are failure prone and when they fail, results can be catastrophic. These failures can easily lead to very long downtimes, and safety hazards [1]. According to an industry-based survey conducted by Yang *et al.* [2] (see Fig. 1), around 31% of the responders answered that the power semiconductor devices are the most fragile components in power converters. Reliability of these critical components degrades with time due to mechanical and thermoelectrical stresses during regular operation, therefore downgrading the performance or even complete failure of the overall power conversion systems [2], [3]. The statistics found in [4] show that degradation in power devices accounts for 55% of the power converter failures. Therefore, reliability and performance of the power converters greatly depend on these power semiconductor devices. By conducting condition monitoring (CM), it is possible to assess the degradation of power semiconductor switches, which eventually can predict failures before they happen. This failure prediction can prevent unwanted system shutdown due to the failures and can estimate the remaining life of live power converters.

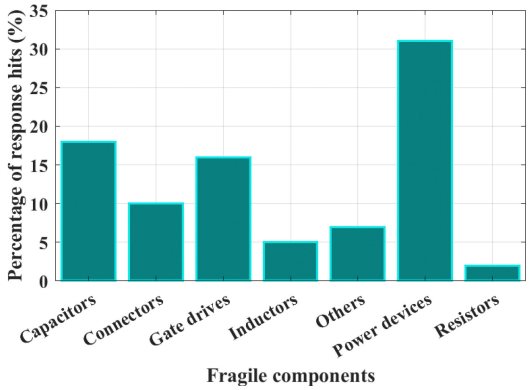

Fig. 1. Survey of different components responsible for converter failure [2].

Two types of aging mechanisms predominately exist among the power semiconductor switches. They are: 1) chip-related aging mechanisms, and 2) package-related aging mechanisms [5], [6]. Chip-related aging involves gate-oxide degradation, which cumulatively shifts the gate-source threshold voltage ($V_{\mathrm{GS(TH)}}$),

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gate leakage current (I_{GSLK}), transconductance or saturation current, or switching turn ON and turn OFF times, etc [7]–[10]. In addition, trapped charges in the gate oxide layer and Si/SiO_2 interface due to gate oxide degradation cause positive $V_{\mathrm{GS(TH)}}$ shift and decrease electron mobility, leading to the increase in the device ON-state channel resistance ($R_{\mathrm{DS(ON)}}$) [11]. Moreover, aluminum bond pad reconstruction and metallization also cause chip degradation, which eventually increases the $R_{\mathrm{DS(ON)}}$. The increase in $V_{\mathrm{GS(TH)}}$ also increases the equivalent series resistance ($\mathrm{ESR_{GS}}$) leading to an increase in the gate-source capacitor impedance ($\mathrm{Z_{eq,GS}}$) [12], [13]. Although chip related degradation causes ultimate device failure, package related failure mechanisms are most frequently observed in power devices [6]. Package related failure/aging leads to an increase in $R_{\mathrm{DS(ON)}}$, ON-state collector-emitter voltage ($V_{\mathrm{CE(ON)}}$), thermal resistance (R_{th}), etc., of a power semiconductor device [5], [6], [14]–[16].

According to recent literature studies, measuring the failure precursors of the power devices, analyzing the model of the degradation process and using system identification are explored to continuously monitor the condition of the power converters. In [17]–[21], $V_{\mathrm{CE(ON)}}$ and/or $R_{\mathrm{DS(ON)}}$ measurements have been carried out to perform device health monitoring. Although these precursors ($V_{\mathrm{CE(ON)}}$ and $R_{\mathrm{DS(ON)}}$) can be measured using specially designed sensors, changes in these quantities are significantly small relative to their OFF-state counterparts, and these sensors often need electrical isolation to block the high dc-link voltage. Therefore, the direct measurement of these parameters is not practical and cost effective for many high voltage applications and could result in low-resolution measurements. It is of paramount interest to detect and track the variation of $V_{\mathrm{CE(ON)}}$ and/or $R_{\mathrm{DS(ON)}}$ without introducing additional sensors or circuitry. Thermal resistance and junction temperature-based CM technique proposed in [22] and [23], can detect solder fatigue inside the packaging of a power module, however, direct measurement of junction temperature is impractical and can only be applied during the idle state of the converter. Switching turn-ON and turn-OFF time-based health monitoring methods proposed in [24] and [25], respectively, can characterize device failure mechanisms along with gate driver circuit degradation. However, the direct measurement of switching transients, often in the range of tens of nanoseconds, requires very high bandwidth and noise immune transient detection circuit with a high-resolution sensor. Recently, other CM methods for gate degradation detection based on Miler Plateau gate voltage [26] and gate leakage current (I_{GSLK}) measurement [10] have been proposed. Like the direct measurement of switching transients, a high-resolution detection circuit with high bandwidth is needed for the abovementioned gate-signal-based CM methods [10], [26], which is very difficult to implement due to the compromise needed between the measurement resolution and signal bandwidth. Moreover, the instrumentation amplifier must withstand large common-mode voltage and is required to offer a very high common-mode rejection ratio even at a very high switching frequency. Although switching transient and gate-signal-based CM methods can be integrated into the gate drivers to make them intelligent, the abovementioned drawbacks along with their ability to only detect gate degradation inhibit their wide range of applications. All of these methods need external sensors to collect aging precursor data that require the use of additional probes, complex hardware as well as digital controllers, which may not be cost effective. Therefore, CM techniques without using internal sensors are indeed highly desirable. System-identification-based CM technique can be implemented without any additional sensors other than those required for the operation of the converter and with minimal additional digital hardware [19], [27], [28]. However, this technique requires an advanced signal processing algorithm, which increases the computation burden. Moreover, derivation of precursor information from external measurements requires establishing an accurate relationship between the device condition and the measurable system performance, otherwise, the variable operating condition of a converter system may produce false results. Data-driven or model-based CM approach proposed in [29] and [30], are based on the comparisons of estimated and measured variables, which require a large number of training data, and they also have a poor estimation of specific variables in different operating conditions.

To overcome these limitations of real-time power converter health monitoring techniques, reflectometry-based method has recently been proven to become a good candidate because this technique does not depend on the direct measurement of the traditional on-site parameters and sensors to detect device aging levels, and therefore, reduces the measurement error. Different reflectometry-based methods have long been used for detecting and locating faults in wires, and a comparative study summarizing different reflectometry methods for fault detection in electrical wiring has been discussed in [31]. Among the known reflectometry techniques, spread spectrum time-domain reflectometry (SSTDR) provides several advantages such as low-cost fault detection in powered/live cables, very high noise immunity, embedded solutions, etc. over the other reflectometry based techniques [31]–[34]. The incident signal of SSTDR is a high-frequency sine modulated pseudonoise sequence (SMPNS), and the corresponding reflections may characterize the level of aging by determining the changes in the impedance. As mentioned earlier, each type of device degradation leads to various impedance changes inside a power device such as $R_{\mathrm{DS(ON)}}$, $\mathrm{Z_{eq,GS}}$, and so on, therefore, this unique feature makes SSTDR an excellent candidate for estimating any device's state of health (SOH). Recently, SSTDR-based technique has been proposed in [35]–[38] for estimating the level of aging associated with power semiconductor switches. However, these techniques could only estimate the device SOH while it was in full conduction mode. Therefore, these methods are only effective while the device is isolated from the circuit and subjected to a dedicated characterization setup with no modulation applied at the gate. That being said, the fast impedance variations in the SSTDR signal propagation path due to high-frequency PWM switching of the device makes interpretation of the SSTDR reflection extremely difficult. The algorithm proposed in this article demonstrates that SSTDR data can be implemented to overcome such limitations resulting in faithful aging detection in power semiconductor switches during the converter operation. Moreover, unlike the traditional sensor or system identification-based CM techniques,

high-frequency noise due to PWM switching does not impact the SSTDR response, therefore making the proposed CM technique effective in a live converter circuit.

This article discusses several case studies regarding real-time SOH estimation of power devices in live converter circuits. First, a single-phase H-bridge grid-tied photovoltaic (PV) inverter was considered where the SSTDR incident signal has been applied across its output terminal nodes. Using the experimental results, authors were able to successfully characterize the degradation level in multiple MOSFETs from this single measurement point. Later, the SSTDR incident signal was applied across the gate-source interface of a power semiconductor device in a synchronous buck converter and a three-phase dc–ac inverter, respectively. Due to the simple implementation of the SSTDR incident signal into the gate-source interface, the SSTDR scheme can potentially be embedded into commercial gate drivers offering built-in-self-test capability, which will eliminate the need for separate SOH modules leading to significant system-level savings [39], [40]. This future integrated gate driver can be termed as intelligent gate driver module (IGDM). After an extensive literature review, only a few papers [10], [41] have been found, which have proposed the concept of implementing this condition-monitoring feature embedded into the gate driver module. However, these methods are not commercially viable as they can only detect gate-oxide degradation based on measuring gate signal and require expensive sensors of high bandwidth with high-resolution detection. Last but not the least, connecting SSTDR hardware to the gate terminal will help in designing it for significantly lower ratings since the gate terminal is always at the lower potential compared to the drain/collector terminal. This will considerably reduce the cost of the CM hardware.

The rest of this article is organized as follows. Section II introduces the SSTDR method and how this can be used in device degradation estimation in a live power converter. Section III describes the accelerated aging testbed and Section IV summarizes the CM monitoring technique of a single-phase H-bridge grid-tied PV inverter applying SSTDR test signal across the ac output node. The CM technique of a synchronous buck converter and 3-phase power inverter applying SSTDR embedded PWM signal across the gate-source interface is discussed in Section V. Section VI discusses the overall aspect of SSTDR-based condition monitoring technique and suggests future research scopes. Finally, the conclusion is provided in Section VII.

II. SSTDR – A New Way of Testing Electronics Live

A. Basic Concepts of Reflectometry

Reflectometry is a well-known technique in electromagnetics, and it has been successfully used for locating and detecting faults in transmission lines [31]–[34], [42], [43] and PV arrays [44], [45], and degradation detection of aged cells in a Li-ion battery pack [46]. As shown in Fig. 2, any incident signal (V_0^+, I_0^+) is sent down the wire and a portion of the signal (V_0^-, I_0^-) is reflected back from the point/node of impedance mismatch or discontinuity in its propagation path. The reflection coefficient (ρ) that represents the ratio between the reflected signal and the

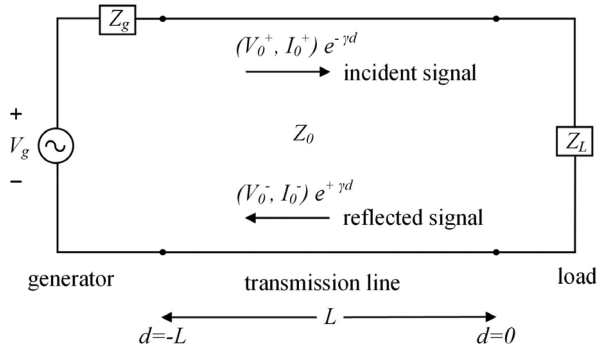


Fig. 2. Schematic diagram of a transmission line of length L and characteristic impedance equal to Z_0. A generator circuit is connected at one end ($d = -L$), and other end ($d = -0$) is connected to load Z_L. An incident signal with voltage and current (V_0^+, I_0^+) traveling towards the load, and a reflected signal with voltage and current (V_0^-, I_0^-) traveling towards the generator.

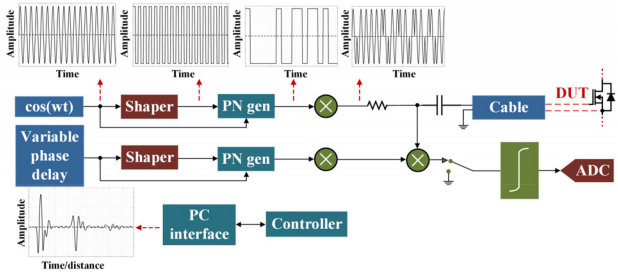


Fig. 3. Schematic diagram of the SSTDR mechanism [34].

incident signal, is defined as follows:

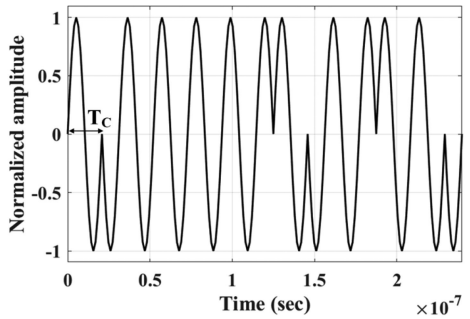
$$\rho = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{1}$$

Here, Z_0 is the characteristics impedance of the cable interconnecting the source and the load/device under test (DUT), and Z_L is the impedance of the load/the DUT.

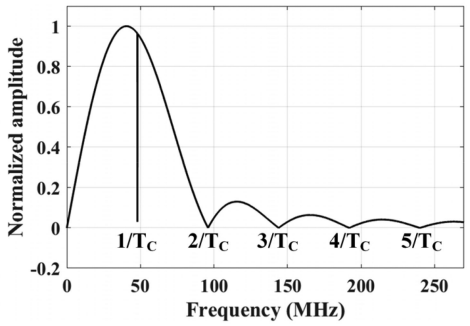
B. SSTDR Operation

Based on the incident signal used in the field, several reflectometry-based fault detection methods exist. Among them, SSTDR uses a SMPNS as the incident signal, which is generated by modulating a pseudonoise code (PN code) with a high-frequency carrier sine wave. PN code consists of randomly generated 1 s and 0 s where each 1/0 is known as a chip [31]–[34], [42]. The frequency of the carrier sine wave is also known as the center frequency of SSTDR. To calibrate the system without any difficulties, the frequency of the carrier sine wave is maintained the same as the chip rate ($f_C = 1/T_C$) of the PN code [34], [42]. The chip rate of the PN code is defined as the number of chips generated each second, and the length of the PN code is defined as the number of chips after the sequence is repeated. SSTDR can be implemented in several ways as discussed in [34], [42], [47], and [48], and a simple schematic diagram is shown in Fig. 3.

As shown in Fig. 3, a sine wave generator (operating at 30–100 MHz) is used as a master system clock, and this generator's



(a)



(b)

Fig. 4. Incident signal of SSTDR with carrier/center frequency equal to 48 MHz. (a) Time-domain representation (a portion of one entire SSTDR sequence is shown here). (b) Frequency-domain (FFT) representation (only the upper side band is shown here).

output is converted to a square wave via a shaper, and the resulting square wave drives a PN sequence generator (PN gen). The output of the PN generator is multiplied with the initial sine wave, generating the SMPNS, which is basically a direct sequence spread spectrum binary phase shift keyed signal. This SMPNS is sent down the wire, and the signal is reflected back if it finds any impedance discontinuity against the characteristic impedance of the propagation path. This reflected signal is cross correlated with the delayed copies of the incident signal with the help of a variable phase delay, and a lobe is generated at a time delay in the autocorrelation plot that corresponds to the distance from the source terminal to the impedance mismatch at the load terminal. A lobe with a positive peak indicates a positive reflection coefficient ($\rho > 0$, if $Z_L > Z_0$) and a negative peak indicates a negative reflection coefficient ($\rho < 0$, if $Z_L < Z_0$).

An example of the SSTDR generated incident signal and the corresponding fast Fourier transformation (FFT) is shown in Fig. 4. The FFT of the PN code is similar to a "sinc" function where the width of the main lobe is twice the chip rate of the PN code. The Fourier transform of the incident signal is similar to a double sideband suppressed carrier signal where the signal has a large spectral distribution since the sinusoidal signal has been used as the modulating signal here. From Fig. 4(b), it is evident that the main lobe shifts further away from 0 Hz once the carrier frequency increases. Since the power in the noise usually centered around 0 Hz, increasing the carrier frequency of SSTDR signal will lead to produce less power in the cross correlation of an SSTDR signal with noise, which

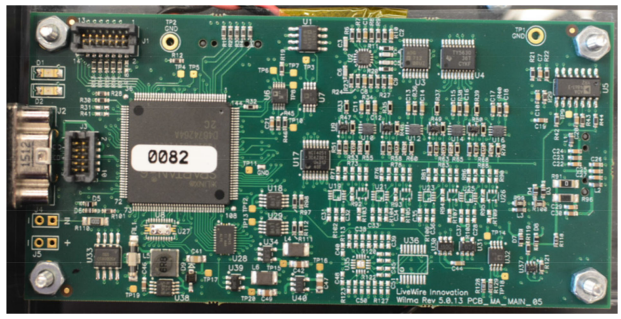
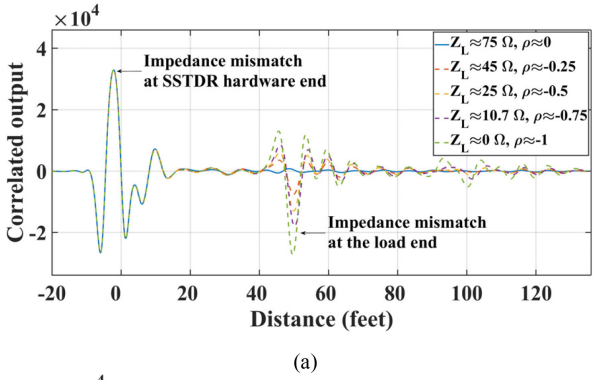


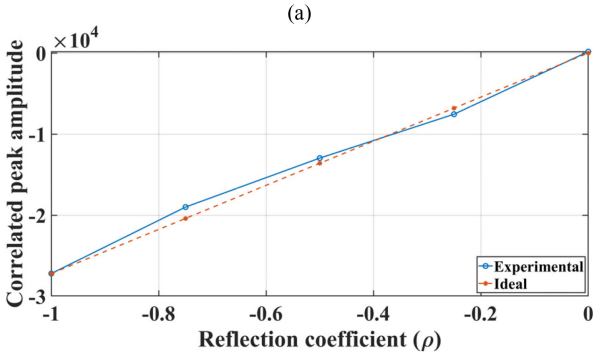
Fig. 5. Photograph of the FPGA-based SSTDR hardware (an R&D product from Livewire Innovation).

will eventually increase the signal-to-noise ratio (SNR) of the system. This ability, in particular, is critical to detect impedance discontinuity, i.e., aging in a DUT when the converter is live. In addition, SSTDR sends down a significantly lower amplitude signal (usually around or below 100 mV and lowest could be 22 mV) that can be placed on top of the existing signals (digital, analog, high-frequency PWM, etc.) at a level much below the noise margin and yet still being able to detect and analyze the SSTDR reflected response. Having the best SNR along with its low voltage characteristics leads to its excellent performance in the live circuit among other reflectometry methods. The authors used a field-programmable-gate-array (FPGA) based SSTDR evaluation kit W50A0071 in this project, which is an R&D product from Livewire Innovation (see Fig. 5). This hardware works in two modes: 1) static and 2) intermittent. In static mode, it scans just for once and, therefore, it is ideal to detect device degradation in a static operating condition. However, intermittent tests scan the system continuously to detect short duration impedance change in SSTDR signal propagation path. The time taken to create and log the autocorrelation data for each scan is approximately 4 ms, which is supposed to be equal to the total time of response, processing, and postprocessing.

From (1), it is evident that the reflection coefficient is negative ($\rho < 0$) for $Z_L < Z_0$ and positive ($\rho > 0$) for $Z_L > Z_0$. Fig. 6(a) shows the different correlation curves that have been generated while applying 48 MHz SSTDR signal passing through a 50 feet RG-6/U coaxial cable having a characteristic impedance of 75-Ω. The first lobe in the autocorrelation plot is due to the impedance mismatch at the hardware end and the second lobe, considered as the main lobe, is due to the impedance mismatch at the load end. The peak value of the main lobe, coined as "autocorrelated peak amplitude", changes with a change in the reflection coefficient. Fig. 6(b) shows the linear relationship between the autocorrelated peak amplitude and the corresponding reflection coefficient obtained from Fig. 6(a). From these two plots, it is evident that, when $\rho \leq 0$, an increased value in Z_L leads to less negative autocorrelated amplitude (or lower magnitude). Since the $R_{DS(ON)}$ and $Z_{eq,GS}$ of a power semiconductor switch is significantly less than that of the SSTDR test cable and the lumped network of the converter circuit, the autocorrelated peak amplitude will be negative ($\rho < 0$), and the increased $R_{DS(ON)}$ and $Z_{eq,GS}$ due to the aging will lower the magnitudes of the autocorrelated amplitudes. For instance, let us consider the equivalent



(a)



(b)

Fig. 6. (a) Variation in correlated amplitudes for the different values of reflection coefficients ($\rho \leq 0$) and load impedances ($Z_L \leq Z_0$) (for 50 feet long, 75 Ω coaxial cable). (b) Variation in the corresponding correlated peak amplitudes for the different values of reflection coefficients ($\rho \leq 0$).

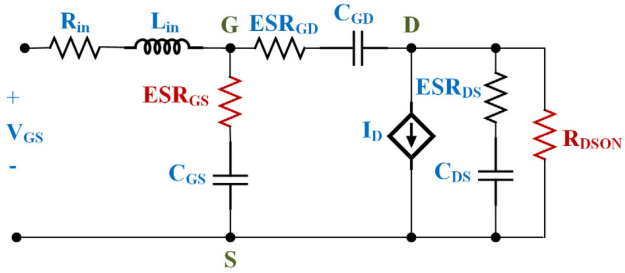


Fig. 7. Simplified equivalent circuit of a power MOSFET [49].

circuit of a MOSFET shown in Fig. 7 [49]. Since $R_{\mathrm{DS(ON)}}$ and $Z_{\mathrm{eq,GS}}$ will increase with aging, the equivalent impedance of an aged device is higher compared to that of a healthy device seen from the gate-source interface. Let the equivalent impedance for a healthy MOSFET seen from gate and source be $Z_{\mathrm{GS,H}}$ and with aging, this impedance is increased to $Z_{\mathrm{GS,A}}$, then if the change in these two measurements is denoted by ΔZ_{GS}, we can express this value as shown in

$$\Delta Z_{\mathrm{GS}} = Z_{\mathrm{GS},A} - Z_{\mathrm{GS},H}. \tag{2}$$

The reflection coefficient, ρ presented in (1), will give the impression of this difference in impedance, and a nonzero value of ΔZ_{GS} will illustrate the aging of the device. For instance, Fig. 8 shows the various reflections for different aging levels (corresponding to different values of $R_{\mathrm{DS(ON)}}$) of the

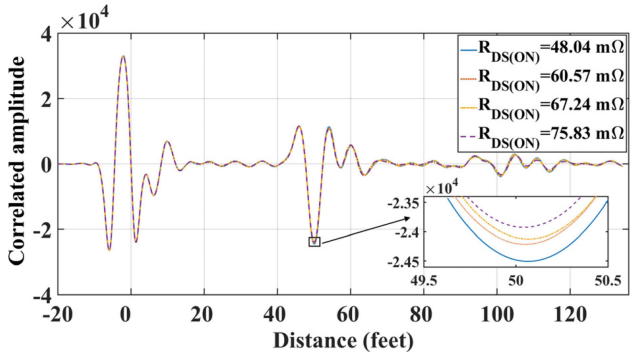


Fig. 8. Correlated amplitude variation for different aging levels (corresponding to different values of $R_{\mathrm{DS(ON)}}$) of a power MOSFET in a buck converter.

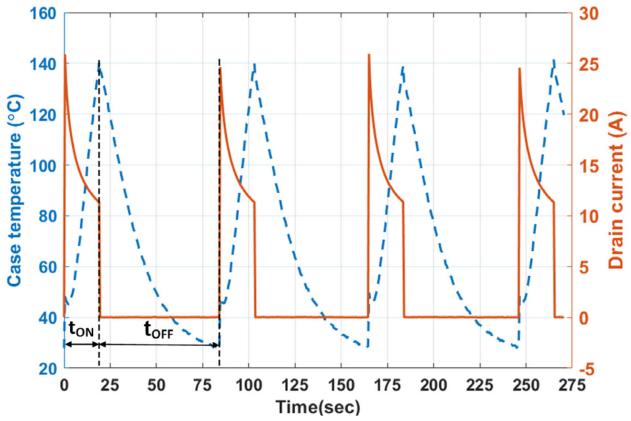
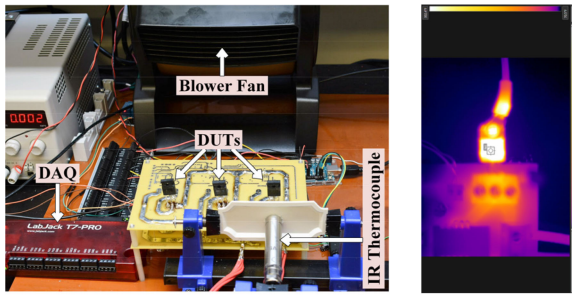


Fig. 9. Case temperature and drain current swing of the DUT during power cycling test of phase-2 (at the start of the aging process for $\mathrm{M_{AP2\_L2}}$).

MOSFET in a buck converter, which was obtained applying a 48 MHz SSTDR signal across the gate-source interface. This test was conducted in a static condition meaning no PWM was applied.

III. Test Setup for Accelerated Aging of Power MOSFETs

Accelerated power cycling tests were implemented in a custom-designed testbed, which was capable of applying electro-thermal stresses to multiple discrete power MOSFETs simultaneously. The accelerated aging was conducted in two separate phases, and devices aged through these separate phases were used as DUTs in two separate case studies discussed in later sections. Please note that the method of accelerated aging was similar in both phases where the temperature swing (ΔT) during this electro-thermal process was achieved by injecting a high current through the device in a controlled manner (as shown in Fig. 9). During the ON-time (t_{ON}) of each power cycle, devices were injected with current until its case temperature (T_{C}) goes up to its upper limit ($T_{\mathrm{C,max}}$) whereas, during the OFF-time (t_{OFF}), the devices were allowed to be cooled down until the T_{C} falls to its lower limit ($T_{\mathrm{C,min}}$). The temperature swing (ΔT) between the $T_{\mathrm{C,max}}$ and $T_{\mathrm{C,min}}$ were maintained constant throughout



(a) (b)

Fig. 10. (a) Custom-built accelerated aging setup. (b) Thermal image during the aging process.

TABLE I
SUMMARY OF THE ACCELERATED AGING PARAMETERS

Phase	MOSFET	$T_{C,min}$/ $T_{C,max}$ (°C)	ΔT (°C)	t_{ON}/ t_{OFF} (sec)	N_f	$\Delta R_{DS(ON)}$= MOSFET $R_{DS(ON)}$- Initial $R_{DS(ON)}$ (mΩ)
1	M_{HP1}	-	-	-	-	0
	M_{AP1}	210/230	20	4/20	2844	38.5
2	M_{HP2}	-	-	-	-	0
	M_{AP2_L1}	30/110	80	14/57	5945	7.19
	M_{AP2_L2}	30/140	110	20/65	6000	12.53
	M_{AP2_L3}	30/110	80	14/57	10500	19.20
	M_{AP2_L4}	30/140	110	20/65	12500	27.79

∗ M_{HP1}=Healthy MOSFET in phase-1, M_{HP2}=Healthy MOSFET in phase-2.
∗ M_{AP1}=Aged MOSFET in phase-1.
∗ M_{AP2_L1}=Aged MOSFET with aging level-1 in phase-2.
∗ M_{AP2_L2}=Aged MOSFET with aging level-2 in phase-2.
∗ M_{AP2_L3}=Aged MOSFET with aging level-3 in phase-2.
∗ M_{AP2_L4}=Aged MOSFET with aging level-4 in phase-2.
∗ Initial $R_{DS(ON)}$ of M_{HP1} is 70.4 mΩ and M_{HP2} is 48.04 mΩ.

the aging process for a certain device. Since the power supply voltage was maintained the same during the t_{ON} of the device, the thermal impedance as well as the $R_{DS(ON)}$ of the device increased gradually from their initial values once the device's temperature increased from the room temperature, resulting in a gradual decrease in the current from its instantaneous high value. During this test, LabJack T-7 Pro data acquisition system was used to measure and record drain-source voltage (V_{DS}), drain current (I_D), and case temperature (T_C) of each switch. These measurements were taken in order to determine the $R_{DS(ON)}$ of the switches. Case temperature (T_C) was measured using an IR thermocouple from OMEGA. The photograph of the actual testbed and the thermal image during the aging process is given in Fig. 10. The applied ΔT, number of power cycles (N_f), $T_{C,min}$, $T_{C,max}$, t_{ON}, t_{OFF}, and the resultant increase in the $R_{DS(ON)}$ ($\Delta R_{DS(ON)}$) of the devices are summarized in Table I, and the detailed descriptions of the two phases of the aging process is given as follows.

Phase-1: A 300V-40 A rated N-channel Si power MOSFET (HiPerFET™ power MOSFET in a TO-247 package) was electro-thermally aged with a temperature gradient (ΔT) of 20 °C where $T_{C,max}$ and $T_{C,min}$ thresholds were maintained at 230 °C and 210 °C, respectively. The t_{ON} and t_{OFF} times were recorded as 4 s and 20 s, respectively. In addition, when the aging process started, the drain current was recorded as 12.8 A at $T_{C,min}$ and 9.2 A at $T_{C,max}$. After 2844 power cycles, the $R_{DS(ON)}$ of the DUT changed from 70.4 mΩ to 108.9 mΩ ($\Delta R_{DS(ON)}$ = 38.5 mΩ). This higher value of $R_{DS(ON)}$ is a clear indication of the device's aging, and this aged device was used as the DUT for SOH monitoring of a single-phase H-bridge grid-tied PV inverter described in case study-1.

Phase-2: In this phase, multiple N-channel Si MOSFETs were electro-thermally aged with similar ratings (600 V, 50 A, MDmesh™ DM2 power MOSFET in a TO-247 package). For instance, as shown in Fig. 9, the MOSFET with aging level-2 (M_{AP2_L2}) was power cycled with ΔT of 110 °C where $T_{C,max}$ and $T_{C,min}$ were maintained at 140 °C and 30 °C, respectively. Initially, during a given cycle, the drain current was recorded as 25 A at $T_{C,min}$ whereas it was measured as 11.3 A at $T_{C,max}$. The dissipated power was recorded to be ∼20.39 W in each cycle. The aging process was continued for 6000 cycles, and it was found that the change in $R_{DS(ON)}$ was 12.53 mΩ. In phase-2, when the switch was turned OFF, a cooling fan (axial fan) was activated to expedite the cooling process. The devices aged in this phase were used as the DUTs in case study-2.

The majority of the studies concerning the reliability of power MOSFET identify increased $R_{DS(ON)}$ as a precursor of aging due to active power cycling [11], [28], [50]. Therefore, $R_{DS(ON)}$ increment will refer to the severity of device degradation throughout this article, although the direct relationship between device aging level and $R_{DS(ON)}$ is still unknown [5], [15].

The following sections discuss several case studies regarding real-time SOH estimation of power devices in live converter circuits.

IV. CASE STUDY-1: SOH MONITORING OF A SINGLE-PHASE H-BRIDGE GRID-TIED PV INVERTER APPLYING SSTDR TEST SIGNAL ACROSS AC OUTPUT NODE

Grid-tied PV inverter is one of the key components in the PV-based renewable energy system where inverters contribute to more challenging reliability issues because of their complicated switching schemes and the use of different component types with dissimilar aging characteristics [51]. In PV-based power system, the inverter itself usually has a much shorter life (∼10 years) than the PV module (more than 20 years) [51], and 36% of lost energy is occurred due to inverter failures as opposed to 5% loss occurred by the PV module failures [52]. Therefore, making the PV inverter more reliable is the key to prevent the unwanted loss of potential energy production in PV power systems. In our first case study, the proposed SOH monitoring algorithm was implemented in a 700 W H-bridge single-phase PV inverter where two SSTDR hardware test points, TP-1 and TP-2, as shown in Fig. 11, has been connected across ac output nodes.

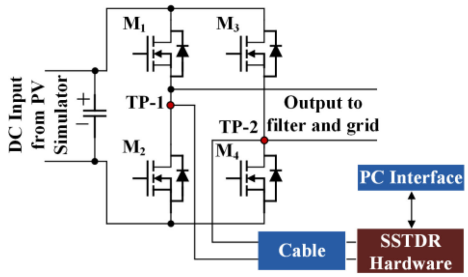


Fig. 11. SSTDR test diagram for detecting device degradation in a single-phase H-bridge grid-tied PV inverter.

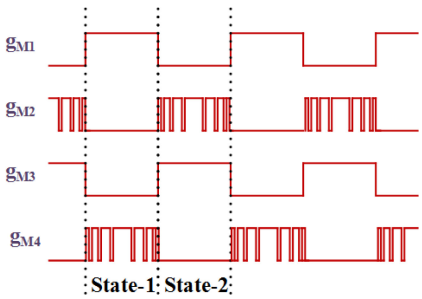


Fig. 12. Switching scheme used for the single-phase H-bridge grid-tied PV inverter under test.

TABLE II
SWITCHING STATES OF THE PV INVERTER (M1, M2, M3, AND M4 REPRESENT ITS FOUR MOSFETS)

State	Sub-State	M_1	M_2	M_3	M_4
1	a	ON	OFF	OFF	PWM (OFF)
	b	ON	OFF	OFF	PWM (ON)
2	a	OFF	PWM (OFF)	ON	OFF
	b	OFF	PWM (ON)	ON	OFF

A. Equivalent Path Impedances

Throughout this article, the term "path impedance" will be used to refer to the equivalent path impedance between the test points seen by the SSTDR test signals. In order to determine the path impedances across the ac output nodes under various operating states, the modulation scheme, or switching states (ON/OFF) of the PV inverter under test was studied [53]. It is worth mentioning that in order to minimize the switching loss, the MOSFET pair M_1 and M_3 are switched at grid fundamental frequency using 60 Hz square wave mode in a complementary fashion whereas the other switch pair M_2 and M_4 are switched using 20 kHz sine modulated PWM (SPWM) mode (see Fig. 12). As a result, at each 60 Hz cycle, two switching states were found, and each of which was further divided into two substates without considering the dead-band and the switching transients (see Table II). That being said, the conduction states or path impedances change rapidly between the two substates where the maximum time duration of each substate is 1/20 kHz = 0.05 ms.

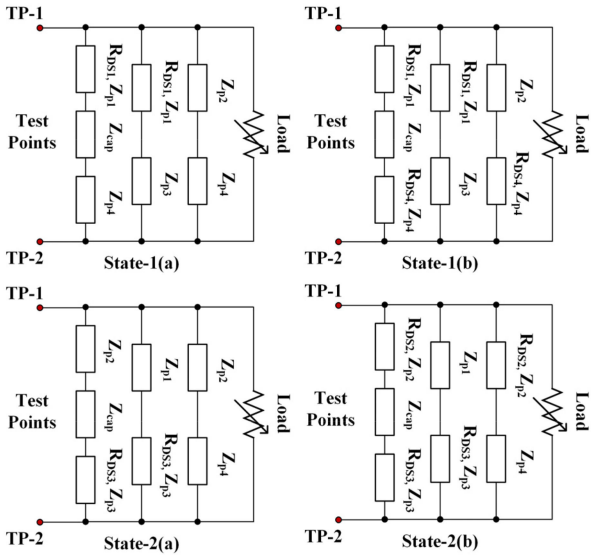


Fig. 13. Various equivalent SSTDR impedance paths inside the PV inverter. Here, Z_{cap}= impedance of the dc bus capacitor, R_{DS}= ON-state channel resistance of the MOSFET, and Z_p= lumped impedance due to the parasitic capacitances of the MOSFET.

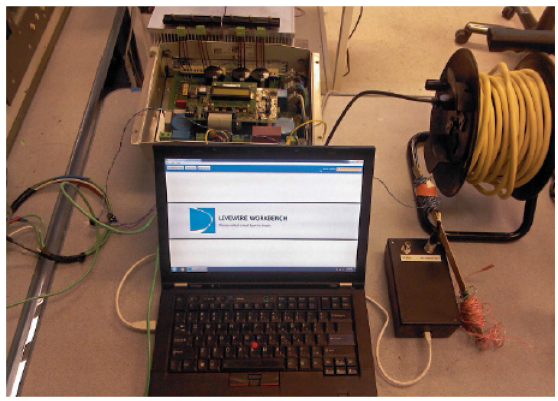


Fig. 14. Experimental test set-up for condition monitoring of H-bridge grid-tied PV inverter under test.

The resulting path impedances corresponding to these switching states are shown in Fig. 13 in a simplified manner.

It is well understood that $R_{DS(ON)}$ and $Z_{eq,GS}$ of a MOSFET increases with the higher level of aging, which will increase each path impedance of corresponding substates. Evidently, this increase in the equivalent impedance affects the propagation of the SSTDR signal. For instance, any degradation in M_1 will affect substate 1(a) and 1(b). In the same way, changes in $R_{DS(ON)}$ of M_3 will affect substates 2(a) and 2(b). Substate 2(b) and 1(b) will be affected by the change in the value of $R_{DS(ON)}$ of M_2 and M_4, respectively.

B. Experimental Setup and Results

Experimental test setup for SOH monitoring of the PV inverter is shown in Fig. 14 with SSTDR test-points connected across its ac output terminals. Two sets of data are required to detect

the aging of a MOSFET: one is for a healthy device (baseline or reference), and the second one is for the aged device. Five groups of tests were conducted to identify the device aging and the first group was considered as the baseline when the inverter with all fresh MOSFETs was scanned in intermittent mode at 24 MHz SSTDR signal. In a similar way, the other four groups (group 1–4) were created, however, this time, each new MOSFET was replaced by the aged MOSFET, one at a time. Thus, in group 1, 2, 3, and 4, the aged MOSFET was used to replace the fresh MOSFETs- M_1, M_2, M_3, and M_4, respectively. A number of continuous scans at each reading were carried out, and at each scan, the negative autocorrelated peak amplitude of the main lobe (corresponding to the distance of the DUT from the SSTDR hardware end) was considered. However, it was observed that within each reading, the autocorrelation peak values generated for the MOSFET with the same aging level were not identical and showed some variations.

This type of variations in the autocorrelation peak is expected when the impedance change occurs faster than the time taken to process the autocorrelation data for each scan. This processing time for the SSTDR hardware used in this work is approximately less than 2 ms. As mentioned earlier, in our experiment, each path impedance changes within 0.05 ms, and that is why we observed such variations in the autocorrelated peak values. One feasible solution to overcome this issue is by redesigning the SSTDR hardware so that the data processing time is lower than the time interval between two consecutive path impedance changes. Unfortunately, such a redesign of this commercial hardware is beyond the scope of this article. That being said, when the MOSFETs are switched at a frequency higher than the 250 Hz (i.e., $T/2 = 2$ ms), it can progressively increase the difficulty level to differentiate between the healthy and aging data from a limited number of scans, and such a brief switching event would add a very little contribution to the aging detection.

From a statistical point of view, the average error due to this random variation in autocorrelated peak data can be significantly reduced over many scans. That is to say that the accumulation of a large SSTDR dataset from several switching events would eventually help in reducing the abovementioned variations. Therefore, data recorded for multiple and consecutive switching events could produce a distinguishable and repeatable signature in the results. This approach of collecting large dataset for a reasonable time can be significantly useful in identifying the degradation in power devices when they are switched at a high frequency. An aging detection algorithm is developed within the scope of this project based on the histogram of such a large number of autocorrelated peak amplitudes, which will be described in the following section.

1) Histogram/Amplitude Distribution Algorithm: Ten readings were taken for each group, and the inverter was scanned at 24 MHz SSTDR signal several times to take each reading. The corresponding autocorrelated peak amplitudes of each reading was divided into one hundred (100) intervals, termed as "bins", in descending order (from higher magnitudes to lower magnitudes). Each bin contains the number count or occurrences of autocorrelated peak amplitudes within a specific range. The frequency distribution of the peak amplitudes in each bin for the ten readings were averaged and coined as "amplitude distribution". The resultant amplitude distribution for each group was compared with the baseline and plotted in Fig. 15. Interestingly, there was a rightward shift from the baseline for each group of these bin plots. The rightward shift of the amplitude distribution indicates that the correlated peak amplitudes with lower magnitudes have higher counts for the aged MOSFET compared to the baseline. This is due to the fact that the aged MOSFET has higher equivalent impedance (combined effect of the increased value of $R_{\mathrm{DS(ON)}}$ and $Z_{\mathrm{eq,GS}}$) than the

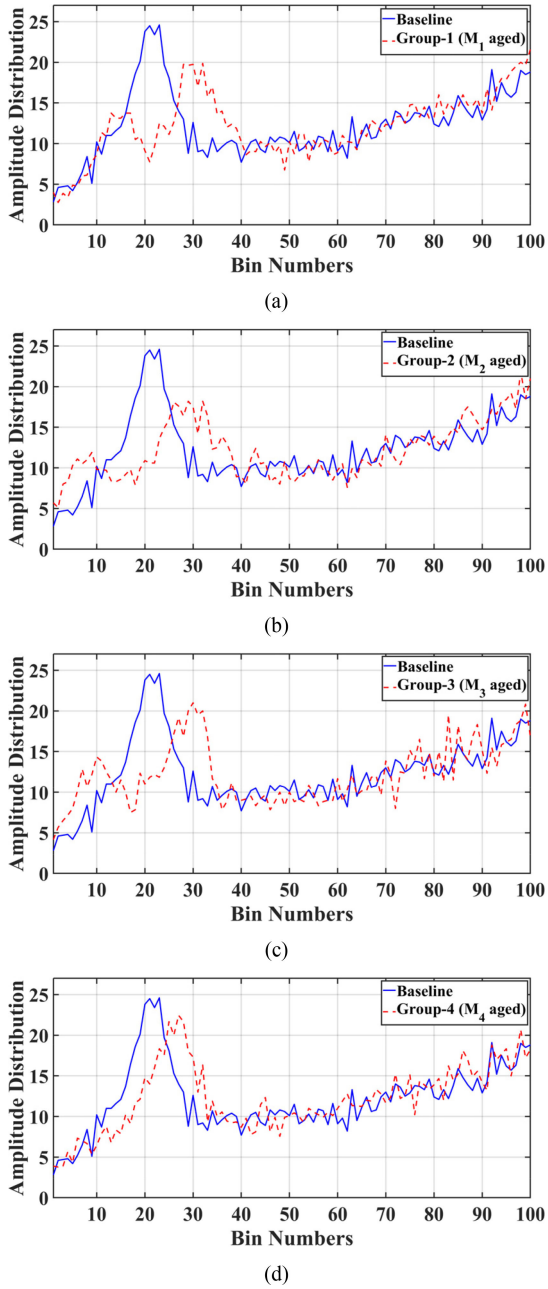


Fig. 15. Amplitude distribution-comparison between baseline and an aged MOSFET at (a) M_1 position: aged M_1 (Group 1), (b) M_2 position: aged M_2 (Group 2), (c) M_3 position: aged M_3 (Group 3), and (d) M_4 position: aged M_4 (Group 4).

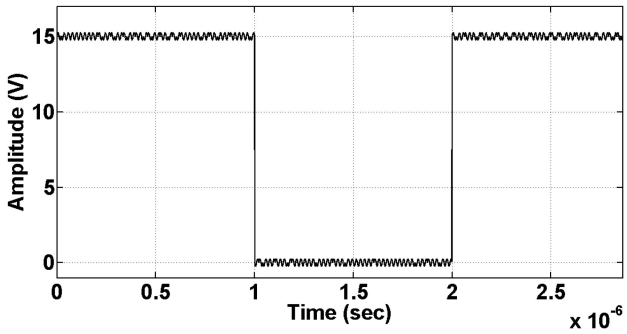


Fig. 16. 100 mV (p-p), 48 MHz SSTDR incident signal superimposed on a 15 V, 500 kHz PWM sequence (with a 50% duty cycle).

healthy device, and this change in the equivalent impedance is experienced by the SSTDR signal, which in turn generates correlated peak amplitudes with lower magnitudes. That is why the later bin numbers of an aged MOSFET have higher counts than that of the healthy device. Therefore, this rightward shift clearly indicates that the combined effect of $Z_{eq,GS}$ and $R_{DS(ON)}$ has increased in an aged MOSFET. Interestingly, variations exist in the amount of rightward shift in the amplitude distribution from the baseline for the aged MOSFETs in group-1, group-2, group-3, and group-4 since the distances of the corresponding MOSFETs are different from the SSTDR test points.

V. Case Study-2: SOH Monitoring of Power Converters Applying SSTDR Test Signal Across Gate-Source Interface: A Platform for IGDM

Previous SSTDR-based SOH monitoring methods required SSTDR test signals to be applied across the drain-source terminals of a power MOSFET or collector-emitter terminals of an IGBT [35]–[38], [54]. As explained in the previous section, SSTDR test points could also be connected across the inverter's ac output terminals, which could be unsuitable for high voltage operation. In case study-2, device condition monitoring was performed while applying SMPNS embedded PWM signals across the gate-source interface of a MOSFET in a dc–dc converter and a three-phase power inverter. Inside the SSTDR hardware, the SSTDR incident signal (SMPNS) has a typical voltage level of 100 mV or below, and the lowest could be as small as 22 mV. This significantly lower amplitude signal with a center frequency of up to 48 MHz embedded in PWM sequence will act as a low-voltage high-frequency noise on top of the 15 V (or 18 V for SiC MOSFETs) PWM gate signal; therefore, it will not impact the normal switching operation of the circuit. A 48 MHz, 100 mV(p-p) SSTDR incident signal superimposed on a 500 kHz, 15 V PWM signal (50% duty cycle) is shown in Fig. 16 for reference. In a nutshell, implementing this SMPNS across the gate and the source of a power MOSFET will serve the following purposes.

1) Unlike the collector/drain terminal, the gate terminal is always accessible and remains at the lower voltage level. This allows us to monitor the high voltage converter easier and safer than it was in the past and helps in designing the SSTDR hardware at a much lower rating.
2) Even with proper scaling, the hardware can be incorporated inside the gate driver board, thus making it intelligent. This feature will allow the system to be monitored autonomously and provide built-in-self–test capability, which eliminates the need for separate SOH modules leading to significant system-level savings.

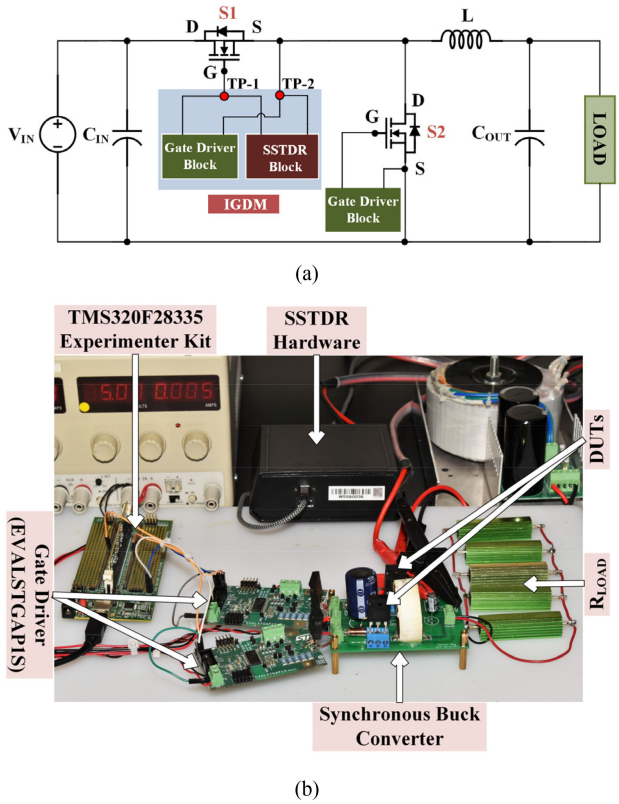


Fig. 17. Experimental set-up for condition monitoring of a synchronous buck converter: (a) schematic, and (b) photograph. Here, IGDM= intelligent gate driver module.

A. Degradation Detection of a Power Device in a DC–DC Converter

Fig. 17 shows the schematic diagram and the photograph of the test setup to perform the online degradation monitoring in a live synchronous buck converter. SSTDR hardware probes were connected across the gate-source of the converter's high side MOSFET (S_1). The switching frequency of the converter was 10 kHz with a duty cycle of 50%. Three groups of tests were conducted to verify the proposed SSTDR algorithm. The first group was considered as a baseline when all MOSFETs were healthy. Then the aged MOSFET (M_{AP2_L4}) was sequentially inserted at two different locations inside the converter; high side and low side (one MOSFET at a time) and considered them as group 1 and 2, respectively. In each test-group, the SSTDR scan was performed multiple times with two carrier frequencies (48 and 24 MHz), and ten readings were obtained in each group. The resultant autocorrelated peak amplitudes were collected

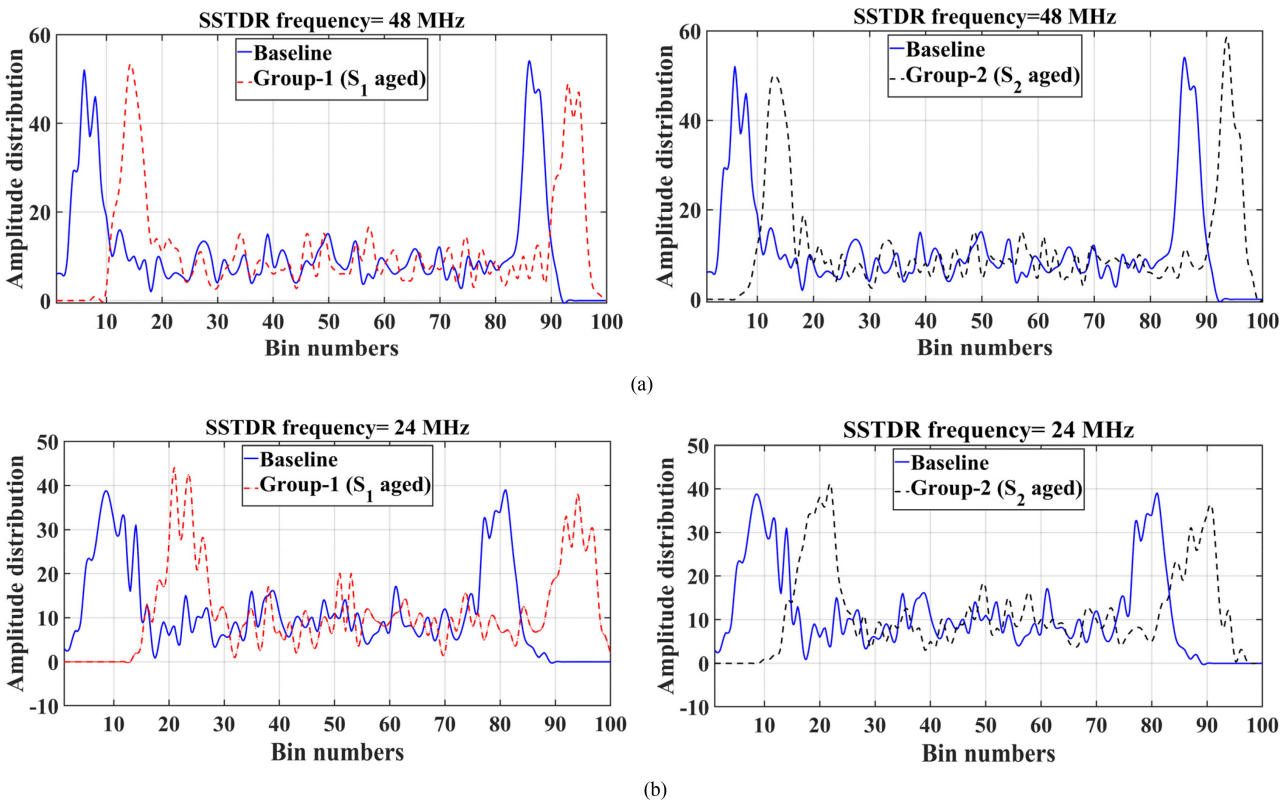


Fig. 18. Comparison of amplitude distributions for synchronous buck converter: (a) SSTDR frequency= 48 MHz; and (b) SSTDR frequency= 24 MHz.

and analyzed to identify device aging. Like SSTDR test-results obtained in H-bridge PV inverter (see Section IV), the SSTDR autocorrelated amplitudes for a synchronous buck converter showed some variations with the same aging level. This is due to the fact that two path impedances are possible in a synchronous buck converter due to two switching states: i) S_1 is ON, S_2 is OFF (state-1), (ii) S_1 is OFF, S_2 is ON (state-2) provided that the dead-band state and switching transients of each MOSFET are ignored, and these path impedances change way faster than 2 ms time interval due to high PWM switching. Therefore, the proposed aging detection algorithm developed for case study-1 based on the histogram of a large number of autocorrelated peak amplitudes has been adopted here as well.

The entire set of autocorrelated peak values for each reading was divided into 100 bins based on their amplitudes of descending order. The histogram of each reading of the corresponding bins was averaged for each group and the resultant amplitude distribution has been plotted in Fig. 18. Similar to the amplitude distribution obtained for the H-bridge PV inverter, there is a rightward shift from the baseline for each group in the bin plots. This indicates that the correlated peak amplitudes with lower magnitudes have higher counts for the aged MOSFET compared to the baseline. This clearly indicates that the combined effect of $Z_{\mathrm{eq,GS}}$ and $R_{\mathrm{DS(ON)}}$ has increased in an aged MOSFET. Interestingly, a small variation exists in the amount of shift in the amplitude distribution from baseline for group-1 and group-2 since the distances of the two MOSFETs from the SSTDR test points are different.

B. Degradation Detection in a Three-Phase Inverter

Three-phase power inverters are commonly used in electric vehicles, motor drives, aircraft, and many other applications [55]. Many of these applications support precious human lives and, therefore, it is of paramount importance to design a highly reliable system. Like many other power converters, three-phase inverters fail in operation due to one or more unpredicted operational conditions and natural degradation in their power switches. For instance, almost 70% of faults in power inverters of variable speed-drives occurs due to degradation in power electronic switches [56]. Therefore, continuous CM of these power inverters can be used to schedule maintenance before serious deterioration or break-down occurs.

A conventional two or three-level three-phase inverter has six switches, and therefore, when the inverter switches operate at several kHz switching frequency, there will be multiple path impedances for SSTDR signal in a complete switching cycle. Due to a higher number of impedance paths in a given switching interval, the rate of variations in these complex path impedances will be higher compared to a single-phase H-bridge PV inverter and dc–dc converter [40]. Therefore, a three-phase inverter will require even larger number of SSTDR test datasets (compared to the other topologies mentioned earlier) in order to reduce the effect of variation in autocorrelated peak data due to fast path impedance change caused by high-frequency PWM switching.

One possible way to overcome this issue is to reduce the switching frequency at system fundamental frequency (for

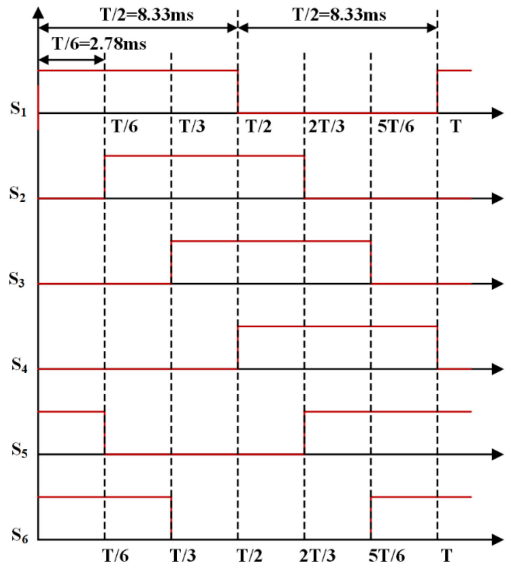


Fig. 19. 60 Hz square wave mode switching scheme of a three-phase inverter.

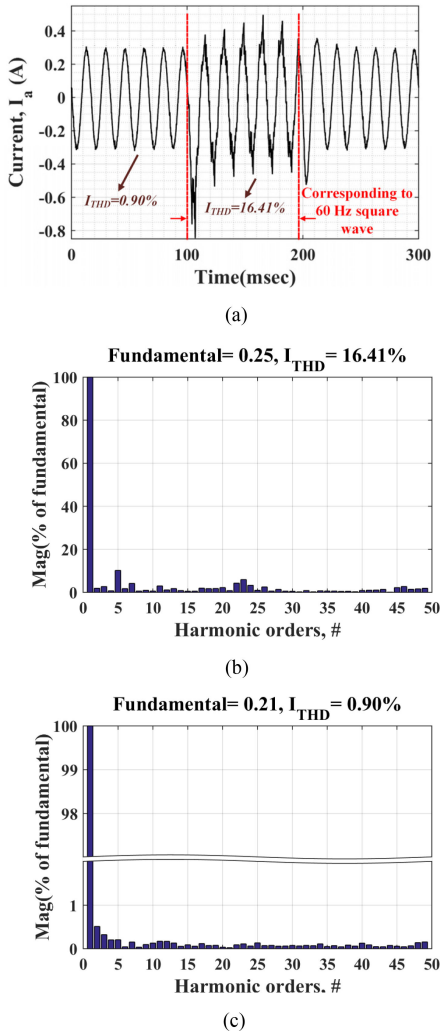


Fig. 20. (a) A-phase current waveform of the three-phase induction motor at two different switching modes of the inverter, (b) corresponding I_{THD} at 60 Hz square wave mode of the inverter, and (c) corresponding I_{THD} at 30 kHz SPWM mode of the inverter.

example, 60 Hz) for a fraction of a second, and this will meet the requirement of minimum time interval needed for SSTDR hardware (i.e., $>$ 2 ms) to avoid the variations in the SSTDR readings generated for the same aging level. For instance, if the inverter operates at 60 Hz square wave mode for a very short time period (a very few cycles such as five-six cycles), SSTDR-based SOH monitoring method will have the following advantages.

1) When the inverter operates at 60 Hz square wave mode with a 50% duty cycle, the path impedance changes three times in each half cycle (i.e., $\sim$T/2 $=$ 8.33 ms) (see Fig. 19). This implies that the time interval between two consecutive path impedances is $\sim$ 2.78 ms, which eliminates the SSTDR hardware limitation.
2) 60 Hz square mode operation will require significantly less amount of data in order to successfully detect the device aging compared to kHz range switching mode since it will reasonably reduce the variation in autocorrelation peak data.
3) A smaller number of required data will greatly decrease the computational time for data processing demanded by the CM hardware.
4) Inverter output will have a fundamental frequency of 60 Hz, which matches the main's frequency in the USA.

Operating the inverter permanently in 60 Hz square wave mode will produce higher harmonic contents at the output compared to the operation in SPWM mode. Therefore, the square wave operation for a prolonged time period is not a practical way to generate ac output either in grid-parallel or standalone configuration. Using the proposed technique, the inverter is intended to operate in square wave mode for a brief period, and the motor will experience this higher total harmonic distortion (THD) level only for a fraction of a second (such as 100 ms). This short time period is negligible compared to the starting time of the motor, which is typically a few seconds for a large motor, and during this startup time, a motor may experience even higher harmonics and 8–10 times higher currents than its rated current [57]. This startup time could be exploited to determine the SOH of the inverter because the fundamental frequency of the motor is much smaller than 60 Hz during startup. This low-frequency operation provides more time for the CM hardware and added flexibility to schedule the CM scheme. Therefore, the inclusion of a temporary square wave operation will have negligible or no impact on the motor's operation although it provides a clear benefit to accurately estimate the SOH.

To observe the effect of operating the inverter without any modulation, a ¼ hp three-phase induction motor was powered by a 30 kHz SPWM inverter operated momentarily in a 60 Hz square wave mode. The inverter runs at 30 kHz SPWM mode during normal operation and was allowed only once to run for 100 ms in 60 Hz square wave mode. This 100 ms window is used to take necessary SOH measurements although this small window has no effect on the operation of the inverter, which we have experimentally verified. The resultant a-phase current (I_{a}) is plotted in Fig. 20(a). There is a slight increase in current during

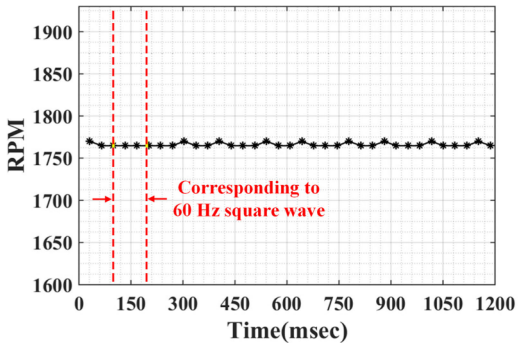


Fig. 21. RPM of the three-phase induction motor at two different switching modes of the inverter.

this 100 ms window because no current feedback controller was used. However, this change in the current level is reasonably below the inrush current threshold of a typical induction motor and did not have any meaningful impact on the rpm of the motor. We need to keep in mind that the motor did not have any load or torque inertia. Therefore, with load, the corresponding change due to this square wave operation will be even smaller.

It is apparent that the current waveform has some level of distortions (see Fig. 20). However, the inverter was operated in 60 Hz square wave mode momentarily, and the minimum time required for a "very short period" harmonic content measurement is 3 s according to IEEE standard 519 [58]; therefore, the resultant current distortion of 100 ms duration is of no consideration and can be treated as transient disturbances commonly prevalent in power systems. Yet, the inverter was allowed to operate for 3 s in 60 Hz square wave mode to measure (not for condition monitoring) the THD in line current (I_a), and the corresponding harmonic spectra are shown in Fig. 20(b), which can be compared with the corresponding harmonic spectra of 30 kHz SPWM operation [see Fig. 20(c)]. This 3 s window was used for conducting the harmonic analysis only, and in real SOH measurement, only a 100 ms window is needed. The rpm of the motor remains almost unaffected in both cases of momentary 60 Hz square wave and 30 kHz SPWM operation (see Fig. 21). In addition, if the inverter runs with a feedback controller, changes in the rpm, if there is any, would be quickly stabilized, which has not been implemented in our case, and this implementation was beyond the scope of this project. On top of that, when the line suffers such common disturbances for a short period of time, the inertia of large machines will maintain a constant speed. Furthermore, if the motor is running a generator in a motor-generator set, the flywheel adds more inertia to increase the ride through time that maintains the power supply for several seconds under such disturbances. This method is equally applicable to grid-tied inverters since grids are designed to be stiff to withstand such momentary disturbances, which are very common in power systems [59]. In fact, a similar kind of modulation can be found in [60], where the DUT does not switch during a certain time of the fundamental period of the inverter to guaranty the accuracy of the precursor parameter measurements.

1) Experimental Setup and Results: A three-phase inverter prototype (testbed), which was designed and built to implement

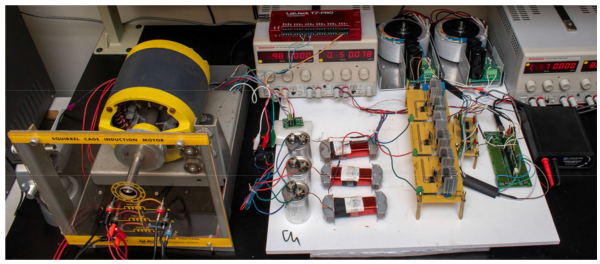


Fig. 22. Three-phase inverter prototype.

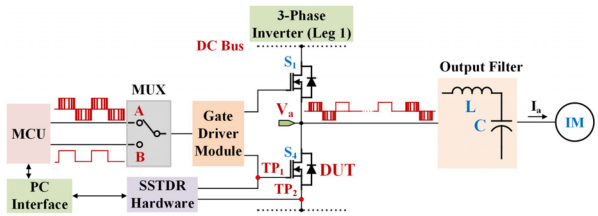


Fig. 23. Block diagram of the proposed synchronization scheme where SSTDR signal is synchronized with 60 Hz square wave gate signal of the bottom MOSFET of the inverter's first leg.

the proposed CM technique is shown in Fig. 22. A 48 MHz SMPNS signal was applied across the gate-source of the bottom MOSFET (S_4) of the inverter's first leg, as shown in Fig. 23. The inverter was being operated continuously at 30 kHz SPWM mode. However, during SSTDR measurement, the 60 Hz square wave mode was activated for a duration of 100 ms to monitor the SOH of the MOSFET at S_4 position. The gate signals (30 kHz SPWM and 60 Hz square wave) were multiplexed and the SSTDR signal (SMPNS) was synchronized accordingly with the 60 Hz square wave signal. In each 60 Hz cycle, four autocorrelated peak amplitude data were recorded leading to a total of 25 data points, approximately, over 100 ms time interval. An autocorrelated baseline with the 100 ms duration was created for the inverter with all six fresh MOSFETs. Similarly, the resultant autocorrelated peak amplitudes were recorded for a 100 ms period with an aged MOSFET having four aging levels (aged in phase-2 of Section III), one at a time, at position S_4. All of these data have been plotted in Fig. 24 and the nonzero differences among the autocorrelated peak amplitudes corresponding to the baseline and different aging levels clearly indicate the aging of the S_4-MOSFET. As expected, SSTDR autocorrelated peak data have decreasing magnitudes with the increasing aging levels (aging level 4> aging level 3> aging level 2> aging level 1> healthy device/baseline). In addition, the amplitude differences between the averages of all baseline data and the autocorrelated peak data corresponding to each aging level (denoted as $\Delta Corr$) have been recorded and plotted as a bar plot in Fig. 25. This plot shows that the amplitude difference between the baseline and the autocorrelated peak data corresponding to an aged MOSFET becomes larger with the level of aging. Therefore, it is evident that this proposed technique can determine the level of aging by measuring the SSTDR reflection data-higher the aging, lower the reflection data.

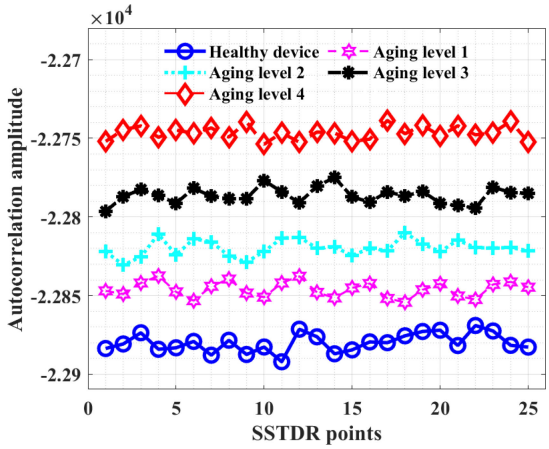


Fig. 24. SSTDR correlated peak amplitude data for multiple aging levels of S_4-MOSFET of the inverter (during 60 Hz square wave mode). Here, aging level 1, 2, 3, 4 represent change in the $R_{\mathrm{DS(ON)}}$ by 7.19, 12.53, 19.2, and 27.79 mΩ, respectively, from initial $R_{\mathrm{DS(ON)}}$ of the healthy MOSFET.

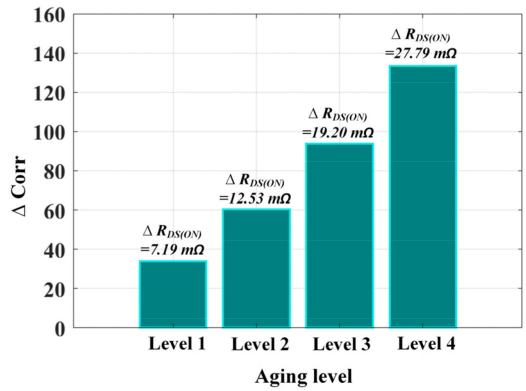


Fig. 25. Change in the average SSTDR correlated amplitude data for multiple aging levels of S_4-MOSFET of the inverter (during 60 Hz square wave mode). Here, initial $R_{\mathrm{DS(ON)}}$ of the healthy MOSFET is 48.04 mΩ.

VI. Discussion

The feasibility of using SSTDR for condition monitoring of power devices has been discussed in two separate case studies provided in Section IV and Section V, respectively. The proposed SSTDR-based CM technique can successfully detect device degradation in a live H-bridge PV inverter and dc–dc converter at the cost of a large amount of SSTDR data acquisition for the purpose of error reduction. In contrast, a little modification in the switching scheme can overcome such limitations inside a three-phase inverter, and this manuscript has presented this concept in detail.

As stated earlier, increased value of $R_{\mathrm{DS(ON)}}$ indicates both chip-related and package-related aging and changes in $V_{\mathrm{GS(TH)}}$ leading to an increase in the $Z_{\mathrm{eq,GS}}$ indicates only chip-related aging. However, the sensitivity of $R_{\mathrm{DS(ON)}}$ due to the gate oxide degradation is relatively low compared to the package-related degradation [11]. Since SSTDR test signal experiences combined effect of increased value of $R_{\mathrm{DS(ON)}}$ and $Z_{\mathrm{eq,GS}}$ due to device aging, it is not possible to differentiate the root cause of the degradation using the proposed CM method. Hence, the natural direction for future research includes the effort on the decoupling of gate oxide and channel degradation, possibly by extracting the transmission-line model parameters of the SSTDR propagation path, taking multiple measurements at different gate-voltage levels, and so on [11]. The authors are presently working on this topic using a very recent federal grant to isolate these two different degradations.

The proposed method is based on the change in $R_{\mathrm{DS(ON)}}$ due to the device aging, and $R_{\mathrm{DS(ON)}}$ is a function of junction temperature (T_{j}). Therefore, measurements need to be taken at identical electrical and temperature conditions. Otherwise, the relationship between the $R_{\mathrm{DS(ON)}}$ along with its corresponding SSTDR data and temperature is required to be stored in a look-up table (LUT). A calibration procedure should be conducted to update this LUT both for electrical loading and T_{j} to compensate for operating condition dependencies [11], [28], [61], [62]. Some studies attempted to compensate for T_{j} using electrothermal and/or loss models [63]–[65], while others have carried out case temperature measurement as a substitute [18], [21], [66], [67]. In addition, commercial solutions presently exist, which uses temperature sensors directly integrated into the power chip structure [68]. CM is easier to be implemented under similar operating conditions if the current level can be controlled and the average junction temperature is relatively stable [11]. For applications with frequent start-stop, it is possible to run the algorithm at the startup under similar operating conditions [28]. As stated earlier, exploiting this startup time to determine the SOH of the inverter provides more time for the CM hardware and add flexibility to schedule the CM scheme. In addition, as the change in $R_{\mathrm{DS(ON)}}$ due to the device aging progress slowly, evaluating it throughout the long-time intervals is a reasonable approach [28].

VII. Conclusion

This article presents an SSTDR based *in situ* degradation detection technique applicable to live power switches in various power converter topologies. The difference in the autocorrelated amplitudes obtained for the healthy and aged devices can be capitalized to determine device degradation; a bigger difference indicates higher degradation. The proposed technique has been implemented in several power converters including a dc–dc converter and a three-phase motor drive. Until today, the SSTDR-based SOH monitoring techniques are only able to detect device degradation while the converter operates in an idle state, therefore, the technique cannot be implemented in live power converter applications. In contrast, the methods proposed in this article can estimate the SOH of a power device regardless of its operating states (live or idle). Furthermore, aging detection from the gate-source interface creates a provision for the development of an intelligent gate-driver architecture with an in-built degradation monitoring unit. Although the tests were carried out to detect aging in power MOSFETs, this technique is equally suitable for other power devices such as IGBTs and SiC MOSFETs. We strongly believe the outcome of this research will create a paradigm shift in the field of online SOH monitoring not only by

incorporating the CM hardware into the gate driver architecture but also by significantly reducing the human errors associated with the traditional precursor parameter based aging detection methodologies. The gate driver manufacturing industries will be greatly benefitted from the outcome of the research by adopting this intelligent gate driver concept. Therefore, this article will create a seminal impact in the reliability sector, and the lifetime of the power converters can be greatly increased by performing scheduled maintenance, which will eventually increase the run time of the power modules and reduce maintenance costs.

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