Letters

A Robust Nondestructive Test Scheme Based on Multistage Anode Voltage Detection for 4500 V Single-Cell Turn-Off Capability of Press-Packed Devices

Jiapeng Liu, *Student Member, IEEE*, Zhanqing Yu, Xiaorui Wang, Chunpin Ren, Zhengyu Chen, Biao Zhao, *Senior Member, IEEE*, Fanglin Chen, and Rong Zeng, *Senior Member, IEEE*

***Abstract*—The turn-OFF capability test for the single cell of power devices is of great significance to both the safe operation assurance and the destruction mechanism research. However, with present techniques, the device under test is supposed to be destroyed once the turn-OFF fault occurs. In this article, a robust nondestructive test scheme based on the multistage anode voltage detection for 4500 V single-cell turn-OFF capability of press-packed devices is proposed. Based on the proposed scheme, a single cell of IGCT is tested until a fault occurs. The result proves that a total bypass time is less than 100 ns for the 2200 V/5 A turn-OFF fault, and thus, the aim of nondestructive tests can be achieved with the proposed method.**

***Index Terms*—High-power devices, multistage voltage detection, nondestructive test, single-cell test.**

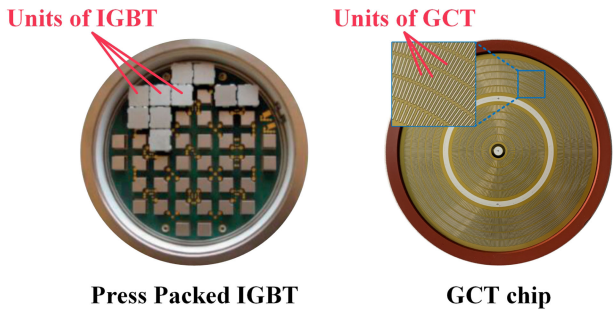

Fig. 1. Paralleled cells in press-packed IGBT [1] and IGCT.

I. Introduction

In RECENT years, with the advantage of low loss, high control flexibility, and renewable energy accessibility, flexible HVdc power systems are developed widely. As the key component of the flexible HVdc system, power devices are required of high power rating, high reliability, and short-circuit failure mode feature. In order to avoid bond wire wearing out and the consequent open circuit, press-packed devices, such as insulated gate bipolar transistor (IGBT) and integrated gate commutated thyristor (IGCT), are favored for HVdc applications. Due to the high current requirement, such devices are usually composed of basic cells connected in parallel, as illustrated in Fig. 1. The detailed and in-depth turn-OFF capability tests on the basic cells of the paralleled device under various conditions are of great significance to both the recognition of the basic failure mechanism of the device and the precise product screening to make a full harness of the degraded products.

Although the turn-OFF capability test is important, it is costly and difficult to be performed repeatedly. Once a turn-OFF failure occurs, the following concentrated thermal accumulation is supposed to cause the regional meltdown. So no further tests can be performed. However, if the consequent destruction can be prevented, not only the turn-OFF capability can be depicted exactly but also the devices can be categorized into various levels. The yield rate can thus be greatly increased and the cost can be further reduced for customers with different requirements.

In order to prevent the device from irreversible thermal destruction after an electrical failure, a robust nondestructive test method with fast fault detection speed and fast fault bypass speed is a prerequisite and in great need.

Due to the significance of nondestructive test method, former researchers have proposed the approach with no active detection [2]–[4] and with a *dv*/*dt* detection [5], [6]. For the former, the load current is bypassed at a fixed time no matter the fault occurs or not. Due to the lack of active control, the time has to be tuned carefully from zero for each individual sample. For the latter, the fault current is bypassed when the descent rate of the anode voltage reaches a critical value. However, the noise in the *dv*/*dt* signal and the possibility of failure with low voltage descent rate, as illustrated in Fig. 2, restrict its further application.

In this article, a novel robust nondestructive test scheme based on the multistage anode voltage detection for the 4500 V single cell turn-OFF capability of press-packed devices is proposed.

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Jiapeng Liu, Zhanqing Yu, Xiaorui Wang, Chunpin Ren, Zhengyu Chen, Biao Zhao, and Rong Zeng are with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: 18811362403@163.com; yzq@tsinghua.edu.cn; wxr_fr@163.com; 18810903251@163.com; chenzhengyu@mail.tsinghua.edu.cn; zhaobiao112904829@126.com; zengrong@tsinghua.edu.cn).

Fanglin Chen is with the State Key Laboratory of Advanced Power Semiconductor Devices, CRRC Times Electric, Co., Ltd., Zhuzhou 412001, China (e-mail: chenfl@csrzic.com).

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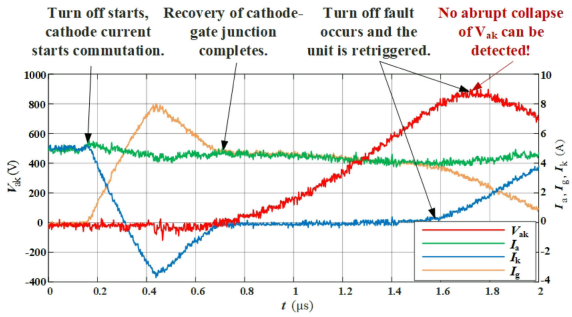

Fig. 2. Turn-OFF failure waveform of IGCT under 2200 V/5 A with small *dv/dt*.

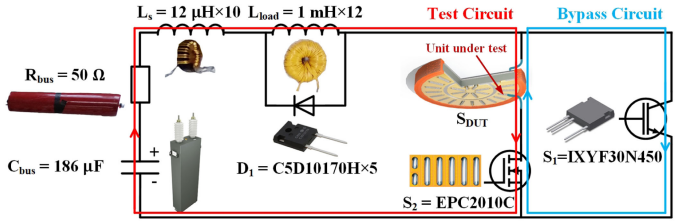

Fig. 3. Optimal design of power loop topology with the bypass function based on the forced commutation.

First, the test circuit for the turn-OFF capability is carefully designed toward a fast bypass speed and low snubber effect. Second, a connection structure for a single-cell test is proposed for high current measurement precision. At last, a multistage anode voltage detection method with robustness and high speed is proposed and realized. The experimental result shows a total bypass time less than 100 ns and the aim of the nondestructive test for the turn-OFF capability can be achieved with the proposed scheme.

II. Design of Test Circuit for 4500 V Single-Cell Turn-Off Capability Toward Ultrafast Bypass Speed and Low Parasitic Snubber Effect

A. Optimal Design of Test Circuit Topology for Single-Cell Turn-Off Capability

In order to evaluate the turn-OFF capability of the device precisely, the test circuit is commonly chosen as inductance loaded for which the trajectory in the *I–V* curve covers a big area during turning OFF, and thus, the turn-OFF capability can be fully tested.

In order to guarantee a sufficient turn-ON time, 12 1 mH inductors connected in series are adopted as the load inductance. Diode D_1 is antiparallel connected to absorb the energy stored in the inductance. Besides, an extra inductor L_s is connected directly in series with the device under test (DUT) to provide overvoltage during turning OFF and can be adjusted independently. And at last, considering the operation mode of high voltage and small current, a current limiting resistor $R_{\rm bus}$ is inserted to limit the fault current and avoid the direct short circuit of the bus capacitor. The existence of $R_{\rm bus}$ will not affect much the trajectory during turning OFF because the voltage drop on it is small compared with the bus voltage. The designed test loop is drawn in Fig. 3.

B. Optimal Design of High-Speed Bypass Circuit Based on Force Commutation

In addition to the test circuit stated above, an extra bypass loop composed of switches S_1 and S_2 is introduced to bypass the fault current once the fault is successfully detected.

When no fault occurs, S_2 is normally ON and S_1 is normally OFF. The load current is controlled through the switching of $S_{\rm DUT}$. Once the fault is detected, S_1 is switched ON and S_2 is switched OFF simultaneously. The load current helps building up the voltage of S_2 until the avalanche voltage is reached and clamped.

Therefore, S_2 works like a high-speed voltage source providing commutation force for the fault current to the S_1 branch in counteraction with the parasitic inductance. After commutation, all fault currents are commutated to the S_1 branch and $S_{\rm DUT}$ is protected.

It can be conducted that the parasitic inductance in the bypass path is supposed to be low enough for high commutation speed. If the inductance reaches a critical value, an oscillation may occur in the bypass path. Extra resistance and diode are required in series connection with $S_{\rm DUT}$ to depress the oscillation.

TABLE I
Parameters and Requirements of Semiconductor Components Toward Ultrafast Bypass Speed and Low Parasitic Snubber Effect

Item	Featured Parameters	Requirements
D_1	1. V_{RRM} = 1700 V×5 2. C ⩽ 160 pF 3. I_F = 14.4 A 4. No reverse recovery charge.	1. Sufficient blocking voltage. 2. Low junction capacitance. 3. Sufficient current capacity. 4. Fast recovery feature.
S_1	1. V_{CES} = 4500 V 2. C_{OES} ⩽ 83 pF 3. $t_{d(on)}$ = 38 ns 4. I_{C110} = 17 A	1. Sufficient blocking voltage. 2. Low junction capacitance. 3. High switching speed. 4. Sufficient current capacity.
S_2	1. Q_g = 3.7nC 2. BV_{DSS} = 200 V	1. High switching speed. 2. Reasonable avalanche voltage.

C. Optimal Design of Circuit Components Toward Ultrafast Bypass Speed and Low Parasitic Snubber Effect

Based on the circuit topology presented above, circuits components, especially semiconductor components D_1, S_1, and S_2 are supposed to be carefully selected to depress the influence raised by nonideal characteristics. Especially, the capacitive snubber effect raised by components needs to be depressed to achieve an inductive load condition, where the *I–V* trajectory during the turn-OFF process will cover a complete rectangle region, and the turn-OFF capability is strictly tested. The main requirements and featured parameters for selected devices are summarized in Table I.

For diode D_1, when DUT is switched ON, D_1 remains reverse biased and withstands a voltage close to the bus voltage. Thus, the selection of D_1 is required to block the bus voltage. When

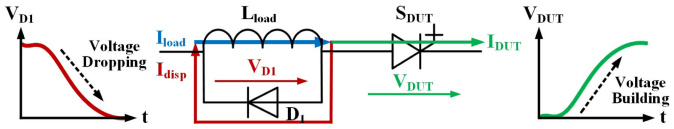

Fig. 4. Illustration of displacement current in D_1 during the turning OFF of DUT.

DUT is switching OFF, the reverse voltage applied to D_1 decreases with the voltage on DUT increasing. As illustrated in Fig. 4, although D_1 remains reverse biased, the displacement current $I_{\rm disp}$ raised by dv/dt of DUT still decreases the load current of DUT during the switching. The effect is especially remarkable in the single-cell test, where the voltage is relatively high but the current is small. Therefore, a small junction capacitance is required to depress the snubber effect. After DUT building up the voltage, D_1 is forward biased and works as the freewheeling diode of $L_{\rm load}$. The stored energy in $L_{\rm load}$ is supposed to dissipate in D_1 and sufficient current conduction capacity is required in avoidance of the thermal breakdown. In addition, at this freewheeling period, if the fault occurs for DUT, the built voltage on DUT may collapse. This will lead to a high voltage and high di/dt recovery process for D_1. Therefore, D_1 is supposed to be a fast recovery diode to withstand this highly stressed recovery process. According to the requirements stated above, D_1 is chosen as five 1700 V SiC Schottky diodes C5D10170H connected in series.

For switch S_1, when no fault occurs, it remained switched OFF continuously. Thus, it is supposed to withstand the bus voltage and the overvoltage of DUT during switching OFF. Similar to D_1, when DUT is switching OFF, the displacement current in S_1 raised by dv/dt of DUT decreases the load current in DUT. In order to depress the snubber effect, a small junction capacitance is required. When the fault occurs, S_1 is switched ON and the fault current flows continuously in this branch until the bus capacitor is totally discharged. Therefore, fast switching speed and sufficient conduction capacity are also necessary. Considering all these requirements, S_1 is chosen as a 4500 V/17 A silicon IGBT IXYF30N450.

For switch S_2, the operation mode is relatively simple. When no fault occurs, S_2 conducts the load current identical to DUT. Once a fault is detected, S_2 is supposed to switch OFF immediately and provides a commutation voltage. In order to satisfy the demand of high switching speed and reasonable avalanche voltage, S_2 is chosen as a 200 V/20 A GaN power transistor EPC2010C.

III. Vacuum Forced Connection Structure and Amplified Current Measurement Interface for Single Cell of Press-Packed Devices

Fig. 5 illustrates the structure of the anode block for the vacuum forced connection and the assembled layout for a single cell of the gate commutated thyristor (GCT) chip. During tests, the air pump is switched ON and the pressure beneath the GCT chip becomes lower than the atmosphere pressure with spiracles connected to the air pump. Therefore, the chip can be pressed to

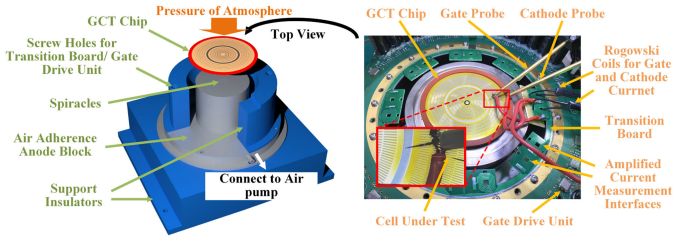

Fig. 5. Vacuum forced connection structure for the single cell of press-packed devices (IGCT in the figure) and connected transition board.

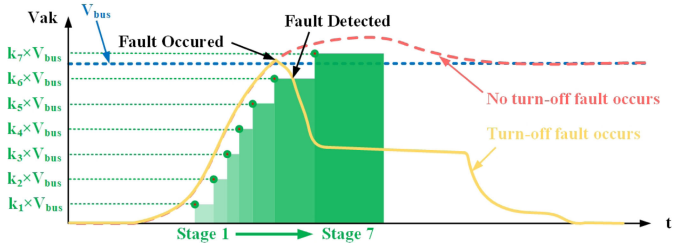

Fig. 6. Working principle of the multistage anode detection method.

the anode block with air pressure and the anode is connected to the main circuit.

The connection of cathode electrode and gate electrode is achieved through probes connected to the transition board. The driving signal from the gate drive is applied through the transition board. Through the transition board, not only the parasitic impendence in the gate drive loop can be well controlled but also the current measurement interface can be implemented. In order to increase the signal-to-noise ratio for the current in the level of 10 A with a Rogowski coil, wires for the cathode and gate signals are wounded for five circles in the transition board. Therefore, the induced voltage in the Rogowski coil multiplies and the measurement precision is much improved.

IV. Novel Multistage Anode Voltage Detection Method With Robustness and Ultrahigh Speed

A. Working Principle of Ultra-High-Speed Multistage Anode Detection Method

Instead of inspecting a sudden voltage drop during the turn-OFF process, a more common feature of the turn-OFF fault is that the device fails to build up voltage within a certain time. The examination of anode voltage after a specific time delay provides robust criteria for the fault detection. However, if only one delay time is selected, when the fault occurs early, the respond time will be critically long due to the time delay for voltage building. On the other side, the real-time examination based on the analog-to-digital conversion (ADC) is not applicable due to high conversion delay compared with the fast changing speed. The compromising method with both controllable high speed and ideal robustness is the multistage anode detection method.

Fig. 6 illustrates the basic working principle of the multistage anode detection method. As exhibited, the anode voltage criteria for multiple stages are configured during building-up process. Once the measured voltage falls below the criteria of the

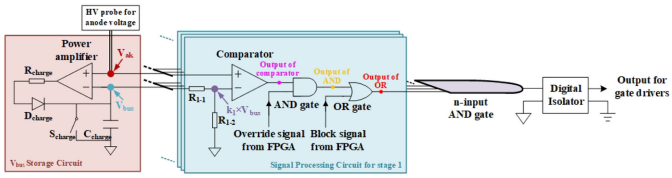

Fig. 7. Schematic view of the detection circuit with low latency and high robustness.

TABLE II
TYPES AND TIME DELAYS OF MODULES IN FAULT DETECTION CIRCUIT

Item	Comparator	AND-OR Gate	Digital Isolator
Type	TLV3501	SN74LVC1G0832	ADuM1100
Time Delay	4.5 ns	<3.4 ns	10.5 ns

corresponding stage, the fault is detected and bypass is activated through the ultrafast analog circuit.

As can be seen, the stage number can be configured flexibly according to the requirement of feedback speed to avoid a thermal meltdown when the fault occurs. An increase in the stage number results in the shortening of responding time as well as the increase in the circuit complexity, and the maximum stage number is restricted by the propagation delay of circuits as well as the output noise of the differential probe.

B. Optimal Design of Detection Circuit With Low Latency and High Robustness

Based on the working principle stated above, an optimal design of the detection circuit is developed. The two main challenges are modifying the criteria conveniently with various working conditions and depressing the signal transmission delay.

For the former aspect, the reference voltages for stages are supposed to change with different bus voltages. With the fine tuning of stage time periods, the circuit is supposed to suit well with the change in working conditions. However, the digital solution based on ADC and digital-to-analog conversion (DAC) may bring in both signal noise and conversion delay. In order to achieve high robustness and low latency, a bus voltage storage circuit based on the power amplifier is adopted in this article, as illustrated in Fig. 7. In the circuit, R_{charge} is the current limit resistor to protect the amplifier and D_{charge} is the diode ensuring the mode of output for the amplifier. When switch S_{charge} is switched OFF, the voltage of C_{charge} can follow the input of attenuated anode voltage signal V_{ak}. Therefore, the level of V_{ak} before triggering can be stored as an analog quantity of the capacitor voltage.

For the latter aspect, in order to shorten the time delay, instead of a programmed processor, only a few high-speed logic gates are implemented for the function realization. A 50 MHz field programmable gate array (FPGA) is only adopted to provide the time delay for different stages, which may not affect the respond speed. Also, as listed in Table II, the types of modules in the signal pathway are carefully selected for the extreme

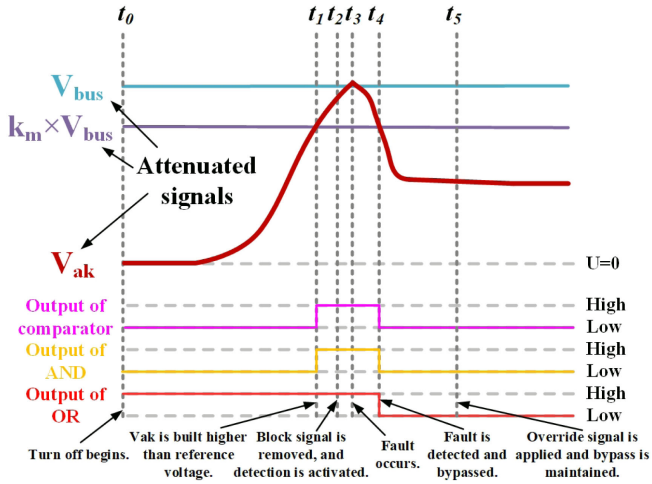

Fig. 8. Sequence diagram of signals in the detection circuit for stage m.

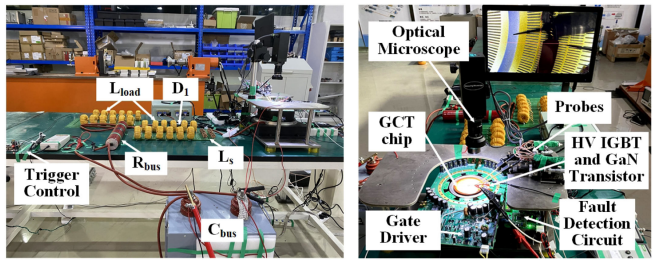

Fig. 9. Structure of the 4500 V nondestructive test platform for the single cell of press-packed devices based on the multistage anode voltage detection.

performance, including the introduction of a magnetic coupler instead of the optical coupler for signal isolation.

Fig. 8 illustrates the time sequence diagram for the fault occurring in stage m. As can be seen, the turn OFF begins at t_0. After a certain waiting delay to t_0, the block signal from FPGA for stage m is removed and the output signal of the comparator can be delivered to backstage circuits. At t_3, the fault occurs and the anode voltage drops suddenly. The output signal of the comparator flips and the output signal of the OR gate also flips, which means the bypass circuit is triggered properly. Then, at t_5, FPGA also sensed the occurrence of the fault, an override signal is applied continually. Therefore, although the voltage in the store capacitor leaks out with time, the system can be locked in protect status until the reset signal is applied.

With the introduction of the analog storage circuit for bus voltage, careful selection of circuit components, and robust self-lock status, the detection circuit proves to be fast and robust.

V. EXPERIMENTAL VALIDATION

In order to check the validation of the proposed scheme, a 4500 V nondestructive test platform implemented with the proposed method is established. Fig. 9 illustrates the structure of the platform. As can be seen, due to the requirements of ultrahigh respond speed, the control signals are transmitted electrically, thus the gate driver, transition board, detection circuit, and bypass circuit are all connected physically. Especially, the bypass

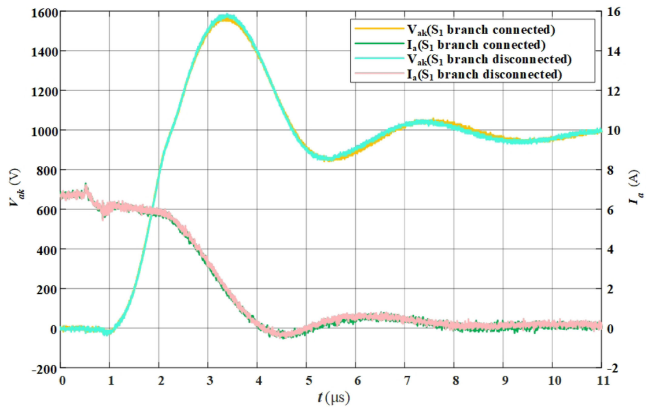

Fig. 10. Comparison of turn-OFF waveforms with and without the S_1 branch being connected.

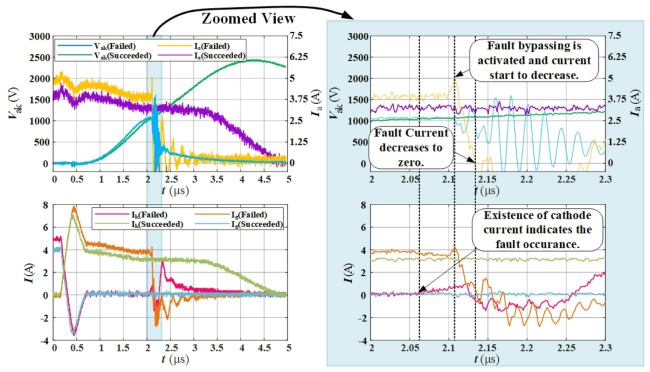

Fig. 11. Single-cell turn-OFF waveforms of IGCT under 2000 V/3.8 A (turned-OFF successfully) and 2200 V/4.9 A (turned-OFF unsuccessfully).

circuit composed of high-voltage IGBT and GaN transistor is placed underneath the transition board in order to reduce the parasitic inductance in the bypass loop and improve the bypass speed.

First, a set of comparative tests with and without the S_1 branch is performed, as illustrated in Fig. 10. The result verifies that the introduction of the S_1 branch does not affect the turn-OFF waveform much. And the small decrease in the anode current before the anode voltage reaching the bus voltage is possibly raised by the sudden application of negative voltage by the gate drive unit of IGCT and the introduction of current limit resistor R_{bus}.

Then, a series of turn-OFF experiments is performed with identical conduction time on the single cell of IGCT. With the increase in the bus voltage, the turn-OFF current increases simultaneously. The last successful turn-OFF is recorded as 2000 V/3.8 A. And when the bus voltage and corresponding turn-OFF current are increased to 2200 V/4.9 A, the fault occurs. Fig. 11 illustrates the waveform of both conditions.

As can be seen from the left part of the figure, at the beginning of the fault occurrence, where the cathode current occurs, the anode voltage still increases but the building speed of the anode voltage slows down at this stage due to the appearance of the cathode current. Under this circumstance, different from the former method based on dv/dt, the detection method based on the multistage anode voltage is able to operate properly. Considering the time delay between cathode current occurrence and fault current decreasing is less than 50 ns, adding that the signal transmission delay is supposed to be more than 10 ns, the fault is detected before the collapse of the anode voltage in Fig. 11. Due to the fast switching speed of devices and the low parasitic inductance in the bypass loop, the fault current is decreased to zero within 40 ns. It can thus be calculated from Fig. 11 that the detection delay based on the multistage anode voltage detection can be decreased by less than 50 ns. Together with the bypass time, the complete fault clearance can be performed within 100 ns. The device is measured again after the test and the result verifies that the blocking voltage of 4500 V is remained. The nondestructive test for the turn-OFF capability can thus be achieved with the proposed method.

VI. Conclusion

In this article, a novel robust nondestructive test scheme based on the multistage anode voltage detection for 4500 V single-cell turn-OFF capability of press-packed devices is proposed. First, the test circuit for the turn-OFF capability is carefully designed toward the fast bypass speed and low snubber effect. Second, a connection structure for the single-cell test is proposed for high current measurement precision. At last, a multistage anode voltage detection method with robustness and high speed is proposed and realized. The experimental result shows a total bypass time of less than 100 ns and the goal of the nondestructive test for the turn-OFF capability is achieved.

Based on the nondestructive test scheme presented in this article, the yield rate and in-depth recognition of the failure mechanism for power devices may be further advanced.

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