Letters

A 4H-SiC MOSFET-Based ESD Protection With Improved Snapback Characteristics for High-Voltage Applications

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***Abstract*—A novel electrostatic discharge (ESD) protection device based on an n-type metal–oxide–semiconductor field-effect transistor (NMOSFET) with segmented topology was proposed and investigated, considering the material characteristics of 4H-SiC, which is a wide-bandgap material (3.3 eV). ESD phenomena are important in terms of semiconductor reliability, and the benefits of using 4H-SiC as a material can provide robustness and excellent thermal reliability to ESD protection devices. The proposed device improves the wide range of snapback phenomena caused by the high critical electric field (2.4 MV/cm), in comparison to using Si (0.25 MV/cm); it also improves triggering characteristics and provides a high holding voltage. The proposed device and a traditional silicon-controlled rectifier, a gate-grounded-NMOS, and a gate-body floating NMOS were fabricated using the 4H-SiC process. The electrical characteristics of the experimental devices, determined by a transmission-line-pulsing system, were comparatively analyzed. Additionally, this article presents the analysis of the optimization of electrical characteristics according to the critical design variables of the proposed device, stacking for high-voltage applications, and reliability test results for high temperatures (300–500 K).**

***Index Terms*—4H-SiC, electrostatic discharge (ESD), gate-grounded n-type metal–oxide–semiconductor (GGNMOS), high-voltage application, reliability, silicon-controlled rectifier (SCR), silicon carbide (SiC), snapback.**

I. Introduction

Wide-bandgap materials, including gallium nitride and silicon carbide (SiC), exhibit excellent performance under high-temperature, high-power, and high-voltage conditions and can considerably improve the area efficiency of power devices with a high-current density relative to the operating voltage. Particularly, SiC can be applied to various fields, such as renewable power systems for aircraft and electric vehicles, and research is underway in various fields to overcome the material limitations of silicon [1], [2]. Notably, SiC-based power devices can have a smaller weight and size than Si-based devices. Several studies on SiC-based power devices and circuits, which have excellent characteristics at high temperatures that far exceed the maximum operating temperature of Si (150 °C) [3], [4], have been reported. However, high-current density within a small area can cause severe electrical stress, owing to the inflow of external surges. Moreover, electrostatic discharge (ESD) may be accompanied by the thermal destruction of integrated circuits (ICs) and devices, which becomes a serious cost issue for industrial-grade chips [5], [6]. Despite the importance of this issue, only a few studies on SiC ESD protection have been published thus far. Recently, the failure mechanism of SiC devices has been investigated for human body model ESD pulses, and the electrical characteristics of the SiC material used in ESD protection devices, which traditionally applied Si materials, have been analyzed [7], [8]. Because ESD protection devices in high-voltage applications have a very large area to optimize the safe operating area, the excellent high-temperature characteristics of SiC, and its high-current density relative to the operating voltage can be of a great advantage in the design of high-voltage ESD protection devices [9]. Although most ESD protection devices exhibit snapback characteristics in terms of area and power efficiency, only a few studies have investigated the optimization of their electrical characteristics to improve the wide range of snapback phenomena occurring in SiC materials. Therefore, this letter proposes a 4H-SiC MOSFET-based ESD protection device that maintains the excellent material characteristics of 4H-SiC under ESD stress and considerably enhances the snapback characteristics. Additionally, the operation mechanism and electrical characteristics are analyzed.

II. Novel 4H-SiC MOSFET-Based ESD Protection

The gate-grounded n-type metal–oxide–semiconductor (GGNMOS) and silicon-controlled rectifier (SCR) are the most common ESD protection devices, and various studies have been conducted on their Si materials [5], [10]–[15]. The GGNMOS has a low-current density compared with an SCR; however, it has

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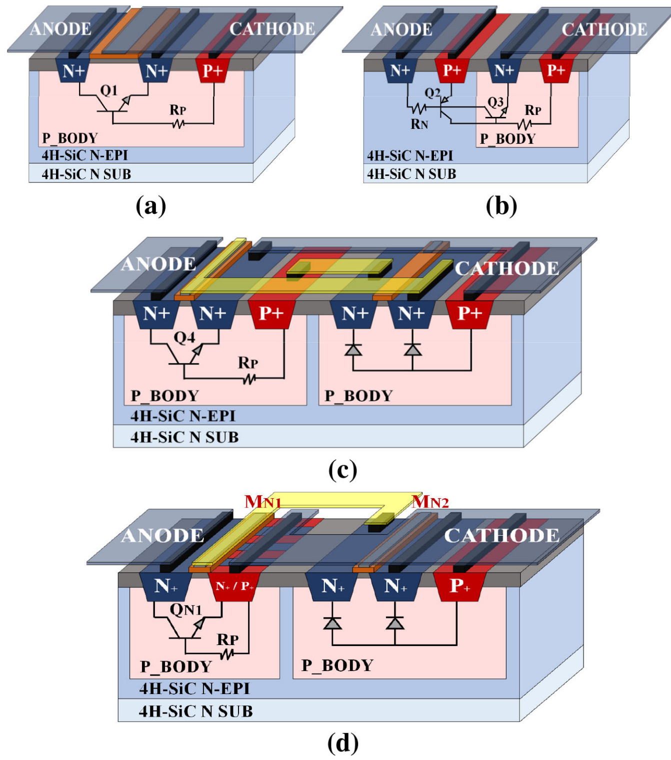

Fig. 1. Cross section of the traditional (a) GGNMOS, (b) SCR, (c) GBFNMOS, and (d) proposed HHFGNMOS structures on the 4H-SiC substrate.

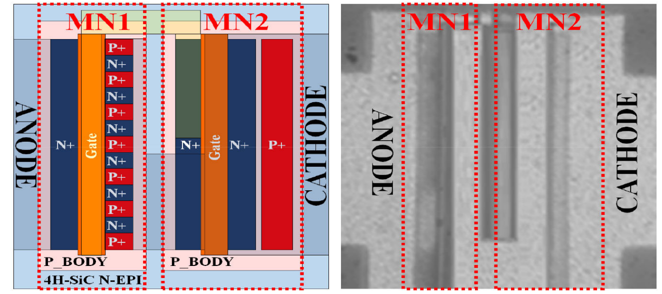

Fig. 2. (Left) layout of HHFGNMOS with 13 segments and (right) 50× magnification image of fabricated HHFGNMOS.

excellent process compatibility and snapback characteristics. Accordingly, most processes provide GGNMOS-based ESD protection devices. Generally, the trigger voltage (V_{T1}) and holding voltage (V_H) of the snapback device depend on the breakdown voltage (BV) and forward voltage drop of the parasitic bipolar transistor, respectively. However, 4H-SiC has approximately ten times the critical electric field (E_C = 2.4 MV/cm) of Si (E_C = 0.25 MV/cm) and approximately three times the built-in potential of the p-n junction (3.4 V at 300 K) [1], [6]. Consequently, a strong snapback with a large difference between V_{T1} and V_H occurs, which is extremely disadvantageous for optimizing the electrical characteristics of the ESD design window to protect the IC core.

Recently, the gate-body floating NMOS (GBFNMOS) [9] has been reported to reduce the high V_{T1} in 4H-SiC. However, because GBFNMOS still has a low holding voltage, and the optimization of the holding voltage depends on the gate length (L), which is the traditional method, a large area increase is required. Therefore, there is a need for a more powerful technology that can simultaneously achieve the improvement of V_{T1} and V_H. Fig. 1 shows the structure of the general SCR, GGNMOS, GBFNMOS, and proposed high holding voltage floating gate NMOSFET (HHFGNMOS) implemented using 4H-SiC. The traditional devices were selected to verify the enhanced electrical characteristics of the HHFGNMOS.

The HHFGNMOS comprises two n-type metal–oxide–semiconductor field-effect transistors (NMOSFETs), that is, M_{N1} and M_{N2}. The gate region of M_{N1} is connected to the drain of M_{N2}. The drain of M_{N1} that discharges most of the ESD current is connected to the anode terminal, and the body and source are combined and then connected to the cathode terminal along with the gate, source, and body of M_{N2}. Under normal operating conditions, M_{N1} does not operate because of the high potential barrier of the reverse junction; however, in ESD mode, an avalanche breakdown occurs between the drain and body of M_{N1} and the generated hole current drives Q_{N1} to discharge the ESD current. As with GBFNMOS, the gate of M_{N1} is floated to the reverse junction of M_{N2} for the gate coupling effect [10], [11]. Thus, while M_{N1} is discharging most of the ESD current, the reverse junction of M_{N2} supports potential bias at the source-body junction to reduce V_{T1} [9], [12]. Additionally, a modified segment topology is applied to the source and body of M_{N1}. In previous studies, the segment topology was variably applied to SCR-based devices because it could simultaneously and effectively reduce the emitter injection efficiency of two parasitic bipolar transistors [13]. In contrast, MOSFET-based devices have relatively good snapback characteristics in Si; thus, extensive research on segment topology applications has not been conducted. On the other hand, the proposed HHFGNMOS has a segmented coupled body and source region. Owing to the segment topology, the body and source bias are simultaneously held. The source of $M_{N1,}$ which corresponds to the emitter area of $Q_{N1,}$ becomes narrower, which decreases the emitter injection efficiency of Q_{N1}. A decrease in emitter injection efficiency increases the voltage drop of the device in the ON-state, leading to an increase in the holding voltage. On the other hand, the reduction of the P+ implant limits the current flowing through the body region, aids forward biasing of $Q_{N1,}$ and lowers the trigger voltage [14], [15]. Hence, the HHFGNMOS improves the strong-snapback phenomenon in 4H-SiC materials by increasing the holding voltage while maintaining the advantages of GBFNMOS as much as possible.

The experimental devices were fabricated on the n-type substrate of a 4H-SiC wafer and have a gate oxide thickness of 500 Å. The source and body were formed by injecting nitrogen and aluminum, respectively, and the processes of N+ implant and P+ implant were performed at 650 °C. The metal process was performed by heat treatment at 1000 °C/2 min in rapid thermal annealing (RTA) with Ni silicide. This heat treatment was performed in a thermal 100 A + HTO ~600 A, 1230 °C/3 h, and N_2O gas atmosphere. Fig. 2 shows the layout

TABLE I
SUMMARY OF JUNCTION DEPTH AND DOPING CONCENTRATION IN 4H-SiC PROCESS

Layer	Junction Depth	Doping Concentration
P-Body	0.7 um	5E18 cm-3
N+ Implant	0.25 um	2.5E19 cm-3
P+ Implant	0.2 um	1.5E19 cm-3
N-epitaxial	13 um	5E15 cm-3

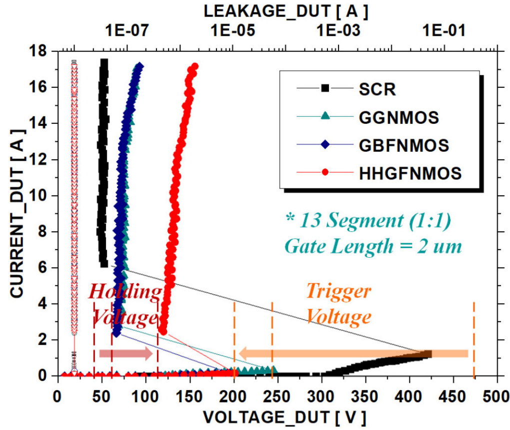

Fig. 3. TLP *I–V* curve of the traditional SCR, GGNMOS, GBFNMOS, and proposed HHFGNMOS structures fabricated through the 4H-SiC process.

of the HHFGNMOS with 13 segmented implant regions and the fabrication results. Table I summarizes the junction depth and doping concentration according to the 4H-SiC process used in fabrication.

III. Measurement Results and Discussion

A. Transmission-Line-Pulse (TLP) Measurement

A TLP [16] system with a rise time of 10 ns and a width of 100 ns was used to verify the electrical and tolerance characteristics of the experimental devices. Fig. 3 shows the TLP *I–V* characteristic curves of the experimental devices made of 4H-SiC. In this experiment, the HHFGNMOS had 13 segmented implant regions at a ratio of 1:1 and a gate length (L) of 2 μm; all experimental devices had the same implant width of 200 μm. Additionally, the SCR had a longer total length of 64 μm (total size: 64 μm × 212 μm = 13 568 μm^2), GGNMOS dimension of 45 μm (total size: 45 μm × 212 μm = 9540 μm^2), GBFNMOS dimension of 92 µm (total size: 92 μm × 212 μm = 19 504 μm^2), and HHFGNMOS dimension of 72 μm (total size: 72 μm × 224 μm = 16 128 μm^2). According to the measurement result, the traditional devices have a strong-snapback waveform because of a very large E_C and low carrier mobility (μ_n = 1000 cm^2/V_s, μ_p = 120 cm^2/V_s) in a 4H-SiC environment. In particular, in the case of SCR, the snapback range is far more expansive due to the BV at low doping levels. This is based on the operating characteristics in the ESD mode that depends on the following [6], [17]:

$$V_H = V_{EB,PNP} + V_{CE,NPN(sat)} \tag{1}$$

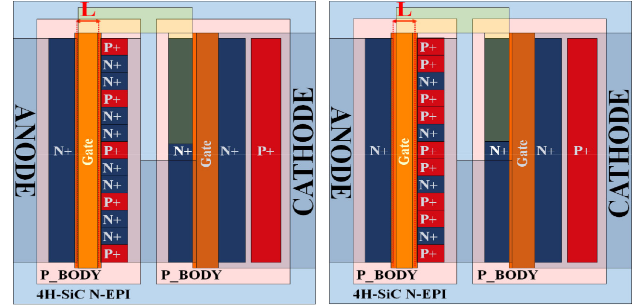

Fig. 4. Structure of HHFGNMOS with 13 segmented implant regions at a ratio of 1:2 (left) and a ratio of 2:1 (right), including design parameter L, and the segment ratio depends on P+:N+.

$$V_{T1} = BV_{AK} + V_{rep} + V_{ren}. \tag{2}$$

V_H depends on $V_{EB,\ \mathrm{PNP}}$ and $V_{CE,\ \mathrm{NPN}\,(sat)}$ (only $V_{CE,\ \mathrm{NPN}}$ is considered for NMOSFET-based devices), which are higher due to a higher built-in potential of the p-n junction of 4H-SiC compared with Si. However, the BV of the snapback device in 4H-SiC is more than ten times higher than that of Si on account of the high critical electric field. In addition, 4H-SiC has low carrier mobility, in particular, hole mobility of approximately four times lower than that of Si; V_{T1} after BV increases considerably owing to the high V_{rep} and V_{ren} (the voltage drop across the base resistance of each parasitic bipolar transistor) in 4H-SiC. Therefore, the traditional devices have a very large gap between V_H and V_{T1}. This does not correspond to SiC power devices with a high operating voltage and limits actual IC applications related to the ESD design window. On the other hand, owing to its structural characteristics, the proposed HHFGNMOS has a V_{T1} of 205 V and V_H of 122 V, and it also has significantly improved snapback characteristics compared with the traditional devices.

B. Optimization of Electrical Characteristics With Design Variables

Fig. 4 shows the layout according to the proposed device's design variables and the segment topology application. The design variable L is the gate region of the device, and the effective base region of Q_{N1} can be adjusted using L. The HHFGNMOS's electrical characteristics were optimized by adjusting the number of segments, segment ratio, and gate length. Fig. 5 shows the change in the electrical characteristics according to the change in the critical design parameters of the HHFGNMOS. As shown in Fig. 5(a) and (b), the gate region of M_{N1} of the HHFGNMOS increased by 4 μm and up to 10 μm. As L increased, the V_H of the HHFGNMOS increased to 108 V. On the other hand, the 13 segmented sources not only significantly increased the V_H of the proposed device to 122 V but also decreased V_{T1} to 205 V. This change in the electrical characteristics of HHFGNMOS is based on the material characteristics of 4H-SiC and the structural characteristics of the HHFGNMOS. Notably, 4H-SiC has very low hole mobility compared with Si. Accordingly, because the increase in the base currents ($I_{B,\ QN1}$) through the adjustment of the base region is relatively small, the synergistic effect of

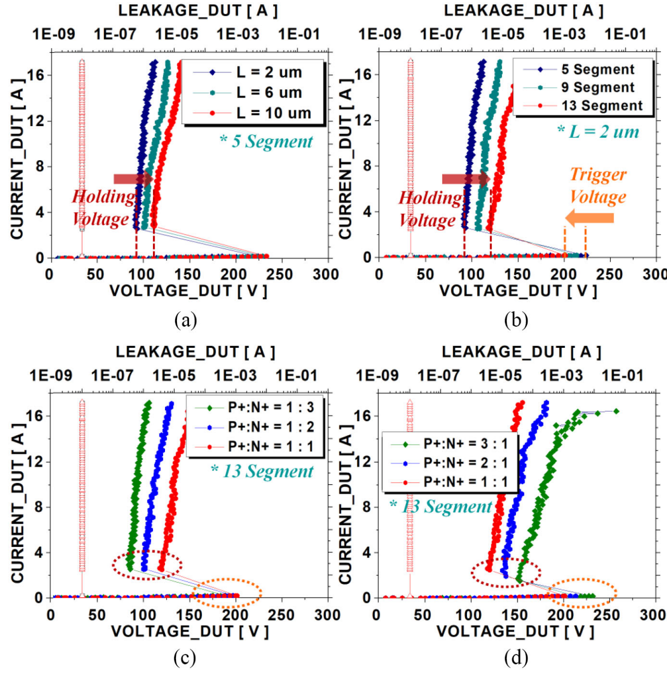

Fig. 5. Change in electrical characteristics according to (a) gate length (L) and (b) number of segments. (c) and (d) Change in segment ratio.

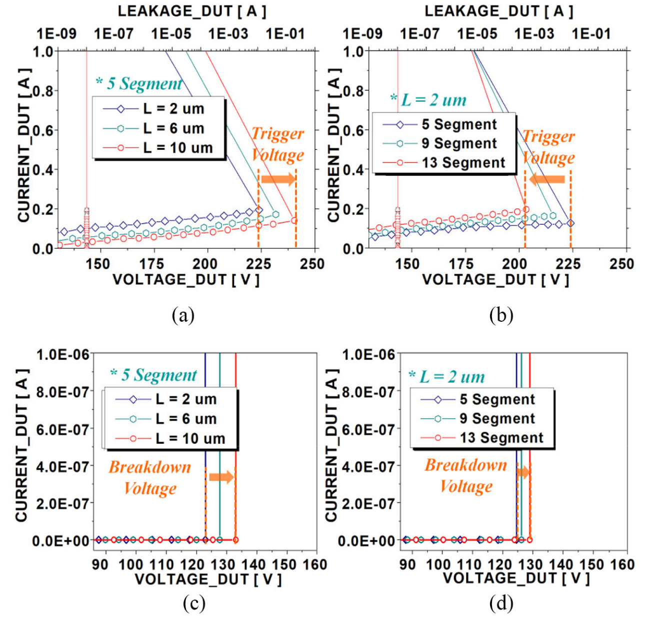

Fig. 6. (a) and (b) Change in trigger voltage and (c) and (d) BV of HHFGNMOS according to design variable L and number of segments.

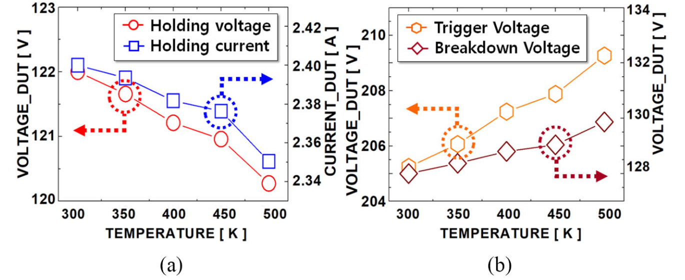

Fig. 7. High-temperature (300–500 K) test results for HHFGNMOS at 1:1 ratio. (a) Holding voltage and holding current. (b) Trigger voltage and BV.

V_H according to the segmented emitter is greater than that due to the adjustment of L. Additionally, the P+ implant region can be simultaneously segmented to reduce V_{T1}. Fig. 5(c) and (d) shows the change in the electrical characteristics according to the segment ratio (P+ : N+) of each implant region based on 13 segments. With an increase in the proportion of the n-type source occupied in the segmented region, a decrease in V_H and V_{T1} is observed. Additionally, with an increase in the proportion of the p-type source occupied in the segmented region, an increase in V_H and V_{T1} is observed. This is because the emitter injection efficiency of Q_{N1} increases as the n-type source area increases, and the body current is limited at a relatively high level as the p-type source area increases. In addition, excessive reduction in the emitter area limits the discharge of ESD currents and increases the ON-resistance of the device. In a 1:1 ratio, the holding voltage is 122 V, which is almost close to the BV of 128 V, whereas in a ratio of 2:1 or higher, V_H exceeded BV, which reduced the effectiveness of ESD protection in the core operating region. Devices with a BV lower than V_H may generate a leakage current before reaching V_H and, in practical applications, the operating voltage of the core is limited to BV. Therefore, the segment ratio of the HHFGNMOS was optimized to 1:1 by considering the ON-resistance and snapback characteristics.

Fig. 6 shows the changes in V_{T1} and BV according to the design variable L and the number of segments that can induce an increase in V_H. With an increase in L, V_{T1} increased by approximately 14 V, and BV increased by 10 V. Moreover, with an increase in the number of segments, V_{T1} decreased by approximately 20 V, and BV increased by 5 V. It occurred because the increase in V_{T1} is caused by the increase in the current discharge path. Unlike the design variable L, which increases the current discharge path, the increase in the segment number of HHFGNMOS reduces the emitter injection efficiency of Q_{N1} and limits the body current to a lower level through a reduction in the p-type source.

Therefore, the HHFGNMOS can achieve a significant structural improvement with modified segment topology in the wide range of snapback characteristics of 4H-SiC with an increase in V_H along with a low V_{T1}.

C. Thermal Reliability and N-Stack Application

Thermal reliability is important in SiC chips requiring high-temperature operation [18]. An increase in temperature affects the snapback characteristics of ESD protection devices due to a decrease in carrier mobility. An increase in temperature not only causes a decrease in carrier mobility but also increases the resistance of the body region and causes an increase in BV and V_{T1}. It also reduces the forward voltage drop of the parasitic bipolar transistor, reducing V_{BE} and decreasing the holding voltage and holding current. Fig. 7 shows the electrical

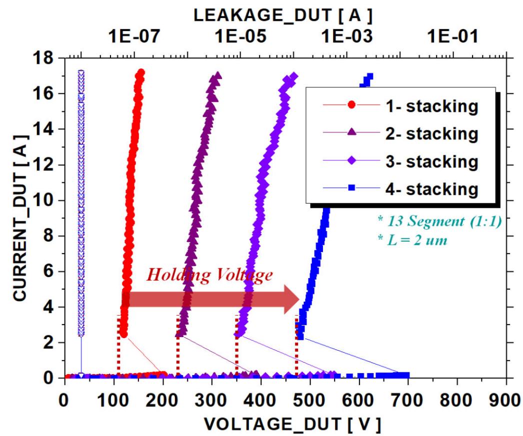

Fig. 8. TLP measurement results for stacked HHFGNMOS structure with 1–4 stacking numbers. Each HHFGNMOS has L=2.0 μm and 13 segmented sources.

TABLE II
SUMMARY OF SNAPBACK PROPERTIES OF EXPERIMENTAL DEVICES: IN THE L DESIGN VARIABLE, THE SEGMENT NUMBER IS FIXED AT 5; AND IN THE SEGMENT NUMBER VARIABLE, $L = 2$; AND THE SEGMENT RATIO DESIGN VARIABLE THE SEGMENT NUMBER IS FIXED AT 13; ALL THE HHFGNMOS IN THE N-STACK HAVE 13 SEGMENTS

Structure			V_H	I_H	V_{T1}	BV	R_{on}
SCR			48 V	6.2 A	424 V	310 V	0.6 Ω
GGNMOS			74 V	2.6 A	250 V	118 V	0.9 Ω
GBFNMOS			71 V	2.2 A	196 V	115 V	1.1 Ω
HHFG NMOS	L (um)	2	89 V	2.6 A	224 V	123 V	1.4 Ω
		6	99 V	2.7 A	229 V	127 V	1.7 Ω
		10	108 V	2.9 A	239 V	133 V	2.2 Ω
	Segment No. (1:1)	5	89 V	2.6 A	224 V	123 V	1.5 Ω
		9	104 V	2.5 A	213 V	125 V	1.7 Ω
		13	122 V	2.4 A	205 V	128 V	2.1 Ω
	P+ : N+ (1: n)	2	100 V	2.3 A	198 V	126 V	1.8 Ω
		3	83 V	2.4 A	191 V	123 V	1.4 Ω
	P+ : N+ (n :1)	2	137 V	1.9 A	213 V	129 V	2.7 Ω
		3	151 V	1.4 A	230 V	132 V	3.9 Ω
	N-Stack	2	246 V	2.4 A	390 V	249 V	4.0 Ω
		3	365 V	2.3 A	550 V	377 V	6.2 Ω
		4	481 V	2.2 A	702 V	509 V	8.4 Ω

characteristics according to the temperature reliability experiment (300–500 K) for the proposed device. In this experiment, the wafer was heated by a hot-chuck control system and the I–V characteristics were measured using a TLP system. Compared with Si, 4H-SiC exhibits a relatively low decrease in carrier mobility as the temperature increases. Therefore, it shows excellent thermal reliability compared with the Si-based ESD protection device. According to the experimental results, at the high temperature of 500 K, the heat loss (reduced holding voltage at 500 K compared with 300 K) rate of the holding characteristic of the proposed device was very low ($<2\%$); the holding voltage was still higher than 120 V. Additionally, the change rate of the trigger characteristics was approximately 3%. Therefore, the stable thermal reliability of the HHFGNMOS brought about by the material characteristics of 4H-SiC was verified.

Considering the high operating voltage of the SiC devices and circuits, the change in the electrical properties of the HHFGNMOS according to the N-stack, as shown in Fig. 8, is very important [19], [20]. Stacked devices are formed on the same substrate and are connected in series through metal lines. As the number of stacked devices increases, the ON-resistance increases and snapback characteristics deteriorate due to an increase in current discharge paths. Therefore, it is advisable to stack as few devices as possible to achieve high holding voltages using N-stack. The V_H of the HHFGNMOS can reach 480 V with only four stacked structures with the improved snapback. Therefore, when applying the HHFGNMOS to high-voltage applications, by selecting appropriate stacking numbers, it is possible to satisfy the safe operating area required by the core. Table II summarizes the electrical properties of the snapback of all experimental devices.

IV. CONCLUSION

In this letter, a novel ESD protection device based on a MOSFET with significantly improved trigger and holding characteristics in the 4H-SiC process was fabricated, and its electrical characteristics and operating mechanism were analyzed. The traditional ESD protection devices in 4H-SiC form a snapback waveform in a very wide voltage range. On the other hand, the proposed HHFGNMOS significantly enhances the snapback characteristics with gate coupling and modified segmented topology. Additionally, we verified the excellent high-temperature reliability by conducting a thermal reliability test in the range of 300–500 K and evaluated the electrical characteristics of the stacked structure by considering the high operating area of SiC devices and circuits. The proposed HHFGNMOS can considerably improve the strong snapback in 4H-SiC materials and has excellent high-temperature reliability. Therefore, this study demonstrated the application of the excellent material properties of 4H-SiC to ESD protection devices. The proposed HHFGNMOS is expected to improve semiconductor reliability considerably in the high-voltage applications of 100 V or more, owing to the material characteristics and improved snapback.

REFERENCES

[1] B. J. Baliga, *Silicon Carbide Power Device*. Cleveland, OH, USA: World Scientific, 2006.
[2] J. Wei, S. Liu, X. Zhang, W. Sun, and A. Q. Huang, "Modeling avalanche induced degradation for 4H-SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11299–11303, Nov. 2020.
[3] J. An and S. Hu, "Experimental and theoretical demonstration of temperature limitation for 4H-SiC MOSFET during unclamped inductive switching," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 206–214, Mar. 2020.
[4] F. Xu *et al.*, "Development of a SiC JFET-based six-pack power module for a fully integrated inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1464–1478, Mar. 2013.

[5] Y. Wang, X. Jin, Y. Peng, J. Luo, and J. Yang, "Design and optimization of high-failure-current dual-direction SCR for industrial-level ESD protection," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4669–4677, May 2020.

[6] O. Semenov, H. Sarbishaei, and M. Sachdev, *ESD Protection Device and Circuit Design for Advanced CMOS TechnolOgies*. New York, NY, USA: Springer, 2008.

[7] P. Denis *et al.*, "Robustness of 4H-SiC 1200V Schottky diodes under high electrostatic discharge like human body model stresses: An in-depth failure analysis," *Diamond Rel. Mater.*, vol. 44, pp. 62–70, 2014, doi: 10.1016/j.diamond.2014.02.002.

[8] P. Lai *et al.*, "Investigation of ESD protection in SiC BCD process," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl.*, 2019, pp. 405–409.

[9] K.-I. Do, B.-S. Lee, and Y.-S. Koo, "Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 283–286, Feb. 2019.

[10] C. Duvvury and C. Diaz, "Dynamic gate coupling of NMOS for efficient output ESD protection," in *Proc. 30th Annu. Proc. Rel. Phys.*, 1992, pp. 141–150.

[11] F. Du *et al.*, "An enhanced gate-grounded NMOSFET for robust ESD applications," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1491–1494, Sep. 2019.

[12] C.-H. Lai, M.-H. Liu, S. Su, T.-C. Lu, and S. Pan, "A novel gate-coupled SCR ESD protection structure with high latchup immunity for high-speed I/O pad," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 328–330, May 2004.

[13] X. Huang, J. J. Liou, Z. Liu, F. Liu, J. Liu, and H. Cheng, "A new high holding voltage dual-direction SCR with optimized segmented topology," *IEEE Electron Device Lett.*, vol. 37, no. 10, pp. 1311–1313, Oct. 2016.

[14] M. D. Ker and T. Y. Chen, "Substrate-triggered technique for on-chip ESD protection design in a 0.18-/spl mu/m salicided CMOS process," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1050–1057, Apr. 2003.

[15] J.-I. Won, J.-W. Jung, I.-S. Yang, and Y.-S. Koo, "Design of ESD protection device using body floating technique in 65 nm CMOS process," *Electron. Lett.*, vol. 47, no. 19, pp. 1072–1073, Sep. 2011.

[16] A. Z. H. Wang, *On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective*. Norwell, MA, USA: Kluwer, 2006.

[17] E. Grund and M. Hernandez, "Obtaining TLP-like information from an HBM simulator," in *Proc. Elect. Overstress/Electrostatic Discharge Symp.*, 2007, vol. 47.

[18] F. Hou *et al.*, "New diode-triggered silicon-controlled rectifier for robust electrostatic discharge protection at high temperatures," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2044–2048, Apr. 2019.

[19] C.-T. Dai and M.-D. Ker, "Study on ESD protection design with stacked low-voltage devices for high-voltage applications," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2014.

[20] Z. Liu, J. J. Liou, S. Dong, and Y. Han, "Silicon-controlled rectifier stacking structure for high-voltage ESD protection applications," *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 845–847, Aug. 2010.