The Current Sharing Strategy of Three-Phase Series Capacitor Boost Converter Based on Charge-Balance Method

Lingling Zhao, Yunfeng Wu, Zhangyong Chen, Lanxiao Shen, and Changhua Zhang

***Abstract*—This article proposed a current sharing strategy for three-phase series capacitor boost converter for continuous conduction mode operation. The phase current can be automatically balanced based on the charge-balance principle, without any additional sensors or devices. And a uniform output voltage expression in full duty ratio range can be obtained. The mechanism of unbalanced current is disclosed. A current sharing strategy is proposed by adjusting the duty ratio in adjacent phase. The selection of capacitor and inductor is discussed via the analysis of topological operation and current deviation. The related characteristics are presented, including uniform output expression, continuous duty ratio operation, insensitivity to inductor parameters, loos analysis, and device stress. Experimental results on 100-W prototype are provided to confirm the feasibility of the proposed strategy.**

***Index Terms*—.**

I. Introduction

MULTIPHASE parallel topology is a popular choice in several industry applications, such as micro-grid [1], automotive [2], battery charger [3], and LED drives [4]. The prime merits of multiphase parallel converter are the smaller output ripple and less electrical stress in each phase, which can help to prevent component damage and cut the cost. However, due to the limitation of the device process and the inevitability of the deviation, parameters of each module are incongruity, resulting in unbalanced current generally. This results in higher switching and conduction losses, early saturation of the phase inductor, and unevenly thermal stress distribution in the system, even operation disfunction [5]–[8].

To solve these problems, current sensors are employed to realize the current sharing by control technique [9]–[16]. The dc droop control and its variants have been applied in microgrids for current sharing purpose [9], [10]. But the droop control has some inherent defects such as voltage deviation, impedances mismatching, circulating current. Aiming at these shortcomings, adaptive droop control methods are proposed [11], [12]. Other control methods with current sensors such as circular chain control [13], master–slave control [14], sliding mode control [15], and phase-shift method [16] are also commonly used to balance phase current. While the adopted current sensors bring the issues of cost increasing, reliability reducing, unevenly thermal.

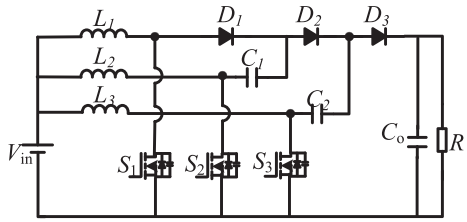

Fig. 1. Topology of three-phase series capacitor boost converter.

Current sharing control without directly using current sensors in every phase has been studied [17]–[20]. These current sharing strategies utilize methods based on the estimation of the parameter mismatches between phases and to adjust the duty ratios to compensate the mismatches. The parasitic resistance [17], the input capacitor voltage ripple [18], and other parameter mismatches [19], [20] are estimated, and then the duty ratios are calculated to balance current. These strategies make the associated control scheme complicated and the converter performance sensitive to converter parameters.

To further improve the performance of multiphase converter, components or cells are added in circuits [21]–[27], such as current sharing capacitor [21], flying capacitor [22], common inductor [23], [24], chain-connected rectifiers [25], and magnetic coupling current balancing cell [26], which can achieve phase current sharing automatically. The series capacitor boost converter topology is proposed in [27], which inherits the merits of switched capacitors and interleaved inductor technique and offers lower converter losses as most of the switches encounter lower voltage stress by adding a capacitor in the adjacent phase. The three-phase structure is shown in Fig. 1. The added capacitors coupled phase operations, resulting in current imbalance in some operation region. Current sharing strategy has been studied for continuous conduction mode (CCM) based on three-phase structure in [28] and discontinuous conduction mode in [29]. However, the duty ratio applying the current sharing strategy in [28] does not change continuously at the edge of operating zone, which may cause a large voltage fluctuation. And the output

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voltage expression becomes more complicated, which increases the complexity of control.

This article proposes a current sharing strategy for three-phase series capacitor boost converter in CCM, based on the principle of capacitor charging balance. Starting with the unique added capacitor structure of the series capacitor topology, the mechanism of unbalanced current is revealed: the independent three-phase currents are affected by the added capacitors by forming a coupling relationship, that and each phase current may be changed by the other phase. Then the charge-balance current sharing strategy is proposed by adjusting the duty ratio based on the ratio capacitor charging time to discharging time. The contribution of the charge-balance current sharing strategy lies in the following.

1) Sensorlesss current sharing: Since the three independent phases are coupled by the added capacitors, the current in each phase can be estimated from other phases. To achieve current sharing in three phases, the duty ratio of each phase needs to be calculated through calculating the duty ratio requirement of the output gain, without adding any current sensor or other device.
2) Uniform output voltage expression: A uniform output voltage expression can be derived by applying the charge-balance current sharing strategy, which is three-times that of the single-phase boost converter. The only variable is the duty ratio of the phase-1, which can simplify the control and improve the reliability of converter.
3) Continuous duty ratio operation: The timing sequence of the three switches is continuous both in size and in phase-shift angle throughout the whole switching period, so the voltage gain is also continuous, which can avoid the big error at critical point.
4) Insensitive to inductors: Results of the simulation with $V_o = 100$ V, $P_o = 100$ W show that current deviation rate in CCM will be within 3% when $L > 300$ μH. Although the current ripple has a certain influence on the current-sharing effect, the result is still within the acceptable range.

The rest of the article is arranged as follows. Section II discusses the basic operating principle and the unbalanced current mechanism of the three-phase topology, based on the capacitor charge-balance principle. In Section III, the charge-balance current sharing strategy for different operating modes is explored. In Section IV, selection of capacitor and inductor has been discussed. In Section V, the related characteristics of the charge-balance current sharing strategy are proposed. In the subsequent, the strategy is validated with experimental results in Section VI. Finally, the article is concluded with a reference to the future work.

II. Operation Principle and Unbalanced Current Mechanism

The basic operating principle of the three-phase series capacitor boost converter and the unbalanced-current mechanism is discussed in this section. The following analysis considers that the converter operate in CCM, which the phase-current would be always continuous.

TABLE I
OPERATING MODES

	V_{L1}	V_{L2}	V_{L3}	i_{C1}	i_{C2}
111	v_{in}	v_{in}	v_{in}	0	0
110	v_{in}	v_{in}	$v_{in}+v_2-v_3$	0	i_3
101	v_{in}	$v_{in}+v_1-v_2$	v_{in}	i_2	$-i_2$
100	v_{in}	$v_{in}+v_1-v_3$	$v_{in}+v_2-v_3$	i_2	i_3
011	$v_{in}-v_1$	v_{in}	$v_{in}+v_2-v_3$	$-i_1$	i_3
010	$v_{in}-v_1$	v_{in}	$v_{in}+v_2-v_3$	$-i_1$	i_3
001	$v_{in}-v_2$	$v_{in}+v_1-v_2$	v_{in}	i_2	$-i_1-i_2$
000	$v_{in}-v_3$	$v_{in}+v_1-v_3$	$v_{in}+v_2-v_3$	i_2	i_3

A. Operation Analysis

The operating modes in a period corresponding to switching logic are quite different. Since a switch has two states, we define that the logic is "1" if a switch turns ON, or "0" if it turns OFF. In CCM, the three-phase converter has eight (2^3) operating modes from 000 to 111. Table I gives the details of the eight switching modes.

The traditional control is the average phase-shift control, where the switches S_1, S_2, and S_3 are evenly displaced with 120° phase-shifted apart from one another with the same duty ratio D, and the three diodes states are opposite to the ON/OFF switching states, respectively. The switches S_1, S_2, and S_3 vary according to the duty ratio variation, then the operating regions are divided into three regions, where $2/3 < D \leq 1$, $1/3 < D \leq 2/3$, and $0 < D \leq 1/3$.

The operating modes of different regions in a switching period are shown in Fig. 2. The combination of 0–1 represents the state of switches, corresponding to Table I. In a switching period, there are six changing states. For example, Fig. 3(a) with 111 signifies that all the switches are ON; the next state 101 signifies that S_1 and S_3 are still ON, but S_2 is turned OFF; the next change is S_2 turns ON, switches' state returns to 111; 110 means that S_1 and S_2 are still ON, but S_3 is turned OFF; switches' state returns to 111 again; then S_1 is turned OFF, switches' state comes in 011. At the top of the switch-state box is the duration of each state, and the total time in a full turn is equal to one switching period T_s. The current of capacitor C_1 and C_2 in one period is represented by two circles, respectively, in which the green represents capacitor is charging, the red represents discharging, and the dotted line indicates that the capacitor is with no current through; the arrow points to clockwise also indicates discharging, and vice versa.

1) 2/3 < D ≤ 1: When the duty ratio is in (2/3, 1/3], the operating modes encompass either 3 or 2 phases being simultaneously on depending on interleaving sequence, which is with maximum voltage gain. The corresponding switching states are shown in Fig. 2(a), and the states changing is 111-101-111-110-111-011, the duration of each state is $(D - 2/3)T_s$ or $(1 - D)T_s$. According to Table I, the voltage gain in this region can be established in terms of the duty ratio D by applying the inductor volt-second balance, which is given by the following equation:

$$M_1 = \frac{V_o}{V_{\text{in}}} = \frac{3}{1-D}. \tag{1}$$

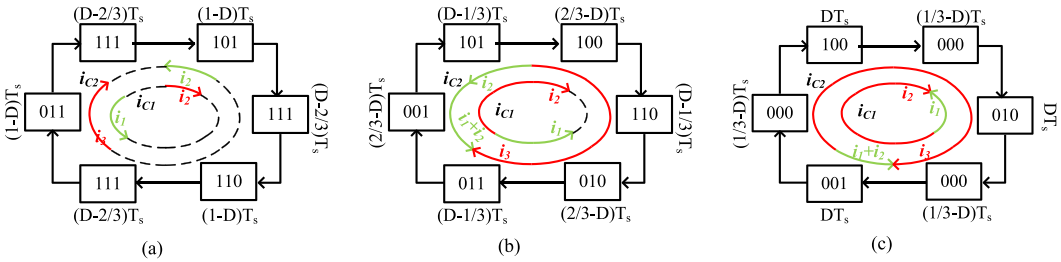


Fig. 2. Switching sequence according to duty ratio for a switch period. (a) $2/3 < D \leq 1$. (b) $1/3 < D \leq 2/3$. (c) $0 < D \leq 1/3$.

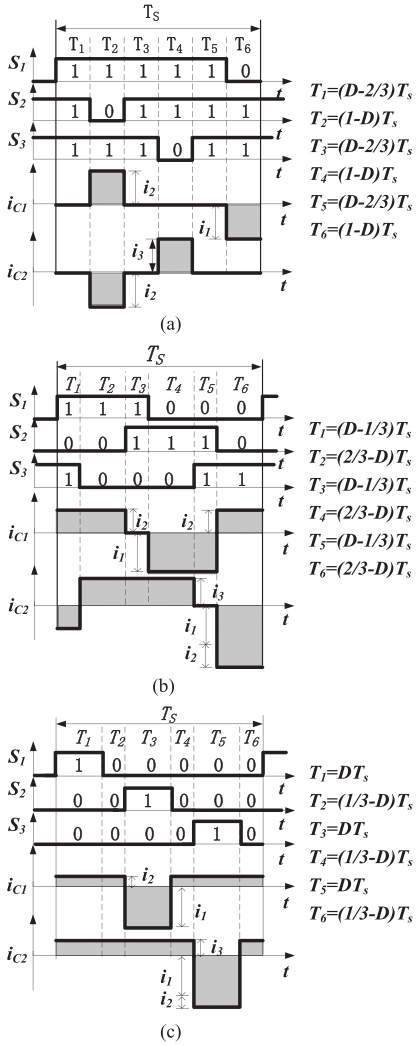


Fig. 3. Diagram of the unbalanced current mechanism. (a) $2/3 < D \leq 1$. (b) $1/3 < D \leq 2/3$. (c) $0 < D \leq 1/3$.

The capacitor current only exists in the in 101 and 011, where the durations of each state are both $(1-D)T_s$. The phase current can be obtained by applying the principle of the capacitor charge-balance. The result shows that the input current is inherently shared among all the three-phases in $2/3 < D \leq 1$ operating mode

$$i_1 = i_2 = i_3 = \frac{i_{\text{in}}}{3}. \tag{2}$$

It is to be noted that the input current is inherently shared among all the three-phases in $2/3 < D \leq 1$ operating mode.

2) 1/3 < D ≤ 2/3: Fig. 2(b) gives the operating details when the duty ratio is (1/3, 2/3], which the switching states changing turn is 101-100-110-010-011-001, with the duration $(D-2/3)T_s$ or $(1-D)T_s$. Similarly, by applying the principle of volt-second balance of inductor, there is

$$M_2 = \frac{V_o}{V_{\text{in}}} = \frac{(2D^2 - 4D + 19/9)}{(1-D)^3}. \tag{3}$$

Meanwhile, C_1 is discharged by i_2 lasting $(1-D)T_s$ and charged by i_1 lasting $1/3T_s$; C_2 discharged by i_3 lasting $2/3T_s$, charged by i_1 lasting $(2/3-D)T_s$ and by i_2 lasting $1/3T_s$. The inductor current can be derived by applying the capacitor charge balance principle, one obtains the following:

$$\begin{cases} i_1 = \frac{(1-D)^2}{2D^2-4D+19/9} i_{\text{in}} \\ i_2 = \frac{1/3(1-D)}{2D^2-4D+19/9} i_{\text{in}} \\ i_3 = \frac{(D^2-5D/3+7/9)}{2D^2-4D+19/9} i_{\text{in}}. \end{cases} \tag{4}$$

It can be observed that the output voltage is not an integer fraction of the input voltage, which expressed by a cubic function. The current in each phase is not equal, and it is difficult to visualize the magnitude relationship.

3) 0 < D ≤ 1/3: When duty ratio is smaller than 1/3, the corresponding switching pattern appears in Fig. 2(c), the switching states changing turn is 100-000-010-000-001-000, and the duration of each state is $(d-1/3)T_s$ or $(2/3-d)T_s$. C_1 is discharged by i_2 lasting $(1-D)T_s$ and charged by i_1 lasting DT_s; C_2 discharged by i_3 lasting $(1-D)T_s$, charged for DT_s by i_1+i_2. This is the region of minimum converter gain with the least duty ratio. Similar to the previous two regions, the voltage gain and the phase current are given by

$$M_3 = \frac{V_o}{V_{\text{in}}} = \frac{1}{(1-D)^3} \tag{5}$$

$$\begin{cases} i_1 = (1-D)^2 i_{\text{in}} \\ i_2 = D(1-D) i_{\text{in}} \\ i_3 = D i_{\text{in}}. \end{cases} \tag{6}$$

And it is clear that in this operating mode, output voltage expression is still complex, which is a cubic function; and the current is not shared in each phase, which phase 1 has the highest current and the least in phase 2.

B. Unbalanced Current Mechanism

As we can see from the analysis above, the three-phase currents are equal in $2/3 < D \leq 1$, but the different conclusions in other regions. We can observe that whether in $2/3 < D \leq 1$, $1/3 < D \leq 2/3$, and $0 < D \leq 1/3$, as shown in Fig. 3, the charge balance of C_1 is only determined by i_1 and i_2, where i_1 is only for charging and i_2 for discharging. Similarly as for C_2, the current i_1 and i_2 is only responsible for charging and i_3 for discharging. Actually, the phase current is obtained by applying the charge balance of capacitor. The principle describes that, in a steady state, the capacitor current over one switching period must be zero. The above findings provide a guarantee for phase current estimation. We can estimate the relationship between three-phase current directly even without the calculation of current.

According to the principle of capacitor charge-balance, the information in Fig. 2 can be converted to Fig. 3, where the positive area is equal to the negative. The relationship of three-phase currents is intuitively shown. It can be concluded in Fig. 3(a) for $2/3 < D \leq 1$ that the discharging current i_2 and the charging current i_1 of C_1 are in T_2 and T_6, respectively, which are both equal to $(1 - D)T_S$. Then the conclusion that $i_1 = i_2$ can be derived by capacitor charge-balance. Meanwhile, the current of C_2 in one switching period, T_4 is also equal to T_2, where $i_3 = i_2$ can be derived. Hence, the result $i_1 = i_2 = i_3$ comes. In Fig. 3(b) for $1/3 < D \leq 2/3$, the relationship between three-phase current can be directly derived similarly. That is, $T_4 + T_5$ for charging current i_1 is smaller than $T_1 + T_2 + T_6$ for discharging current i_2, so that i_1 is bigger than i_2 through the principle of capacitor charge balance. For the operating mode of C_2, in the same way, it is concluded that i_2 is the smallest. So it can be intuitively seen that the phase current value is presented by $i_1 > i_3 > i_2$. The charging and discharging process of the capacitors in $0 < D \leq 1/3$ is sketched in Fig. 3(c), with the relationship $i_1 > i_3 > i_2$.

The principle of capacitor charge balance must be satisfied in all systems. Specifically, for the three-phase series capacitor boost converter, the product of charge time and charge current should be equal to the product of discharge current and discharge time. In other words, if the charging time is not equal to discharging time, then the charging current and discharging current will not equal. Therefore, the current sharing strategy can be derived via adjusting the ratio between the charge time and discharge time.

III. Proposed Current Sharing Strategy

In this section, a method named charge-balance current sharing strategy is proposed, which can effectively operate in full duty ratio. This strategy comes from the analysis results already developed in Section II. The operating time of i_1 and i_2 can be adjusted based on the charge-balance of C_1, to achieve the equivalent of i_1 and i_2. In this premise that $i_1 = i_2$, the charge balance of C_2 can be used to correct the value of i_3. Therefore, two steps of charge-balance current sharing operation can achieve the purpose of three-phase current sharing. The following is a detailed analysis of the current sharing strategy in different duty ratio range.

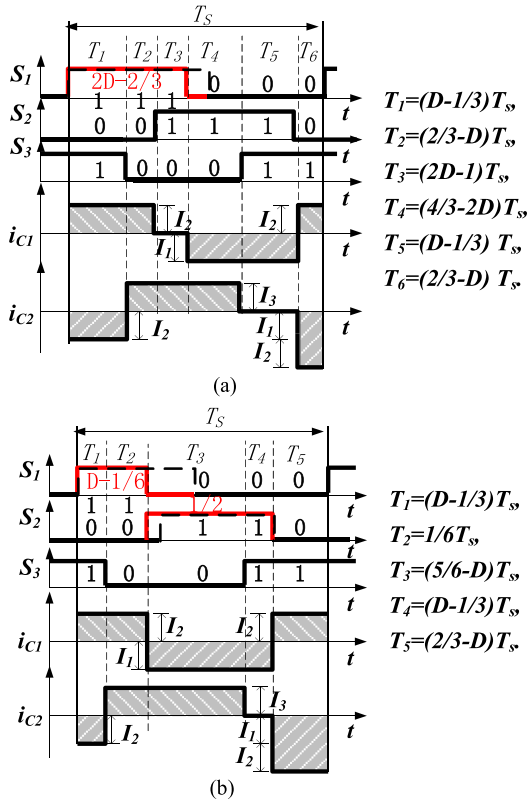


Fig. 4. Diagram of the unbalanced current mechanism. (a) $1/2 < D \leq 2/3$. (b) $1/3 < D \leq 1/2$.

A. Current Sharing Strategy in $2/3 < D \leq 1$

Since the current in three-phase are inherently shared in $2/3 < D \leq 1$, no other current sharing operation is needed in this region. The operation of current sharing control in $2/3 < D \leq 1$ is completely consistent with the average phase-shift control, which S_1, S_2, S_3 are evenly displaced with 120° phase-shifted apart from one another with the same duty ratio D, as shown in Fig. 3(a).

B. Current Sharing Strategy in $1/3 < D \leq 2/3$

Fig. 4 is the timing sequence of the charge-balance current sharing strategy and phase current estimation in $1/3 < D \leq 2/3$. Since the state duration between $(2/3 - D)T_s$ and $(D - 1/3)T_s$ takes $D = 1/2$ as the critical point, there is a subtle difference in the current sharing strategy. The current sharing strategy of this region is divided into two smaller regions which the one is $1/2 < D \leq 2/3$ and the other is $1/3 < D \leq 1/2$.

For understanding the process of charge-balance current sharing strategy, the time-adjusting operations in this region are described as an example.

The first step, for achieving the purpose of $i_1 = i_2$, the required operation is to balance the charging time and discharge time for C_1. The time of i_1 should be extended to be equal to i_2. T_4' is extended to $(2D - 1)T_s$, and T_2 stays

TABLE II
CAPACITOR CHARGING CURRENT STRATEGY IN A SWITCH PERIOD WITH CONTINUOUS CHANGE

	S_1	S_2	S_3	$M=3/(1-D_1)$
$2/3<D_1\leq1$	D_1 ,shift by 0°	D_1 ,shift by120°	D_1 ,shift by 240°	9++
$1/3<D_1\leq2/3$	D_1 ,shift by 0°	$D_1/2+1/3$,shift by 120°	$D_1/2+1/3$,shift by 240°	9~4.5
$1/6<D_1\leq1/3$	D_1 ,shift by 0°	1/2 ,shift by $D_1*2\pi$	D_1 +1/6 ,shift by 240°	4.5~3.6
$0<D_1\leq1/6$	D_1 ,shift by 0°	1/2 ,shift by $D_1*2\pi$	1/3 ,shift by 240°	3.6~3

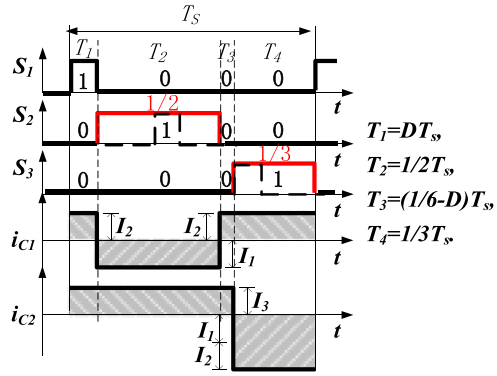


Fig. 5. Current sharing strategy in $0 < D \leq 1/6$.

when *1/2* $< D \leq$ *2/3;* $T_4' = (5/6 - D)T_s$ *[*T_3 in Fig. 4(b)*],* $T_2 = 1/6T_s$ when *1/3* $< D \leq$ *1/2*

$$(T_1 + T_2' + T_6) \times i_2 = (T_4' + T_5) \times i_1. \tag{7}$$

The second step, i_3 can be equal to the other two phases current by performing a similar calculation on the charge time and discharge time ratio of C_2. The equation indicates that i_3 can be equal to the other two phase current inherently in the premise of $i_1 = i_2$

$$(T_2' + T_3 + T_4') \times i_3 = (T_1 + T_6) \times i_2 + T_6 \times i_1. \tag{8}$$

In 1/2 $< D \leq$ 2/3, the timing sequence of current-sharing operation is $D_1 = 2D - 2/3$, $D_2 = D_3 = D$, and the phase-shifting angle is as same to the traditional phase-shift control with 120°. By applying this current sharing strategy, solution for the voltage gain leads to the following:

$$M_{1/2<D\leq2/3} = \frac{V_o}{V_{\text{in}}} = \frac{9}{5 - 6D} = \frac{3}{1 - D_1}. \tag{9}$$

In 1/2 $< D \leq$ 2/3, the timing sequence of current-sharing operation is $D_1 = D - 1/6$, $D_2 = 1/2$, $D_3 = D$, and S_2 should be turned ON immediately when S_1 is turned OFF. The voltage gain is calculated as follows:

$$M_{1/3<D\leq1/2} = \frac{V_o}{V_{\text{in}}} = \frac{18}{7 - 6D} = \frac{3}{1 - D_1}. \tag{10}$$

C. Current Sharing Strategy in $0 < D \leq 1/3$

In the last region of $1/3 < D \leq 1/2$, D_1 has reached a minimum of 1/6, where $D_1 = D - 1/6$, so it only needs to perform current sharing operation in $0 < D_1 \leq 1/6$. The current sharing operation details is displayed in Fig. 5, which the timing sequence is $D_1 = D$, $D_2 = 1/2$, and $D_3 = 1/3$, and the phase-shift angles of S_1 and S_3 remained, S_2 is turned ON immediately after S_1 is turned OFF. The voltage gain is calculated by applying the principle of volt-second balance that

$$M_{0<D<1/6} = \frac{V_o}{V_{\text{in}}} = \frac{3}{1 - D} = \frac{3}{1 - D_1}. \tag{11}$$

D. Summary of Current Sharing Strategy

As a summary, Table II are listed the operating details of charge-balance current sharing strategy in a whole duty ratio range. The output voltage has a uniform expression with D_1, which is as follows:

$$V_o = \frac{3}{1 - D_1} V_{\text{in}}. \tag{12}$$

It is also worth noting that the timing change of S_1, S_2, and S_3 is continuous both in size and in phase-shift angle.

IV. CAPACITORS AND INDUCTORS SELECTION

A. Capacitor Selection

The added capacitors in adjacent phase are important components, which leads the relationship between phase changes from independent to coupling. The capacitors operate as switch, there are several points to consider when choosing a capacitor.

First, the addition capacitors should allow the converter to operate in original state, without causing resonance. The resonant frequency formed by capacitor and inductor in every phase should be sufficiently low. Then there is not excessive resonant ringing across the power switch when the switch is turned OFF. For design purposes, one-half of the resonant period must exceeds the maximum OFF time of switch. An assumption is proposed that one-half the resonant period formed by L and $C_{1,2}$ is much longer than the maximum switching OFF time, and the limit of capacitor can be estimated

$$\pi\sqrt{L_r C_{1,2}} >> T_{\text{Sw}} \rightarrow C_{1,2} >> \frac{(1 - D)^2}{\pi^2 L_r {f_{\text{S}}}^2}. \tag{13}$$

Current capability is another aspect that needs to be considered in the application of converters to high power occasions. In a series capacitor boost converter, $I_{\text{in}} = M \times I_o$, and M can be more than 10 at these occasions, and the maximum value of current of C_1 is *1/3* I_{in}, C_2 is *2/3* I_{in}. So the current capacity of capacitor is worth considering. In addition, the capacitor should have a small ESR to reduce losses.

In this article, a CBB capacitor which has low ESR and good current capability with the value of 4.7 μF was selected in simulation and experimental platform.

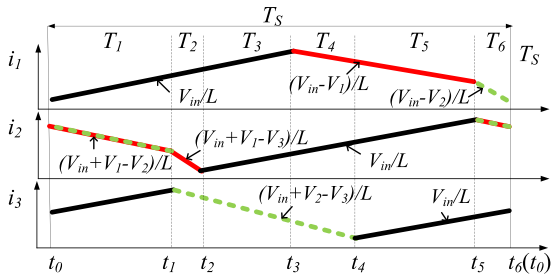


Fig. 6. Waveforms of the three-phase current $1/3 < D_1 < 2/3$.

B. Inductors Selection

The charge-balance current sharing strategy proposed in this article is mainly based on the charge-balance principle of the two intermediate capacitors. The average phase current in a period is estimated by the charging and discharging current of capacitor. In fact, the periodic average current is replaced by the partial current. The process of current-sharing is calculating the result of charging and discharging current to replace a phase average current. Therefore, the method of estimating periodic phase current by partial phase current is analyzed, in order to evaluate the influence on the current sharing effect.

Taking $1/3 < D_1 < 2/3$ as an example, Fig. 6 shows the waveforms of the three-phase current in one switching period, which is corresponding to Fig. 4(a). The solid red line indicates the charging and discharging current of C_1, and the green dotted line indicates the charging and discharging current of C_2. There are some overlaps between the two lines, means the stage current is operating on C_1 and C_2 at the same time.

For the process of charging and discharging in C_1, the partial current in red is used to achieve the current sharing result of i_1 & i_2. The stage in which i_1 actually participates in charging mode is T_4–T_5, and i_2 as discharging current is only T_1, T_2, and T_6. Assume that the beginning inductor current value is $i_{n(t0)}$. In the first subinterval of i_1, which includes $T_1 + T_2 + T_3$, the inductor current changes with slope V_{in}/L; in the second subinterval which includes T_4+T_5, the inductor current changes with slope $(V_{\text{in}}-V_1)/L$; in the last subinterval which includes T_6, the inductor current changes with slope $(V_{\text{in}} - V_2)/L$;. The value at subinterval end is (final value) = (initial value) + (length of interval) (average slope), and hence, the value at the end of the second subinterval can be calculated

$$\begin{cases} i_{1(t3)} = i_{1(t0)} + \frac{V_{\text{in}}}{L} \times \left(2D - \frac{2}{3}\right) T \\ i_{1(t5)} = i_{1(t3)} + \frac{V_{\text{in}}-V_1}{L} \times (1-D)T \\ i_{1(t6)} = i_{1(t5)} + \frac{V_{\text{in}}-V_2}{L} \times \left(\frac{2}{3} - D\right) T = i_{1(t0)}. \end{cases} \tag{14}$$

Then, the average value of i_1 in one switching period can be expressed as follows:

$$I_1 = \frac{1}{T_s} \sum_{i=0}^{6} \frac{1}{2} (i_{1(ti)} + i_{1(ti+1)}) * T_{i+1}. \tag{15}$$

The average partial current of charging for C_1 which is in red can be described as follows:

$$I_{1(C1)} = \frac{1}{2} * (i_{1(t3)} + i_{1(t5)}). \tag{16}$$

Similarly, the average value of i_2 can be expressed by the same way as follows:

$$I_2 = \frac{1}{T_s} \sum_{i=0}^{6} \frac{1}{2} (i_{2(ti)} + i_{2(ti+1)}) * T_{i+1} \tag{17}$$

$$\begin{aligned} I_{2(C1)} = {} & \frac{1}{T_1 + T_2 + T_6} \\ & \times \left[(i_{1(t0)} + i_{1(t1)}) \times \frac{T_1}{2} + (i_{1(t1)} + i_{1(t2)}) \right. \\ & \left. \times \frac{T_2}{2} + (i_{1(t3)} + i_{1(t4)}) \times \frac{T_6}{2} \right]. \end{aligned} \tag{18}$$

The charge-balance current sharing strategy conditions by assuming $I_{1(C1)} = I_{2(C1)}$ through the principle of capacitor charging balance

$$I_{2(C1)} \times (T_1 + T_2 + T_6) = I_{1(C1)} \times (T_4 + T_5). \tag{19}$$

In the same way, for C_2, the green dotted line is used to achieve the current sharing between i_3 and i_1, i_2. There are

$$\begin{aligned} I_{1,2(C2)} = {} & \frac{1}{2T_6 + T_1} \times \left[(i_{1(t5)} + i_{1(t6)}) * \frac{T_6}{2} \right. \\ & \left. + (i_{2(t5)} + i_{1(t1)}) * \frac{T_6 + T_1}{2} \right] \end{aligned} \tag{20}$$

$$I_3 = I_{3(C2)} = \frac{1}{2} \times (i_{3(t1)} + i_{3(t4)}). \tag{21}$$

The current sharing operation requirements are that

$$I_{1,2(C2)} \times (2T_1 + T_6) = I_{3(C2)} \times (T_2 + T_3 + T_4). \tag{22}$$

For the operating modes in $1/6 < D \leq 1/3$ and $0 < D \leq 1/6$, the current error can be obtained via the same steps. From the above analysis, it can be seen that the three-phase current is not completely equal, which is related to the value of inductor. It is necessary to evaluate the influence of the inductor value on current-sharing.

In order to establish a clear relationship between the actual phase current and average current, a current deviation rate ΔI, should be introduced as follows:

$$\Delta I_i = \left| \frac{I_i - I_{\text{in}}/3}{I_{\text{in}}/3} \right| \times 100\%. \tag{23}$$

In order to reflect the influence of inductor on the effect of current sharing, a Pspice simulation platform with the output of 100 V and 100 W was established. MOS for IPP60R099C6 with fs = 100 kHz, diode for MUR20200CT, $C_1 = C_2 =$ 4.7 μF, the output capacitor is C_o = 300 μF are selected in the simulation. In each operating mode, the only variable is inductor value which is between 200 and 600 μH with a step of 100 μH. For each inductor value, a group of phase current data has been sampled, and finally a relationship curve between current rate and inductor value is plotted. Current deviation in

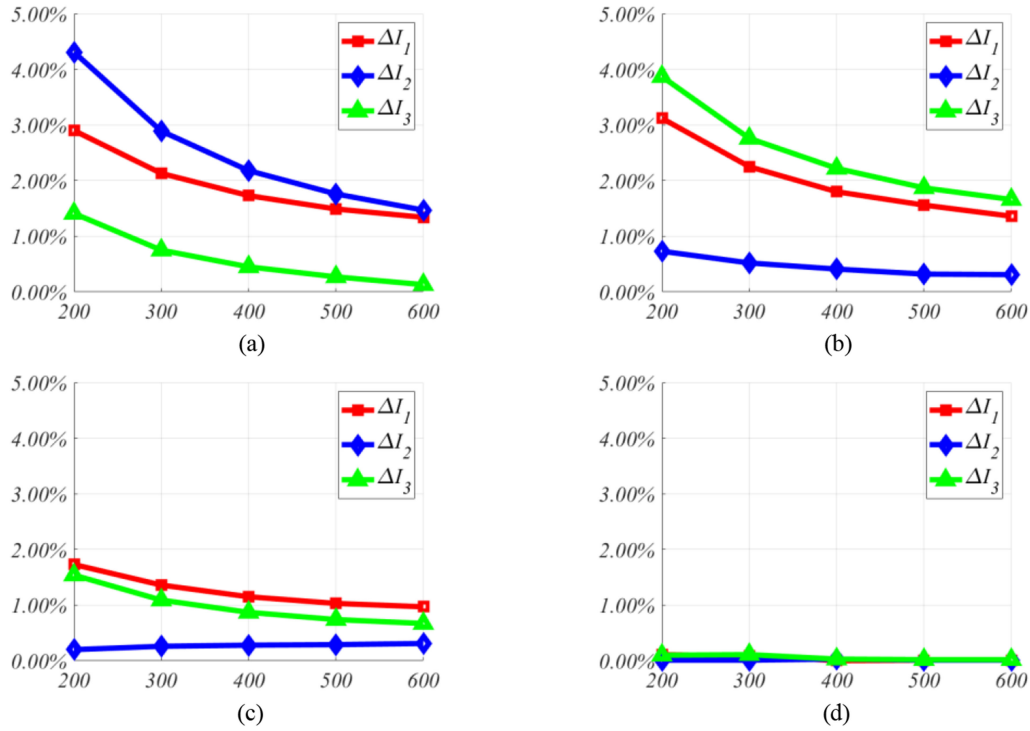


Fig. 7. Current deviation rate with inductor in different operating zone. (a) $D_1 = 0.1$, M = 3.33. (b) $D_1 = 0.28$, M = 4.17. (c) $D_1 = 0.52$, M = 6.25. (d) $D_1 = 0.7$, M10.

four operating modes is tested, as shown in Fig. 7. ΔI_1, ΔI_2, and ΔI_3 decrease when the inductor value increases, which also corresponds to the theoretical analysis. And ΔI_1, ΔI_2, *and* ΔI_3 can approach to zero if the inductor is big enough. Therefore, it can be estimated from the above analysis that although the ripple has a certain influence on the current sharing effect, the result is still obvious within the acceptable range.

In this article, the value of 250 μH was selected for inductor in simulation and experimental platform.

V. Related Characteristics

A. Sensorless Current Sharing

By applying the charge-balance current sharing strategy, the currents can be evenly distributed to three phases in full duty ratio range. The only needed operation is to adjust the duty ratio, without adding any current sensor and other device. Since the three-phases are coupled by the added capacitors, the current in each phase can be estimated from others, then the demand for current sensors is eliminated.

B. Uniform Output Voltage Expression

The converter has different current-sharing operations in different regions, but a uniform output voltage expression in whole duty range. The output voltage expression [12] is simplified to a linear function compared with the average phase-shift control, which has three expressions in different regions correspond to (1), (3), and (5), as shown in Fig. 8. The gain of output voltage

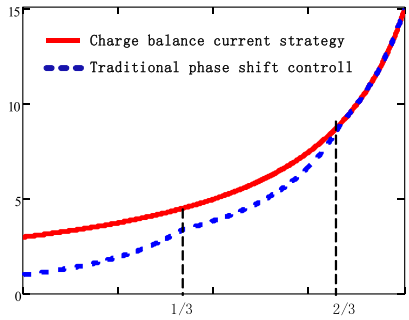


Fig. 8. Compared curve of output voltage gain with average phase-shift control.

by applying the charge-balance current sharing strategy is from 3 to $+\infty$.

C. Continuous Duty Ratio Operation

The charge-balance current sharing strategy can be applied by calculating the only variable D_1, and the timing sequence of the other two switches is deterministic. It is worth noting that the timing changes of S_1, S_2, and S_3 are continuous both in size and in phase-shift angle in full duty ratio range, as shown in Table II. Therefore, the continuity of output voltage can be guaranteed, which can avoid the big error at critical point.

D. Insensitive to Inductors

As the analysis and the simulation results in Section IV-B, ΔI_1, ΔI_2, and ΔI_3 decreases with the inductor value increase of

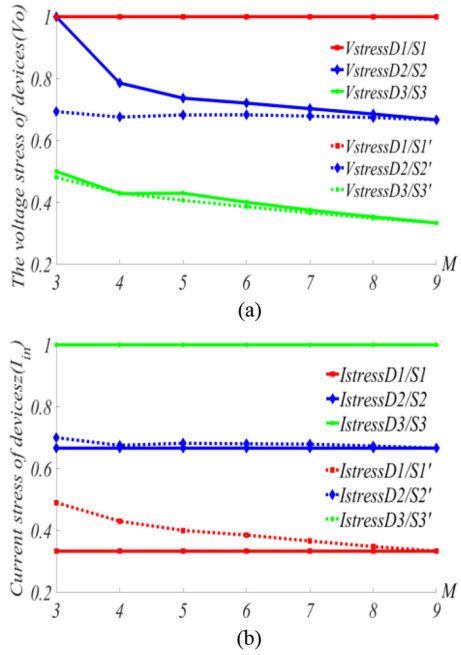


Fig. 9. Voltage and current stress compared with traditional phase-shift control. (a) Voltage stress. (b) Current stress.

the x-coordinate. Statistically speaking, ΔI_1, ΔI_2, and ΔI_3 are all within 3% When $L \geq 300\ \mu$H. Therefore, although the current ripple has a certain influence on the current sharing effect, the result is still obvious within the acceptable range, and the result of current-sharing is insensitive to inductors in CCM.

E. Voltage and Current Stress

The voltage and current stress for each device has not changed in expression because no devices or modes are added. The voltage stress expression of switch and diode is V_o in phase-1, $V_o - V_1$ in phase-2, $V_o - V_2$ in phase-3. The current stress expression of switch and diode is I_1 in phase-1, $I_1 + I_2$ in phase-2, $I_1 + I_2 + I_3$ in phase-3. While the duration of modes is changed, leading to different capacitor voltage, which has different effects on the voltage stress of the devices; and the current stress of the devices will also be changed due to the current sharing operation.

The voltage and current stress applying charge-balance current sharing strategy is compared with that applying traditional phase-shift control, with M as the variable in 3–9. The result is shown in Fig. 9(a), which the solid line is the current-sharing strategy proposed in this article, and the dotted line is the traditional phase-shifting strategy. The voltage stress of phase-1 switch S_1 and diode D_1 is equal to the output voltage V_o. The voltage stress of phase-2 S_2 and D_2 is increased at low voltage gains. And the voltage stress of S_3 and D_3 is nearly equal. The current stress compared with the traditional phase-shift control is shown in Fig. 9(b). Since the strategy proposed in this article can achieve current-sharing in three phase, every phase current is equal to $1/3I_{\rm in}$. It can be seen that the maximum current stress is the input current on S_3 and D_3. The current stresses of D_1 & S_1, D_2 & S_2 are reduced by applying the charge-balance current sharing strategy.

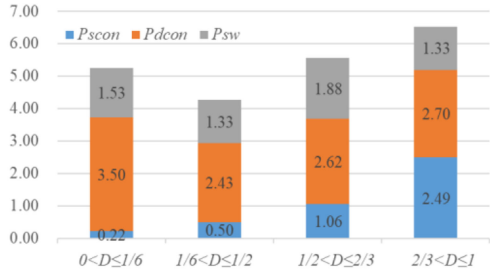


Fig. 10. Loss in different operating mode.

F. Loss Analysis

In order to evaluate the characteristic of charge balance current sharing strategy comprehensively, the loss of topology in different operating modes is analyzed. Generally, the total loss is composed of MOS conduction loss, diode conduction loss, and MOS switching loss.

1) MOS Conduction Loss: The common calculation for the MOS conduction loss is the product of MOS conduction current square and the MOS ON-resistance $R_{\rm DS(on)}$, and the conduction current of S_1, S_2, S_3 are determined by operating modes, which the expression is concluded as follows:

$$P_{S\rm CON(1,2,3)} = \left(\frac{T_{\rm SCON(1,2,3)} I_{S\rm CON(1,2,3)}}{T_S}\right)^2 R_{\rm DS(ON)}. \tag{24}$$

2) Diode Conduction Loss: The diode conduction loss is expressed as the product of conduction current and conduction voltage, which the current is determined by the mode, and the voltage is the inherent performance of the device

$$P_{D\rm CON(1,2,3)} = \frac{T_{D\rm CON(1,2,3)} I_{D\rm CON(1,2,3)}}{T_S} V_F. \tag{25}$$

3) MOS Switching Loss: MOS switching loss can be calculated by the triangle principle, that is, the 1/2 product of ON (or OFF) voltage and current is represented one time switching loss

$$P_{\rm SW(1,2,3)} = \left(\frac{V_{Sr(1,2,3)} T_r I_{S(1,2,3)}}{2} + \frac{V_{Sf(1,2,3)} T_f I_{S(1,2,3)}}{2}\right) \times f_s. \tag{26}$$

It is worth noting that the phase current is equal to 1/3 input current. The rms input current in CCM is as follows:

$$I_{\rm rms} = \sqrt{\left(\frac{P_0}{V_{\rm in}}\right)^2 + \frac{\Delta {I_L}^2}{12}}. \tag{27}$$

In order to quantify the loss, the parameters are adopted as follows: $V_o = 100$ V, $P_{\rm o} = 100$ W, MOS for IPP60R099C6 ($R_{\rm DS\text{-}ON} = 0.09\ \Omega$, $T_r = 15$ ns, $T_f = 65$ ns) with $f_s = 100$ kHz, and diode for MUR20200CT ($V_F = 0.9$ V). Under this condition, the loss of four groups input data is represented in different operating modes: $D_1 = 0.1$, $V_{\rm in} = 30\ V$; $D_1 = 0.28$, $V_{\rm in} = 24\ V$; $D_1 = 0.53$, $V_{\rm in} = 16\ V$; $D_1 = 0.7$, and $V_{\rm in} = 10\ V$. The results are shown in Fig. 10.

TABLE III
COMPARISON RESULTS

Comparison items	Sensorless-Current-sharing	Control strategy complexity	Gain function complexity	Duty ratio continuity
Average phase-shift control	worst	best	best	best
Current-sharing strategy in [28]	best	worst	worst	worst
Charge-balance current sharing strategy	best	next	best	best

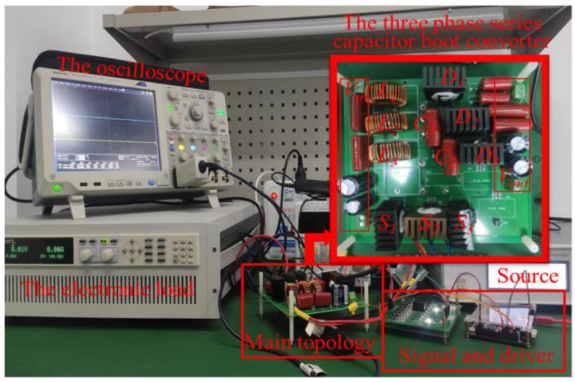


Fig. 11. Experimental prototype.

TABLE IV
EXPERIMENTAL PARAMETERS

Items	Value
Input voltage	10-30V
Output voltage	100V, 100W
Mediate capacity C_1, C_2	CBB, 4.7u
Phase inductor	250μH
Switch type	IPP6R099C6
Diode type	MBR20200CT
Switching frequency	100kHz

G. Comparison Results

As introduced in Section I, some general current sharing control and their characteristic are discussed, so there is no more enumeration. Specially, two control methods for the series capacitor boost converters are compared with the charge-balance strategy. One is the traditional phase-shift control, which has three output voltage expressions in different regions correspond to (1), (3), and (5). The other control method for this topology is the current sharing strategy proposed by Roy and Ayyanar in [28]. The details is listed in the Appendix, including operating duty ratio, the status of current sharing, and converter gain at different operating regions.

The comparison results are shown in Table III.

1) For realizing the sensorless-current-sharing, the average phase-shift control needs auxiliary components, which is relatively the most difficult; the other two control methods are easy to achieve.
2) As to the control strategy complexity, charge-balance current sharing strategy is after the average phase-shift control, but also a simple control method.

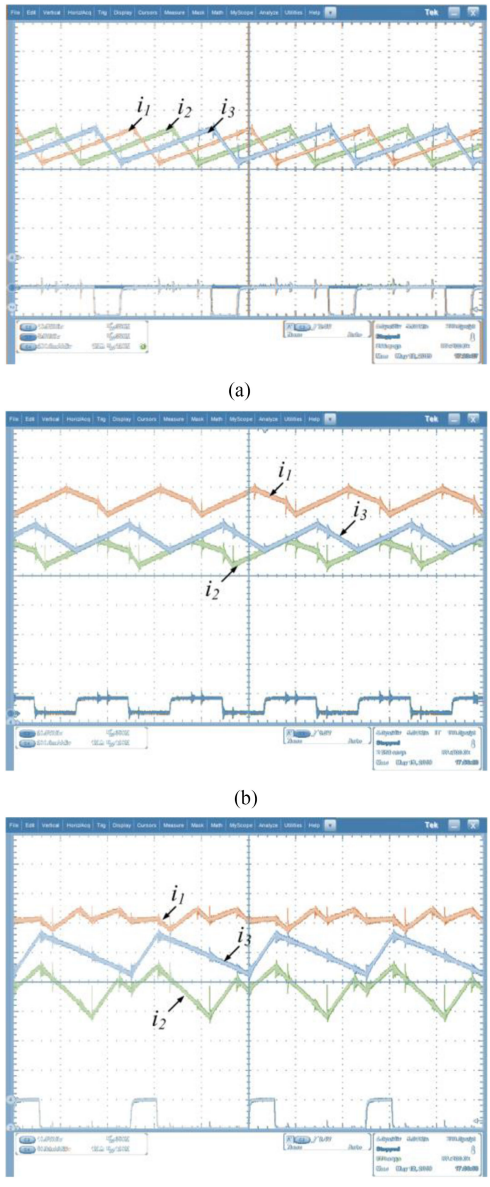
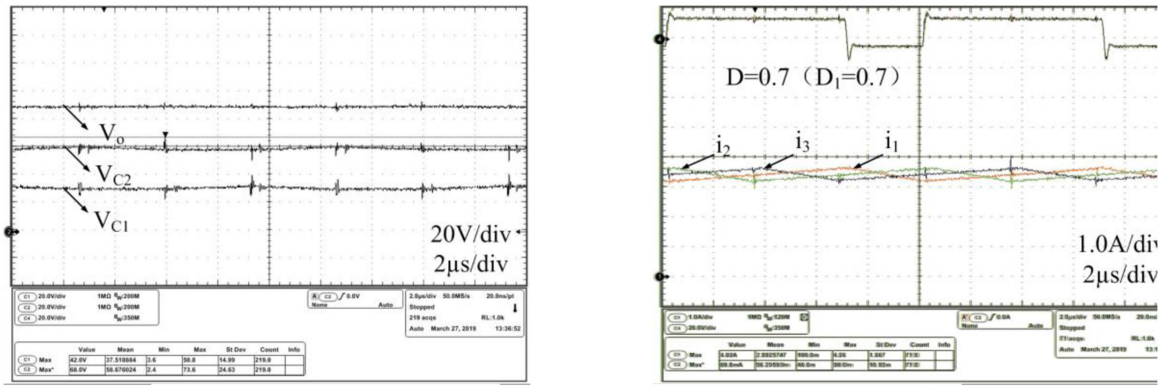


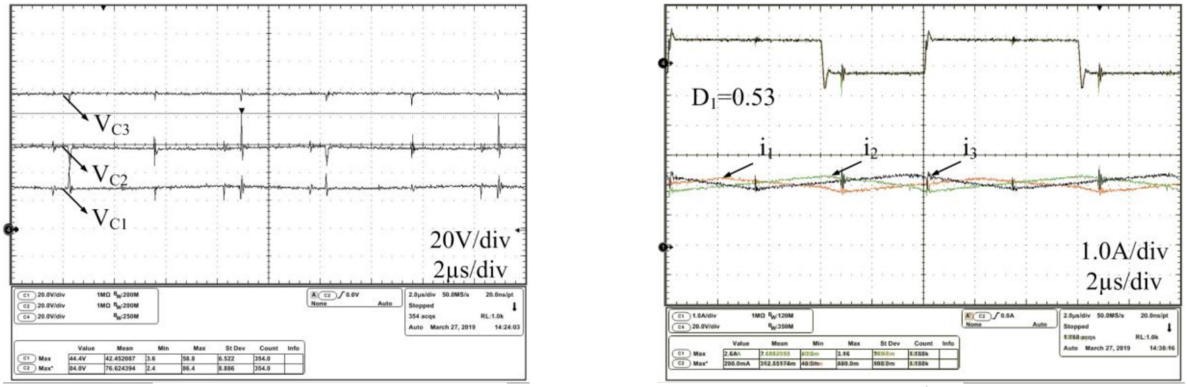
Fig. 12. Experimental waveform of the unbalanced phase current. (a) $2/3 < D \leq 1$. (b) $1/3 < D \leq 2/3$. (c) $0 < D \leq 1/3$.

3) The gain function is a simple division between output and input, which is related to the complexity of the control algorithm and the stability of a system. The charge-balance current sharing strategy is outstanding with the uniform liner output expression, while others are expressed by different cubic function in different duty ratio region.



(a) (b)

Fig. 13. Experimental results in $2/3 < D_1 \leq 1$ when $D_1 = 0.7$. (a) Voltage of C_1, C_2, and output. (b) Three-phase current.



(a) (b)

Fig. 14. Experimental results in $1/2 < D_1 \leq 2/3$ when $D_1 = 0.53$. (a) Voltage of C_1, C_2, and output. (b) Three-phase current.

4) The duty ratio continuity is also as an evaluation, because it will affect whether the system can get correct output, especially at the changing point of the operation area. The performance of the charge-balance current sharing strategy in this respect is also satisfactory.

VI. Experimental Results

In order to test and validate the effect of charge-balance current sharing strategy, a 100 W prototype was established, which is driven by field-programmable gate array signals, as shown in Fig. 11. The output voltage is maintained to 100 V with the input voltage range 10–30 V. The performance is given based on the device parameters in Table IV.

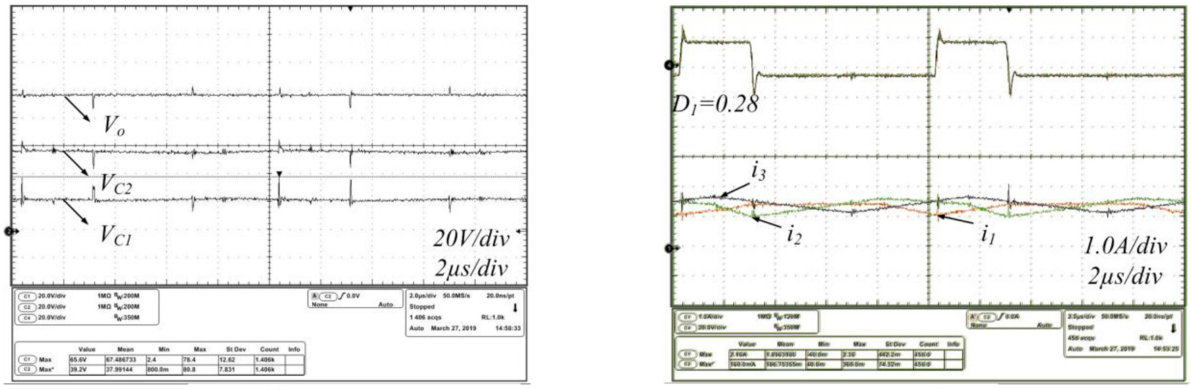
First, the actual performance of three duty ratio range is test based on the traditional phase-shift control, as shown in Fig. 12. The results from Section II are verified. In detail, three-phase current is equal in $2/3 < D \leq 1$, whereas $D_1 = 0.7$; and the phenomenon of $i_1 > i_3 > i_2$ in $1/3 < D \leq 2/3$ in $0 < D \leq 1/3$ is also revealed in Fig. 12(b) and (c).

The performance applying the charge-balance current sharing strategy is also tested in different operating mode, and the results are shown in Figs. 13–16.

Fig. 13 shows the experimental results of $D_1 = 0.7$ in the condition of $V_{\text{in}} = 10$ V and $M = 10$, which is in the range of $2/3 < D \leq 1$. The timing of S_1 in the figure can be used for positioning by readers. Two capacitors' voltage and output voltage is in Fig. 13(a), which $V_1 = 31.92$ V, $V_2 = 62.17$ V, $V_{\text{out}} = 90.02$ V. It is basically consistent with the theoretical analysis. The control method is that $D_1 = D_2 = D_3 = 0.7$, S_2 is shifted by 120° from S_1, and S_3 is shifted by 240° from S_1. The experimental result of phase current is shown in Fig. 13(b). The current-sharing are achieved automatically.

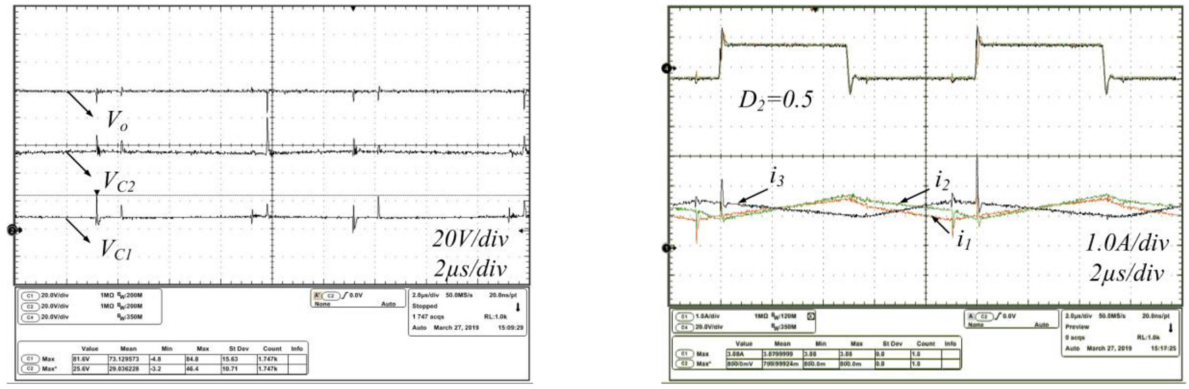
Fig. 14 shows the experimental results of the current sharing operation in $1/3 < D_1 \leq 2/3$, where $D_1 = 0.53$ in the 16 V input-voltage experiment. According to the proposed charge-balance current sharing strategy, phase-2 shifts 120° from phase-1 with $D_2 = 0.6$, and phase-3 shifts 240° from phase-1 with $D_3 = 0.6$. Fig. 14(a) shows the capacitor voltage and the output voltage, which $V_1 = 29.97$ V, $V_2 = 59.21$ V, $V_{\text{out}} = 97.83$ V. Basically, it is also consistent with the theoretical analysis. The converter can achieve three-phase current sharing automatically by applying the charge-balance current sharing strategy in $1/3 < D_1 \leq 2/3$, as shown in Fig. 14(b). The increasing and decreasing trends of three-phase currents are different, but the average values are almost equal in a switch period.

Fig. 15 shows the experimental results in $1/6 < D_1 \leq 1/3$. The duty ratio is $D_1 = 0.28$, and the input voltage is 24 V. The switching timing is $D_1 = 0.28$, $D_2 = 0.5$, $D_3 = 0.45$, phase-2 shifts 100° from phase-1, and phase-3 shifts 240° from



(a) (b)

Fig. 15. Experimental results in $1/6 < D_1 \leq 1/2$ when $D_1 = 0.28$. (a) Voltage of C_1, C_2, and output. (b) Three-phase current.



(a) (b)

Fig. 16. Experimental results in $0 < D_1 \leq 1/6$ when $D_1 = 0.1$. (a) Voltage of C_1, C_2, and output. (b) Three-phase current.

phase-1. Voltage information $V_1 = 23.97$ V, $V_2 = 57.23$ V, $V_{\text{out}} = 97.63$ V is shown in Fig. 15(a), which is consistent with the theoretical analysis. Fig. 15(b) shows the current information of the converter, in which the current sharing is realized automatically.

Fig. 16 shows the experimental results when the input voltage is 30 V, which adopted $D_1 = 0.1$ in the range of $0 < D_1 \leq 1/3$. The switching timing is $D_1 = 0.1$, $D_2 = 0.5$, $D_3 = 0.33$, phase-2 shift 36° from phase-1, and phase-3 shift 240° from phase-1. Fig. 16(a) shows the voltages of $V_1 = 9.87$ V, $V_2 = 56.30$ V, and $V_{\text{out}} = 99.42$ V, whose results are essentially in agreement with the theoretical analysis. Fig. 16(b) shows the balanced three-phase currents after applying the proposed current sharing strategy.

The theoretical analysis is verified by the experimental results in which the charge-balance current sharing has the features of uniform output voltage expression and automatic current-sharing in full duty ratio range.

VII. Conclusion

The charge-balance current sharing strategy for the three-phase series capacitor boost converter is proposed in this article, which is suitable for CCM operation in full duty ratio range. The strategy can automatically balance the phase current by adjusting the duty ratio, without any additional sensors or devices. And a uniform output voltage expression in full duty ratio range can be derived.

The operating modes of the three-phase series capacitor boost converter are analyzed based on different duty ratio range. The main idea of the current-sharing strategy is applying the principle of capacitor charge-balance by adjusting the ratio of charging time and discharging time. The key to selecting inductor and capacitor is carried out. And some characteristics are compared with two control methods which are proposed in Section I. Finally, the experimental results show that applying the current sharing strategy can establish accurate current-sharing in full duty ratio region. The strategy can also achieve the uniform output expression, the continuous switch timing changes and insensitivity of inductor parameters.

The main idea is still effective for the four-phase or more phase of series capacitor topology. The charge-balance current sharing strategy is a widely applicable method for the current-sharing of multiphase series capacitor topology.

APPENDIX

TABLE V
OUTPUT VOLTAGE EXPRESSION OF THE AVERAGE PHASE-SHIFT CONTROL [28]

Condition	Current sharing	Duty ratio	Ideal gain	
2/3<D≤1	Inherent sharing with equal D	$\frac{2}{3} < D_1 = D_2 = D_3 \le 1$	$\frac{3}{(1-D)}$	∞-9
1/3<D≤2/3	Typically not shared with equal D	$\frac{1}{3} < D_1 = D_2 = D_3 \le \frac{2}{3}$	$\frac{(2D^2-4D+19/9)}{(1-D)^3}$	9-3.375
	Modified D (Asym PWM)—shared equally	$D_1 = 2D-\frac{2}{3}; D_2 = D_3 = D; \frac{1}{2} \le D \le \frac{2}{3}$	$\left(\frac{5}{9}-\frac{2}{3}D\right)^{-1}$	9-4.5
	Modified D (Sym PWM)—shared equally	$D_1 = \frac{13}{5}D-\frac{16}{15}; D_2 = \frac{1}{5}D+\frac{8}{15}; D_3 = D;$ $\frac{3}{7} \le D \le \frac{2}{3}$	$\left(\frac{23}{45}-\frac{3}{5}D\right)^{-1}$	9-3.94
0<D≤1/3	Typically not shared with equal D	$0 \le D_1 = D_2 = D_3 \le \frac{1}{3}$	$\frac{3}{(1-D)^3}$	3.375-1
	Modified D-higher gain (case2)—shared equally	$D_1 = D, D_2 = \frac{1}{2}+\frac{1}{2}D; D_3 = \frac{1}{3}, 180°$ interleaving with D_1 in phase with D_2	$\frac{3}{(1-D_2)(1-D_3)}$	3.94-3
	Modified D-lower gain (case1)—RMSerror minimized	$D_1 = 0, D_2 = D; D_3 = \frac{D_2}{1+D_2}$ 180°interleaving	$\frac{3}{(1-D_2)(1-D_3)}$	3-1

REFERENCES

[1] E. Alizadeh, M. Hamzeh, and A. M. Birjandi, "A multifunctional control strategy for oscillatory current sharing in DC microgrids," *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 560–570, Jun. 2017.

[2] K. E. Harouri, S. E. Hani, I. Aboudrar, A. Ahmed, and N. Naseri, "Energy production by electric vehicle for vehicle-to-grid (V2G) applications," in *Proc. 6th Int. Renewable Sustain. Energy Conf.*, Rabat, Morocco, 2018, pp. 1–6.

[3] S. Y. Ou and L. Y. Liu, "Design and implementation of a four-phase converter with digital current sharing control for battery charger," in *Proc. IEEE Int. Telecommun. Energy Conf.*, Osaka, Japan, 2015, pp. 1–6.

[4] X. Liu, X. Li, Q. Zhou, and J. Xu, "Flicker-free single switch multi-string LED driver with high power factor and current balancing," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6747–6759, Jul. 2019.

[5] M. Gleissner and M.-M. Bakran, "Design and control of fault-tolerant non-isolated multiphase multilevel dc-dc converters for automotive power systems," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1785–1795, Feb. 2016, doi: 10.1109/TIA.2015.2497218.

[6] M. Moradpour, A. Serpi, and G. Gatto, "Dead-time analysis of a universal SiC-GaN-based DC-DC converter for plug-in electric vehicles," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Washington, DC, 2018, pp. 1134–1139.

[7] J. Lu, M. Savaghebi, and Y. Guan, "DC-link protection and control in modular uninterruptible power supply," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3942–3953, May 2018.

[8] H. Kim, M. C. Choi, S. Kim, and D. Jeong, "An AC–DC LED driver with a two-parallel inverted buck topology for reducing the light flicker in lighting applications to low-risk levels," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3879–3891, May 2017.

[9] M. Hamzeh, A. Ghazanfari, Y. A. I. Mohamed, and Y. Karimi, "Modeling and design of an oscillatory current-sharing control strategy in DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6647–6657, Nov. 2015.

[10] Y. Zhu, F. Zhuo, F. Wang, B. Liu, and Y. Zhao, "A wireless load sharing strategy for islanded microgrid based on feeder current sensing," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6706–6719, Dec. 2015.

[11] P. Wang, X. Lu, X. Yang, W. Wang, and D. Xu, "An "improved distributed secondary control method for DC microgrids with enhanced dynamic current sharing performance," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6658–6673, Sep. 2016.

[12] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, "Adaptive droop control strategy for load sharing and circulating current minimization in low-voltage standalone DC microgrid," *IEEE Trans. Sustain. Energy*, vol. 6, no. 1, pp. 132–141, Jan. 2015

[13] J. Han and J. Song, "Phase current-balance control using DC-link current sensor for multiphase converters with discontinuous current mode considered," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4020–4030, Jul. 2016.

[14] J. Ao, Z. Wang, J. Chen, L. Peng, and Y. Chen, "The cost-efficient gating drivers with master-slave current sharing control for parallel SiC MOSFETs," in *Proc. IEEE Transp. Electrific. Conf. Expo, Asia-Pac.*, Bangkok, Thailand, 2018, pp. 1–5.

[15] V. Repecho, D. Biel, R. Ramos-Lara, and P. G. Vega, "Fixed-switching frequency interleaved sliding mode eight-phase synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 676–688, Jan. 2018.

[16] Z. Li, H. Li, L. Zhao, X. Zheng, H. Pang, and M. Gao, "A current-sharing driving method for multilevel current reinjection converter," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 877–888, Jan. 2019.

[17] J. Gordillo and C. Aguilar, "A simple sensorless current sharing technique for multiphase DC–DC buck converters," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3480–3489, May 2017.

[18] L. Yifei, W. Yubin, and W. Shanshan, "Sensorless current sharing in two-phase input-parallel output-parallel DC-DC converters," in *Proc. 18th Int. Conf. Elect. Mach. Syst.*, Pattaya, Thailand, 2015, pp. 1919–1924.

[19] R. F. Foley, R. C. Kavanagh, and M. G. Egan, "Sensorless current estimation and sharing in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2936–2946, Jun. 2012.

[20] W. Huang and J. A. A. Qahouq, "Input voltage ripple-based sensorless current sharing autotuning controller for multiphase DC–DC converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4117–4125, Sep./Oct. 2016.

[21] K. I. Hwu and W. Z. Jiang, "Nonisolated Two-Phase interleaved LED driver with capacitive current sharing," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2295–2306, Mar. 2018.

[22] O. Kirshenboim and M. M. Peretz, "Combined multilevel and two-phase interleaved LLC converter with enhanced power processing characteristics and natural current sharing," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5613–5620, Jul. 2018.

[23] H. Wang, Y. Chen, Y. Liu, J. Afsharian, and Z. Yang, "A passive current sharing method with common inductor multiphase LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6994–7010, Sep. 2017.

[24] H. Wang, Y. Chen, and Y. Liu, "A Passive-Impedance-Matching technology to achieve automatic current sharing for a multiphase resonant converter," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9191–9209, Dec. 2017.

[25] J. Shi, T. Liu, J. Cheng, and X. He, "Automatic current sharing of an input-parallel output-parallel (IPOP)-connected DC–DC converter system with chain-connected rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2997–3016, Jun. 2015.

[26] B. Lin and Y. Lin, "Parallel current-fed resonant converter with balance current sharing and no input ripple current," *IET Power Electron.*, vol. 12, no. 2, pp. 212–219, Feb. 2019.

[27] Y. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007.

[28] J. Roy and R. Ayyanar, "Sensor-less current sharing over wide operating range for extended-duty-ratio boost converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8763–8777, Nov. 2017.
[29] P. S. Shenoy and M. Amaro, "Improving light load efficiency in a series capacitor buck converter by uneven phase interleaving," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2784–2789.
[30] I. O. Lee, S. Y. Cho, and G. W. Moon, "Interleaved buck converter having low switching losses and improved step-down conversion ratio," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3664–3675, Aug. 2012.

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