Single-Phase LED Driver With Reduced Power Processing and Power Decoupling

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***Abstract*—Reduced power processing is a new trend to improve the conversion efficiency of light-emitting diode (LED) driver systems. Based on the concept, a new LED driver architecture is proposed in this article, which requires fewer power semiconductors compared with prior works, leading to the potential of lower cost and higher efficiency. A new ac/dc LED driver topology is derived accordingly based on the architecture to achieve the constant output current and unity power factor with significant energy storage reduction of the 100-/120-Hz energy buffer. Through a split and shared inductor, the required magnetic energy storage in the derived topology is the same as the conventional single-stage power factor correction converter, indicating high power density. Experimental evaluation verifies the performance in terms of improved power quality and conversion efficiency.**

***Index Terms*—Active buffering, active decoupling, electrolytic capacitor, light-emitting diode (LED) driver, power processing, single phase.**

I. Introduction

LIGHT-EMITTING diodes (LEDs) have the advantages of higher efficacy, longer lifespan, and faster response over the conventional lighting sources [1]. For offline LED applications, a dedicated LED driver capable of ac to dc conversion, should provide a regulated dc current to supply LEDs, while maintain a high power factor (PF) to comply with electric standards, such as the IEC 61000-3-2 [2]. On top of these requirements, recently, there is a growing trend to develop ac/dc LED drivers without electrolytic capacitors (E-caps) [3]. E-caps are generally needed in the conventional single-stage LED driver to buffer the twice-line ripple power inherent in any single-phase power-conversion systems. Fig. 1 illustrates the ripple power, which is defined as the instantaneous power mismatch between the input and output side, and highlighted in red and yellow. Furthermore, E-caps are also known for their short service lifetime [4]. Eliminating E-caps in LED drivers has become a very important target to improve LED driver technology. Long lifespan capacitor technologies such as film capacitors and ceramic capacitors exist, but they cannot be applied directly in lieu of E-caps in the single-stage LED driver due to their higher cost and lower energy storage density [5].

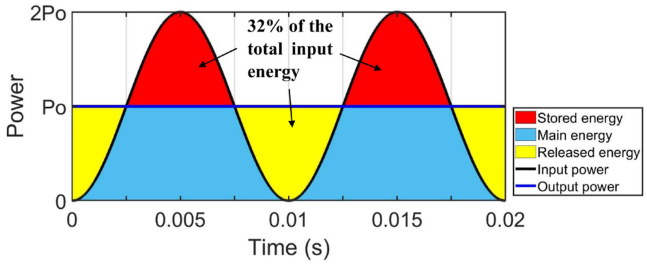

Fig. 1. Power and energy flow analysis.

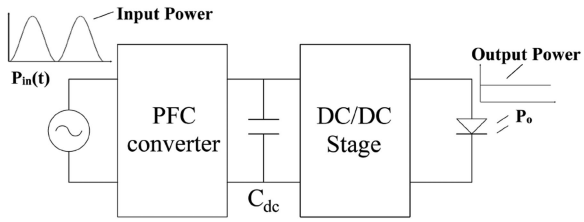

Fig. 2. LED driver with a full power processing scheme [9].

Active buffering approach is an effective approach to address the aforementioned dilemma [6], [7]. In this approach, ripple power is actively diverted to a buffer capacitor and the stringent requirement of the output voltage ripple is thus decoupled, bringing in an opportunity to reduce the energy storage requirement of the capacitor via increasing the voltage swing on it. The reduced energy storage requirement enables long lifespan capacitors to be employed in the system without compromising power density and cost [8]. Fig. 2 shows a typical cascaded ac/dc conversion architecture with the active buffering [9]–[12]. The architecture consists of two stages to separately perform power factor correction (PFC) and current regulation, where the ripple power is, therefore, buffered at the buffer capacitor $C_{\rm dc}$. The capacitance of the $C_{\rm dc}$ can be effectively reduced by allowing a higher voltage swing on it. Despite its effectiveness in capacitance reduction, a critical problem of the cascaded two-stage topology lies in its potentially low efficiency. Power needs to be processed twice by the two stages to reach the output. Assuming that the efficiencies of the PFC and dc/dc stage are η_1 and η_2, respectively, the total power loss can be calculated by

$$P_{\rm loss} = P_{\rm in}(1-\eta_1) + P_{\rm in}\eta_1(1-\eta_2) \tag{1}$$

where $P_{\rm in}$ is the average input power over a line period.

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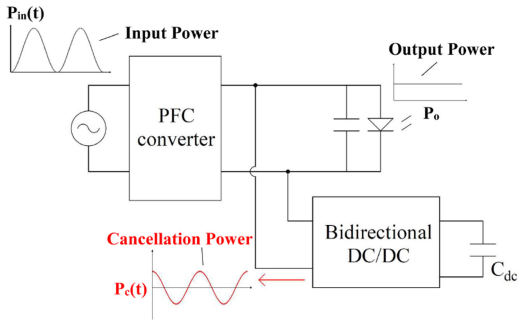

Fig. 3. LED driver with a bidirectional power processing scheme [14].

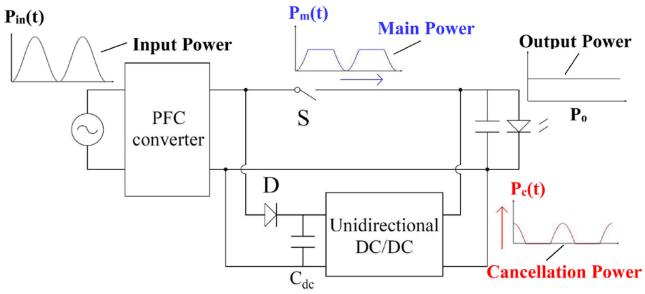

Fig. 4. LED driver with a unidirectional power processing scheme [15].

To improve the system efficiency, the bidirectional power processing scheme, as shown in Fig. 3, is proposed in [13] and [14]. This architecture consists of the PFC stage, and the bidirectional dc/dc converter paralleled at the output side. The bidirectional dc/dc converter is designed to produce compensating power for the twice-line ripple cancellation. As the ripple power weigh only 32% of P_{in}, the dc/dc stage processes less power than that in the cascaded two-stage architecture, leading to reduced power losses and potentially higher efficiency. Mathematically, the power losses with the bidirectional power processing architecture can be calculated as

$$P_{\text{loss}} = P_{\text{in}}(1-\eta_1) + 0.32P_{\text{in}}\eta_1(1-\eta_2^2) \tag{2}$$

where η_1 and η_2 refer to the efficiencies of the PFC converter and the bidirectional dc/dc converter, respectively. The power loss analysis shows that η_2 is squared in the loss analysis since the ripple power is processed twice by the dc/dc converter.

Another driver architecture utilizing a unidirectional power processing scheme, as shown in Fig. 4, is recently proposed [15]. The ripple power is only processed once by the dc/dc stage in this architecture, which indicates better efficiency compared to the bidirectional counterpart, but additional switches, *S* and *D*, are needed to ensure proper input power distribution. The power loss in the unidirectional architecture can be calculated as

$$P_{\text{loss}} = P_{\text{in}}(1-\eta_1) + 0.32P_{\text{in}}\eta_1(1-\eta_2) + P_s + P_d \tag{3}$$

where η_1 and η_2 represent the efficiencies of the PFC converter and the unidirectional dc/dc converter, respectively. P_s and P_d refer to the power losses on the extra switch *S* and diode *D*, respectively. The extra loss resulted from *S* and *D* will offset

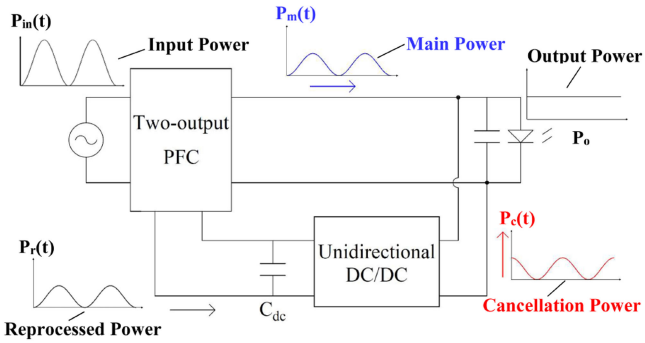

Fig. 5. LED driver with an improved unidirectional power processing scheme based on the two-output PFC converter.

the efficiency gain with this architecture. On top of this disadvantage, all architectures mentioned previously require two stages to process the power, which may lead to the usage of extra magnetic energy storage compared to the conventional single-stage architecture and inevitably increases the size of the LED driver.

This article proposes a new ac/dc architecture to improve the previous architectures of reduced power processing, as shown in Fig. 5. The proposed architecture consists of a two-output PFC stage and a unidirectional dc/dc stage. Due to the two-output characteristic, the input power distribution is inherently achieved without dedicated switching devices, which removes the P_s and P_d losses in (3). The solution naturally leads to lower cost, simpler topology, and higher efficiency. Besides, this article also demonstrates that the unidirectional dc/dc stage in the Fig. 5 can be integrated with the two-output PFC stage through sharing inductor, which avoids the usage of extra magnetic storage as mentioned in the previous architectures.

The rest of this article is organized as follows. Section II introduces the operating principle of the topology. Section III provides detailed design information. Section IV verifies the proposed topology through simulation and experiments. Finally, Section V concludes this article.

II. Operational Principle

As illustrated in the Fig. 5, the input power $P_{\text{in}}(t)$ is divided into two proportions, $P_r(t)$ and $P_m(t)$, by the two-output PFC stage, where $P_m(t)$ directly flows to the load without being reprocessed and $P_r(t)$ needs to be further reprocessed by the unidirectional dc/dc stage to generate $P_c(t)$ and cancel the ripple power in $P_m(t)$.

Based on the proposed architecture, a topology is derived from the single-stage buck–boost converter as shown in Fig. 6. The derivation comes from two simple steps. First, the main inductor of the buck–boost topology is split into two small inductors to work as the two-output PFC converter mentioned in the Fig. 5. Then, an extra power flow path constructed by S_2, C_{dc}, and D_b is introduced to generate $P_c(t)$ and realize the active buffering function, which emulates the unidirectional dc/dc converter through sharing L_b with the two-output PFC converter.

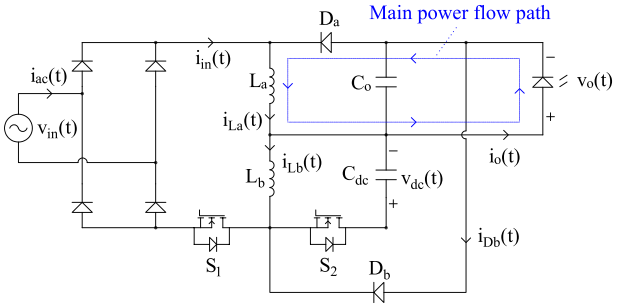

Fig. 6. Proposed topology derived from the proposed architecture.

A. Operating Modes and Waveforms

Similar to the conventional buck–boost converter, the proposed topology works in the discontinuous conduction mode (DCM) to achieve a high power factor. The operation is divided into five modes. The equivalent circuits of each mode are shown in Fig. 7. The corresponding waveforms are illustrated in Fig. 8, which are described in the following.

1) Mode 1 [t_o–t_1]: S_1 is turned ON at t_o. Both L_a and L_b are charged simultaneously by the input voltage until S_1 is turned OFF at t_1 as shown in Fig. 7(a). The peak inductor current, $i_{pk}(t)$, during this mode can be determined by

$$i_{pk}(t) = \frac{|v_{\text{in}}(t)|D}{(L_a + L_b)f_{\text{sw}}} \tag{4}$$

where D is the duty cycle for S_1, and f_{sw} is the switching frequency. The input current is exactly the inductor current during this mode and zero in any other modes, so the average input current within one switching period is

$$\begin{aligned} i_{\text{av}}(t) &= \frac{i_{pk}(t)DT_s}{T_s} \\ &= \frac{D^2}{(L_a + L_b)f_{\text{sw}}}|v_{\text{in}}(t)|. \end{aligned} \tag{5}$$

From (5), the input current is proportional to the input voltage and power factor correction can, therefore, be naturally achieved with a constant duty ratio.

2) Mode 2 [t_1–t_2]: S_1 is turned OFF at t_1. The energy stored in L_a is directly released to the LEDs through D_a without any processing, which creates the main power flow path, $P_m(t)$, as highlighted in the Fig. 6. L_a is fully discharged at t_2. Meanwhile, the energy stored in L_b is first released to the buffer capacitor through S_2, as shown in Fig. 7(b), which creates the reprocessed power, $P_r(t)$, as illustrated in the Fig. 5. After $i_{Lb}(t)$ drops to zero, L_b is charged reversely by the buffer capacitor and i_{Lb} becomes negative. A short dead time is applied to S_2 to ensure the output capacitance of S_2 is fully discharged so that S_2 can be turned ON with zero-voltage switching (ZVS). S_2 works like a synchronous rectifier when L_b is releasing power to C_{dc}, which lowers the conduction loss.

3) Mode 3 [t_2–t_3]: The buffer capacitor continues to charge L_b like the conventional buck–boost converter. The ON-time of S_2, $T_{\text{on}}(t)$, controls how much energy is discharged from the

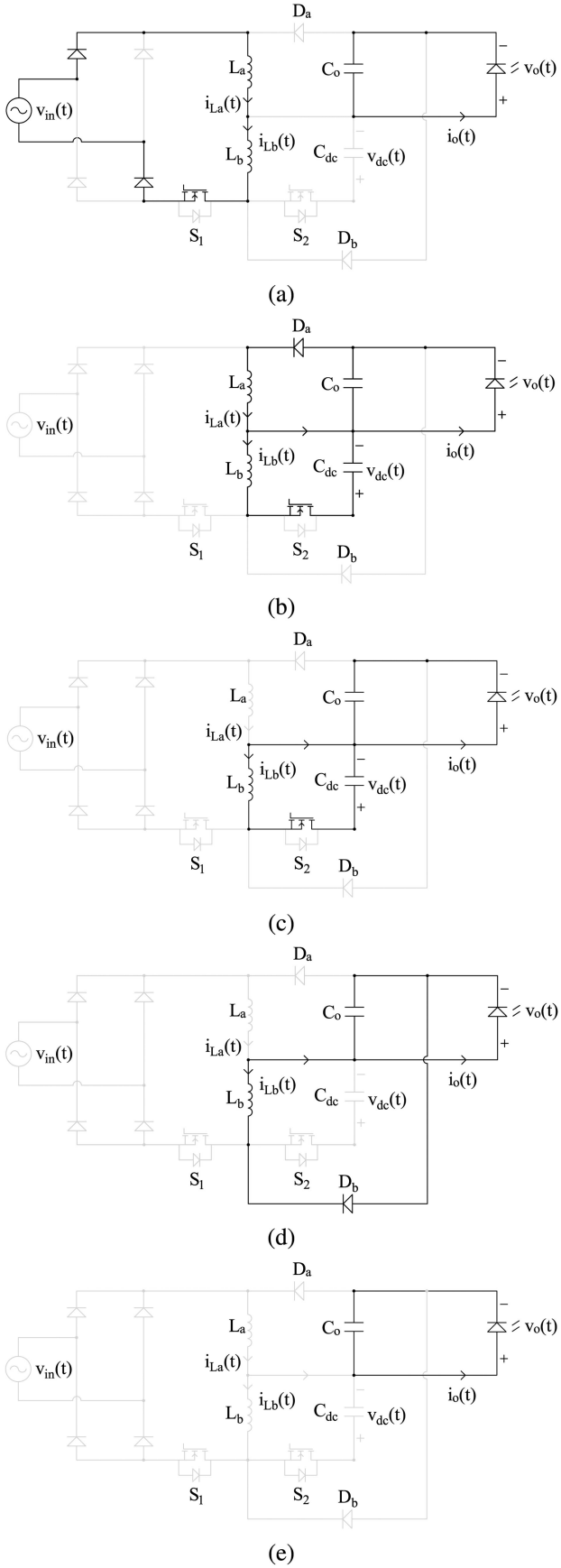

Fig. 7. Operating modes. (a) Mode 1:[t_o-t_1]. (b) Mode 2:[t_1-t_2]. (c) Mode 3:[t_2-t_3]. (d) Mode 4:[t_3-t_4]. (e) Mode 5:[t_4-t_5].

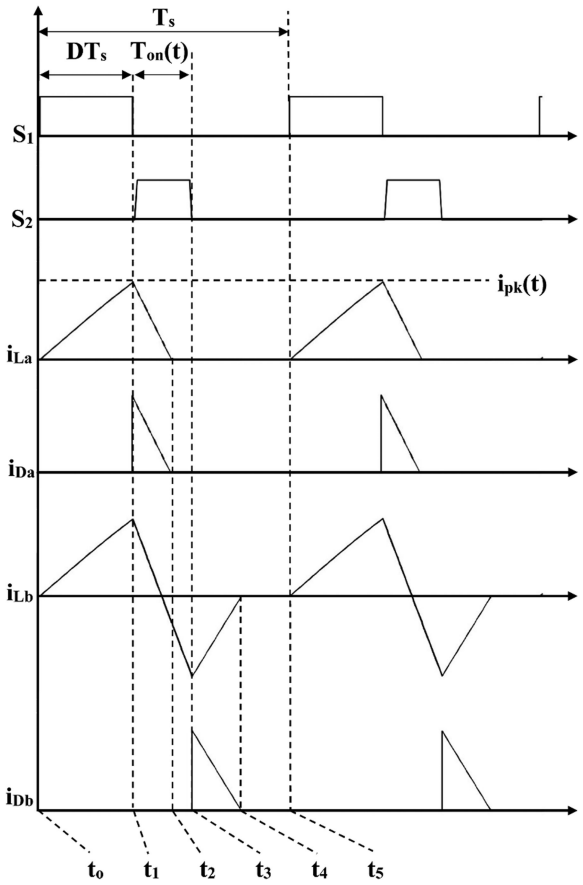

Fig. 8. Detailed waveforms of operation.

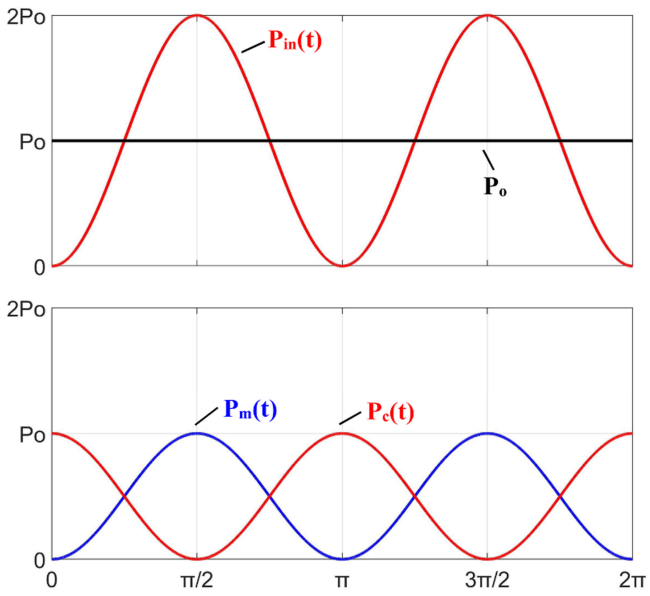

Fig. 9. Power processing scheme in the proposed configuration.

buffer capacitor to create $P_c(t)$ and is taken as the control variable to ensure a constant output current. It is worth mentioning that S_2 can be turned OFF before t_2 when there is no need to discharge the buffer.

4) Mode 4 [t_3–t_4]: S_2 is turned OFF at t_3 and the energy stored in L_b is released to the LEDs through D_b as shown in Fig. 7(d), which creates $P_c(t)$. At t_4, L_b is fully discharged.

5) Mode 5 [t_4–t_5]: All energy stored in the inductors is released and the output capacitor maintains the load power.

B. Advantages and Comparisons

The power processing scheme with the split inductors is introduced as follows. According to the operating principle mentioned previously, the input energy stored in L_a and L_b during the ON-state of S_1 are $0.5L_a i_{pk}(t)^2$ and $0.5L_b i_{pk}(t)^2$, respectively. Averaging the input energy stored in L_a and L_b over a switching period, $P_m(t)$ and $P_r(t)$ can be calculated as

$$\begin{cases} P_m(t) = \dfrac{f_{sw} L_a i_{pk}(t)^2}{2} \\ P_r(t) = \dfrac{f_{sw} L_b i_{pk}(t)^2}{2}. \end{cases} \tag{6}$$

From (6), $P_{\text{in}}(t)$ is distributed proportionally into $P_r(t)$ and $P_m(t)$. The distribution ratio, k, is defined as

$$\begin{aligned} k &= \frac{P_r(t)}{P_{\text{in}}(t)} \\ &= \frac{P_r(t)}{P_r(t) + P_m(t)} \\ &= \frac{L_b}{L_a + L_b}. \end{aligned} \tag{7}$$

Thus, $P_m(t)$ can be calculated as

$$\begin{aligned} P_m(t) &= (1-k) P_{\text{in}}(t) \\ &= 2(1-k) P_o (\sin(\omega t))^2 \end{aligned} \tag{8}$$

where P_o is the output power and $P_r(t)$ can be calculated as

$$\begin{aligned} P_r(t) &= P_{\text{in}}(t) - P_m(t) \\ &= 2P_o(\sin(\omega t))^2 - 2(1-k)P_o(\sin(\omega t))^2 \\ &= 2\,kP_o(\sin(\omega t))^2. \end{aligned} \tag{9}$$

The aforementioned analysis is based on the proposed topology, which is operated as the two-output PFC converter shown in Fig. 5. The advantage lies in the natural distribution of the input power without additional components. It clearly shows the simplicity in term of component count in contrast with the prior study including *S* and *D* in Fig. 4. The advantage leads to higher power density and lower cost in comparison. In a steady state, the sum of $P_c(t)$ and $P_m(t)$ should be P_o. $P_c(t)$ can, therefore, be derived as

$$\begin{aligned} P_c(t) &= P_o - P_m(t) \\ &= P_o - 2(1-k)P_o(\sin(\omega t))^2 \\ &= 2(1-k)P_o(\cos(\omega t))^2 + (2k-1)P_o. \end{aligned} \tag{10}$$

As $P_c(t)$ is generated by a unidirectional converter according to Fig. 5, $P_c(t) \geq 0$ must hold for all time. Thus

$$k \geq 0.5. \tag{11}$$

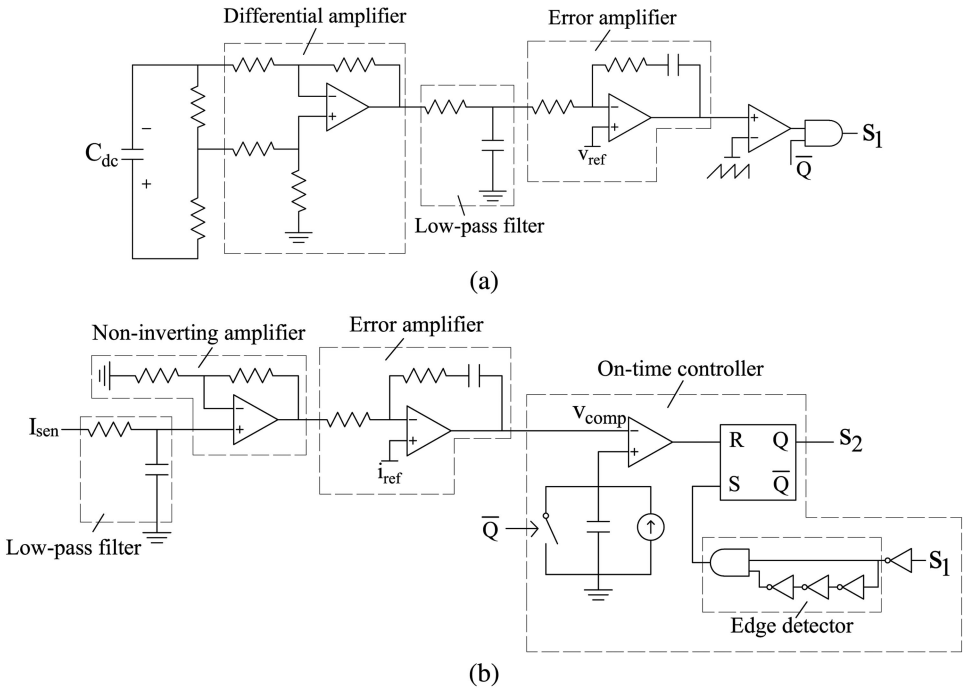

Fig. 10. Circuit diagram of the control circuit. (a) Control circuit to adjust D. (b) Control circuit to adjust $T_{\text{on}}(t)$.

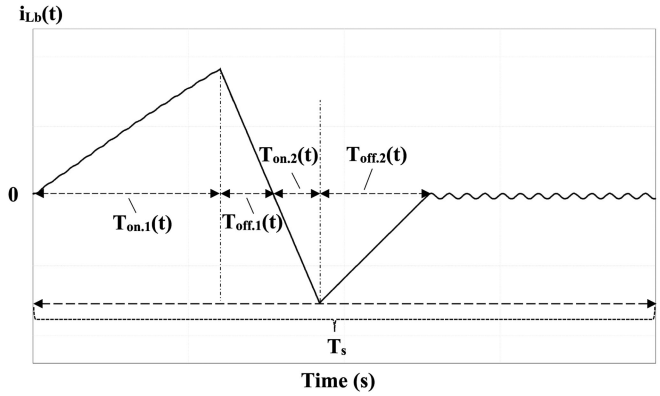

Fig. 11. Detailed waveform of $i_{Lb}(t)$ within one switching period.

The proposed power processing scheme is illustrated in Fig. 9 when k is selected to be 0.5. The sum of $P_c(t)$ and $P_m(t)$ produces the ideal dc to supply the LED loads. Another advantage becomes clear that the topology does not increase the requirement of the magnetic energy storage compared to the conventional single-stage buck–boost LED driver. In the conventional DCM buck–boost LED driver, the maximum magnetic energy storage requirement is $0.5L_mI_{pk}^2$, where L_m denotes the inductance of the buck–boost inductor and I_{pk} is the peak inductor current corresponding to the maximum input power. In the proposed topology, the analysis shows that the existing positive peak and negative peak of $i_{Lb}(t)$ correspond to the maximum values of $P_r(t)$ and $P_c(t)$, respectively. The maximum value of $P_r(t)$ is determined by

$$\max(P_r(t)) = 2kP_o \tag{12}$$

while the maximum value of $P_c(t)$ is

$$\begin{aligned}\max(P_c(t)) &= 2(1-k)P_o + (2k-1)P_o \\ &= P_o.\end{aligned} \tag{13}$$

Given the fact that k should be higher than 0.5, it can be concluded that

$$\max(P_r(t)) > \max(P_c(t)). \tag{14}$$

Rearranging (6), the positive peak of $i_{Lb}(t)$ can be calculated as

$$I_{pk.\text{positive}} = \sqrt{\frac{2\max(P_r(t))}{f_{\text{sw}}L_b}} \tag{15}$$

while the negative peak of $i_{Lb}(t)$ can be calculated as

$$I_{pk.\text{negative}} = \sqrt{\frac{2\max(P_c(t))}{f_{\text{sw}}L_b}}. \tag{16}$$

Thus, according to (14)–(16), we can conclude that

$$I_{pk.\text{positive}} = I_{pk}. \tag{17}$$

The positive peaks of i_{La} and i_{Lb} are the same and happen at the maximum input power like the conventional buck–boost converter in the DCM operation. Therefore, the maximum magnetic energy storage in the proposed driver is $0.5(L_a + L_b)I_{pk}^2$, which is exactly the same as the conventional buck–boost topology, while L_m is simply split into $(L_a + L_b)$.

Table I presents a direct comparison between the recently published LED drivers and the proposed LED driver in terms of the requirement of magnetic energy storage, reprocessed power, number of power semiconductors, and efficiency. The conventional single-stage buck–boost converter is taken as the

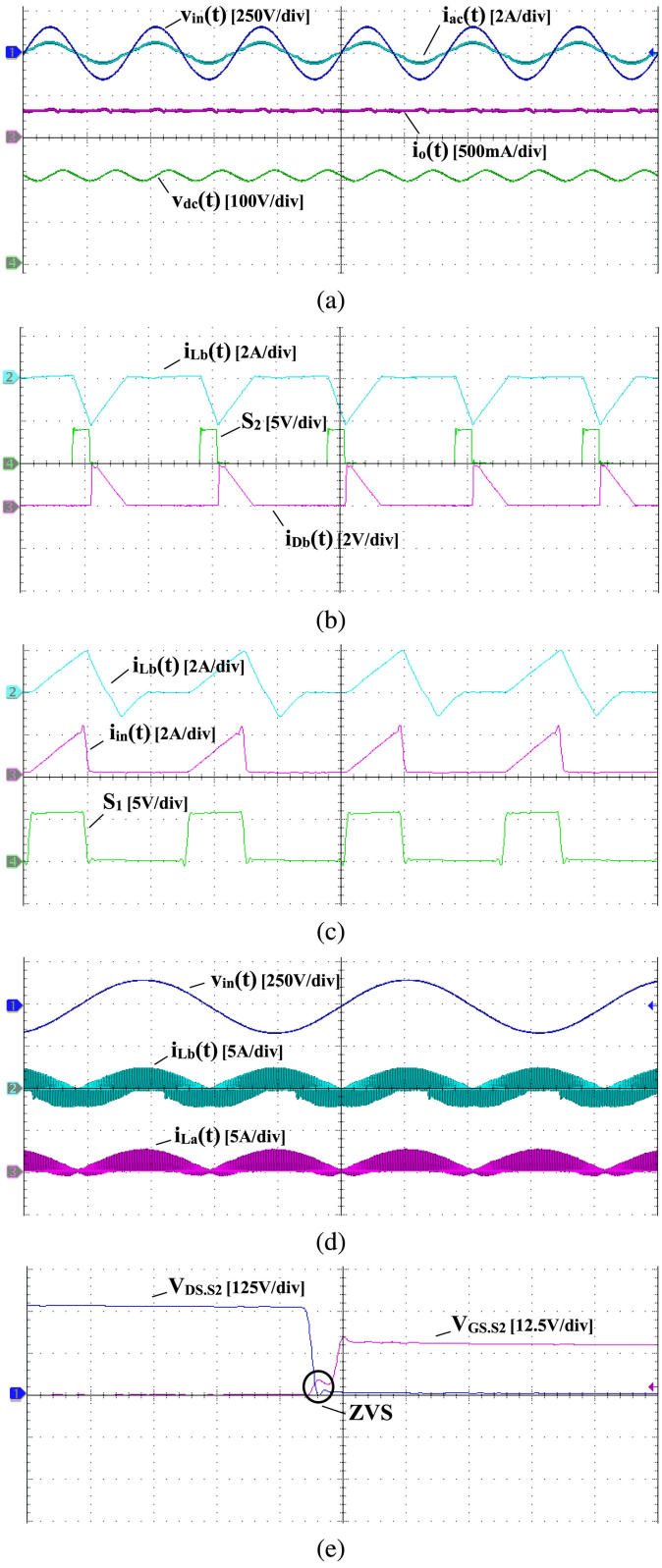

Fig. 12. Experimental waveforms. (a) Waveforms of the input voltage, the ac current, the output current, and the dc-link voltage. (b) Waveforms of $i_{Lb}(t)$, $i_{Db}(t)$, and the control signal for S_2 during the zero crossing of the input voltage. (c) Waveforms of $i_{Lb}(t)$, $i_{\text{in}}(t)$, and the control signal for S_1. (d) Overview of $v_{\text{in}}(t)$, $i_{Lb}(t)$, and $i_{La}(a)(t)$. (e) Drain–source voltage and gate–source voltage of S2 during the switching transient.

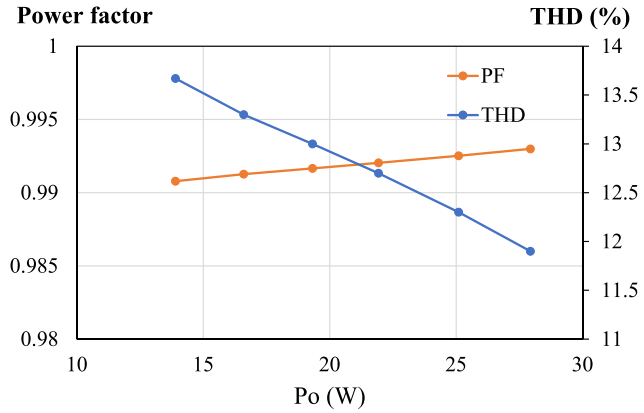

Fig. 13. THD and power factor of the proposed driver.

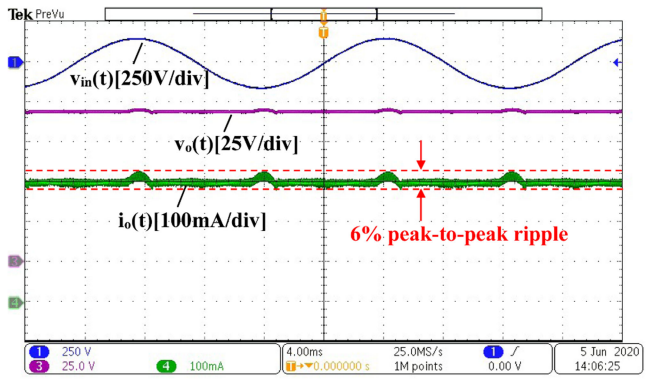

Fig. 14. Detailed waveforms of the output voltage and current.

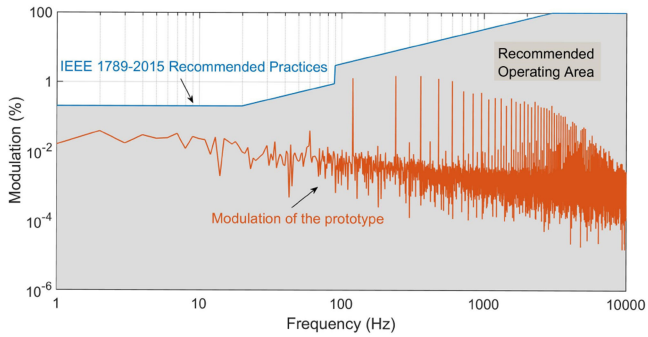

Fig. 15. Modulation of the proposed driver.

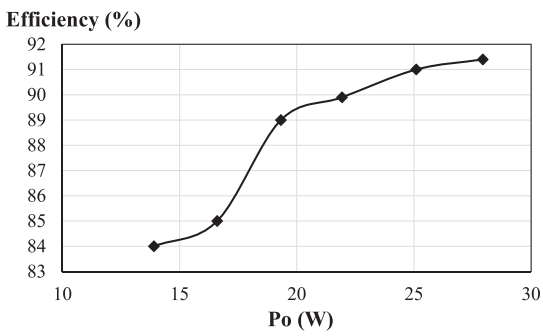

Fig. 16. Efficiency of the proposed driver.

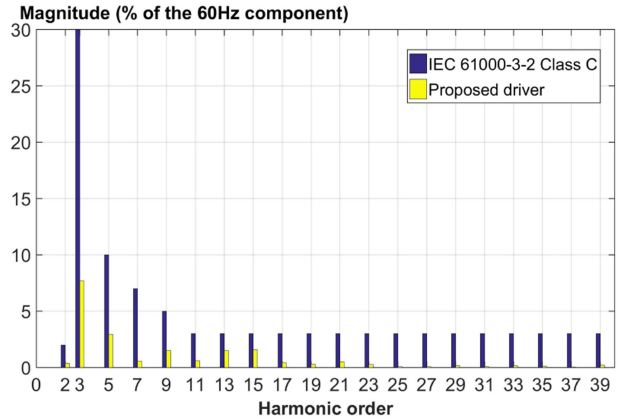

Fig. 17. Harmonic spectrum of the prototype at full power.

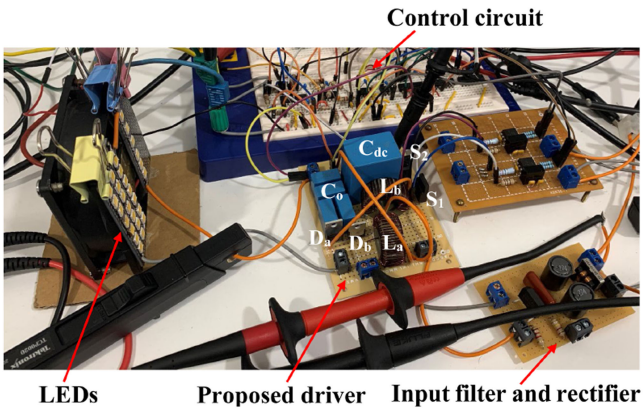

Fig. 18. Prototype and experimental setup.

benchmark for the comparison of the normalized magnetic energy storage requirement. It is shown that the proposed driver uses fewer switches and diodes and requires smaller size of inductors compared to the prior-art drivers, which leads to the potentials of higher efficiency, higher power density, and lower cost.

III. Design

The section includes the design process for the controlled modulation and circuit parameters.

A. Control Circuit Design

The automatic power decoupling control strategy concluded in [16] is adopted due to its simplicity and effectiveness. The proposed control circuit is shown in Fig. 10. D directly determines the input power. At a steady state, the input and output power should be balanced within each line period and the average value of $V_{\rm dc}(t)$, $V_{\rm DC}$, should be constant. Thus, D is taken as a control variable to maintain constant $V_{\rm DC}$. Fig. 10(a) is the control circuit to adjust D, in which $V_{\rm DC}$ is obtained through an *RC* filter and fed to an error amplifier. The error amplifier actively adjusts its output to track the reference voltage $V_{\rm ref}$. Finally, the PWM signal for S_1 is generated by comparing the output from the error amplifier with a sawtooth signal.

$T_{\rm on}(t)$ is controlled to maintain the constant output current. The control circuit to adjust $T_{\rm on}(t)$ is shown in Fig. 10(b), which contains the low-pass filter, noninverting amplifier, error amplifier, and ON-time controller. After the turn-OFF of S_1, the falling edge of S_1 is detected by the edge detector circuit and the output of the edge detector circuit will trigger an SR latch to turn ON S_2. $T_{\rm on}(t)$ is modulated by the ON-time controller, where higher $V_{\rm comp}$ indicates longer $T_{\rm on}(t)$. Therefore, the output current can be regulated via the error amplifier to actively adjust $V_{\rm comp}$.

B. Inductor Design

First, the ratio k should be chosen such that there is sufficient energy to create the desired $P_c(t)$ to cancel the ripple in $P_m(t)$. With reference to the Section II, k should be at least 0.5 to achieve the target. Considering power losses during the reprocessing state, k should be slightly higher than 0.5. Assuming the efficiency of the unidirectional dc/dc stage is η, the k should be chosen such that

$$\eta {\rm AVG}(P_r(t)) > {\rm AVG}(P_m(t)) \tag{18}$$

where the AVG$(\cdot)$ is the average operator over a line period. After solving the (18), we can get

$$k > \frac{1}{1+\eta}. \tag{19}$$

Second, the $(L_a + L_b)$ should be designed such that the converter maintains DCM operation. To maintain the DCM operation, the inductors should be fully discharged within every switching period. As shown in Fig. 11, the conduction period of L_b can be divided into four sections—$T_{\rm on.1}(t), T_{\rm off.1}(t), T_{\rm on.2}(t)$, and $T_{\rm off.1}(t)$, and they can be calculated as

$$\begin{cases} T_{\rm on.1}(t) = \dfrac{\sqrt{4(L_a+L_b)T_sP_o}}{V_{\rm in}} \\ T_{\rm off.1}(t) = \dfrac{k|\sin(\omega t)|\sqrt{4(L_a+L_b)T_sP_o}}{v_{dc}(t)} \\ T_{\rm on.2}(t) = \dfrac{\sqrt{4(1-k)L_bT_sP_o\cos^2(\omega t)+2(2k-1)L_bT_sP_o}}{v_{dc}(t)} \\ T_{\rm off.2} = \dfrac{\sqrt{4(1-k)L_bT_sP_o\cos^2(\omega t)+2(2k-1)L_bT_sP_o}}{v_o(t)}. \end{cases} \tag{20}$$

The maximum value of $(L_a + L_b)$ that allows the converter to work in DCM can be derived by solving the following inequality:

$$\max(T_{\rm on.1}(t) + T_{\rm off.1}(t) + T_{\rm on.2}(t) + T_{\rm off.2}(t)) \le T_S. \tag{21}$$

Considering disturbances in the grid voltage and the load variation, a safety margin should be included and the $(L_a + L_b)$ should be selected slightly lower than its maximum value.

IV. Verification

A 27-W prototype was built to verify the operation of the proposed topology. Table II summarizes the design parameters of the prototype. Fig. 12(a) shows the input current, the output current, and the buffer voltage of the prototype. The sinusoidal input current and constant output current are achieved as expected. Fig. 12(b) shows the waveforms measured around

TABLE I
COMPARISON OF RECENTLY PUBLISHED LED DRIVERS AND THE PROPOSED LED DRIVER

	[6]	[7]	[8]	[14]	[15]	Proposed driver
Magnetic energy storage requirement (p.u.)	1.09	1	1.1	1.8	1.27	1
Percentage of reprocessed power	8%	32%	32%	64%	32%	50%
Number of switches	3	3	3	3	3	2
Number of diodes	3	3	3	1	3	2
Peak Efficiency	89.5%	83%	86%	88%	90%	91.5%
Power Rating	23W	15W	28W	33.6W	16W	27W

TABLE II
DESIGN PARAMETERS OF THE 27-W PROTOTYPE

Parameters	Values
Input voltage,$v_{in}(t)$	110V RMS AC
Line frequency	60Hz
Output capacitor, C_o	3.3μF 200V
Buffer capacitor, C_{dc}	20μF 400V
Inductance of L_a	180μH
Inductance of L_b	220μH
Diodes (D_a and D_b)	IDH06G65C5
Switches (S_1 and S_2)	IPA60R280CFD7
LEDs	CLN6A-MKW
Output current	0.3A
Output voltage	90V
Switching frequency	50kHz

the zero crossing of the input voltage and it shows that i_{Lb} is charged reversely when S_2 is turned ON and the energy stored in L_b is later released through D_b when S_2 is turned OFF, which complies with the theoretical analysis. Fig. 12(c) shows that L_a and L_b are charged simultaneously when S_1 is turned ON and the driver works in DCM. An overview of i_{La} and i_{Lb} is shown in Fig. 12(d). The ZVS turn-ON of S_2 is verified in Fig. 12(e), where the drain–source voltage decreases to zero before the gate signal rises up.

The power factor and THD of the prototype at different output power are measured and shown in Fig. 13. The waveforms of output voltage and current are shown in Fig. 14. It shows that the peak-to-peak current ripple is measured to be 6% of the averaged value. The modulation of the driver is shown in Fig. 15 to demonstrate the compliance with IEEE recommended practices. The efficiency with respect to the output power is shown in Fig. 16. It is shown that the proposed topology can achieve 91% peak efficiency at the full power. Fig. 17 shows the harmonic spectrum of the input current and the low-order harmonics are well controlled under the limits of the international standard, IEC 61000-3-2 Class C. Finally, a photograph of the experiment setup is shown in Fig. 18.

V. CONCLUSION

The article presents a new solution of the reduced power processing LED driver that requires fewer switches and smaller magnetics in comparison with other recently published architectures. Through a split and shared inductor, the proposed topology successfully adds active buffering and reduces power processing without extra magnetic component compared to the conventional single-stage approach. The experimental results show that the proposed driver achieves high power factor, high efficiency, and constant output current. It also shows the advantage of the simple analog control circuits, which can be fully integrated in the future. The proposed topology simplifies the driver circuit and neglects the usage of electrolytic capacitors projecting for a long service lifetime.

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