Robust Control of Interconnected Power Electronic Converters to Enhance Performance in DC Distribution Systems: A Case of Study

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***Abstract*—This article presents the design and evaluation of robust controllers, based on linear programming, Kharitonov's theorem and Chebyshev's theorem, in order to enhance the performance of a typical structure of multistage converters present in direct current (dc) systems. In such electric power distribution systems, point-of-load converters act as a constant power load (CPL), which introduces a destabilizing nonlinear effects to their supply bus voltage. The multistage converter system uses a simplified scheme based on a cascaded converter, which is comprised of two dc–dc buck converters in a series connection. The robust controllers evaluated overcome the negative incremental impedance instability problem due to CPL, which causes a high risk of instability in interconnected converters. Thereby, the robust controllers evaluated ensure robust control performance and stability with a minor performance degradation compared to a conventional controller when the cascaded converter system is subjected to parametric uncertainties. The control methodologies evaluated are applied in both dc–dc buck converters. Assessments on the performance of the control methodologies evaluated are conducted. Experimental validations on a 160-W dc–dc cascaded converter system test board are carried out to verify the theoretical claims.**

***Index Terms*—Buck converter, cascaded converter system, constant power load (CPL), dc distribution system, dc–dc converter, robust control.**

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I. Introduction

NOWADAYS, dc–dc switched power converters are growing up attention in several studies, due to the increase of use of such systems for power interfacing in several types of renewable energy sources, e.g., solar photovoltaic [1], [2], wind turbine [2], biomass [3], hydropower [4], and others, constituting the called dc microgrid (MG). Hence, research on dc MGs have become an attractive alternative to integrate more efficiency and suite better various renewable energy sources with energy storage systems [5], [6], where power electronic converters are the main power processing units for interfacing the sources, which facilitates connection to the conventional power system [7].

Thereby, the stability conditions and performance of this type of converter is extensively investigated, aiming at ensuring the high quality in conversion and high performance when the MGs are subject to uncertainties (structured or nonstructured) due to measurements, electrical variables, unmodeled dynamics, and others [8], [9]. However, cascaded converters are not fully investigated in dc distribution systems in comparison with parallel converters, which present lower flexibility, great thermal and electrical stress in static switches[10]. In addition, when cascaded converters are used, effects related to the mathematical model are neglected due to the tolerance of electronic components (resistors, inductors, and capacitors) and parametric uncertainties (load and input voltage variations). Moreover, cascaded systems have important control dynamics to be addressed with control strategies in order to ensure robust stability and robust performance, simultaneously, when cascade converters system are subjected to a uncertainty variation, e.g., input voltage variation or variation in resistive or electronic loads connected to dc bus. Electronic loads behave as constant power load (CPL), producing an instantaneous power variation to a feeder converter, acting with negative resistance behavior [7], [11], [12].

According to [13]–[17], a dc MG can be described as a set of energy supply elements connected to loads through a common dc bus. Energy can be generated by several forms, such as renewable source or traditional generation that can be operated either in grid-connected mode or islanded mode. In [18] and [19], an overview about the several issues, such as design, control, stability, operation and protection of dc distribution systems, is

discussed. In addition, research works in [14] and [20] presented a review of practical stability criteria applied on the dc MGs that addressed design techniques of the parameters of the system.

Research works presented in [10], [12], [14], [15], and [20] discussed about the stability problems in MGs with CPL connected into the common dc bus, investigating and purposing ways to stabilize these systems. In [12], the stabilization of the CPL by using input filters is investigated; in order to design the filter, a modified loop shape technique was used, including damping desired information in the design process, so that the filter is able to handle CPL. This technique is validated for both simulation and hardware-in-loop, where the experimental tests showed that the proposed methodology can properly stabilize the system when connected to a CPL. Notice that this CPL behavior is caused by the induction motor. In [15], a predictive control technique is applied in a dc MG system to improve dynamic stabilization of the dc MG that supplies a converter that operates as a CPL. Thus, The main results showed that the proposed methodology can correct quickly these oscillations. However, the CPL is developed by an uninterruptible power system inverter device as a particular example of a CPL. In [14] and [20], an overview and review of the stabilization and control techniques applied in the dc MG, as well as architectures of the power converters were investigated. In particular, several architectures of dc MGs were presented, with a review of several techniques to stabilize the MG.

According to [21], the stability conditions of the dc MG supplying a CPL are investigated, where to design the control technique, the eigenvalues analysis was used, and the domain of attraction near equilibrium is also obtained using the quadratic Lyapunov function; however, only simulations are performed to assess the performance of the proposed methodology. In [22], a comparative study of control schemes for MG stabilization with a CPL is addressed; then, some techniques to mitigate unwanted oscillations by the CPL were discussed. Moreover, the benefits and drawbacks of each methodology as well as several recommendations to ensure stability and to maintain the performance of the system were presented. According to the state-of-art investigated, there is a lack of experimental research of robust control strategies to stabilize dc MGs.

Since dc MGs are discussed and analyzed as a solution for dc distribution systems, which are generally composed of multiple stages of power converters [16], [17], to contribute in this research area, this article presents the application of robust control approaches into the power electronic converters that compose a structure generally present in dc distribution systems. The aim of this article is to enhance the system performance, in addition to ensuring robust stability, to overcome the instability problems caused by a CPL and the dynamic interactions of power converters.

The main contributions of this article are briefly summarized as follows.

1) It provides practical tools to enhance robustness of fixed-order controllers, incorporating converter parameter uncertainties, such as components (resistors, inductors, and capacitors) tolerances, input voltage variations, and load variations in the controller design process.

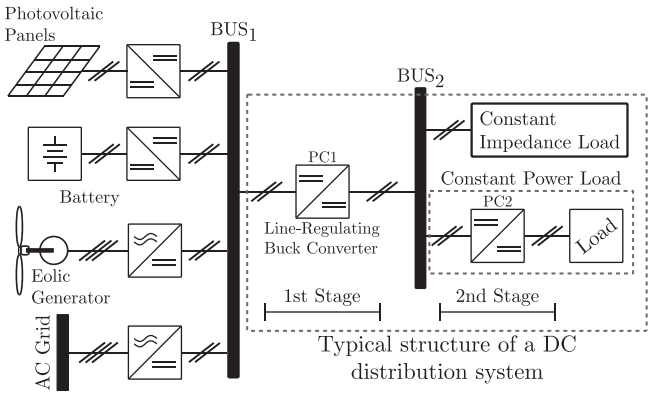

Fig. 1. Simplified dc distribution system.

2) These techniques can be extended for a hybrid control structure when nonlinear systems are transformed into linear systems to overcome system uncertainties, external disturbances, and measurement noises.
3) It introduces a comprehensive point of view about the complexity for designing the robust controllers addressed and how the constraints and type of solution involved in the control design problem influence in the robustness of controllers.

A 160-W prototype is fabricated and experimentally evaluated. Detailed analysis of the large-signal stability analysis based on the nonlinear model of converter, the design of control methodologies, and the experimental results comparing the different control strategies addressed are reported herein.

The remainder of this article is organized as follows. Section II introduces the system description and problem formulation, addressing the nonlinear analysis of the interconnected power converter. Section III presents a brief review about the robust control methodologies addressed in this article. The experimental results are discussed in Section IV. Finally, Section V concludes the article.

II. System Description and Problem Formulation

DC distribution systems usually consist of multistage power converters to provide the integration of a variety of load and sources in order to achieve proper system operation [23]. Such systems are known as cascaded power electronic converters that employ tightly regulated point-of-load (POL) dc–dc converters for power conditioning and voltage regulation [7]. POL dc–dc converters behave as a CPL due to regulation capability. This kind of load is nonlinear and introduces undesired oscillations in the dc-bus voltage that may degrade the stability margin or even destabilize the cascaded system even though, each stage is well designed for a stand-alone operation [7], [11], [23]

Fig. 1 presents a typical structure present in dc distribution systems. In the first stage, a buck converter (PC1) feeds a dc bus (BUS_2), which is connected to loads, whereas the second stage (PC2) transforms the intermediate bus voltage (BUS_2) to tightly regulate outputs for a load. The authors are aware that this is a simplified model. However, it provides the basis to analyze

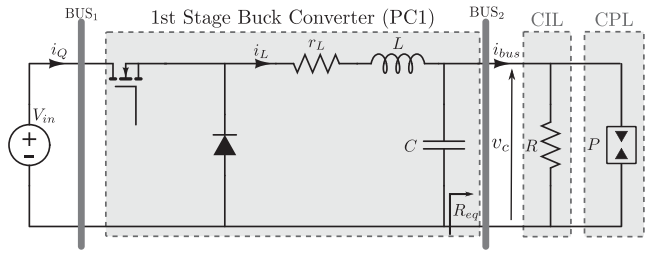

Fig. 2. Simplified structure of the dc distribution system under study.

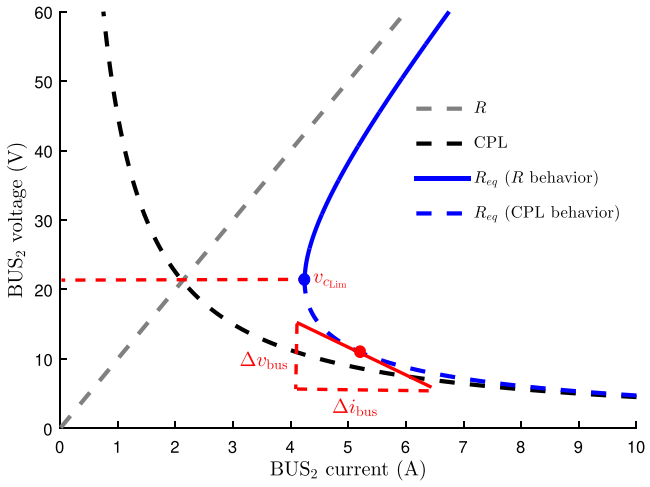

Fig. 3. Equivalent load (R_{eq}) for the simplified structure of the dc distribution system under study.

the large-signal stability of multistage converters found in dc distribution systems [16], [17].

Since the typical dc distribution systems have a cascaded converter architecture, power electronic converters with POL regulation behave as a CPL due to their regulation capability. Thereby, the dynamic behavior of the buck converter at the first stage can be studied using the model shown in Fig. 2, where R and P represent the constant impedance load (CIL) and CPL, respectively. Note that the CIL means any kind of load that the impedance does not change with the voltage or current magnitude variation.

A. Equivalent Load

From the simplified model of the dc distribution, the BUS_2 current (i_{bus}) and equivalent load (R_{eq}) are given by

$$i_{\text{bus}} = \underbrace{\frac{v_c}{R}}_{i_{\text{CIL}}} + \underbrace{\frac{P}{v_c}}_{i_{\text{CPL}}} \text{ and } R_{\text{eq}} = \frac{v_c}{i_{\text{bus}}} \tag{1}$$

where v_c is the capacitor voltage, and i_{CIL} and i_{CPL} represent the currents across CIL and CPL, respectively.

Fig. 3 presents the i–v characteristic of each type of load, which are obtained according to (1) with $R = 10\,\Omega$ and $P = 45$ W.

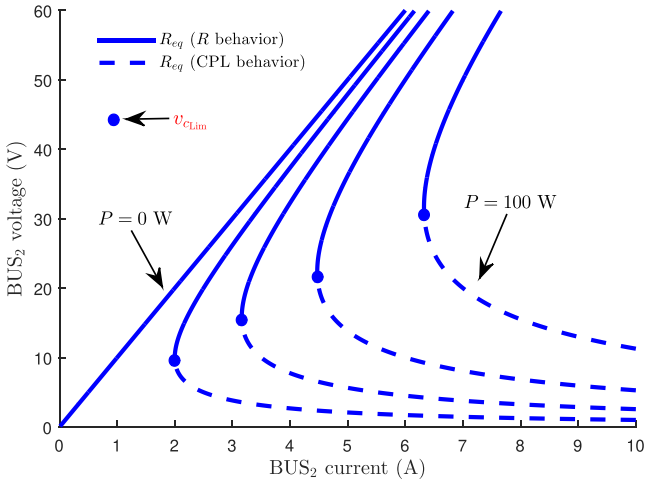

Fig. 4. Equivalent load curves for varying P and R fixed (10 Ω).

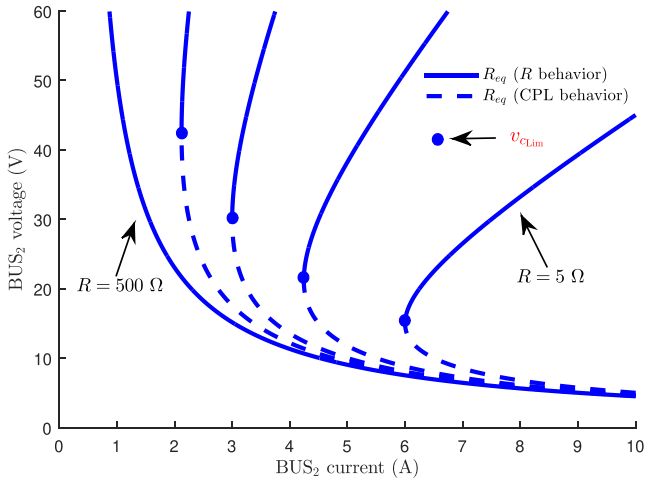

Fig. 5. Equivalent load curves for varying R and P fixed (45 W).

The incremental impedance of the resistive load is always positive ($\Delta v/\Delta i > 0$), i.e., current increases when voltage increases and vice versa. Although the instantaneous value of CPL impedance is positive ($v/i > 0$), the incremental impedance is always negative ($\Delta v/\Delta i < 0$). Due to the appearance of any disturbance, this negative incremental impedance has a negative impact on the power quality of the multistage converter systems leading to instability or voltage collapse. The equivalent load seen from PC1 [c.f. Fig. 2 and (1)] is highly nonlinear with the behavior dependent on the value of v_c, as shown in Fig. 3 (blue lines). Under the dc-bus capacitor voltage limit $v_{c_{\text{Lim}}} = \sqrt{\text{PR}}$, the equivalent load behaves as a CPL, whereas above this limit, it has a similar behavior as a resistive load.

Since the nonlinear behavior of the equivalent load depends on the operation conditions of CIL and CPL, any variation of their operating points (resistance load variation ΔR or power variation ΔP) yields to new dynamic behaviors of the equivalent load. Thus, Figs. 4 and 5 show the equivalent load when one type of load is kept constant and the other varies.

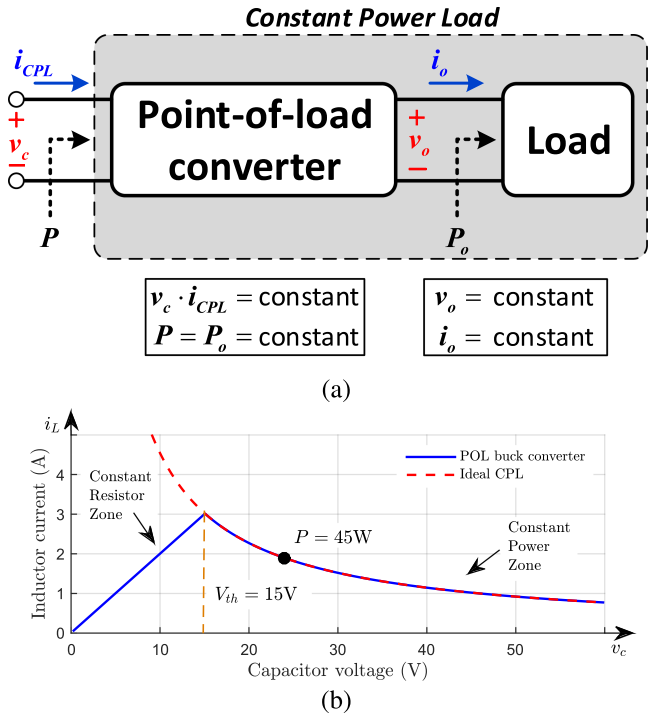

Fig. 6. (a) Block diagram of a POL converter and its input/output voltages and currents. (b) Constant power behavior of a buck converter (24–15 V) feeding a 5-Ω resistive load.

An increase in CPL power leads to an increase in $v_{c_{\text{Limit}}}$ without affecting the shape, but it shifts the curve to an upper right position (cf., Fig. 4). On the other hand, An increase in CIL power, i.e., decrease in R, reduces both $v_{c_{\text{Limit}}}$ and the positive incremental impedance (cf., Fig. 5). Therefore, the equivalent load has a piecewise defined characteristic dependent on the POL operation, assuming both CPL and CIL characteristics. The aforementioned dynamic characteristic of the equivalent load must be taken into account during the design of a robust controller with respect to load variations.

B. POL Buck Converter

The POL buck converter exhibits the important characteristic of almost-perfect regulation at the output terminals independent of the input perturbations [24], as illustrated in Fig. 6(a). Thus, the output power of the POL converter is constant and in turn the input power is almost constant. It is assumed that the output power of the POL converter is equal to the input power $P = P_o$.

There are two major differences between an ideal CPL and a POL buck converter. The first one occurs when the input voltage (v_c) is less or equal than the voltage threshold (V_{th}), which is the designed output voltage v_o of the buck converter with control loop. At this situation, the controller saturates the duty cycle, causing the switching component to remain closed; consequently, the POL converter becomes a resistive load, losing its CPL characteristic, dividing the equivalent system in two regions as illustrated in Fig. 6(b), which was experimentally validated in [25]. Therefore, the voltage–current characteristics of a POL buck converter is represented mathematically as a piecewise function (1) [23], [24]

$$\xi(v_c) = \begin{cases} \frac{P}{v_c}, & \text{if } v_c > V_{\text{th}} \\ \frac{P}{V_{\text{th}}^2} v_c, & \text{if } v_c \leq V_{\text{th}}. \end{cases} \tag{2}$$

The second difference occurs at high frequencies. An ideal CPL respond equally to every frequency, whereas the POL buck converter is only able to respond to frequencies within the closed-loop bandwidth; consequently, the POL buck converter bandwidth must be sufficiently high to make the consumed power independent of the intermediate dc BUS_2 voltage variation [7], [23].

C. Stability Analysis of the Simplified DC Distribution System

The simplified dc distribution system (cf., Fig. 2) is used to perform the large-signal stability analysis of the PC1 with CIL and CPL. Thus, the dynamic behavior of a dc–dc buck converter feeding a CIL and a CPL can be represented as

$$L\frac{di_L}{dt} = uV_{\text{in}} - v_c - r_L i_L \tag{3}$$

$$C\frac{dv_c}{dt} = i_L - \frac{v_c}{R} - \xi(v_c) \tag{4}$$

where v_c and i_L are the instantaneous capacitor voltage and the instantaneous inductor current, respectively, $\xi(v_c)$ is a piecewise function that represents the POL buck converter at the second stage (cf., Fig. 1), V_{in} is assumed as the BUS_1 voltage, R is the resistive load (CIL), P is the CPL, r_L is the equivalent series resistor of the inductor, and u is the switching function.

The aim is to perform a large-signal stability analysis, thus, it is considered that the switching function assumes only the values $u \in \{0, 1\}$, representing the states of the switching device opened (OFF) and closed (ON), respectively. Besides, the analysis of the boundary controller considers the dynamics of each switch state as the basis to the design process. Therefore, for each switch state, a dynamic analysis is presented for the state-space variables $x = \{i_L, v_c\}$ with $i_L > 0$ and $v_c > 0$. Unless indicated otherwise the PC1 buck converter parameters used in this article are $V_{\text{in}} = 50$ V, $C = 2200\,\mu$F, $L = 2.5$ mH, $r_L = 1\,\Omega$, and $V_{\text{th}} = 15$ V [cf., Fig. 6(b)].

It is well-known that a buck converter may operate in two different conduction modes, continuous conduction mode (CCM) and discontinuous conduction mode, depending on the instantaneous value of inductor current. In CCM, the buck converter operates with nonnull inductor current at any time. Thereby, in this article, the dynamic analysis only focuses on CCM.

From the dynamical point of view, it is important to know the location and the type of equilibrium points for both switching states ($u = 0$ and $u = 1$). These equilibrium points are the intersection of the nullclines of the state-space variables (3) and (4) given by

$$n_1 : \; i_L - \frac{v_c}{R} - \xi(v_c) = 0 \tag{5}$$

$$n_2 : \; uV_{\text{in}} - v_c - r_L i_L = 0. \tag{6}$$

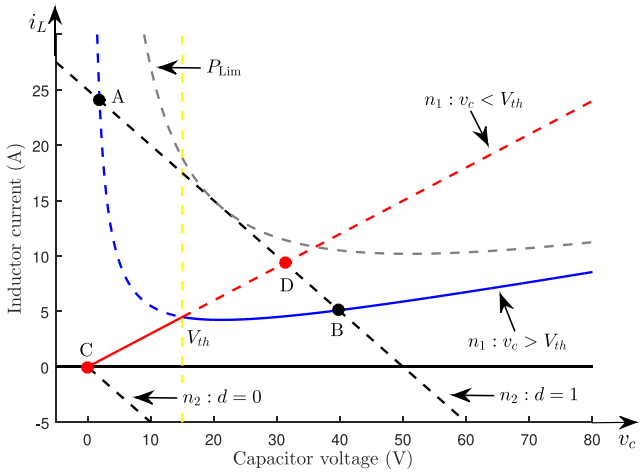

Fig. 7. Nullclines of the simplified dc distribution system and the equilibrium points. Additionally, the CPL power limit (P_{Lim}) curve is introduced.

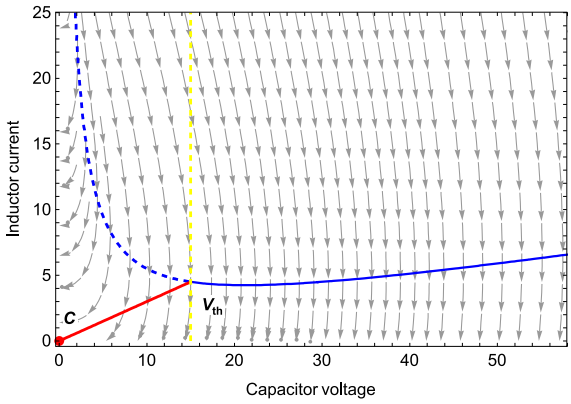

Fig. 8. Phase portrait and nullclines when the switch is OFF ($r_L = 2\,\Omega$, $P = 45$ W, $R = 10\,\Omega$) showing the convergence to equilibrium **C**.

Fig. 7 shows the nullclines of the simplified dc distribution system, the equilibrium points, and the CPL power limit (P_{Lim}) curve.

Figs. 8 and 9 show the phase portrait for both switching states $u = 0$ and $u = 1$, respectively.

When the switching device is OFF ($u = 0$), there is an intersection of the nullclines n_1 and n_2 at the origin (cf., Fig. 7). Moreover, Fig. 7 shows a possible equilibrium point D, which may be calculated using piecewise function $\xi(v_c)$ and the nullclines n_1 and n_2

$$(v_{c_{\text{C}}}, i_{L_{\text{C}}}) = (0, 0) \tag{7}$$

$$v_{c_{\text{D}}} = \frac{V_{\text{in}}}{1 + r_L\left(\frac{1}{R} + \frac{P}{V_{\text{th}}^2}\right)} \tag{8}$$

$$i_{L_{\text{D}}} = v_{c_{\text{D}}}\left(\frac{1}{R} + \frac{P}{V_{\text{th}}^2}\right). \tag{9}$$

On the other hand, when the switching device is ON ($u = 1$), n_2 is shifted V_{in} units to the right and some equilibrium points may appear (cf., Fig. 7). Thereby, using the nullclines n_1 and n_2, the necessary condition (10) must be respected to the emergence

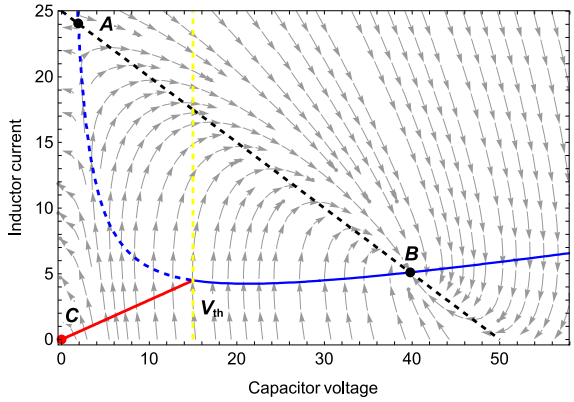

Fig. 9. Phase portrait and nullclines when the switch is ON ($r_L = 2\,\Omega$, $P = 45$ W, $R = 10\,\Omega$) showing the convergence to equilibrium **B**. The high value of r_L is shown to make easier to visualize the **A** equilibrium point.

of equilibrium points

$$P < \frac{V_{\text{in}}^2}{4r_L\left(1 + \frac{r_L}{R}\right)} = P_{\text{Lim}} \tag{10}$$

as shown in Fig. 7.

If $P = P_{\text{Lim}}$, a *saddle-node bifurcation of equilibria* occurs; and if $P < P_{\text{Lim}}$, two equilibrium points emerge at $(v_{c_{\text{A}}}, i_{L_{\text{A}}})$ and $(v_{c_{\text{B}}}, i_{L_{\text{B}}})$

$$v_{c_{\text{A,B}}} = \frac{V_{\text{in}} \pm \sqrt{V_{\text{in}}^2 - 4r_L P\left(1 + \frac{r_L}{R}\right)}}{2\left(1 + \frac{r_L}{R}\right)} \tag{11}$$

$$i_{L_{\text{A,B}}} = \frac{v_{c_{\text{A,B}}}}{R} + \frac{P}{v_{c_{\text{A,B}}}}. \tag{12}$$

Regarding the piecewise characteristic of the system, if the following statements hold:

1) if $V_{\text{th}} < v_{c_{\text{A}}}$, A, B, and D are real;
2) if $v_{c_{\text{A}}} < V_{\text{th}} < v_{c_{\text{B}}}$, B is real and, B and D are virtual (nonadmissible);
3) if $v_{c_{\text{B}}} < V_{\text{th}}$, D is real and, A and B are virtual.

The stability of these equilibrium points are analyzed from the Jacobian matrix J of the corresponding linearized system

$$\text{J} = \begin{bmatrix} -\frac{1}{C}\left(\frac{1}{R} + \dot{\xi}(v_c)\right) & \frac{1}{C} \\ -\frac{1}{L} & -\frac{r_L}{L} \end{bmatrix} \tag{13}$$

where $\dot{\xi}(v_c)$ is the first derivative of ξ with respect to v_c. Therefore, from the trace and determinant of J, we can conclude the following.

1) The **C** equilibrium point is always a stable nodal sink.
2) The **A** equilibrium point is always a saddle point. However, this article addresses the real load profile of a POL buck converter instead of an ideal CPL, thus, there is no separatrix caused by A as mentioned in [11] and [17]; hence, no voltage collapse may occur.
3) The **B** equilibrium point is a stable for

$$P \leq \frac{V_{\text{in}}^2}{\frac{\left(CRr_L^2 + L(R+2r_L)\right)^2}{LR(L+CRr_L)}}, \qquad \text{if } C \leq \frac{L}{r_L^2} \tag{14}$$

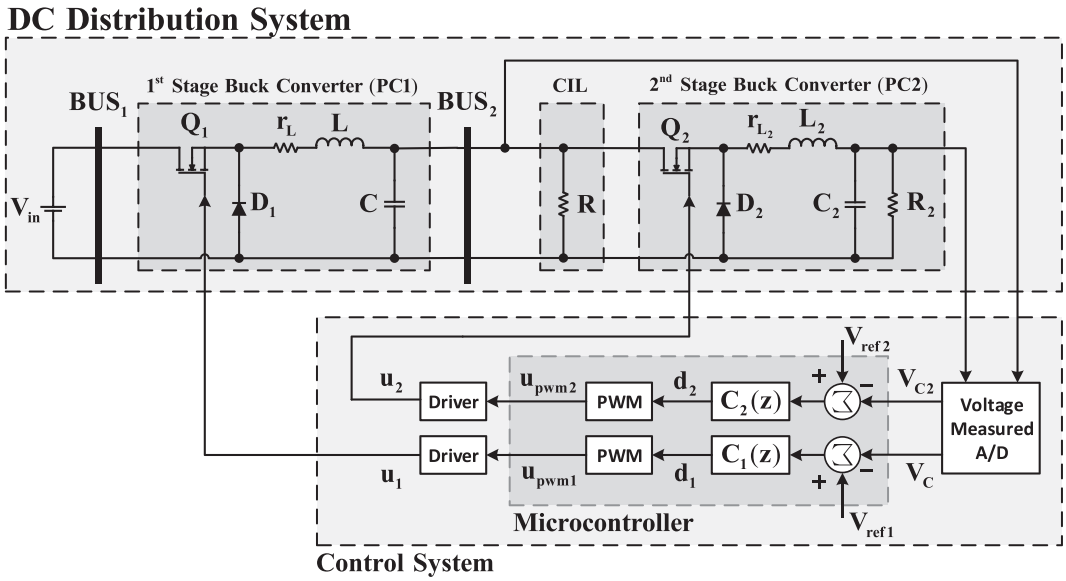

Fig. 10. Control system for the two cascaded power converters.

or

$$P < P_{\mathrm{Lim}}, \qquad \text{if } C > \frac{L}{r_L^2} \tag{15}$$

and unstable for

$$\frac{V_{\mathrm{in}}^2}{\frac{\left(CRr_L^2+L(R+2r_L)\right)^2}{LR(L+CRr_L)}} < P < P_{\mathrm{Lim}}, \text{ if } C < \frac{L}{r_L^2}. \tag{16}$$

In the transition of the two cases occurs a *Hopf bifurcation* that gives rise to a limit cycle surrounding the unstable equilibrium point.

III. Control System for the DC Distribution System

This section introduces the robust controller design for both power electronic converters of the first (PC1) and second (PC2) stages, respectively, as shown in Fig. 10.

A. Modeling of Buck Converters of the First and Second Stages

The large-signal behavior of PC1 in CCM is represented by (3) and (4). Using the state-space averaging technique, this dynamic can be written as

$$\begin{cases} L\frac{di_L}{dt} = d_1 v_{\mathrm{in}} - v_c - r_L i_L \\ C\frac{dv_c}{dt} = i_L - \frac{1}{R}v_c - \frac{P}{v_c} \end{cases} \tag{17}$$

where d_1 represents the duty cycle that controls the pulsewidth modulation (PWM) gate drive of PC1.

On the other hand, the dynamic of a buck converter with a resistive load is well-known, thus, (18) represents the large-signal behavior of PC2 in CCM

$$\begin{cases} L_2\frac{di_{L_2}}{dt} = d_2 v_c - v_{c_2} - r_{L_2} i_{L_2} \\ C_2\frac{dv_{c_2}}{dt} = i_{L_2} - \frac{1}{R_2}v_{c_2} \end{cases} \tag{18}$$

where d_2 represents the duty cycle that controls the PWM gate drive of PC1 and v_{c_1} is the input voltage of the PC1.

The large-signal model does have nonlinear terms arising from the product of two time varying quantities. We can linearize the model by expanding about the operating point and removing second order terms. Thereby, let us assume the time-varying variables are equal to some given (dc) quiescent values, plus superimposed small ac variations as

$$\begin{cases} v_{\mathrm{in}} = \mathrm{V_{in}} + \tilde{v}_{\mathrm{in}} \\ d_1 = \mathrm{D}_1 + \tilde{d}_1 \\ i_L = \mathrm{I_L} + \tilde{i}_L \\ v_c = \mathrm{V_C} + \tilde{v}_c \end{cases} \text{ and } \begin{cases} v_c = \mathrm{V_c} + \tilde{v}_c \\ d_2 = \mathrm{D}_2 + \tilde{d}_2 \\ i_{L_2} = \mathrm{I_{L_2}} + \tilde{i}_{L_2} \\ v_{c_2} = \mathrm{V_{c_2}} + \tilde{v}_{c_2} \end{cases} \tag{19}$$

where $\tilde{v}_{\mathrm{in}}$, $\tilde{d}_1$, $\tilde{i}_L$, $\tilde{v}_c$, $\tilde{d}_2$, $\tilde{i}_{L_2}$, and $\tilde{v}_{c_2}$ represent the small-signal values, and $\mathrm{V_{in}}, \mathrm{D}_1, \mathrm{I_L}, \mathrm{V_c}, \mathrm{D}_2, \mathrm{I_{L_2}}, \mathrm{V_{c_2}}$ represent the dc values, i.e., the operating points.

The perturbation yields the linear small-signal state-space equations in (19) and the following equation:

$$\begin{cases} L\frac{d\tilde{i}_L}{dt} = \mathrm{V_{in}}\tilde{d}_1 + \mathrm{D}_1\tilde{v}_{\mathrm{in}} - \tilde{v}_c - r_L\tilde{i}_L \\ C\frac{d\tilde{v}_c}{dt} = \tilde{i}_L - \frac{1}{R_L}\tilde{v}_c \end{cases} \tag{20}$$

$$\begin{cases} L_2\frac{d\tilde{i}_{L_2}}{dt} = \mathrm{V_c}\tilde{d}_2 + \mathrm{D}_2\tilde{v}_{c_1} - \tilde{v}_{c_2} - r_{L_2}\tilde{i}_{L_2} \\ C_2\frac{d\tilde{v}_{c_2}}{dt} = \tilde{i}_{L_2} - \frac{1}{R_2}\tilde{v}_{c_2} \end{cases} \tag{21}$$

with

$$R_L = R_1 || R_{\mathrm{CPL}},\ R_{\mathrm{CPL}} = -\frac{\mathrm{V_c}^2}{P}. \tag{22}$$

Note that at given operating point, a CPL (PC2) can be approximated by a negative resistance.

Hence, the duty cycle-to-output voltage transfer function for both PC1 and PC2 can be obtained from the following equations:

$$G_{vd_1}(s) = \left.\frac{\tilde{v}_c(s)}{\tilde{d}_1(s)}\right|_{\tilde{v}_{\rm in}(s)=0}, G_{vd_2}(s) = \left.\frac{\tilde{v}_{c_2}(s)}{\tilde{d}_2(s)}\right|_{\tilde{v}_c(s)=0}$$

$$G_{vd_1}(s) = \frac{\frac{\rm V_{in}}{LC}}{s^2 + \left(\frac{1}{R_L C} + \frac{r_L}{L}\right)s + \left(\frac{1}{LC} + \frac{r_L}{R_L LC}\right)} \quad (23)$$

$$G_{vd_2}(s) = \frac{\frac{\rm V_c}{L_2 C_2}}{s^2 + \left(\frac{1}{R_2 C_2} + \frac{r_{L_2}}{L_2}\right)s + \left(\frac{1}{L_2 C_2} + \frac{r_{L_2}}{R_2 L_2 C_2}\right)}. \quad (24)$$

B. Robust Controller Design

Since the dynamics of power converter change due to variations of their loads, the equilibrium points are, in general, uncertain. In fact, the loads that the power converters feed are unknown. Thus, it is a common procedure to linearize the system about the operating point of interest and design a linear control. However, generally in the classic controller design, it neglects the effect of the load variation and the uncertainties of converter components, which may lead to performance degradation. Aiming to ensure robustness and minimize transient responses under parametric uncertainties (load and input voltage variations), robust controllers, based on robust parametric approaches, are design and applied in the power converters PC1 and PC2 (cf., Fig. 10).

The main advantage of the robust control approaches, addressed in this article, is that allows to take into account from the outset in the controller design process a prior knowledge about the possible range assumed for the values of system's physical parameters, incorporating available information about components' (resistors, inductors, and capacitors) tolerances or defined by designer.

The design procedure of the robust voltage controllers is performed by using a voltage proportional-integral-derivative (PID) controllers. $C_1(s)$ regulates the dc $\rm BUS_2$ voltage and $C_2(s)$ control the POL regulation of PC2 (cf., Fig 10). Note that $C_1(s)$ and $C_2(s)$ are single-input and single-output (SISO) controllers, i.e., they are decoupled and each one is tuned depending on the model of each subsystem (PC1 and PC2)

$$C_1(s) = \frac{K_d s^2 + K_p s + K_i}{s} \quad (25)$$

$$C_2(s) = \frac{K_{d_2} s^2 + K_{p_2} s + K_{i_2}}{s}. \quad (26)$$

In order to design robust controllers, a region of uncertainty is previously defined. In this context, the uncertainties are defined by CPL power variation (ΔP), resistance loads variations (ΔR and $\Delta \rm R_2$), input voltages variations ($\Delta \rm V_{in}$ and $\Delta \rm V_c$), and variation of equivalent series resistor of the inductors L and L_2 ($\Delta \rm r_L$ and $\Delta \rm r_{L_2}$)

$$\Delta \rm P = [P^{min}, P^{max}]$$
$$\Delta \rm R = [R^{min}, R^{max}]$$
$$\Delta \rm R_2 = [R_2^{min}, R_2^{max}]$$
$$\Delta \rm V_{in} = [V_{in}^{min}, V_{in}^{max}]$$
$$\Delta \rm V_c = [V_c^{min}, V_c^{max}]$$
$$\Delta \rm r_L = [r_L^{min}, r_L^{max}]$$
$$\Delta \rm R_2 = [r_{L_2}^{min}, r_{L_2}^{max}]. \quad (27)$$

Thereby, these uncertainties build a box region in the plant parameters, as a result, the duty cycle-to-output voltage transfer functions (23) and (24) become in interval plants

$$G_{vd_1}(s) = \frac{\frac{\Delta \rm V_{in}}{LC}}{s^2 + \left(\frac{1}{\Delta \rm R_L C} + \frac{\Delta \rm r_L}{L}\right)s + \left(\frac{1}{LC} + \frac{\Delta \rm r_L}{\Delta \rm R_L LC}\right)} \quad (28)$$

$$G_{vd_2}(s) = \frac{\frac{\Delta \rm V_c}{L_2 C_2}}{s^2 + \left(\frac{1}{\Delta \rm R_2 C_2} + \frac{\Delta \rm r_{L_2}}{L_2}\right)s + \left(\frac{1}{L_2 C_2} + \frac{\Delta \rm r_{L_2}}{\Delta \rm R_2 L_2 C_2}\right)}. \quad (29)$$

Note that $\Delta \rm R_L$ is calculated from (22) and given by

$$\Delta \rm R_L = \Delta R_1 || \Delta R_{CPL},\ R_{CPL} = -\frac{V_c{}^2}{\Delta P}.$$

For simplification, the interval duty cycle-to-output voltage transfer functions presented in (28) and (29) can be represented as follows:

$$G_{vd_1}(s) = \frac{[b_0]}{s^2 + [a_1]s + [a_0]} \quad (30)$$

$$G_{vd_2}(s) = \frac{[n_0]}{s^2 + [m_1]s + [m_0]} \quad (31)$$

where

$$[a_1] = \left(\frac{1}{\Delta \rm R_L C} + \frac{\Delta \rm r_L}{L}\right),\ [m_1] = \left(\frac{1}{\Delta \rm R_2 C_2} + \frac{\Delta \rm r_{L_2}}{L_2}\right)$$
$$[a_0] = \left(\frac{1}{LC} + \frac{\Delta \rm r_L}{\Delta \rm R_L LC}\right),\ [m_0] = \left(\frac{1}{L_2 C_2} + \frac{\Delta \rm r_{L_2}}{\Delta \rm R_2 L_2 C_2}\right)$$
$$[b_0] = \frac{\Delta \rm V_{in}}{LC},\ [n_0] = \frac{\Delta \rm V_c}{L_2 C_2}.$$

Since G_{vd_1} and G_{vd_2} are interval plant, their corresponding closed-loop characteristic polynomial will be closed-loop characteristic interval polynomials given by

$$\Phi(s) = [\Delta^{\rm min}, \Delta^{\rm max}] = s^3 + [\gamma_2]s^2 + [\gamma_1]s + [\gamma_0] \quad (32)$$

$$\Phi_2(s) = [\Delta_2^{\rm min}, \Delta_2^{\rm max}] = s^3 + [\delta_2]s^2 + [\delta_1]s + [\delta_0] \quad (33)$$

where

$$[\gamma_0] = [b_0]K_i,\ [\delta_0] = [n_0]K_{i_2}$$
$$[\gamma_1] = [a_0] + [b_0]K_p,\ [\delta_1] = [m_0] + [n_0]K_{p_2}$$
$$[\gamma_2] = [a_1] + [b_0]K_d,\ [\delta_3] = [m_1] + [n_0]K_{d_2}.$$

Assuming that the desired dynamic of the closed-loop system for PC1 and PC2 are represented by (32) and (33), respectively

$$\Delta_d(s) = (s+\alpha)(s^2 + 2\xi\omega_n s + \omega_n^2)$$
$$\Delta_d(s) = s^3 + \phi_2 s^2 + \phi_1 s + \phi_0 \quad (34)$$

$$\Delta_{d_2}(s) = (s+\beta)(s^2 + 2\xi_2\omega_{n_2}s + \omega_{n_2}^2)$$
$$\Delta_{d_2}(s) = s^3 + \varphi_2 s^2 + \varphi_1 s + \varphi_0. \tag{35}$$

Note that an auxiliary pole must be added in order to not affect the desired dynamics of the system.

In order to tune the controllers, the closed-loop polynomial parameters (32) and (33) are compared with the desired closed-loop polynomial (34) and (35), which represent the desired dynamics. This problem can be written in its matrix format, presenting the following relationship (34)

$$\underbrace{\begin{bmatrix}[b_0] & 0 & 0\\ 0 & [b_0] & 0\\ 0 & 0 & [b_0]\end{bmatrix}}_{A_1}\underbrace{\begin{bmatrix}K_d\\ K_p\\ K_i\end{bmatrix}}_{X_1} = \underbrace{\begin{bmatrix}\phi_2 - [a_2]\\ \phi_1 - [a_1]\\ \phi_0\end{bmatrix}}_{B_1} \tag{36}$$

$$\underbrace{\begin{bmatrix}[n_0] & 0 & 0\\ 0 & [n_0] & 0\\ 0 & 0 & [n_0]\end{bmatrix}}_{A_2}\underbrace{\begin{bmatrix}K_{d_2}\\ K_{p_2}\\ K_{i_2}\end{bmatrix}}_{X_2} = \underbrace{\begin{bmatrix}\varphi_2 - [m_2]\\ \varphi_1 - [m_1]\\ \varphi_0\end{bmatrix}}_{B_2} \tag{37}$$

When the system is subject to parametric uncertainties, the controller performance may deteriorate. Therefore, the controller must guarantee robust performance within an acceptable region of closed-loop parameters variation, so that the closed-loop poles are located in a certain region. Thereby, a desired region is defined as follows:

$$\Delta_d := \{\phi_i^{\min} \le \phi_i \le \phi_i^{\max}\} \tag{38}$$

$$\Delta_{d_2} := \{\varphi_i^{\min} \le \varphi_i \le \varphi_i^{\max}\}. \tag{39}$$

Therefore, according to [9], [7], and[11], it is possible to formulate a linear inequalities set (40) and (41), as shown at the bottom of this page, which restricted the controller and desired polynomial coefficients in the predefined intervals, as shown (34) and (35).

Thus, (40) and (41) can be rewritten as

$$B_1(\phi^{\min}) \le A_1 X_1 \le B_1(\phi^{\max}) \tag{42}$$

$$B_2(\varphi^{\min}) \le A_2 X_2 \le B_2(\varphi^{\max}). \tag{43}$$

The robust controller design problem is summarized in the choice of X_1 and X_2 (if possible) to satisfy the set of inequalities (40) and (41).

The solution of this problem can be idealized, as a solution to a linear programming problem, therefore different techniques can be used to solve it. However, its standard solution is sometimes efficient and fast, so that this problem can be rewritten as a problem of local minimization, subject to restrictions.

According to [8] and [9], the aforementioned robust performance control design problem for the pre-established conditions can be rewritten as the following optimization problem:

$$X_1 = \arg\left(\min f(X_1)\right)$$
$$\text{s.t.} \begin{bmatrix}A_1\\ -A_1\end{bmatrix} X_1 \le \begin{bmatrix}B_1(\phi^{\max})\\ -B_1(\phi^{\min})\end{bmatrix} \tag{44}$$

$$X_2 = \arg\left(\min f(X_2)\right)$$
$$\text{s.t.} \begin{bmatrix}A_2\\ -A_2\end{bmatrix} X_2 \le \begin{bmatrix}B_2(\varphi^{\max})\\ -B_2(\varphi^{\min})\end{bmatrix} \tag{45}$$

where $f(.)$ is a linear cost function that must be built and minimized according to the control goals. In this article, the cost function $f(.)$ has been chosen to be the sum of the elements of vector of the controller parameters X_1 and X_2, such as suggested in [8] and [9].

On the other hand, according to Lucas *et al.* [7], the optimization problem for the pre-established conditions can be rewritten as a problem of local minimization, subject to following restrictions:

$$X_{a_1} = \arg\left(\min f(X_{a_1})\right)$$
$$\text{s.t.} \begin{bmatrix}A_{a_1}\\ -A_{a_1}\end{bmatrix} X_{a_1} \le \begin{bmatrix}B_1(\phi^{\max})\\ -B_1(\phi^{\min})\\ 0\end{bmatrix} \tag{46}$$

$$X_{a_2} = \arg\left(\min f(X_{a_2})\right)$$
$$\text{s.t.} \begin{bmatrix}A_{a_2}\\ -A_{a_2}\end{bmatrix} X_{a_2} \le \begin{bmatrix}B(\varphi^{\max})\\ -B(\varphi^{\min})\\ 0\end{bmatrix} \tag{47}$$

with

$$X_{a_1} = \begin{bmatrix}X_1\\ R_{c_1}\end{bmatrix}, A_{a_1} = \begin{bmatrix}A_1 & \|a_1\|_2\\ -A_1 & \|a_1\|_2\\ 0_{1\times 3} & -1\end{bmatrix}$$

$$X_{a_2} = \begin{bmatrix}X_2\\ R_{c_2}\end{bmatrix}, A_{a_2} = \begin{bmatrix}A_2 & \|a_2\|_2\\ -A_2 & \|a_2\|_2\\ 0_{1\times 3} & -1\end{bmatrix}$$

where $\|a_{(.)}\|_2$ is the Euclidian norm of coefficients of $A_{(.)}$, the cost function is defined as the sum of controller gains within the radio $R_{(.)}$, and the parameter vector $X_{a_{(.)}}$ contains the controller gains and the radio of the largest ball of Chebyshev theorem, which is contained in the polytope with the larger uncertainty of the systems.

Then, the feasible solution, for each of the cases, is used to set the control structures defined in (25) and (26). In order to obtain the discrete equivalent of the designed controller, the Tustin method is used to perform the discrete approximation.

$$\begin{bmatrix}\phi_2^{\min} - [a_2]\\ \phi_1^{\min} - [a_1]\\ \phi_0^{\min}\end{bmatrix} \le \begin{bmatrix}[b_0] & 0 & 0\\ 0 & [b_0] & 0\\ 0 & 0 & [b_0]\end{bmatrix}\begin{bmatrix}K_d\\ K_p\\ K_i\end{bmatrix} \le \begin{bmatrix}\phi_2^{\max} - [a_2]\\ \phi_1^{\max} - [a_1]\\ \phi_0^{\max}\end{bmatrix} \tag{40}$$

$$\begin{bmatrix}\varphi_2^{\min} - [m_2]\\ \varphi_1^{\min} - [m_1]\\ \varphi_0^{\min}\end{bmatrix} \le \begin{bmatrix}[n_0] & 0 & 0\\ 0 & [n_0] & 0\\ 0 & 0 & [n_0]\end{bmatrix}\begin{bmatrix}K_{d_2}\\ K_{p_2}\\ K_{i_2}\end{bmatrix} \le \begin{bmatrix}\varphi_2^{\max} - [m_2]\\ \varphi_1^{\max} - [m_1]\\ \varphi_0^{\max}\end{bmatrix} \tag{41}$$

TABLE I
CONVERTER SPECIFICATIONS

Symbol	Parameter	Value
	PC1	
V_{in}	dc BUS_1 voltage	50 V
V_c	dc BUS_2	24 V
f_{s1}	Switching frequency	5 kHz
P_1	Output power	160 W
	PC2	
V_{in}	dc BUS_2 voltage	24 V
V_{c_2}	Point-of-Load Regulation	15 V
f_{s2}	Switching frequency	10 kHz
P_2	Output power	45 W

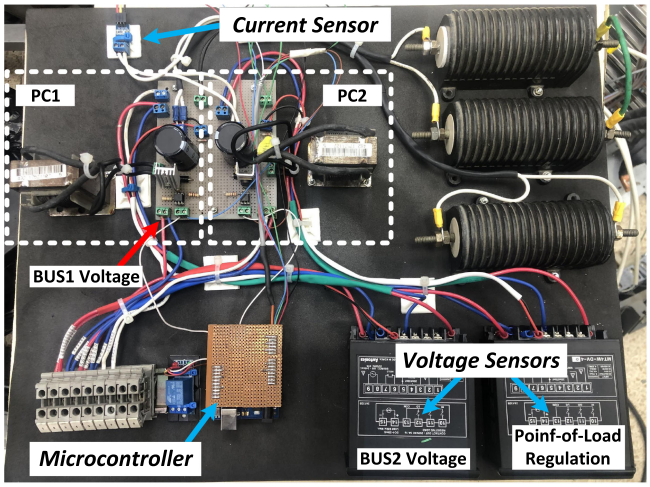

Fig. 11. Photograph of the implemented laboratory prototype.

TABLE II
MAIN COMPONENT LIST

Mosfets (Q_1 and Q_2)	IRF9540N (Infineon)
Diodes (D_1 and D_2)	UF5406 (Vishay)
Capacitors (C and C_2)	2200μF - 100 V (Antel)
Inductance of Inductor (L and L_2)	2.5mH ($r_L = r_{L_2} = 50m\Omega$)
Resistive Loads	$R = 10\Omega$, $R_2 = 5\Omega$
Optocoupler	4n25 (Vishay)
Voltage Sensors	MT4W-DV-4O (Autonics)
Current Sensor	ACS712 (Allegro)
PWM Controller	AT91SAM3X8E (Microchip)

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness and robustness of the aforementioned robust control methodologies, a prototype with the specifications in Table I and photograph in Fig. 11, was designed, implemented, and tested. It is worth to mention that in this setup is also compared to a classical control methodology based on a pole-placement approach. Table II summarizes the components employed in the setup of the laboratory prototype. Table III shows the lower and upper limits for each parameter to define a hyperbox region of uncertainties in order to design robust controllers considering parametric uncertainties.

TABLE III
UNCERTAINTIES CONSIDERED

Symbol	Nominal	Min	Max
P	45 W	25 W	100 W
R	10 Ω	5 Ω	15 Ω
R_2	5 Ω	2.5 Ω	7.5 Ω
V_{in}	50 V	40 V	60 V
V_c	24 V	18 V	30 V
r_L	50 mΩ	48.5 mΩ	52.5 mΩ
r_{L_2}	50 mΩ	48.5 mΩ	52.5 mΩ

TABLE IV
VALUES OF PARAMETERS FOR THE DESIGNED CONTROLLERS

Controller Gains	K_p	K_i	K_d
	PC1		
Classical Control	0.019193	6.593599	$3.598881e^{-5}$
B-Robust Control	0.010353	8.145317	$3.908687e^{-5}$
K-Robust Control	0.018929	8.145317	$4.660043e^{-5}$
	PC2		
Classical Control	0.034890	70.86413	$3.779969e^{-4}$
B-Robust Control	0.016934	90.72151	$3.481663e^{-4}$
K-Robust Control	0.306752	90.72150	$5.713145e^{-4}$

For the following experimental tests, it is important to mention that the resistive loads (R and R_2) are considered fixed. Thus, to cause a disturbance into the dc BUS_2 voltage V_c, a CPL power variation is performed changing the POL regulation V_{c_2} of PC2. Thereby, the voltage threshold V_{th} changes depending on the power consumption of PC2. According to the analysis carried out in Section II, an increase in CPL power leads to a change of the equilibrium points, which causes degradation in the system performance. Moreover, variations in the dc BUS_1 voltage (V_{in}) are also considered.

Two SISO controllers are used to regulate the outputs for each subsystem (PC1 and PC2), dc BUS_2 voltage V_c, and POL regulation V_{c_2}. Then, the control law for each subsystem is implemented in a microcontroller (cf., Figs. 10 and 11). The controller gains are tuned considering the uncertainties described in Table III and setting the following requirements: settling time $t_{set_1} \leq 200$ ms and damping factor $\xi \geq 0.69$ for PC1 and settling time $t_{set_2} \leq 50$ ms and damping factor $\xi_2 \geq 0.69$ for PC2.

By introducing the box region of uncertainties into the desired performance region and solving the linear goal programming problem given in (42)–(45), the robust controllers are tuned according to [7], [8], and [11]. The classical controller is based on a classical pole-placement control technique using the nominal values of Table III. Table IV summarizes each controller gains for the designed controllers. Hereinafter, the robust controllers obtained by (44) and (45) will be referred as *B-robust control* and by (46) and (47) as *K-robust control*.

The next subsections present and discuss the stability analysis of the simplified dc distribution system and the main results for CPL power variation (change of POL regulation of PC2) and dc BUS_1 voltage, respectively, aiming at evaluating the

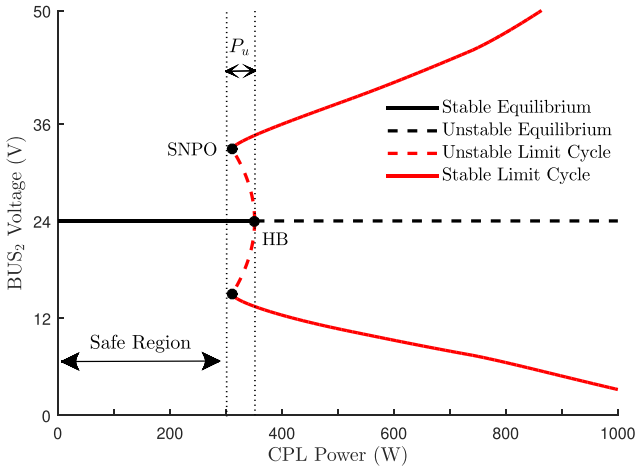

Fig. 12. Bifurcation diagram of the dc distribution system $P \times V_{\text{bus}_2}$.

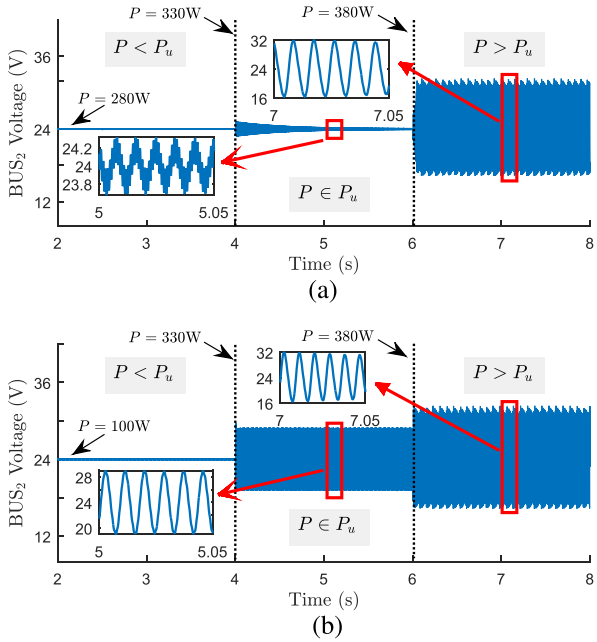

Fig. 13. V_{bus_2} time response of the simulated dc distribution system under three different CPLs (P). (a) Stable case inside P_u region. (b) Unstable case inside P_u region.

performance of the dc distribution system under the three control strategies (classical control, B-robust control, and K-robust control).

A. *Bifurcation Analysis*

The linear stability analysis is only valid for small deviations around the operating point. Furthermore, it is not able to predict the global behavior of the system, which helps to define a safe operating region. Thereby, in order to analyze the BUS$_2$ voltage stability, a bifurcation analysis [16] is performed for the dc distribution system in closed-loop under CPL power variation. A bifurcation diagram of the BUS$_2$ voltage as a function of the P parameter is illustrated in Fig. 12. Note that P is the CPL power. The diagram is built through the numerical continuation method using the POL converter model (2)–(4).

Two bifurcations and three main regions appear in the bifurcation diagram (cf., Fig. 12). The main dynamic behaviors in time domain of V_{bus_2} relative to these regions are presented in Fig. 13. The saddle-node bifurcation of periodic orbits (SNPO) occurs due to the passive region (constant resistor zone) present in the POL buck converter (cf., Fig. 6), which give rise to the simultaneously appearance of a stable limit cycle (stable oscillations) and an unstable limit cycle (unstable oscillations). When the value of P increases from this point, the amplitude of the stable limit cycle increases and the amplitude of unstable limit cycle decreases until collapses with the equilibrium point at HB in a so-called subcritical *Hopf bifurcation*, remaining after it only an unstable equilibrium point and an stable limit cycle around it.

Note that for values of P inside the P_u region, although the system is locally stable, it may become oscillatory when the BUS$_2$ voltage is disturbed and cross the unstable limit cycle. If this happens, the BUS$_2$ voltage is attracted by the stable limit cycle and starts to oscillate, as shown in Fig. 13(b). In contrast to Fig. 13(a) (P changes from 280 to 330 W), a large power variation (P changes from 100 to 330 W) is performed in Fig. 13(b) to enter in the P_u region, leading to voltage oscillation. Therefore, the safe region is composed of all the values of P located to the left of the SNPO bifurcation point. As a consequence of this analysis, the dc distribution system should be designed to operate in the safe region regardless the intermittent sources, since the power provided by them have a stabilizing effect. It is worth to mention that this article assumes that the balance of power between the source and the loads is always guaranteed. Therefore, the effect of the input power on system reliability is not a focus of this article.

B. *CPL Power Variation*

This experiment aims to evaluate the closed-loop performance of the simplified dc distribution system (cf., Figs. 10 and 11) under CPL power variation, i.e., variation in the desired POL regulation of PC2.

Fig. 14 shows the experimental results for positive variation of CPL power under the three control approaches. Initially, the system feeds only the CIL (R) for that reason the CPL power is zero until $t = 0.8$ s; at this time, PC2 is connected to the dc BUS$_2$ causing a disturbance in it. Then, the system reaches its steady state. After that ($t = 1.5$ s), a CPL power variation is performed from 45 to 100 W, as shown in Fig. 14. Fig. 15 shows the zoomed area near CPL power variation from 0 to 45 W and from 45 to 100 W.

The experimental results show that all controllers are able to achieve stable operation of the dc distribution system despite variations in CPL power. However, the impact in the dc BUS$_2$ voltage (sag voltage) caused by the connection or variation of its POL regulation (desired CPL power) of PC2 is less while is

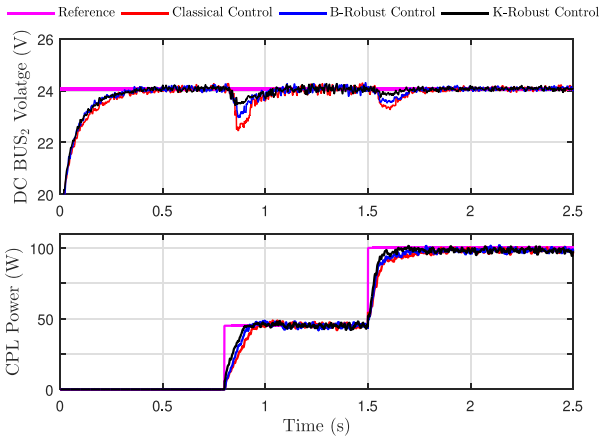

Fig. 14. Closed-loop system performance for positive CPL power variation.

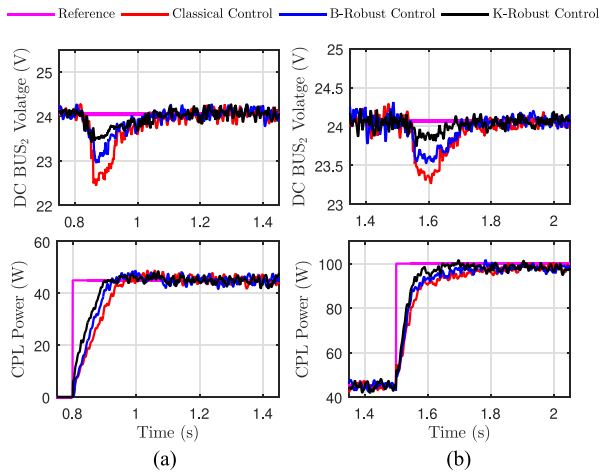

Fig. 15. Zoomed area near CPL power variation from 0 to 45 W and from 45 to 100 W.

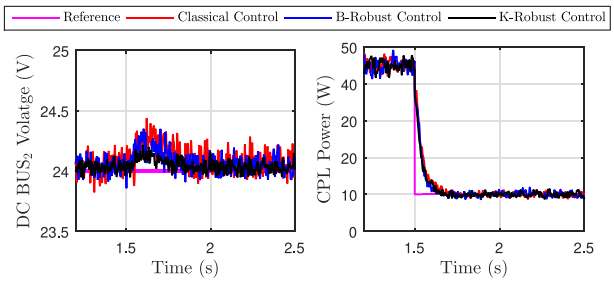

Fig. 16. Closed-loop system performance for negative CPL power variation.

regulated by K-robust control approach; in addition, the closed-loop performance of PC2 is also enhanced.

Fig. 16 shows the experimental results for a negative variation of CPL power. When the system is set to its nominal operating condition ($V_c = 24$ V, $P_2 = 45$ W, and $R = 10\,\Omega$, cf., Tables I and II), the system is subjected to a CPL power variation from 45 to 10 W.

The result demonstrates (cf., Fig. 16) that all controllers can compensate oscillations in the dc BUS_2 voltage ($\mathrm{V_c}$) and ensure system stability under negative CPL power variation.

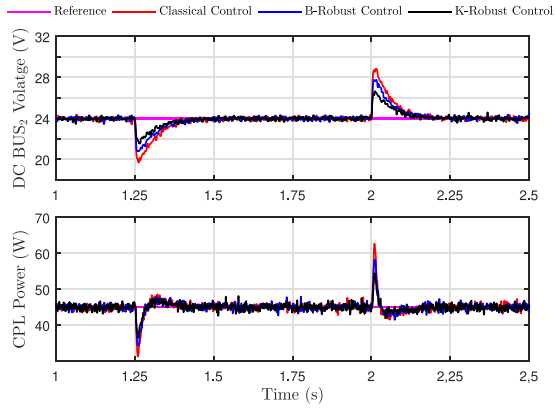

Fig. 17. Closed-loop system performance for dc BUS_1 voltage variation.

However, the closed-loop system performance is improved when is controlled by K-robust control approach.

C. DC BUS_1 Voltage Variation

This experiment evaluates the closed-loop performance of the simplified dc distribution system under dc BUS_1 voltage ($\mathrm{V_{in}}$) variation. When cascaded converter system is operating in its steady state ($V_c = 24$ V, $P_2 = 45$ W, and $R = 10\,\Omega$), the system is subjected to a dc BUS_1 voltage ($\mathrm{V_{in}}$) variation from 50 to 40 V at time $t = 1.25$ s. Then, another dc BUS_1 voltage variation is performed, returning to its initial condition ($\mathrm{V_{in}} = 50$ V) at time $t = 2$ s, as shown in Fig. 17.

Fig. 17 presents the experimental results of closed-loop system performance dc BUS_1 voltage ($\mathrm{V_{in}}$) variation.

The results show that a variation in the dc BUS_1 voltage causes disturbances in the POL regulation of the power electronic converters involved (PC1 and PC2) since the dynamical model depends on the input voltage of each converter. Thereby, oscillation effects (voltage sag and voltage swell) are introduced into the dc BUS_1 voltage ($\mathrm{V_{in}}$) and the CPL power (P_o) (cf., Fig. 17). The K-robust control outperforms the other control approaches due to the minimum voltage oscillation occurrence (voltage sag and voltage swell) in the dc BUS_2 voltage.

D. Final Discussion

The experimental results show that the robust control methodologies addressed in this article outperform the classical control methodology. This is because the classical control design neglects the effect of system uncertainties, such as load and input voltage variation; in addition, it uses nominal mathematical models, which naturally present errors. In contrast, the robust control methodologies take into account all possible uncertainties of the system from the outset in the controller design process. For that reason, the system performance degradation is greater for the classical control approach.

On the other hand, the K-robust control approach provides a better control performance in comparison with B-robust control. This is because K-robust control solves the LMI optimization problem by convex optimization using the linear programming approach, Kharitonov theorem, and Chebyshev theorem, which

allow constraints to be introduced into the polytope with the larger uncertainties in order to find a feasible solution.

Therefore, it can be claimed that the type of solution of the LMI problem (set of linear inequality constraints) may lead to find a control with better robustness. Hence, the constraints and type of solution involved in the control design problem are important to obtain the best controller.

Since this article adopts a fixed-order controller structure, the complexity to implement robust controllers depends on the robust control techniques, constraints, and the control objectives addressed to solve the optimization LMI problem. However, they are easy to implement due to the fixed-order structure, allowing the deployment of standard industry structures, such as PID and lead–lag.

In the particular case of robust controllers addressed in this article, there is no complexity in the control algorithm because they are based on linear programming approach to find a feasible solution in the set of linear inequality constraints.

On the other hand, robust control approaches can be extended for a hybrid control structure [24], [26], [27] when nonlinear systems are transformed into linear systems to provide robustness against parametric uncertainties, external disturbances, and measurement noises. Recently, Lucas *et al.* [24] performed a comparison between linear, robust, nonlinear, and nonlinear robust controllers in a cascaded converter system. The proposed design method in [24] is based on the combination of a feedback linearization control approach and a robust control approach. Results show that the proposed control approach [24] overcomes system uncertainties more effectively, reducing oscillation amplitude and faster transient response. Thus, it can be claimed that the use of robust control is an important tool to enhance the reliability and robustness of the power electronic converters.

V. Conclusion

In this article, we present the design and evaluation of robust control approaches for interconnected power converters in order to enhance performance in dc distribution system. Moreover, this article has discussed the typical CPL characteristic present in dc distribution systems due to multistage converter architecture. The destabilizing effect imposed by this kind of load, as the large-signal stability analysis of the feeder converter (PC1) dynamics is presented, showing that the system may be open loop unstable.

The robust controllers are applied in the power electronics converters, PC1 and PC2, in order to ensure system stability under CPL and BUS_1 voltage changes. The robust controllers are also compared with a classical controller based on pole-placement methodology.

All controllers were fully verified using 160-W laboratory prototype with two interconnected dc-dc buck converters in series connection. The K-robust control showed better dynamic behavior, such as minor overshoot and fast transient response. Thus, a K-robust controller more effectively compensates the oscillations (voltage sag and voltage swell) caused by CPL and dc BUS_1 voltage variations ensuring the desired performance.

Finally, a discussion about the controller performances is introduced. Thereby, the incorporation of available information about tolerance of converter components and system uncertainties in the controller design process, allows to obtain controllers with greater robustness. Therefore, robust control theory is suitable for the design of control systems for power electronic converters.

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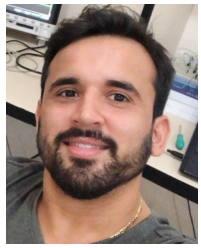

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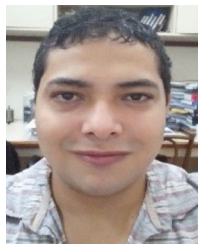

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