Power Loss Reduction in Buck Converter Based Active Power Decoupling Circuit

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***Abstract*—Active power decoupling (APD) circuits enable the use of long lifetime capacitors (film or ceramic capacitors) in single-phase power converters. Owing to the inclusion of the APD circuits, the literature reports 1.5%–1.8% drop in efficiency of single-phase converter at rated power. This reduction in conversion efficiency is one of the significant challenges in the practical use of APD circuits. This article proposes an approach to reduce the power loss in the bidirectional buck converter based APD circuit. This approach is presented with the help of analytical calculations and graphical representation of operation of APD circuit. The proposed approach requires rapid variation in the average voltage of the buffer capacitor with a change in inverter power. To achieve this, an enhanced control technique is suggested with a duty ratio injection controller. The steady state and transient response of the proposed control technique are validated with simulation and experimentation. Further, the reduction in power losses realized by the proposed approach is verified with the help of a developed laboratory prototype. The proposed approach obtains up to 1% improvement in efficiency of single-phase converter at rated power, when compared with existing APD approaches.**

***Index Terms*—Active power decoupling (APD), dc–ac converter, efficiency improvement, energy buffer, single phase.**

I. Introduction

In THE past few decades, single-phase ac–dc/dc–ac converters have found applications in every walk of life. In these converters, a large value of aluminum electrolytic capacitor (AEC) is used to support the instantaneous mismatch between power at dc port and ac port. A limited ripple current handling capability, low lifetime, and rapid wear at high temperatures impose limitations on the use of AECs [1]. The Google Little Box Challenge witnessed the elimination of AECs to improve power density of single-phase inverters [2], [3]. Various techniques to eliminate AECs from design of single-phase converters are discussed in literature [4]–[7]. The most popular technique is to decouple the voltage regulation and energy buffering requirements so that the value of capacitance required is reduced significantly [8]. This technique is called active power decoupling (APD). Wherein a buffer capacitor is used for energy buffering, along with an active circuit to control power flow between buffer capacitor and dc port.

The bidirectional buck converter based APD circuit requires simple control, low switch count, and a small value of buffer capacitor. Owing to these key advantages, a bidirectional buck converter based APD circuit is one of the most widely discussed topologies in literature [9]–[14]. In buck converter based APD circuit, voltage across the buffer capacitor comprises dc component and ripple component. The reference for the ripple voltage component is popularly generated with a feedback from dc-link voltage [10]–[13]. Further, dc voltage component of buffer capacitor voltage is controlled with the help of an open-loop duty ratio signal [10] or with the help of a low bandwidth voltage controller [11]. Usually, the dc voltage component is maintained at $\frac{1}{\sqrt{2}}$ times the dc-link voltage [11] or at half of the dc-link voltage [10]. Apart from the dc component of the buffer capacitor voltage, capacitor's value is also an important choice during design. In the absence of large value of capacitor connected at the dc port, buffer capacitor is bulk energy storage available in the system. Hence, designers select the value of buffer capacitor to achieve desired performance during rapid load changes.

In addition, power loss in APD circuit limits their usability in single-phase power converters. A drop in the conversion efficiency by 1.8% and 1.5% at rated power due to inclusion of APD circuit is reported in [9] and [10], respectively. A combination of AECs and APD circuit to improve conversion efficiency is presented in [14]. However, owing to the use of AECs, the design is not suitable for long lifetime applications. An approach for optimal design of APD circuits for given specifications is discussed in [11] and [15]. The conversion efficiency at rated power is considered for selection of optimal design. However, the discussion omits light load efficiency of single-phase power converters, which is also important [16]. To enhance efficiency under light load conditions, a partial power decoupling technique is discussed in [17]. A reduction in the power buffered by APD circuit is suggested for reducing power loss in the APD circuit. However, the tradeoff between the reduction in losses and increase in dc-link voltage ripple may not be acceptable in applications with stringent voltage ripple requirements. To reduce losses without increasing ripple in dc-link voltage, a soft switching technique is discussed in [18]. However, this approach requires wide variation in switching frequency and complex controller to maintain low conduction losses [19]. To improve efficiency with constant switching frequency operation, a peak

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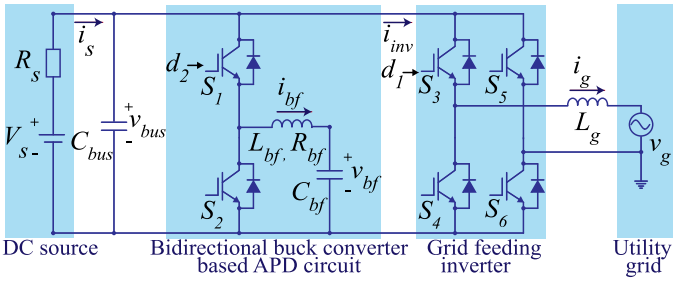

Fig. 1. Bidirectional buck converter based APD circuit with dc source and grid interfacing inverter.

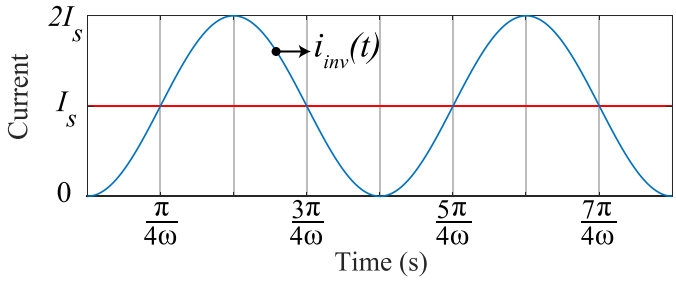

Fig. 2. Graphical representation of current drawn by inverter $i_{\text{inv}}(t)$.

voltage control technique is discussed in [20]. The peak voltage controller is employed to control the peak value of voltage across the buffer capacitor and improve conversion efficiency under light load conditions. Owing to the presence of a peak detector circuit with a sampling frequency of 100 Hz, the control bandwidth of the peak voltage controller is limited well below 100 Hz. Hence, during the change in load power, bandwidth limitation of peak voltage controller may lead to distortion in voltage waveforms. This problem is exacerbated in the presence of rapid changes in load power.

In light of the above discussion, this article proposes an approach to improve the efficiency of the bidirectional buck converter based APD circuit. The proposed approach reduces power loss in APD circuit under all loading conditions, without compromising on steady-state and transient performance. Moreover, it does not require additional circuit elements and operates with a constant switching frequency. First, the operating constraints of the APD circuit are analyzed and graphical representations for operating constraints are discussed. This is followed by a discussion on the power losses in the APD circuit and their relationship with the buffer capacitor voltage. Based on the aforementioned analysis, the proposed approach for power loss reduction is elaborated. The reduction in power loss is realized with the proposed reference generation and duty ratio injection controller. A brief discussion on stability assessment of the proposed control technique is also provided. Further, the impact of selection of parameters on the power loss in APD circuit is also presented. The controller performance and reduction in power losses are validated with the help of circuit simulations and hardware prototype.

The rest of the article is arranged as follows. The analysis of operating constraints and power losses in the APD circuit is carried out in Section II. Section III describes the proposed approach and control technique to implement minimum power loss operation. The simulation studies, experimental validation, and related discussions are included in Section IV. Finally, Section V concludes the article.

II. Analysis of Operating Constraints and Power Loss in APD Circuit

Fig. 1 shows the single-phase grid feeding inverter topology with bidirectional buck converter based APD circuit. The operating constraints on the buffer capacitor voltage in the APD circuit are derived in Section II-A. Further, the relationship between power loss and the buffer capacitor voltage is discussed in Section II-B. Based on the conclusions drawn in this section, an enhanced approach to determine the buffer capacitor voltage with reduced power loss is proposed in the next section.

A. Analysis of Operating Constraints for APD Circuit

There are three operating constraints for the satisfactory operation of a buck converter based APD circuit. Two of them, which are based on fundamental operation of buck converter, are stated as follows.

Cons-1: The output voltage of the buck converter is positive. Hence, the peak-to-peak voltage ripple ΔV_{bf} across buffer capacitor should always be less than twice of its average voltage $2V_{bf}$ ($\Delta V_{bf} < 2V_{bf}$).

Cons-2: In a buck converter, output voltage is less than input voltage. Hence, the sum of $2V_{bf}$ and ΔV_{bf} should be less than twice of dc-link voltage $2V_{\text{bus}}$ ($2V_{bf} + \Delta V_{bf} < 2\ V_{\text{bus}}$).

The third operating constraint for APD circuit is derived as follows. The instantaneous power injected into the grid $p_g(t)$ by the single-phase inverter operating at unity power factor is given by

$$p_g(t) = \frac{V_g I_g}{2} - \frac{V_g I_g}{2}\cos(2\omega t) \tag{1}$$

where V_g is the peak value of grid voltage and I_g is the peak value of grid current. The angular frequency of the grid is given by ω. The dc-link voltage V_{bus} is assumed to be ripple free. By neglecting the switching frequency components, the current $i_{\text{inv}}(t)$ drawn by an ideal inverter is given by

$$i_{\text{inv}}(t) = \frac{p_g(t)}{V_{\text{bus}}} = \frac{V_g I_g}{2V_{\text{bus}}} - \frac{V_g I_g}{2V_{\text{bus}}}\cos(2\omega t). \tag{2}$$

The above equation is rewritten as

$$i_{\text{inv}}(t) = I_s - I_s\cos(2\omega t) \tag{3}$$

where I_s is the magnitude of dc current supplied by dc source to the inverter and is equal to $\frac{V_g I_g}{2V_{\text{bus}}}$. The dc component and second harmonic component of $i_{\text{inv}}(t)$ are supplied by the dc source and buck APD circuit, respectively. Fig. 2 shows the graphical representation of $i_{\text{inv}}(t)$. When the instantaneous value of $i_{\text{inv}}(t)$ is greater than I_s, the APD circuit supplies energy to the dc-link by discharging the buffer capacitor. The equation for energy ΔE

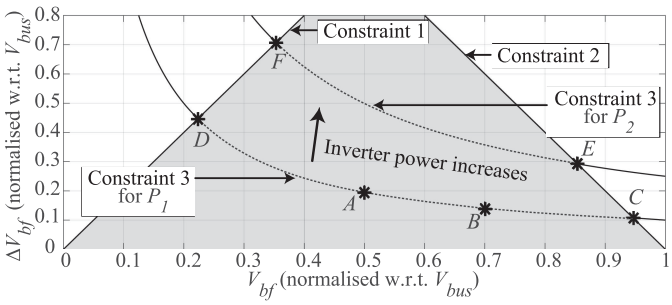

Fig. 3. Graphical illustration of operating constraints and operating points for the buck APD circuit.

supplied by the APD circuit to dc-link from $t = \frac{\pi}{4\omega}$ to $t = \frac{3\pi}{4\omega}$ is given by

$$\Delta E = \int_{\frac{\pi}{4\omega}}^{\frac{3\pi}{4\omega}} V_{\text{bus}} \cdot I_s \cos(2\omega t) dt = -\frac{V_{\text{bus}} I_s}{\omega}. \tag{4}$$

The negative sign in (4) indicates that the stored energy of the buffer capacitor is maximum at $t = \frac{\pi}{4\omega}$ and minimum at $t = \frac{3\pi}{4\omega}$. The maximum stored energy of the buffer capacitor must correspond to the maximum voltage across buffer capacitor and vice versa. Hence, the equation for ΔE is also given by

$$\begin{aligned}\Delta E &= \frac{1}{2} C_{bf} \left[\left(V_{bf} - \frac{\Delta V_{bf}}{2} \right)^2 - \left(V_{bf} + \frac{\Delta V_{bf}}{2} \right)^2 \right] \\ &= -C_{bf} V_{bf} \Delta V_{bf}. \end{aligned} \tag{5}$$

By equating the expressions for ΔE in (4) and (5), the third operating constraint for APD circuit is formulated as

$$V_{bf} \Delta V_{bf} = \frac{I_s V_{\text{bus}}}{\omega C_{bf}} = \alpha \tag{6}$$

where α is an operating constant, which depends on value of buffer capacitor, grid frequency, and inverter power.

Cons-3: The product of V_{bf} and ΔV_{bf} should remain constant for a given inverter power ($V_{bf} \Delta V_{bf} = \alpha$).

The aforementioned operating constraints are plotted graphically in Fig. 3. The graph is plotted between per-unit values of V_{bf} and ΔV_{bf}. The values of V_{bf} and ΔV_{bf} are normalized with respect to dc-link voltage V_{bus}. Considering constraints 1 and 2, the highlighted region in Fig. 3 is a viable region of operation for buck APD circuit. The graphical representation of equality constraint 3 for an inverter power value P_1 is also shown in Fig. 3. The combinations of V_{bf} and ΔV_{bf} values, which satisfy constraint 3, should lie on the curve representing this constraint. The combinations of V_{bf} and ΔV_{bf} values are termed as operating points of the APD circuit. While considering all three constraints for viable operation of the APD circuit at inverter power P_1, the dotted curve between points C and D is a locus of viable operating points for the APD circuit.

Amongst the locus of viable operating points for APD circuit at inverter power P_1, two operating points are marked in Fig. 3, namely A and B. Point A has an intercept of 0.5 p.u. on the horizontal V_{bf} axis. Hence, the APD controller, which maintains V_{bf} at 0.5 times the V_{bus}, selects the operating point A. Whereas, point B has an intercept of $\frac{1}{\sqrt{2}}$ p.u. on the horizontal V_{bf} axis. Hence, the APD controller, which maintains V_{bf} at $\frac{1}{\sqrt{2}}$ times the V_{bus}, selects the operating point B. The methods of operating point selection and their effect on power loss in APD circuit are studied in subsequent sections.

B. Analysis of Power Losses in APD Circuit

To analyze the power loss in APD circuit, an expression for voltage across buffer capacitor $v_{bf}(t)$ is derived as follows. As per the discussion in Section II-A, the APD circuit supplies current $I_s \cos(2\omega t)$ to dc-link with voltage V_{bus}. Hence, the instantaneous buffer capacitor power $p_{bf}(t)$ is given by

$$p_{bf}(t) = v_{bf}(t) \cdot C_{bf} \frac{\mathrm{d}v_{bf}(t)}{\mathrm{d}t} = V_{\text{bus}} I_s \cos(2\omega t). \tag{7}$$

By solving first-order differential equation and then substituting the expression for α from (6), $v_{bf}(t)$ is given by

$$v_{bf}(t) = \sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}. \tag{8}$$

The conduction losses and switching losses of power devices along with loss in the equivalent series resistance (ESR) of buffer inductor are major factors contributing to the overall losses in APD circuit. For power loss evaluation, the expressions for duty ratio of APD circuit $d_2(t)$ and current $i_{bf}(t)$ through buffer inductor L_{bf} are derived as follows:

$$i_{bf}(t) = C_{bf} \frac{\mathrm{d}v_{bf}(t)}{\mathrm{d}t} = \frac{\omega C_{bf} \alpha \cos(2\omega \mathrm{t})}{\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}}. \tag{9}$$

From (8), $d_2(t)$ is expressed as

$$d_2(t) = \frac{v_{bf}(t)}{V_{\text{bus}}} = \frac{\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}}{V_{\text{bus}}}. \tag{10}$$

The formulae for conduction losses in the switches and diodes are given by

$$P_{S,\text{cond}} = V_{\text{on}} \cdot I_{S,\text{ave}} + R_{\text{on}} \cdot I_{S,\text{rms}}^2 \tag{11}$$

$$P_{D,\text{cond}} = V_d \cdot I_{D,\text{ave}} + R_d \cdot I_{D,\text{rms}}^2 \tag{12}$$

where V_{on} and R_{on} are ON-state zero-current forward voltage drop and ON-state resistance of power semiconductor device, respectively. Similarly, V_d and R_d are ON-state zero-current forward voltage drop and ON-state resistance of diode, respectively. The $I_{S,\text{ave}}$ is value of average current and $I_{S,\text{rms}}$ is value of rms current through the switch. The $I_{D,\text{ave}}$ is value of average current and $I_{D,\text{rms}}$ is value of rms current through the diode. The equation for $I_{S,\text{ave}}$ is given by

$$I_{S,\text{ave}} = \frac{\omega}{\pi} \int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} i_{bf}(t) \cdot d_2(t) dt. \tag{13}$$

Using (9) and (10), (13) is rewritten as

$$I_{S,\text{ave}} = \frac{\omega}{\pi} \int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega C_{bf} \alpha \cos(2\omega \mathrm{t})}{V_{\text{bus}}} dt. \tag{14}$$

From (14), the value of switch average current remains constant for a given value of α. Similarly, the equation for $I_{S,\text{rms}}$ is derived

as

$$I_{S,\text{rms}} = \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega^2 C_{bf}^2 \alpha^2 \cos^2(2\omega \text{t})}{V_{\text{bus}}\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}} dt. \quad (15)$$

From (15), for a given value of α, as the value of V_{bf} increases, the switch rms current reduces. Hence, from (11), (14), and (15), for a given value of α, switch conduction loss reduces as the value of V_{bf} increases.

The equation for $I_{D,\text{ave}}$ is given by

$$I_{D,\text{ave}} = \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} i_{bf}(t)\cdot(1-d_2(t))dt. \quad (16)$$

Using (9) and (10), (16) is rewritten as

$$I_{D,\text{rms}} = \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega C_{bf}\alpha \cos(2\omega \text{t})}{\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}} dt - \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega C_{bf}\alpha \cos(2\omega \text{t})}{V_{\text{bus}}} dt. \quad (17)$$

There are two integrals in (17) with opposite signs. For a given value of α, as the value of V_{bf} increases, the value of first integral reduces, whereas the value of second integral remains constant. Hence, as the value of V_{bf} increases, the value of diode average current reduces. Similarly, the equation for $I_{D,\text{rms}}$ is derived as

$$I_{D,\text{rms}} = \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega^2 C_{bf}^2 \alpha^2 \cos^2(2\omega \text{t})}{V_{bf}^2 + \alpha \sin(2\omega t)} dt - \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega^2 C_{bf}^2 \alpha^2 \cos^2(2\omega \text{t})}{V_{\text{bus}}\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}} dt. \quad (18)$$

There are two integrals in (18) with opposite signs. The numerator terms for both the integrals are exactly identical. Whereas, V_{bf}^2 term appears without square root in denominator of first integral and inside square root in denominator of second integral. Hence, for a given value of α, as V_{bf} increases, the reduction in the value of first integral is expected to be more than reduction in the value of second integral. Therefore, in overall effect, as the value of V_{bf} increases, the diode rms current reduces as well. In conclusion, from (12), (17), and (18), for a given value of α, diode conduction loss reduces as the value of V_{bf} increases.

The ESR of the inductor L_{bf} is given by R_{bf}. The power loss in R_{bf} in terms of rms value of $i_{bf}(t)$, $I_{bf,\text{rms}}$, is given by

$$P_{R_{bf}} = I_{bf,\text{rms}}^2 R_{bf}. \quad (19)$$

Using (9), (19) is rewritten as

$$P_{R_{bf}} = \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{3\pi}{4\omega}} \frac{\omega^2 C_{bf}^2 \alpha^2 \cos^2(2\omega \text{t}) R_{bf}}{V_{bf}^2 + \alpha \sin(2\omega t)} dt. \quad (20)$$

From (20), for a given value of α, as the value of V_{bf} increases, the power loss in R_{bf} reduces.

The proportionality of switching loss in the switches is given by

$$P_{S,\text{sw}} \propto I_{\text{sw}} \cdot V_{\text{sw}} \quad (21)$$

where I_{sw} is the forward switch current and V_{sw} is the voltage blocked by the switch. The expression for switching losses, by substituting for I_{sw} in terms of $i_{bf}(t)$ and V_{sw} in terms of V_{bus}, is rewritten as

$$P_{S,\text{sw}} \propto \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega C_{bf}\alpha \cos(2\omega \text{t}) V_{\text{bus}}}{\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}} dt. \quad (22)$$

From (22), for a given value of α, as the value of V_{bf} increases, the switching loss reduces. Similarly, the proportionality of reverse recovery losses in the diodes is given by

$$P_{D,rr} \propto I_{rr} \cdot V_{rr} \quad (23)$$

where I_{rr} is the forward diode current and V_{rr} is the voltage blocked by the diode. The expression for reverse recovery losses, by substituting for I_{rr} in terms of $i_{bf}(t)$ and V_{rr} in terms of V_{bus}, is rewritten as

$$P_{D,rr} \propto \frac{\omega}{\pi}\int_{\frac{-\pi}{4\omega}}^{\frac{\pi}{4\omega}} \frac{\omega C_{bf}\alpha \cos(2\omega \text{t}) V_{\text{bus}}}{\sqrt{V_{bf}^2 + \alpha \sin(2\omega t)}} dt. \quad (24)$$

From (24), for a given value of α, as the value of V_{bf} increases, the reverse recovery loss reduces.

In summary, for a given value of operating constant α, the overall power losses in the APD circuit reduce with an increase in the value of V_{bf}. This conclusion is also consistent with the characteristics of a buck circuit, where the power loss reduces as the output voltage increases for the same output power. For a given value of operating constant α, (6) indicates that ΔV_{bf} is inversely proportional to V_{bf}. Hence, it is evident that the power losses in the APD circuit increase with an increase in the value of ΔV_{bf}.

A summary of the conclusions drawn in this section is given as follows. Considering the operating constraints for an inverter power value P_1, the dotted curve between points C and D in Fig. 3 gives the locus of viable operating points for APD circuit. The power loss analysis for the APD circuit indicates that the total power loss in the APD circuit increases with an increase in the value of ΔV_{bf}.

III. Proposed Technique

In this section, the proposed approach for the selection of minimum loss operating point for APD circuit is discussed. The reference generation and duty ratio injection controller required to implement the proposed approach is also described. A method to analyze the impact of proposed controller on the stability of the system is also provided.

A. Operating Point for Minimum Power Loss

This article proposes selection of the operating point defined by the intersection of curves representing constraint 2 and 3. The power loss at an operating point increases with an increase in the value of ΔV_{bf}. Hence, the operating point with a minimum intercept on vertical ΔV_{bf} axis is expected to have a minimum power loss. Given the hyperbolic nature of the curve representing constraint 3, the point of intersection of curves representing constraint 2 and constraint 3 is a viable operating point with

minimum ΔV_{bf} intercept. Hence, the proposed operating point has minimum power loss amongst the locus of viable operating points. The minimum power loss operating point is hereinafter called optimum operating point. The proposed approach for selection of optimum operating point is illustrated graphically with Fig. 3. The operating constraint 3 is plotted for two values of inverter power, namely P_1 and P_2 ($P_1 < P_2$). The loci of viable operating points for both power levels are also marked with dotted lines. The dotted line between points C and D shows the locus of viable operating points for inverter power P_1. Whereas, the dotted line between points E and F shows the locus of viable operating points for inverter power P_2. The proposed approach selects the operating point C at inverter power P_1 and operating point E at inverter power P_2. The graph also shows that the points C and E are the viable operating points having a minimum ΔV_{bf} intercept at inverter power P_1 and P_2, respectively. Hence, the points C and E are the optimum operating points at inverter power P_1 and P_2, respectively.

The implementation of the proposed approach imposes additional control requirements, discussed as follows. The curve representing the constraint 3 changes depending on the inverter power, and the position of optimum operating point also changes. Hence, with the change in inverter power, the optimum operating point shifts on the line representing constraint 2. This is seen from Fig. 3, where optimum operating point changes from C to E when the inverter power increases from P_1 to P_2. Observing the V_{bf} intercepts of the points C and E, it is clear that average voltage across the buffer capacitor V_{bf} must change with change in inverter power. This task becomes even more challenging in the presence of rapid changes in inverter power. In case the APD controller slowly changes the value of V_{bf}, the operating point may land in the unstable operating region outside the gray area. This may lead to distortion in the buffer capacitor voltage and dc-link voltage waveforms. Hence, fast response of the APD controller to change V_{bf} is desired.

B. Controller Description

1) Reference Generation and Duty Ratio Injection: Fig. 4 shows the proposed controller for the bidirectional buck converter based APD circuit. The optimum operating point is defined as the intersection of curves representing constraint 2 and 3. The reference for V_{bf}, V_{bf}^* corresponding to the optimum operating point is calculated as follows. Based on (6), the operating constraint 3 is rewritten as

$$V_{\text{bus}} I_s = \omega C_{bf} V_{bf}^* \Delta V_{bf}. \tag{25}$$

In a practical buck converter, the maximum output voltage is less than input voltage and it is limited by the dead time of switches and circuit losses. Hence, a safety factor λ is introduced to account for the said limitation, where λ is defined as the ratio of maximum output voltage to the input voltage. The operating constraint 2 considering the safety factor λ is given by

$$\lambda V_{\text{bus}} = V_{bf}^* + \frac{\Delta V_{bf}}{2}. \tag{26}$$

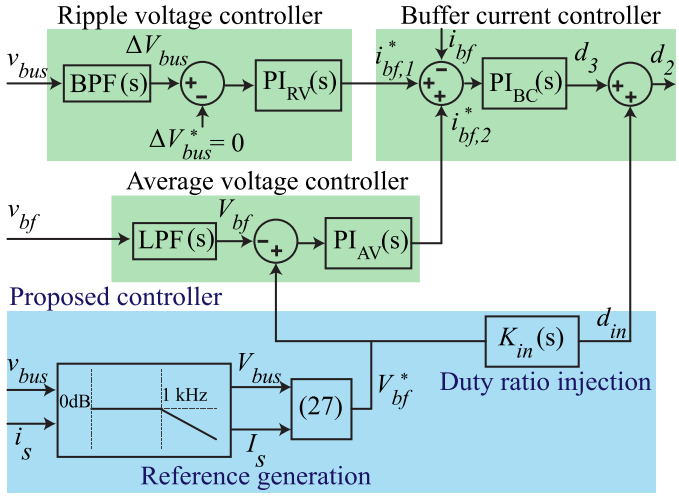

Fig. 4. Proposed controller for bidirectional buck converter based APD circuit.

The value of λ is chosen to be less than 1. Solving (25) and (26), V_{bf}^* is given by

$$V_{bf}^* = \frac{\lambda V_{\text{bus}}}{2} + \frac{1}{2}\sqrt{(\lambda V_{\text{bus}})^2 - \frac{2V_{\text{bus}} I_s}{\omega C_{bf}}}. \tag{27}$$

Before substituting the values in (27), the measured values of v_{bus} and i_s are filtered to eliminate the switching frequency components and noise. With proper control of APD circuit, the ripple components of v_{bus} and i_s are limited to a small value. Hence, their effect on the computation of V_{bf}^* is insignificant. The average voltage controller and duty ratio injection controller use the value of V_{bf}^* calculated from (27), as shown in Fig. 4. The duty ratio injection controller is a set point feed-forward controller. The inverse of the plant is suggested as the feed-forward gain. The plant, for the feed-forward signal under consideration, is defined as

$$\frac{\widetilde{v_{bf}}}{\widetilde{d}} = \left(\frac{1}{L_{bf}C_{bf}s^2 + R_{bf}C_{bf}s + 1}\right) \cdot V_{\text{bus}}. \tag{28}$$

The transfer function given by (28) is strictly proper and, hence, its inverse is noncausal. A simple solution to this problem is to add a pair of zeros at high frequency and calculate the inverse of the transfer function.

However, it is possible to take a simplifying assumption for the frequency-dependent term in (28). For a frequency range of zero to the resonance frequency ($\omega_r = \frac{1}{L_{bf}C_{bf}}$), the magnitude of the frequency-dependent term is close to unity and the phase is close to zero degree. Hence, the frequency-dependent term is approximated as a constant β. With this assumption, the transfer function in (28) is simplified as

$$\frac{\widetilde{v_{bf}}}{\widetilde{d}} = \beta \cdot V_{\text{bus}}. \tag{29}$$

The inverse of the transfer function given by (29) is causal and easy to implement. The ideal value of β is 1. However, the value is fine-tuned manually to obtain a satisfactory transient response. In this article, the duty ratio injection controller is implemented with the simplification given by (29).

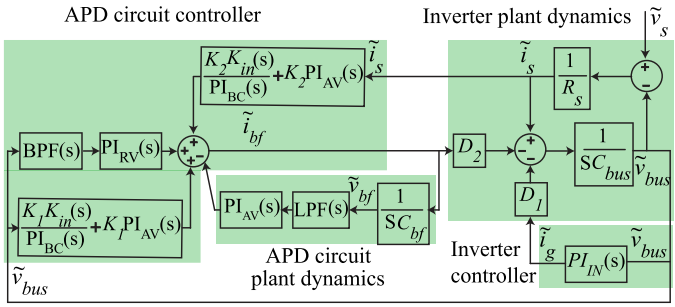

Fig. 5. Simplified small signal control block diagram of the system.

2) Voltage and Current Controllers: Apart from the proposed controller, Fig. 4 shows three other controllers present in the APD controller, namely the average voltage controller, buffer current controller, and ripple voltage controller. The ripple voltage controller is used to mitigate the voltage ripple in the dc-link voltage. First, the ripple components in the dc-link voltage are filtered and amplified with a band pass filter (BPF). The parameters of BPF are selected empirically to achieve the desired voltage ripple mitigation [10], [11]. The output of BPF is compared with a zero reference. The generated error signal is fed to a proportional-integral (PI) controller and a part of buffer current reference $i^*_{bf,1}$ is generated. The second part of the buffer current reference $i^*_{bf,2}$ is produced by the average voltage controller. The bandwidth of the average voltage controller is limited due to the presence of low pass filter (LPF) in the feedback path. This also limits the response of the average voltage controller during a rapid change in inverter power. Hence, the average voltage controller does not interfere with the action of the duty ratio injection controller during rapid load transients. The buffer current controller is used to ensure that the buffer inductor current follows its reference. The current controller generates a part of the duty ratio signal d_3 and a second part d_{in} is produced by duty ratio injection controller. The sum of these two parts generates the duty ratio signal d_2 for switch S_1, as depicted in Fig. 1.

C. Stability Analysis

Following a disturbance, the ability of the system to regain the equilibrium operating point is an important characteristic of a stable control system. To analyze the impact of changes in source voltage on the system, a small signal linearization based stability analysis is carried out as follows. The current control loops for buffer inductor current and grid current control are usually designed to have a large bandwidth (typically one-tenth of the switching frequency). On the other hand, the outer control loops are usually of less bandwidth. Therefore, to analyze the stability of the proposed controller in outer loop, the inner current controllers are assumed to be fast enough.

Fig. 5 shows the simplified control block diagram of the system. The control blocks for inverter controller, APD controller, and the plant dynamics are identified. Here, $\text{PI}_{\text{IN}}(s)$ is the dc-link voltage controller of the single-phase inverter. In the APD controller, the reference generation part of the proposed controller is linearized to get the constants K_1 and K_2. Using this control block diagram, the transfer function $\frac{\tilde{v}_{\text{bus}}}{\tilde{v}_s}$ is found. The denominator polynomial of the transfer function $\frac{\tilde{v}_{\text{bus}}}{\tilde{v}_s}$ is of the 11th order (corresponding to 11 poles). The locations of these poles are found in Section IV-A to assess the stability of the system. The proposed controller and duty ratio injection technique provides satisfactory steady-state and transient response, as supported by the simulation and experimental results in the next section.

TABLE I
PARAMETERS SELECTED FOR SIMULATION AND EXPERIMENTATION

Parameters	Simulation	Experimentation
Rated power	500 W	500 W
Grid voltage	110 V	110 V
Grid frequency	50 Hz	50 Hz
Source voltage, V_s	205 V - 225 V	205 V - 225 V
Source resistance, R_s	10 Ω	10 Ω
DC-link voltage, V_{bus}	200 V	200 V
Grid-side inductor, L_g	3.5 mH	3.5 mH
Buffer inductor, L_{bf}	3.5 mH	3.5 mH
Buffer inductor ESR, R_{bf}	0.4 Ω	0.4 Ω
Buffer capacitor, C_{bf}	160μF	160μF
Bus capacitor, C_{bus}	4.4μF	4.4μF
Inverter switching frequency	10 kHz	10 kHz
APD circuit switching frequency	20 kHz	20 kHz
Safety factor, λ	0.93	0.93
Inverter IGBTs	-	FSBB20CH60
Buck converter IGBTs	-	IKA15N65H5
IGBT gate drivers	-	FOD8316
Digital controller	-	TMS320F2808

IV. Simulation Results, Experimental Results, and Discussion

The validity of the proposed technique for loss reduction is established with the help of circuit simulation and experimental studies. The circuit diagram in Fig. 1, along with the proposed controller shown in Fig. 4, are considered for both simulation and experimentation. The parameters selected for the same are listed in Table I.

A. Simulation Studies

To validate the performance of the proposed controller, circuit simulation is performed in the MATLAB/Simulink software environment. An inverter power profile is selected for studying the effect of load transients and steady-state operation at various inverter power levels. Step changes in the source voltage V_s are used to command the rapid changes in the inverter power. The dc-link voltage reference is kept constant at 200 V. Moreover, the steady-state and transient performance of the APD circuits is compared with the AEC-based circuit. For the realization of the AEC-based circuit, the bidirectional buck converter is replaced with a 1-mF AEC at the dc-link of the inverter.

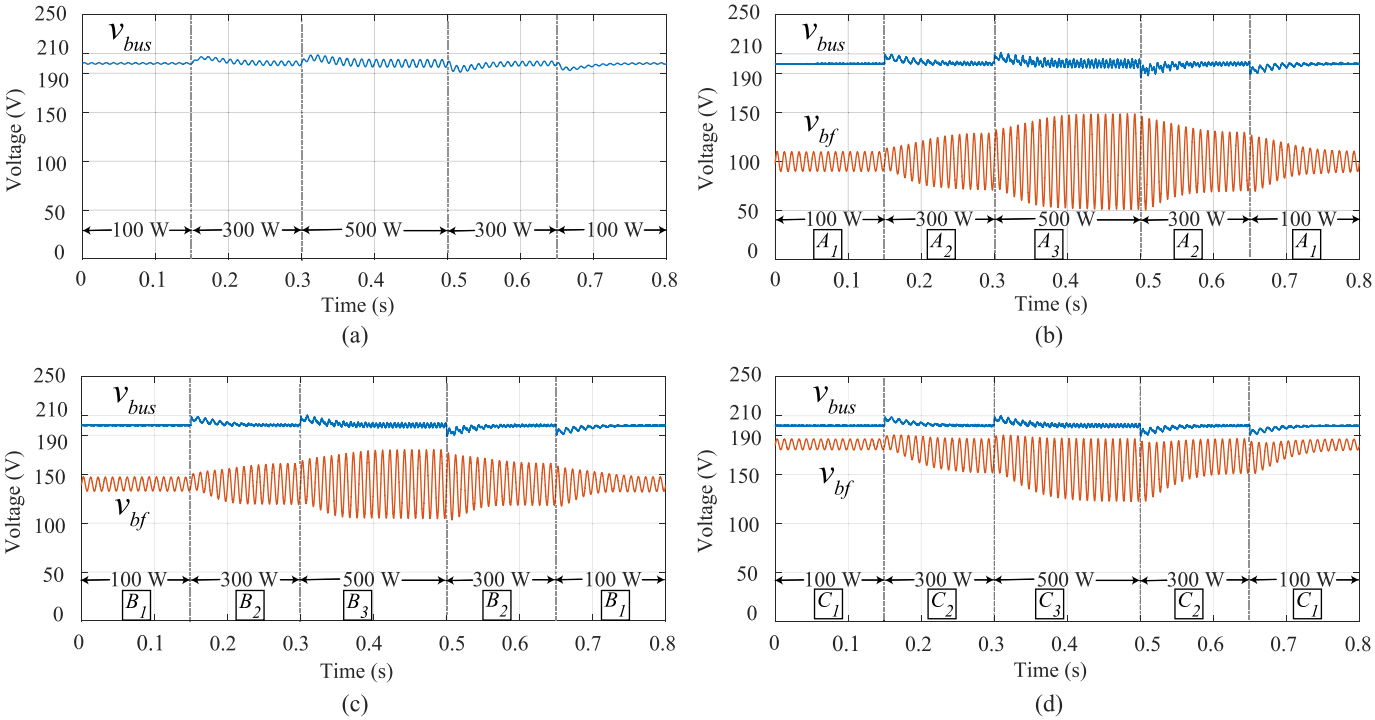

Fig. 6. Simulation results for single-phase grid feeding inverter with (a) 1-mF AEC connected at dc-link, (b) bidirectional buck converter based APD-A approach, (c) bidirectional buck converter based APD-B approach, and (d) bidirectional buck converter based proposed APD approach.

The proposed approach is also compared with existing APD control approaches, in which the average voltage of the buffer capacitor V_{bf} is controlled. The approach which maintains V_{bf} at 0.5 times the dc-link voltage is hereinafter called APD-A approach. The approach which maintains V_{bf} at $\frac{1}{\sqrt{2}}$ times the dc-link voltage is hereinafter called APD-B approach.

Fig. 6 shows the simulation results for AEC-based circuit and the bidirectional buck converter based APD circuits. Fig. 6(a) shows the simulation results of AEC-based circuit. Despite 40% step change in inverter power (magnitude of 200 W), the dc-link voltage of the inverter is within the limits of 190 and 210 V. Also, the peak-to-peak ripple in the dc-link voltage at rated power is close to 5%. Fig. 6(b) shows the simulation results of the APD-A approach and the steady-state operating points are marked. The operating points selected by the APD-A approach are also shown in Fig. 7, marked as A_1, A_2, and A_3. In Fig. 7, the graph is plotted between values of V_{bf} and ΔV_{bf}. The operating constraints are also shown for the simulated APD circuit. In the APD-A approach, the average voltage of the buffer capacitor is kept at 100 V for all inverter power values. This is well supported by the simulated waveforms and V_{bf} intercept of the operating points selected by the APD-A approach. In Fig. 6(c), the simulation results of the APD-B approach and the steady-state operating points are shown. Fig. 7 shows the operating points selected by APD-B approach, which are marked as B_1, B_2, and B_3. For all inverter power values, the average voltage of the buffer capacitor is kept at 141 V in the APD-B approach. This is also supported by the simulated waveforms and V_{bf} intercept of the operating points selected by the APD-B approach.

Fig. 6(d) shows the simulation results of the proposed approach and the optimum operating points are also marked. It

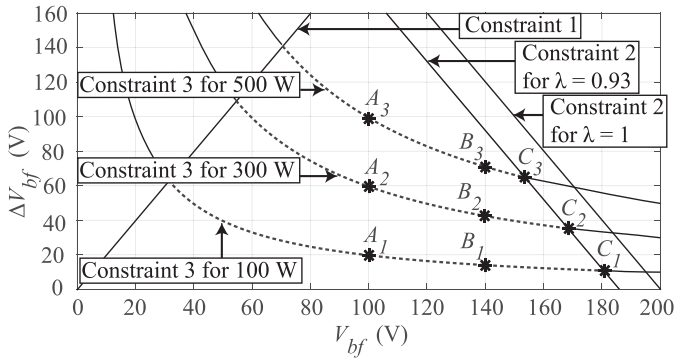

Fig. 7. Graphical illustration of operating constraints and operating points for the simulated APD circuit design ($V_{\text{bus}} = 200$ V, $C_{bf} = 160\,\mu$F, $\omega = 314$ rad/s).

is seen that the average voltage of the buffer capacitor changes with inverter power. The proposed control technique achieves rapid variation in the average voltage of the buffer capacitor without distortion in voltage waveforms. The controller ensures that the bidirectional buck converter is operated at the optimum operating point. The proposed approach maintains the dc-link voltage within the limits of 190 and 210 V, despite large step changes in the inverter power (40% of rated power). The peak-to-peak ripple in the dc-link voltage at rated power is close to 2%. Hence, the proposed controller achieves satisfactory steady-state and transient response. Moreover, the transient and steady-state performance of the proposed controller is comparable to the AEC-based circuit, in spite of the 84% reduction in capacitance value.

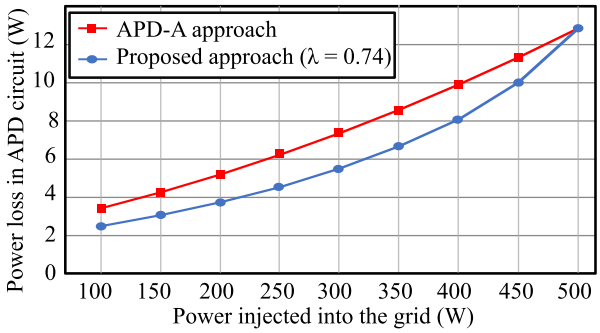

Fig. 8. Comparison between calculated power loss in the APD-A approach and the proposed approach for same voltage rating of buffer capacitor.

The operating points selected by the proposed approach are shown in Fig. 7, marked as C_1, C_2, and C_3. In Fig. 7, the constraint 2 is shown for two values of safety factors (λ), namely 0.93 and 1. It is seen that, as the value of λ increases, the ΔV_{bf} intercept of the optimum operating point reduces. Hence, the power loss at the optimum operating point is expected to reduce with an increase in the value of λ. Hence, to improve conversion efficiency, it is preferable to have a large value of λ, which is dependent on dead time of switches and their ON-state voltage drops as discussed in [21]. The effect of parameter λ and value of buffer capacitor on the power loss in the proposed APD approach is discussed as follows.

1) Effect of Parameter λ: The value of parameter λ dictates the maximum voltage across the buffer capacitor and, hence, its voltage rating. The value of parameter λ is also understood as per unit value of maximum voltage across the buffer capacitor at steady state, where dc-link voltage is taken as base value.

When the value of λ is selected as 0.74, the maximum voltage across buffer capacitor in the APD-A approach and the proposed approach becomes comparable. Hence, the voltage rating of the buffer capacitor is expected to be same in both cases. Fig. 8 shows the comparison between calculated power loss in the APD-A approach and the proposed approach for the same capacitor voltage rating. At rated load, since there is no voltage margin to raise the average voltage of the buffer capacitor, the proposed technique and the APD-A approach become equivalent. Hence, the power loss in APD circuit in both cases is the same. However, under part load conditions, the proposed technique changes the average voltage of buffer capacitor to reduce power loss in the APD circuit. As shown in Fig. 8, the proposed technique achieves up to 2 W reduction in power loss in APD circuit. Hence, the proposed technique is capable of reducing power loss in the APD circuit without increasing the voltage rating of the buffer capacitor. However, if higher value of λ is selected and the voltage rating of the buffer capacitor is increased, further reduction in power loss is possible.

2) Effect of Value of Buffer Capacitor, C_{bf}: Table II shows the effect of value of buffer capacitor on the proposed APD approach at rated inverter power. An increase in the value of buffer capacitor reduces the voltage ripple across it. This allows the proposed controller to increase the value of V_{bf}^*, thereby reducing power losses in the APD circuit. Although increasing C_{bf} reduces losses, the reduction in losses follow diminishing returns. This is also supported by the diminishing incremental action of the proposed controller.

TABLE II
EFFECT OF VALUE OF BUFFER CAPACITOR C_{bf} ON THE PROPOSED APD APPROACH AT RATED INVERTER POWER

Value of buffer capacitor, C_{bf}	V_{bf}^* provided by the reference generation controller (λ = 0.93)	Total power loss in APD circuit
160 μF	154 V	7.41 W
200 μF	161 V	6.85 W
240 μF	166 V	6.56 W
280 μF	169 V	6.38 W
320 μF	171 V	6.24 W
360 μF	173 V	6.16 W

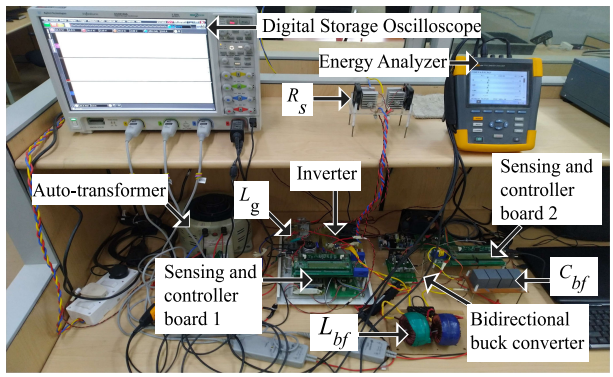

Fig. 9. Developed laboratory setup of bidirectional buck converter based APD circuit with grid interfacing single-phase inverter.

3) Stability Analysis of Designed System: Using the method described in Section III-C, small signal stability analysis is carried out. The control parameters used are listed as follows: $\mathrm{PI_{IN}}(s) = \frac{0.1s+9}{s}$, $\mathrm{BPF}(s) \simeq \frac{2.5s}{s^2+0.6283s+628.3^2}$, $\mathrm{PI_{RV}}(s) = \frac{2s+0.001}{s}$, $\mathrm{PI_{BC}}(s) = \frac{0.6s+1}{s}$, $\beta = 1$, $\mathrm{PI_{AV}}(s) = \frac{0.001s+0.005}{s}$, $\mathrm{LPF}(s) = \frac{62}{s+62}$, and $K_{\mathrm{in}} = 0.005$.

All 11 poles of the transfer function $\frac{\tilde{v}_{\mathrm{bus}}}{\tilde{v}_s}$ with the proposed controller are located in the left half plane. Hence, the small signal stability of designed system is ensured. The dominant poles of the transfer function $\frac{\tilde{v}_{\mathrm{bus}}}{\tilde{v}_s}$ with the proposed controller are located at

$$\begin{bmatrix} -1.667 + 0i & -3.179 + 5.048i & -3.179 - 5.048i \end{bmatrix}.$$

The dominant poles of the transfer function $\frac{\tilde{v}_{\mathrm{bus}}}{\tilde{v}_s}$ without the proposed controller are located at

$$\begin{bmatrix} -1.666 + 0i & -3.168 + 4.976i & -3.168 - 4.976i \end{bmatrix}.$$

Hence, it is observed that the proposed controller does not change the location of dominant poles significantly.

B. Experimental Results

An experimental prototype of inverter and the APD circuit is developed in laboratory to validate the performance of the proposed scheme, as shown in Fig. 9. To experimentally compare the steady-state and transient performance of the AEC-based circuit and the proposed approach, an inverter power profile is

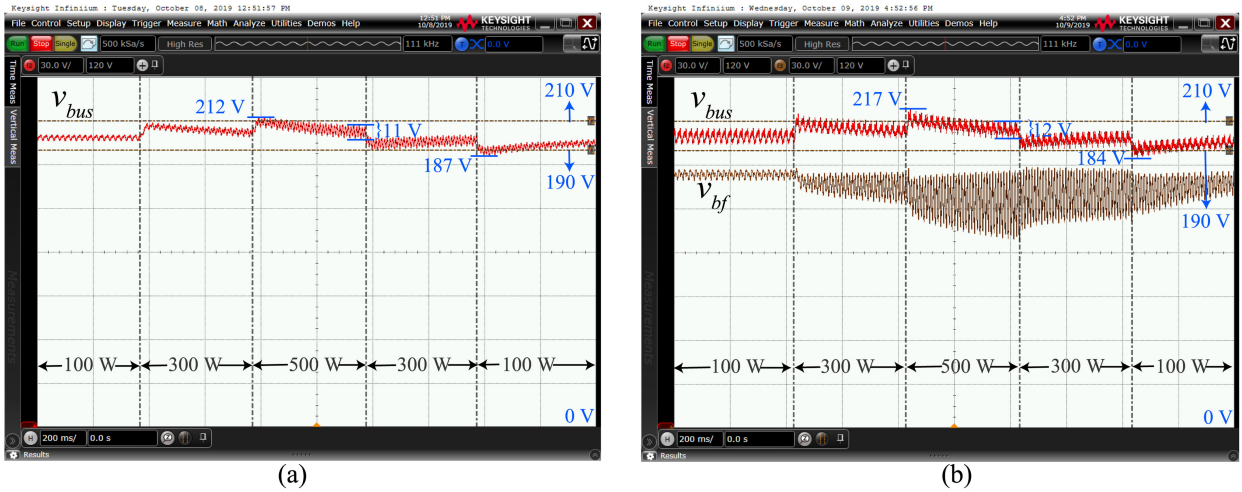

Fig. 10. Experimental results for single-phase grid feeding inverter with (a) 1-mF AEC connected at dc-link and (b) bidirectional buck converter based proposed APD approach (dc-link voltage, v_{bus}: 30 V/div; buffer capacitor voltage, v_{bf}: 30 V/div; time: 0.2 s/div).

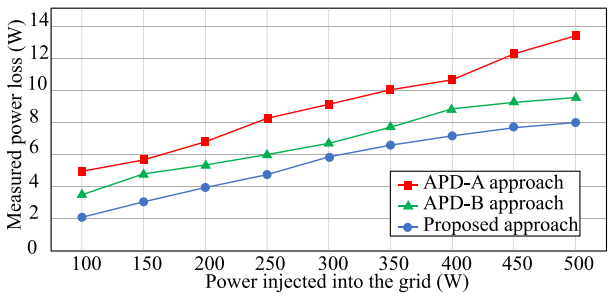

Fig. 11. Measured losses in developed prototype of bidirectional buck converter based circuit with three control approaches viz., APD-A approach, APD-B approach, and proposed approach.

TABLE III
CONVERSION EFFICIENCY OF SINGLE-PHASE INVERTER PROTOTYPE

Inverter Power in W	Efficiency of AEC based inverter in %	Drop in % efficiency with APD circuits		
		APD-A	APD-B	Proposed
100	67.18	4.69	3.31	1.99
150	76.78	3.59	3.04	1.94
200	83.92	3.20	2.52	1.86
250	86.91	3.15	2.29	1.82
300	89.41	2.89	2.12	1.85
350	90.67	2.68	2.06	1.76
400	91.79	2.47	2.05	1.66
450	92.69	2.51	1.89	1.57
500	93.10	2.49	1.77	1.49
CEC Efficiency	86.22	3.06	2.32	1.80

selected. Similar to the simulation studies, the inverter power is varied with the help of step changes in the source voltage. The dc-link voltage reference is kept constant at 200 V. Fig. 10(a) shows the experimental results for the AEC-based circuit. The steady-state voltage ripple at the rated power is 5.5% of the dc-link voltage. The peak deviations from the voltage reference of 200 V are found to be 212 and 187 V. Fig. 10(b) shows the experimental results for the bidirectional buck converter based proposed approach. The proposed control technique successfully maintains the operation at optimum operating point, despite rapid and substantial changes (200 W, 40% of rated power) in inverter power. The steady-state voltage ripple at the rated power is 6% of the dc-link voltage. The peak deviations from the voltage reference of 200 V are found to be 217 and 186 V. The experimental results validate the satisfactory steady-state and transient performance of the proposed controller.

To measure the losses in the bidirectional buck converter, the oscilloscope-based technique is used. The experimentally measured power loss results for all three APD approaches are shown in Fig. 11. At rated power, the proposed approach offers 40% reduction in losses compared with the APD-A approach and 15% reduction in losses compared with the APD-B approach. At 20% of rated power, the proposed approach achieves 57% reduction in losses compared with the APD-A approach and 40% reduction in losses compared with the APD-B approach. The values of measured power losses support the conclusions drawn with the help of loss calculation formulae and graphical analysis.

The input to output efficiency of the single-phase inverter is measured for AEC-based circuit and bidirectional buck converter based circuits. The measured efficiency values are shown in Table III. At rated power, compared to the AEC-based approach, the APD-based approaches lead to a 1.5%–2.5% drop in conversion efficiency. This reiterates the need to consider the impact of APD circuit on conversion efficiency of single-phase converters. At rated power, the proposed approach achieves 1% higher conversion efficiency than the APD-A approach and 0.3% higher conversion efficiency than the APD-B approach. At 20% of the rated inverter power, the proposed approach has a 2.7% higher conversion efficiency than the APD-A approach and 1.3% higher conversion efficiency than the APD-B approach. California Energy Commission (CEC) efficiency is an additional metric used for the assessment of the variation of efficiency with inverter power. The proposed approach shows 1.26% higher CEC efficiency than the APD-A approach and 0.52% higher

CEC efficiency than the APD-B approach. This efficiency improvement is expected to alleviate the impact of inclusion of APD circuit on the efficiency of single-phase converters.

V. Conclusion

This article proposes an approach to reduce power losses in the bidirectional buck converter based APD circuit. First, a graphical representation for the operation of bidirectional buck converter based APD circuit is discussed to develop an intuitive understanding. This graphical representation serves as framework for analysis of operating point selection by APD approaches. The proposed approach suggests that the average voltage across the buffer capacitor should be changed with inverter power. This is achieved with the help of reference generation and duty ratio injection controller. The effect of inclusion of proposed controller on the stability of the system is analyzed with the help of small signal modeling. The guidelines for the selection of controller parameters and their impact on the performance of APD circuit are also provided. The steady-state and transient performance of the proposed controller is supported by simulation and experimentation. Further, the power loss reduction claims are presented with the help of analytical calculations and validated with the help of power loss measurements in experimental setup. When compared with the approach of controlling average voltage across buffer capacitor at 0.5 times the dc-link voltage, the proposed approach offers 40% reduction in measured power loss in APD circuit at rated power. When compared with the approach of controlling average voltage across buffer capacitor at $\frac{1}{\sqrt{2}}$ times dc-link voltage, the proposed approach offers 15% reduction in measured power loss in APD circuit at rated power.

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