Multilevel CSC System Based on Series–Parallel Connected Three-Phase Modules With Optimized Carrier-Shift SPWM

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***Abstract*—Current source converter (CSC) is widely used in high power applications. To increase the system power rating, both series and parallel connections can be adopted and implemented easily. In this article, a mixed series–parallel CSC structure is proposed for high power application. An optimized carrier-shift sinusoidal pulsewidth modulation (SPWM) is adopted for the mixed system to simultaneously improve the dc-link voltage quality and achieve multilevel ac output, which can potentially reduce the size of dc- and ac-side filters. Meanwhile, the system reliability can be significantly improved due to the modular design with carrier-shift SPWM and inherent short-circuit protection of CSC. With these advantages, the proposed mixed series–parallel CSC structure can be an attractive candidate for medium-voltage drives, high-voltage direct current, and offshore wind power applications. Simulation and experimental results verify the effectiveness of the novel mixed series–parallel CSC system with optimized carrier-shift SPWM.**

***Index Terms*—Current source converter (CSC), modular system, series–parallel structure, sinusoidal pulsewidth modulation (SPWM).**

I. Introduction

CURRENT-SOURCE converters (CSCs) can provide the advantages of four-quadrant operation, inherent short-circuit protection, low *dv/dt* waveforms, and voltage boosting capability, which make the CSC widely applied in renewable energy generation (solar photovoltaics, wind turbine generation), medium-voltage (MV) drives, and high-voltage direct current (HVdc) system [1]. Employing specific configurations and applying moderated switching modulations brings higher performance and consequently, more industrial applications [2]. Both parallel and series connections of multiple CSCs can be adopted for high power applications. Meanwhile, improved modulation strategies can be implemented to achieve better performance.

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Modular parallel CSC structure, formed by connecting the outputs in parallel with a shared output filter, can improve the system current/power rating, reliability, and output harmonic performance [3]–[9]. The dc current balance control with multilevel space vector modulation (SVM) for 2-CSC parallel CSC system was addressed in [3]. In [4], a multilevel selective harmonic elimination (SHE) with optimized switching angle design was adopted for parallel current source rectifier (CSR). A bi-trilogic sinusoidal pulsewidth modulation (SPWM) adopted for N-CSC ($N \geq 3$) parallel system was introduced in [5], and the detailed digital implement process was explained in [6]. Multilevel SVM-based common-mode voltage (CMV) reduction method for transformerless CSC-fed high-power MV drives was introduced in [7] and [8]. Simultaneous dc current balance and CMV reduction method by optimizing the redundant switching state selection was investigated in [9] and [10].

Series CSC structure, on the other hand, can also increase system power range to satisfy high-voltage applications. A symmetrical phase angle control method adopted for series connected GTO-based CSR system was introduced in [11], which can improve the supply current quality. Some researchers studied series connected CSC system as an alternative structure for wind turbine generation [12]–[16], which enjoys high reliability due to inherent short-circuit protection of CSC. The characteristics of series thyristor converter connected wind turbine system were analyzed in [12]. A series CSC connected multiphase generator with multiwinding transformer was introduced in [13]. Some control methods such as average dc voltage control, power control [14], and dc-link current coordinate control [15], [16] had been studied to improve the system performance. A hybrid line-commutated converter (LCC) and pulsewidth modulation (PWM) CSC was proposed in [17] for HVdc application. Series PWM CSC configuration was adopted for offshore wind power transmission, where multiple wind turbines are connected to the series CSCs to build up the transmission voltage [18] and multiwinding or multiple two-winding transformers were needed for onshore grid connection.

However, there was no research to combine the series and parallel connection together to achieve much higher power range, improved ac/dc performance, and system reliability. Therefore, a novel multilevel CSC structure based on series–parallel connected three-phase CSC module adopted on either grid side or generator side, as shown in Fig. 1, is proposed in this article. The

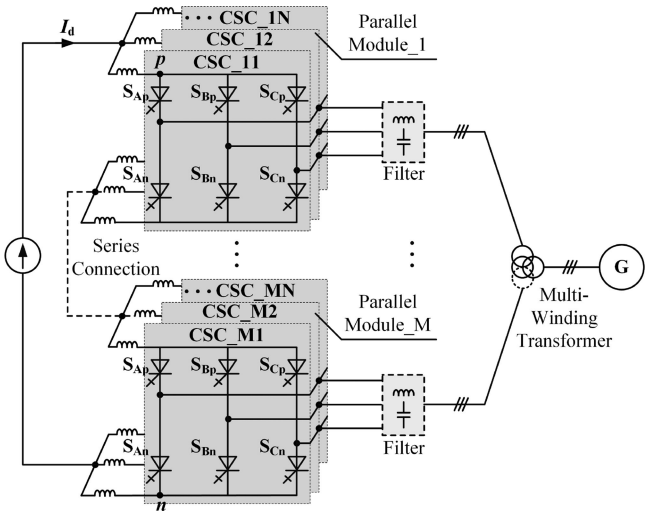

Fig. 1. Mixed series–parallel CSC system.

paralleled CSCs can be regarded as a module; then, each paralleled module can be connected in series, the number of parallel and series CSCs is very flexible to be determined according to the system power rating.

For parallel or series CSC application, both multilevel SVM and SHE are difficult to develop mainly due to large number of redundant switching states. For example, there are 729 switching states available for 3-CSC parallel or series system and redundant switching state selection is very complex to achieve superior performance. On the contrary, the carrier-based SPWM enjoys inherent scalability, modularity, and easy-implement features for parallel or series CSC application. A carrier-shift SPWM based on direct duty-ratio PWM (DDPWM) for parallel CSC application was proposed in [19], which results in small CMV and circulating current. However, the system performances of series CSC as well as mixed series–parallel CSC systems with carrier-shift modulation were not studied yet.

In this article, an optimized carrier-shift SPWM was proposed for the novel series–parallel connected multilevel CSC system to simultaneously improve the dc-link voltage and ac output qualities, which can potentially reduce the size of dc-link inductance and ac output filter. The rest of this article is organized as follows. In Section II, the basic operation principles of DDPWM and its application for parallel or series CSC structures are introduced. Then, the sub-dc-link current analysis and dc-link voltage performance with optimized carrier-shift DDPWM are introduced in Section III. Section IV shows the simulation and experiment results to verify the effectiveness of proposed methods. Finally, the conclusion is given in Section V.

II. Carrier-Shift SPWM and Modular CSC System

This section mainly focuses on the principle of DDPWM and its application to modular CSC system. Two different carrier types—phase disposition (PD) and phase opposition disposition (POD)—are compared. The ac current features of parallel CSC and the dc voltage features of series CSC will be analyzed separately.

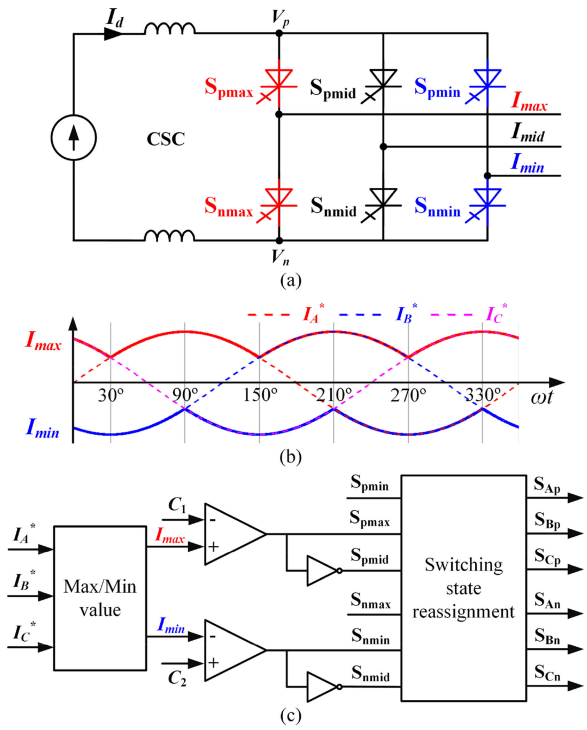

Fig. 2. DDPWM for single CSC. (a) CSC diagram in Max-Mid-Min phase. (b) $I_{\max}$ and $I_{\min}$ waveforms. (c) Digital implement.

A. Principle and PWM Sequence of DDPWM

The proposed carrier-shift SPWM is based on DDPWM, which can directly produce the gating signals for CSC with simple mapping [20]. To achieve direct gating signal production, the six switches are identified as S_{pmax}/S_{nmax}, S_{pmid}/S_{nmid}, and S_{pmin}/S_{nmin} according to the magnitude of three phase references ($I_A{}^*$, $I_B{}^*$, and $I_C{}^*$). The output phases are renamed as Max-Mid-Min phase instead of A-B-C phase, as shown in Fig. 2(a). The maximum, medium, and minimum values (identified as $I_{\max}$, I_{mid}, and $I_{\min}$) among the three phase references can be obtained first. In Max-Mid-Min phase, $I_{\max}$, I_{mid}, and $I_{\min}$ can be synthesized by S_{pmax}/S_{nmax}, S_{pmid}/S_{nmid}, and S_{pmin}/S_{nmin}, respectively.

The waveforms of $I_{\max}$ and $I_{\min}$ with balanced three phase references are shown in Fig. 2(b). As $I_{\max}$ is always greater than 0, and $I_{\min}$ is always less than 0, thus $I_{\max}$ can be synthesized by using I_{dc} and 0, $I_{\min}$ can be synthesized by using $-I_{\mathrm{dc}}$ and 0. That means the lower leg of Max phase S_{nmax} and upper leg of Min phase S_{pmin} are never turned ON ($S_{nmax} = S_{pmin} = 0$). As one and only one switch among the three upper and lower switches should be ON at the same time, which can be restricted by $S_{pmax} + S_{pmid} + S_{pmin} = 1$ and $S_{nmax} + S_{nmid} + S_{nmin} = 1$, the gating signals in Max-Mid-Min phase can be expressed as

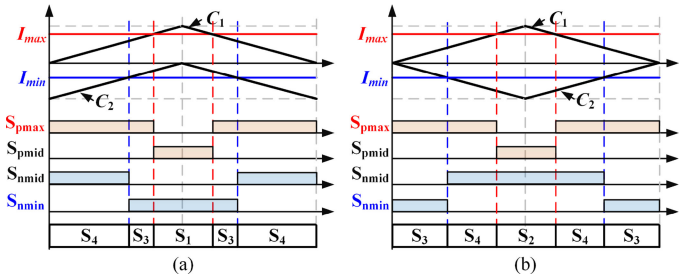

Fig. 3. Gating signals of single CSC with DDPWM: (a) PD; and (b) POD.

TABLE I
SWITCHING STATE REASSIGNMENT OF DDPWM

Interval	[Max-Min]	Switching State Reassignment			
[-30°-30°]	[I_C^*-I_B^*]	$S_1 \rightarrow I_1$	$S_2 \rightarrow I_7$	$S_3 \rightarrow I_6$	$S_4 \rightarrow I_5$
[30°-90°]	[I_A^*-I_B^*]	$S_1 \rightarrow I_6$	$S_2 \rightarrow I_9$	$S_3 \rightarrow I_1$	$S_4 \rightarrow I_2$
[90°-150°]	[I_A^*-I_C^*]	$S_1 \rightarrow I_3$	$S_2 \rightarrow I_8$	$S_3 \rightarrow I_2$	$S_4 \rightarrow I_1$
[150°-210°]	[I_B^*-I_C^*]	$S_1 \rightarrow I_2$	$S_2 \rightarrow I_7$	$S_3 \rightarrow I_3$	$S_4 \rightarrow I_4$
[210°-270°]	[I_B^*-I_A^*]	$S_1 \rightarrow I_5$	$S_2 \rightarrow I_9$	$S_3 \rightarrow I_4$	$S_4 \rightarrow I_3$
[270°-330°]	[I_C^*-I_A^*]	$S_1 \rightarrow I_4$	$S_2 \rightarrow I_8$	$S_3 \rightarrow I_5$	$S_4 \rightarrow I_6$

$$S_{pmax} = \bar{S}_{pmid} = \begin{cases} 1, & I_{max} >= C_1 \\ 0, & I_{max} < C_1 \end{cases}$$
$$S_{nmin} = \bar{S}_{nmid} = \begin{cases} 1, & I_{min} < C_2 \\ 0, & I_{min} >= C_2 \end{cases} \quad (1)$$

where the gating signals of S_{pmax} and S_{pmid} are generated by comparing I_{max} with upper carrier (C_1), while the gating signals of S_{nmin} and S_{nmid} are produced by comparing I_{min} with lower carrier (C_2). The two ON-state switches are used to represent the switching states, therefore, there are four switching states (S_1 = [S_{pmid}; S_{nmin}]; S_2 = [S_{pmid}; S_{nmid}]; S_3 = [S_{pmax}; S_{nmin}]; S_4 = [S_{pmax}; S_{nmid}]) available in a single CSC.

Fig. 3(a) and (b) shows the gating signals of PD and POD in Max-Mid-Min phase by assuming that the references are constant in each carrier period. It is easy to find that the PWM sequence of DDPWM is 5-segment and half-wave symmetric with both PD and POD. The dwell times are determined by the references I_{max} and I_{min}. After producing the gating signals in Max-Mid-Min phase, they should be reassigned to A-B-C phase according to the current reference magnitude. The current references can be divided into six intervals based on their magnitudes, and the detailed switching state reassignment mapping is listed as Table I, where I_1 to I_6 are the six active states and I_7 to I_9 are the three zero states in A-B-C phase.

With the help of the above analysis, the current vector selection and PWM sequence of DDPWM in A-B-C phase with PD and POD can be obtained as in Fig. 4. The vector diagram can be divided into six sectors and each sector can be divided into two subsectors equally due to different zero vector selection and

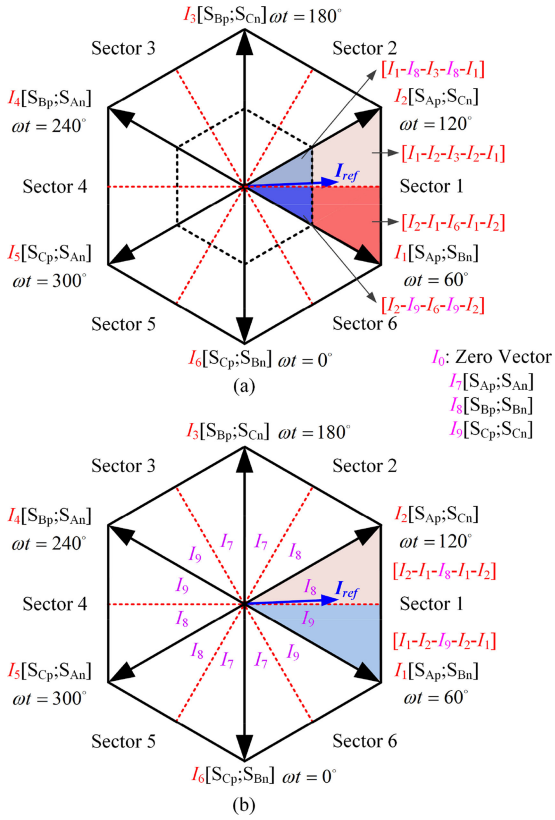

Fig. 4. PWM sequence of DDPWM: (a) PD; and (b) POD.

PWM sequence. Besides these, the PWM sequence of PD is also related to the modulation index. Taking POD as an example, when the current reference is located in Sector 1, the PWM sequences in the two subsectors marked by different colors in Fig. 4(b) are [I_1-I_2-I_9-I_2-I_1] and [I_2-I_1-I_8-I_1-I_2], respectively. Since there are four switching actions in each carrier period, the average switching frequency is two-thirds of the carrier frequency.

B. Parallel CSC System

Parallel CSC enjoys the benefits of modularity, improved fault tolerance and reliability, extended power range beyond semiconductor limits, as well as better output current harmonic performance, which attracted increased attention in recent years. An *N*-CSC parallel CSC system with a shared dc-link is shown in Fig. 5.

The DDPWM can be simply implemented to parallel CSC system, which can be achieved by comparing I_{max} and I_{min} with a set of symmetrical triangular carriers [19]. Taking 2-CSC parallel system shown in Fig. 6 as an example, I_{max} are compared with the carrier C_{11} and carrier C_{21} to determine the turn ON/OFF action of $S_{pmax1(2)}$. Meanwhile, I_{min} are compared with carrier C_{12} and carrier C_{22} to determine the turn ON/OFF action of $S_{nmin1(2)}$. The gating signal of $S_{pmax1(2)}$ and $S_{nmin1(2)}$ can be

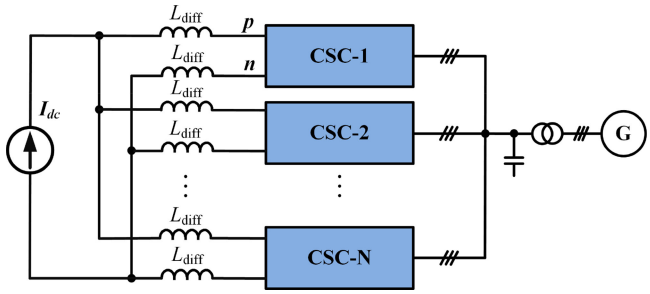

Fig. 5. Parallel CSC structure.

expressed as

$$\mathrm{S}_{\mathrm{pmax1(2)}} = \begin{cases} 1, & I_{\max} >= C_{11(21)} \\ 0, & I_{\max} < C_{11(21)} \end{cases}$$

$$\mathrm{S}_{\mathrm{nmin1(2)}} = \begin{cases} 1, & I_{\min} < C_{12(22)} \\ 0, & I_{\min} >= C_{12(22)} \end{cases} \tag{2}$$

where C_{11} and C_{21} are the upper carriers and C_{12} and C_{22} are the lower carriers for CSC-1 and CSC-2, respectively.

The carrier interleaving angle for 2-CSC parallel connection is set as 180° for both PD and POD, as shown in Fig. 6(b) and (c). As can be seen, the resultant PWM sequence of each CSC is also shifted 180°. The total ac output current is symmetrical in each half-cycle and the waveforms of PD and POD are totally the same with 2-CSC connection. Generally, the equivalent carrier frequency will increase to *N* times with $2N + 1$ level output by shifting the carriers for *N*-CSC parallel system. The average switching frequency of each paralleled module is still two-thirds of the carrier frequency. Meanwhile, it can guarantee small CMV and circulating current despite the parallel module number [19].

Since the detailed features of multilevel ac current output of parallel CSC system with carrier-shift DDPWM had been well analyzed in [19], this section mainly compares the output PWM current performances of PD and POD with different parallel CSC numbers ($N = 1$, 2, 3, and 4), as shown in Fig. 7, in terms of the total harmonic distortion (THD). The carrier interleaving angle is set as 360°/*N* for both PD and POD. It is obvious that the THD performance of output current can be significantly improved with the increase of parallel CSC module number since higher current level can be achieved, which can help to reduce the ac-side filter size. When the parallel module number is even, the output waveforms of PD and POD are totally the same and result in the same THD performances. POD is better than that of PD when the parallel module number is odd. However, the difference is smaller with the increase of modulation index range as well as the number of parallel CSC modules.

As the carrier-shift SPWM shows superior performance in terms of ac output current, a further study of this modulation employed in series CSC system will be introduced.

C. Series CSC System

Apart from parallel CSC connection adopted for high power applications, the series CSC structure had also been well investigated in wind energy-based HVdc application. The series CSC structure can be employed in either grid side or generator side. Fig. 8 shows a typical series CSC structure, where *M* CSCs are connected in series manner on the dc side, while the ac sides are connected to the grid with a multiwinding transformer.

Although the benefits of series CSC structure had been well addressed in some studies in the literature, no research focus on the possibility of dc-link voltage improvement with carrier-shift modulation had been made. Thus, this section will mainly investigate the dc-link voltage features. The total dc-link voltage V_{pn} with series connection is the sum of each sub-dc-link voltage, which can be expressed as

$$V_{pn} = V_{pn1} + V_{pn2} + \cdots + V_{pnM} \tag{3}$$

where V_{pn1} to V_{pnM} are the dc-link voltages for each series CSC module. Obviously, the voltage level can be increase through series connection and the dc component of dc-link voltage can be expressed as

$$V_{pn\_\mathrm{DC}} = \frac{3M}{2} m_a V_{\mathrm{mag}} \cos\varphi \tag{4}$$

where *M* is the number of series CSC module, m_a is the modulation index, and φ is the power factor angle.

The carrier-shift DDPWM analyzed for parallel CSC structure can also be extended to series structure; the dc-link voltage of a 2-series CSC system, as shown in Fig. 9, is explained as an example. Fig. 9(b) and (c) shows the gating signals and V_{pn} waveform in one carrier period with PD and POD, respectively. The actual dc-link voltage in CSC is an envelope waveform of line voltage, which is related to the switching state and the output voltage waveforms. The output voltages (V_x, V_d, and V_n) are assumed to be constant in each carrier period when the carrier ratio is relatively high, therefore, the dc-link voltage of each CSC is also half-wave symmetrical, which is similar to the current PWM. With series connection, the total dc-link voltage would be a half-wave symmetrical waveform in each half-carrier period for both PD and POD, which means that the equivalent switching frequency will be doubled. As a result, the quality of dc voltage can be improved with series connection.

Fig. 10 shows the dc-link voltages and their harmonic distribution of POD with different number of series modules. The output frequency is 60 Hz, carrier frequency is 1 kHz, and modulation index is 0.8. It is obvious that the dc component can be increased to *M* times with *M* series modules. Moreover, the voltage quality can be improved by adopting carrier-shift DDPWM where the dominant high-order harmonic increases to *M* times, which will help to reduce the dc-side filter size.

Fig. 11 compares the dc-link voltage THD of PD and POD to evaluate voltage ripple reduction with series connection ($M =$ 1, 2, 3, and 4). The carrier interleaving angle is set as 360°/*M*. Similar to the ac output trend of parallel CSC, the dc-link voltages of PD and POD are totally the same when the series module number is even. When the module number is odd, it shows an inverse trend compared with the parallel case; the overall performances are similar when the module number is three.

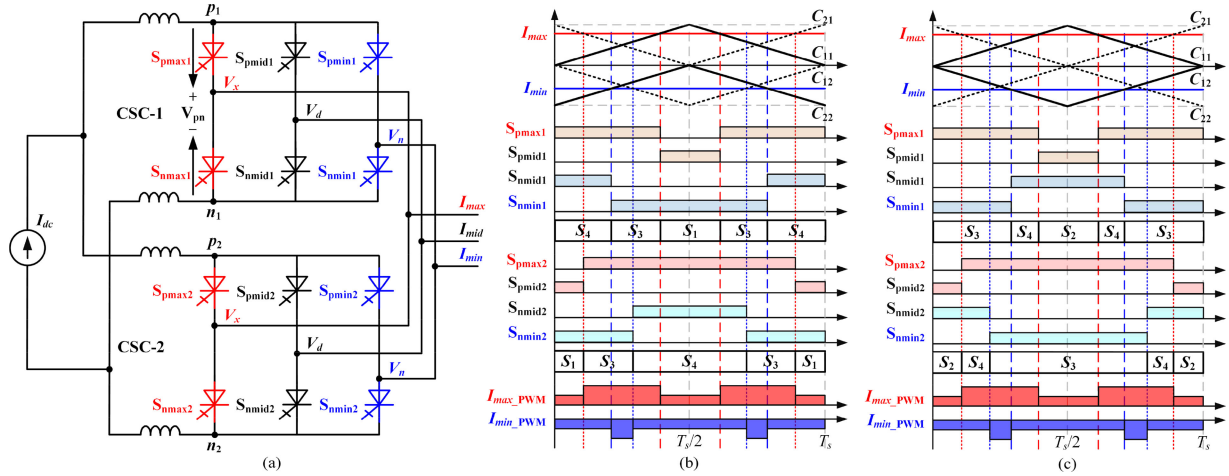

Fig. 6. Output current waveform of 2-CSC parallel system with carrier-shift DDPWM: (a) PD; and (b) POD.

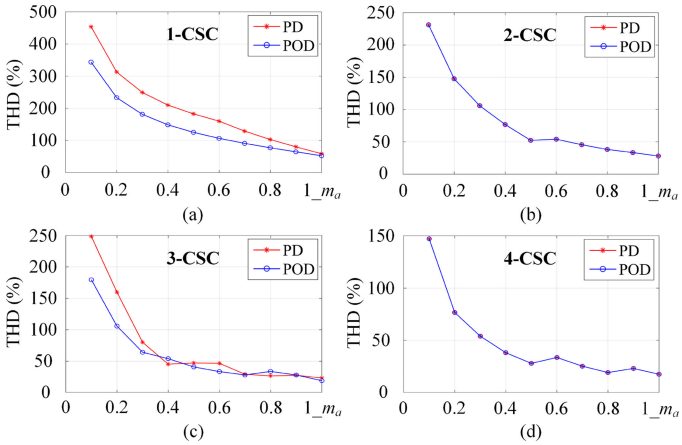

Fig. 7. THD of ac output PWM current with parallel connection. (a) Single CSC. (b) Two CSCs. (c) Three CSCs. (d) Four CSCs.

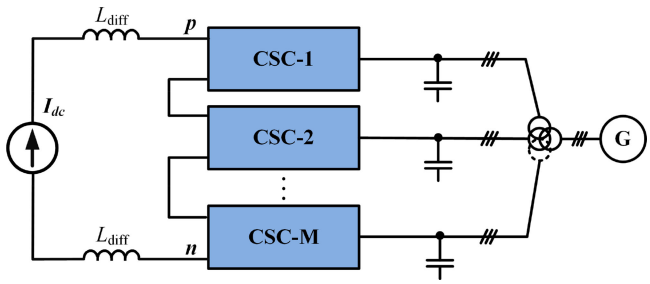

Fig. 8. Series CSC structure.

III. Proposed Series–Parallel CSC System

Based on the analysis in Section II, the carrier-shift DDPWM can be adopted in either parallel or series CSC system with improved ac outputs or dc-link voltage. The carrier-shift DDPWM is implemented for series–parallel CSC system to simultaneously improve the ac- and dc-side performances. To analyze, the paralleled CSCs are regarded as a module, and then, the paralleled modules are connected in series.

A. Sub-DC-Link Current Analysis

The paralleled module, as shown in Fig. 1, is a shared dc-link parallel structure. The sub-dc-link current in each parallel module should be balanced, otherwise, large circulating current or unequal dc current level deteriorates the output quality and even damages the semiconductor. The dc currents are influenced by the inverter-side positive and negative dc-link bus voltages, which are changed with the switching states. A detailed dc current influence with multilevel SVM was introduced in [3] which verified that the dc current could be changed with the switching state and the output voltage. Therefore, the possible switching states with carrier-shift DDPWM are analyzed to explain the dc current influence.

The positive dc bus voltage under the four switching states are $V_{\rm d}$, $V_{\rm d}$, $V_{\rm x}$, and $V_{\rm x}$, while the negative dc bus voltages are $V_{\rm n}$, $V_{\rm d}$, $V_{\rm n}$, and $V_{\rm d}$ in Max-Mid-Min phase; their values are equal to phase voltages $V_{\rm a}$, $V_{\rm b}$, $V_{\rm c}$ in A-B-C phase, according to Table I. There are 16 different switching state combinations for 2-CSC parallel system. The dc current influences with different switching state combinations are shown as Table II. The symbol "↓," "x," and "↑" represent decrease, no change, and increase.

The positive dc difference Δi_p and negative dc current difference Δi_n are not changed when the switching states of two CSCs are the same. The influences are opposite when the switching state order is exchanged, for example, the influence of combination [S_1; S_3] and [S_3; S_1] are opposite. Taking the switching sequence shown in Fig. 6(c) as an example, the PWM sequence is half-wave symmetric and the first half-sequence is [S_3; S_2]-[S_3; S_4]-[S_3; S_3]-[S_4; S_3]-[S_2; S_3]. As [S_3; S_2] and [S_2; S_3]; [S_3; S_4] and [S_4; S_3] have opposite dc current influence and their dwell time is equal, it is easy to conclude that the sub-dc current difference is closed to zero in each half-carrier cycle, as shown in Fig. 12. Therefore, the dc current can be balanced naturally with 180° interleaving angle due to the symmetry

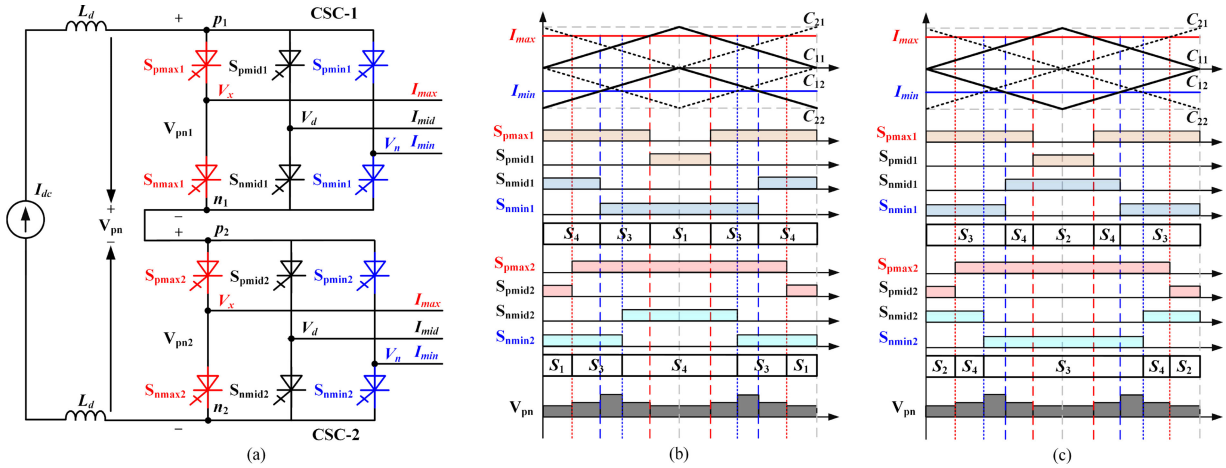

Fig. 9. DC-link voltage waveform of 2-CSC series system with carrier-shift DDPWM: (a) PD; and (b) POD.

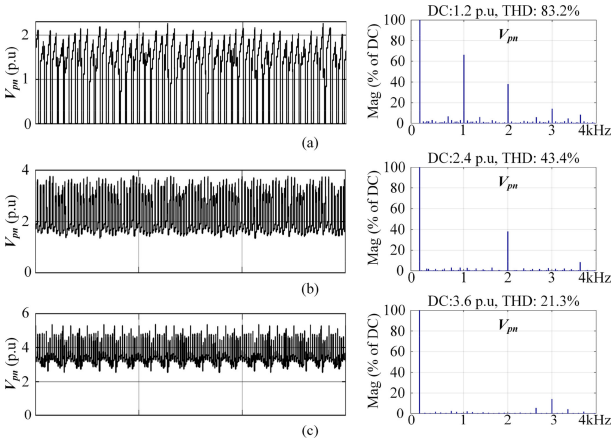

Fig. 10. DC-link voltage and harmonic distribution of POD with series connection (interleaving angle 360°/M). (a) Single CSC. (b) Two CSCs. (c) Three CSCs.

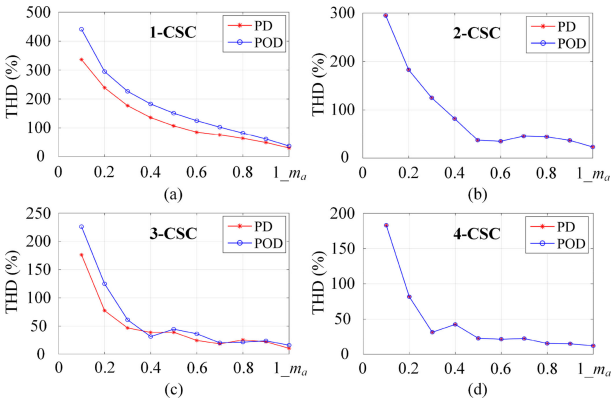

Fig. 11. THD of dc-link voltage with series connection. (a) Single CSC. (b) Two CSCs. (c) Three CSCs. (d) Four CSCs.

switching state combination. Similar analysis can be extended to *N*-CSC parallel system where the optimized interleaving angle is 360°/*N*. To actively adjust the dc current sharing error under non-ideal situations, such as parameter mismatch between parallel

TABLE II
DC CURRENT INFLUENCE UNDER SWITCHING STATES

	S_1	S_2	S_3	S_4
S_1	Δi_p: x; Δi_n: x	Δi_p: x; Δi_n: $\uparrow(V_d>V_n)$	Δi_p: $\uparrow(V_x>V_d)$; Δi_n: x	Δi_p: $\uparrow(V_x>V_d)$; Δi_n: $\uparrow(V_d>V_n)$
S_2	Δi_p: x; Δi_n: $\downarrow(V_d>V_n)$	Δi_p: x; Δi_n: x	Δi_p: $\uparrow(V_x>V_d)$; Δi_n: $\downarrow(V_d>V_n)$	Δi_p: $\uparrow(V_x>V_d)$; Δi_n: x
S_3	Δi_p: $\downarrow(V_x>V_d)$; Δi_n: x	Δi_p: $\downarrow(V_x>V_d)$; Δi_n: $\uparrow(V_d>V_n)$	Δi_p: x; Δi_n: x	Δi_p: x; Δi_n: $\uparrow(V_d>V_n)$
S_4	Δi_p: $\downarrow(V_d>V_n)$; Δi_n: $\downarrow(V_d>V_n)$	Δi_p: $\downarrow(V_x>V_d)$; Δi_n: x	Δi_p: x; Δi_n: $\downarrow(V_d>V_n)$	Δi_p: x; Δi_n: x

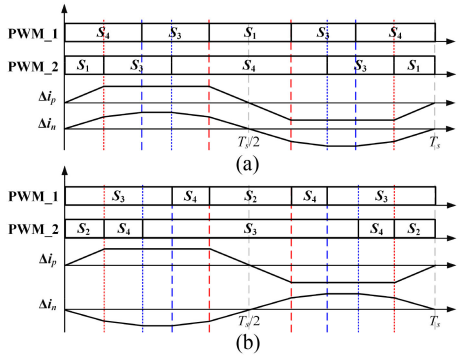

Fig. 12. Sub-dc-link current influence with carrier-shift DDPWM: (a) PD; and (b) POD.

modules as well as noninteger ratio between carrier-frequency and fundamental frequency, the active dc current balance method introduced in [21] can be simply fulfilled by exchanging the PWM sequences of the parallel CSCs alternatively.

B. Optimized Interleaving Angle Design

Consider an *M*·*N* series–parallel CSC system, where *N* CSCs are paralleled together as a parallel module and *M* parallel modules are series connected. To achieve natural dc current balance, the interleaving angle of the paralleled CSC in each

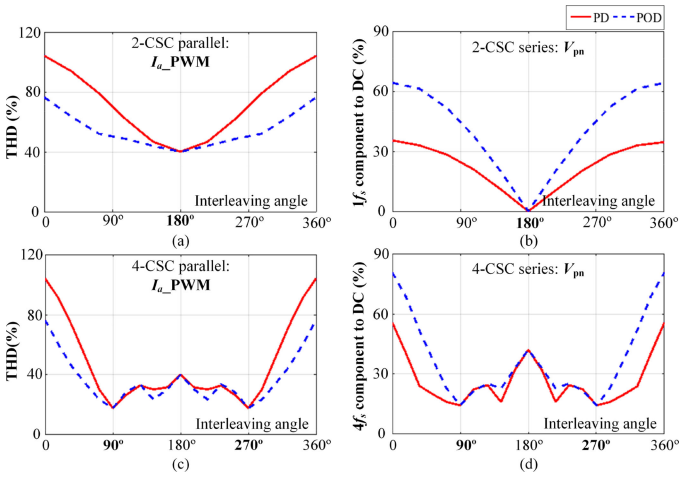

Fig. 13. THD of ac current and dc voltage ($m_a = 0.8$). (a) 2-CSC parallel. (b) 2-CSC series. (c) 4-CSC parallel. (d) 4-CSC series.

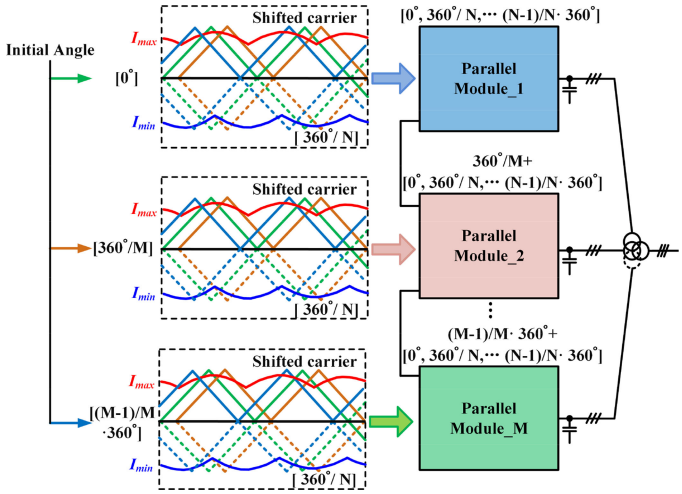

Fig. 14. Carrier-shift SPWM for modular series–parallel connected CSC system.

parallel module is 360°/*N*. To determine the best interleaving angle for a mixed series–parallel CSC system to simultaneously improve the dc-link voltage and ac outputs, the ac-side current and dc-side voltage performance with different interleaving angles are compared.

Fig. 13(a) and (c) shows the THD performance of output current PWM for 2-CSC and 4-CSC parallel system, while Fig. 13(b) and (d) shows the dominant harmonic of dc voltage for 2-CSC and 4-CSC series system with different interleaving angles. It shows that the quality of ac current and dc voltage is influenced by the interleaving angle. The best interleaving angle for 2-CSC parallel or series system is 180°, while 90° (or 270°) is the best one for 4-CSC parallel or series system (both PD and POD). Similar conclusions can be extended to *N*-CSC parallel or *M*-CSC series system, the optimized interleaving angle of each CSC should be 360°/*N* or 360°/*M* to achieve the best performance.

Therefore, the interleaving angle for mixed series–parallel CSC system should be designed properly. The interleaving angles can be divided into *M* sets, each set is assigned for the corresponding parallel module and the interleaving angle is 360°/*N*, while different sets are interleaved with 360°/*M*, as shown in Fig. 14. For example, the interleaving angles of 2-parallel 3-series CSC as shown should be divided into three sets ([0°; 180°], [120°; 300°], and [240°; 60°]), which can be assigned to each paralleled module to achieve the best ac output and dc voltage performance.

IV. Simulation and Experiment Verifications

Simulation and experiment are conducted to verify the proposed methods. The parameters of the simulation and experimental system are listed in Table III. The same *RL* load is adopted for each parallel module to verify the proposed modulation strategy. The carrier frequency with both PD and POD is 1 kHz, the output frequency is 60 Hz, and the modulation index is 0.8. The dc voltage and ac output features of the novel series–parallel CSC system are first verified with simulation results. Then, the experiment results verify the effectiveness of the proposed carrier-shift DDPWM for series or parallel CSC structures in the end.

TABLE III
Simulation and Experiment Parameters

	Parameters	Simulation	Experiment
CSI	DC current	10A	3A
	Differential inductance	10mH	10mH
	Output filter	120μF	120μF
	Output frequency	60Hz	60Hz
	Carrier frequency	1kHz	1kHz
	Modulation index	0.8	0.8
Load	Resistance	5.76Ω	5.76Ω
	Inductance	5mH	5mH

A. Simulation Results

Fig. 15 shows the simulation results for a 2 × 3 series–parallel system, where each parallel CSC module consists of two CSCs and three parallel modules are connected in series. The interleaving angles can be designed in three sets ([0°; 180°], [120°;300°], and [240; 60°]). The ac outputs (phase current PWM, phase current, and voltage) of one parallel module are shown as Fig. 15(a), from which it can be seen that each parallel module produces five-level current output and effectively reduces the THD. The harmonic distributions of current PWM and dc-link voltage are shown as Fig. 15(b) and (c), respectively. The dominant harmonic of ac output is increased to 2 kHz, while the dominant harmonic of dc-link voltage is increased to 3 kHz. The overall performance of PD and POD are similar, which is consistent with the theoretical analysis in Section II.

Fig. 16(a) shows the ac outputs and dc voltage of a 3 × 2 series–parallel system, where the interleaving angles can be designed in two sets ([0°; 120°; 240°] and [180°;300°; 60°]). As it can be seen, the current output of each parallel module is level seven and the equivalent switching frequency is 3 kHz, as shown

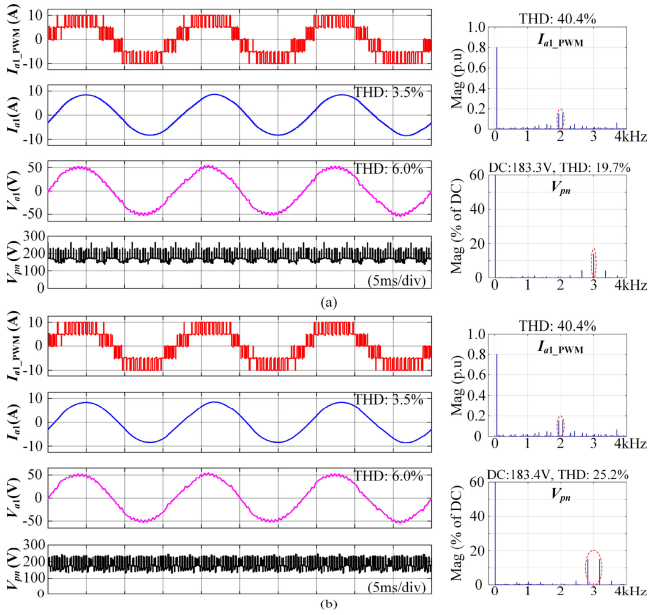

Fig. 15. Simulation results of 2-parallel 3-series CSC system: (a) PD and (b) POD.

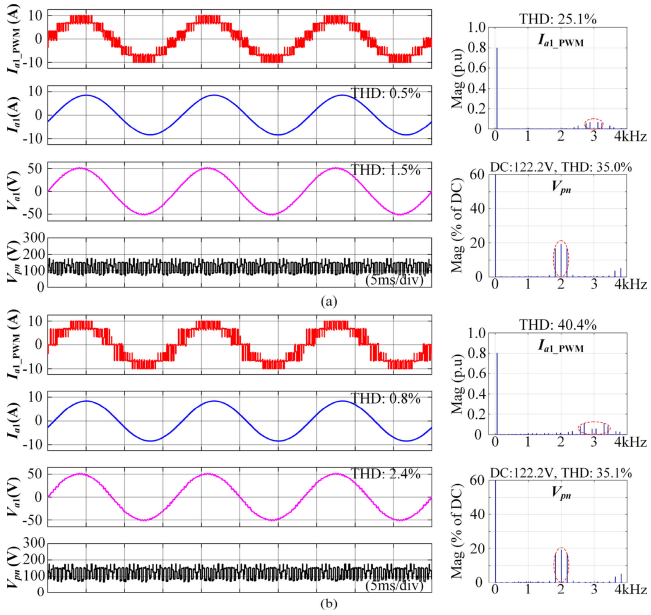

Fig. 16. Simulation results of 3-parallel 2-series CSC system: (a) PD and (b) POD.

in Fig. 16(b). PD enjoys better output quality with lower THD compared with that of POD. The dominant high-order harmonic of dc voltage is 2 kHz and PD and POD have similar dc voltage performances. The simulation results can verify that the mixed series–parallel CSC structure can simultaneously improve ac and dc performance.

B. Experiment Results

To verify the proposed carrier-shift PWM strategies, the experiments are first conducted in two parallel CSCs with shared dc-link, mainly to investigate the ac-side improvement. Then, the two CSCs can be connected in series and the dc voltage performance will be analyzed. Moreover, a 2×2 series–parallel CSC system will be investigated. The setup is designed by series connected MOSFET and diode, as shown in Fig. 17. Each parallel module contains two three-phase CSCs, and two parallel modules are connected in series. A dSPACE MicroLabBox DS1202 is adopted to generate the gating signals. Each parallel module is connected to a separate *RL* load.

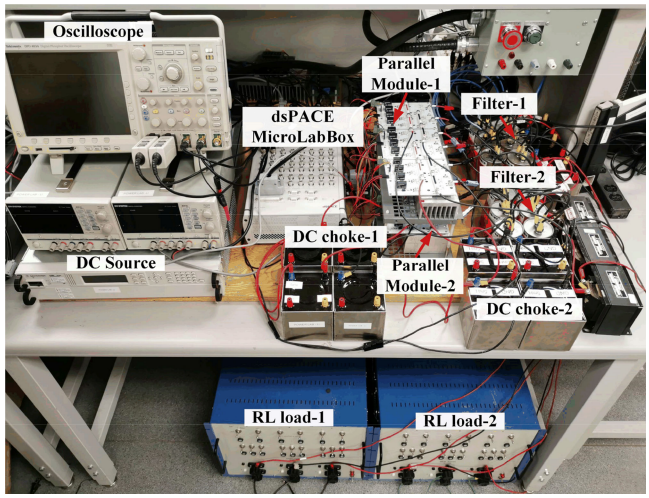

Fig. 17. Experiment setup.

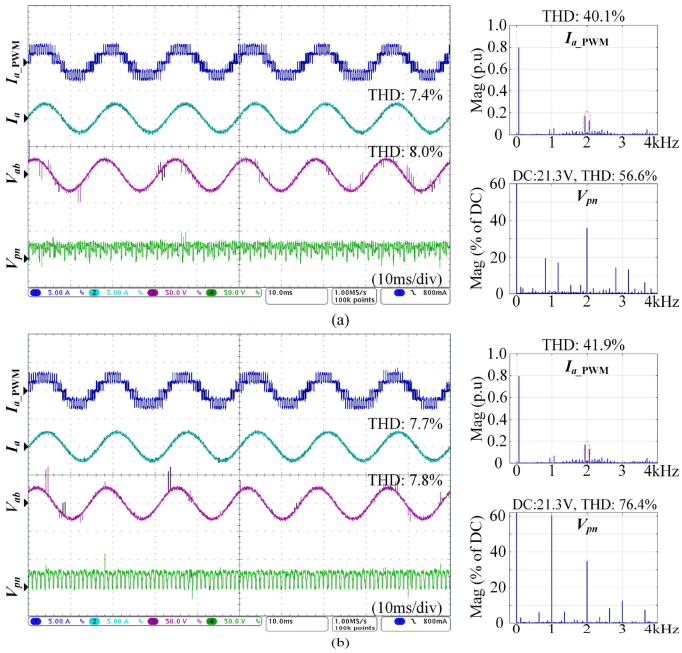

Fig. 18. Experimental results of 2-CSC parallel system with shared dc-link: (a) PD and (b) POD.

Fig. 18 shows the experimental result of 2-CSC parallel system with shared dc-link. The inverter-side dc-link voltage of CSC-1 is measured. As it can be seen, the output performances of PD and POD are similar, five-level current PWM

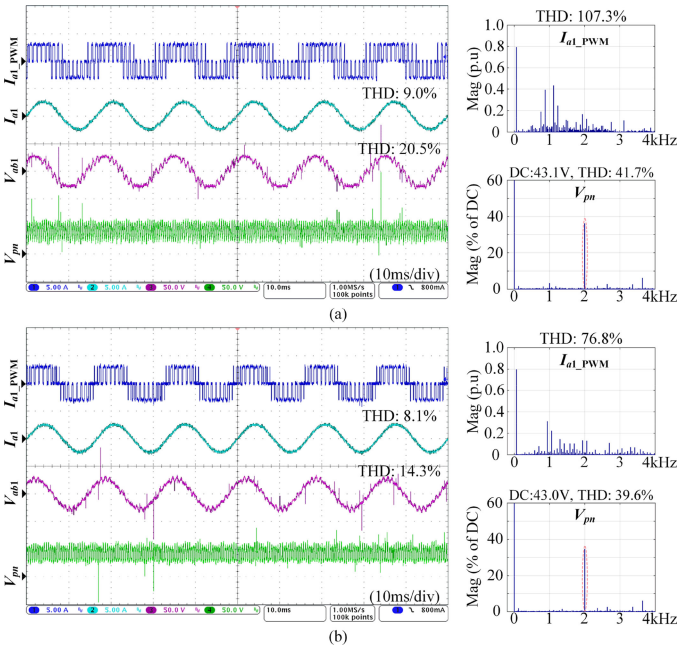

Fig. 19. Experimental results of 2-CSC series system: (a) PD; and (b) POD.

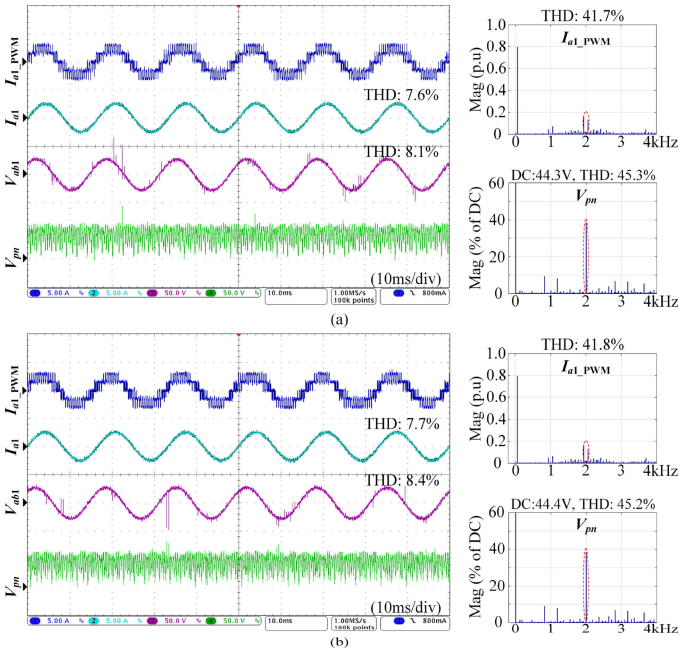

Fig. 20. Experimental results of mixed 2 × 2 series–parallel CSC system: (a) PD; and (b) POD.

can be achieved, and the THDs are 40.1% and 41.9%, which are almost the same and consistent with the PWM sequence analysis in Section II. However, PD enjoys better dc voltage performance where the 1-kHz component can be effectively suppressed compared with POD, which is consistent with the comparison results, as shown in Fig. 7.

The experiment results of a 2-CSC series system with the proposed carrier-shift DDPWM is shown as Fig. 19. The total inverter-side dc-link voltage is added up by the series CSCs. The PWM current output quality of POD (THD: 76.8%) is better than that of PD (THD: 107.3%), which results in better ac current and voltage outputs. The phase current THD is reduced from 9.0% to 8.1% and the line-to-line voltage THD is reduced from 20.5% to 14.3%. The dominate high-order harmonic of dc voltage for both PD and POD is increased to 2 kHz and the THD performances are similar.

Fig. 20 shows the experimental results of mixed series–parallel CSC system by adopting carrier-shift DDPWM with PD and POD, respectively. The interleaving angles are designed as two sets ([0°, 180°]; [180°, 0°]). The inverter-side dc-link voltage is measured between the positive dc bus of CSC-11 and negative dc bus of CSC-21, as indicated in Fig. 1. As it can be seen, each parallel module can achieve five-level current output and the equivalent switching frequency is 2 kHz. Meanwhile, the dominant high-order harmonic of dc voltage is 2 kHz. It verified that the mixed series–parallel structure with carrier-shift DDPWM can guarantee better ac output and dc voltage simultaneously. The harmonic performance of PD and POD are very close, the THD of output current is 41.7% and the THD of dc voltage is 45.3% for PD, while they are 41.8% and 45.2% for POD. Since the parallel and series module number are both even, and the outputs of PD and POD are totally the same, which is also consistent with the theoretical analysis.

V. Conclusion

This article proposed a novel multilevel CSC structure based on series–parallel connected module to increase the system power rating and reliability. Parallel modules can generate multilevel output, while the dc voltage quality can be improved due to series connection with carrier-shift SPWM. Therefore, the novel series–parallel structure can achieve better ac and dc performances simultaneously with proper interleaving angle design. The improved performance can reduce the sizes of dc- and ac-side filters potentially. Other inherent advantages along with the carrier-shift DDPWM, such as small CMV, circulating current, and natural dc current balance ability, can further make the proposed structure an attractive candidate for high power applications, such as MV drives, offshore wind power, and HVdc application. Future research will focus on the control method and fault tolerance strategy development.

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