Letters

Low MOSFET Count Isolated DC–AC Converter

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***Abstract*—This letter proposes a novel soft-switched single-stage-isolated dc–ac converter topology from the industry point of view. The proposed converter requires a lesser number of MOSFETs compared to a widely studied cycloconverter-type (CCT)-isolated dc–ac converter topology. This converter provides lower duty cycle loss, better efficiency, and electromagnetic interference performance compared to a CCT dc–ac converter. Also, it is thermally more stable, thus requires a smaller heat sink. The converter operation is demonstrated in a 1-kW prototype developed with SiC MOSFETs.**

***Index Terms*—Isolated dc–ac, single stage, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

UNINTERRUPTIBLE power supply (UPS) industry is always in search of innovative isolated dc–ac converter topologies that can boost the efficiency and power density without compromising the reliability. There are several isolated dc–ac power converter topologies reported in the literature, which can be broadly classified into conventional two-stage and relatively new single-stage solutions [1]–[8].

The two-stage dc–ac converters employ a front-end-isolated dc–dc stage followed by a sine wave inverter [1]–[3]. Many manufactures prefer dual active bridge (DAB)-type dc–dc configuration to achieve higher efficiency especially for power more than 3 kW [1], [2]. This approach requires eight switches, which increases the development cost. As a cost-effective solution, half-bridge-type DAB with four switches is proposed in [3]. In many products, the secondary side active bridge is replaced by a diode bridge rectifier for further cost reduction. Although these converters provide desired performance, they have following two major concerns from a product perspective.

1) A bulky electrolytic capacitor bank is necessary to integrate the dc–dc stage and dc–ac inverter, which reduces the power density. Typically, the standard electrolytic capacitors are rated for 105 °C. Thus, a lot of design efforts go into thermal management to achieve a longer product life.
2) The control complexity is high. It requires an additional dc voltage sensor to regulate the output of the dc–dc stage.

In the recent past, academia showed a great interest to address these issues by proposing many single-stage dc–ac converter solutions that eliminate the intermediate dc-link capacitors and additional voltage sensors. These converters are mostly either pulsating dc type (PDT) or cycloconverter-type (CCT) dc–ac converters [4]–[8], [11]–[15]. In PDT converters, the dc-link capacitors at the output of the dc–dc stage are eliminated and a pulsed dc voltage is generated. This voltage is converted to an ac voltage by a low-frequency unfolder circuit [4], [5], [15].

The CCT single-stage dc–ac converters are widely explored in academia, which requires a full bridge at the dc side and a cycloconverter at the ac side [6]–[8]. Although these single-stage converters attempt to address the issues of conventional two-stage solutions, they are not that popular in the industry due to following major reasons.

1) *Component Count and Loss:* The CCT single-stage dc–ac converter requires 12 MOSFETs for a single-phase system [6]. Such a high switch count reduces efficiency.
2) *Duty Cycle Loss:* The CCT converters can provide natural commutation for the current through leakage inductor and the output ac inductor avoiding the requirement of snubber circuit [6]. However, the output voltage becomes zero during this commutation interval resulting in duty cycle loss, which reduces the average output ac voltage.
3) *Electromagnetic Interference (EMI) Performance:* High switch count adversely affects the EMI performance of the single-stage CCT dc–ac converter. Thus, bulky EMI filters are required [9].
4) *Thermal Management:* More number of switching components increases the average heat sink temperature.

This letter proposes an isolated single-stage dc–ac converter topology addressing the aforementioned issues observed in conventional CCT dc–ac converters for industrial implementation. The improved features of the proposed converter are as follows.

1) The MOSFET count is reduced by two.
2) Duty cycle loss is drastically minimized for same power.
3) Converter operates under soft switching (SS).
4) The CE peak is reduced by 12 dB·μV.
5) Average heat sink temperature is reduced by 10 °C.

This letter focuses on the converter operation for unity power factor load.

II. Topology, Operation, and Control

A. Topology Configuration

The proposed single-stage dc–ac converter topology is shown in Fig. 1. It consists of a half-bridge (M_{p1-p4}) at the dc side and a low MOSFET count cycloconverter (M_{s1-s6} and D_{s1-s4}) at the ac

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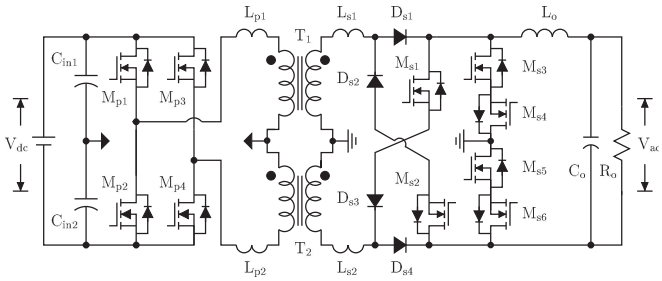

Fig. 1. Circuit configuration of the proposed single-stage dc–ac converter.

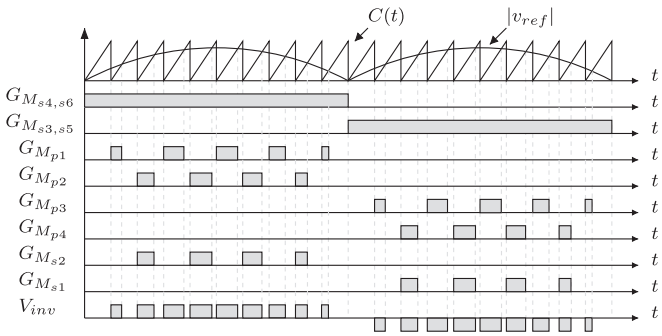

Fig. 2. Gate signals for different switches in the proposed dc–ac converter.

side. These units are isolated through two transformers (T_1 and T_2) each rated for half of the power rating. The operating devices can be categorized into two groups depending on the polarity of the output ac current. The devices M_{p1}, M_{p2}, M_{s2}, D_{s1}, D_{s2}, and transformer T_1 operate during positive half-cycle. Similarly, M_{p3}, M_{p4}, M_{s1}, D_{s3}, D_{s4}, and transformer T_2 operate during negative half-cycle.

The dc-side devices (M_{p1}–M_{p4}) are modulated with a modulating signal

$$m(t) = |v_{\text{ref}}| = (2V_{\text{ac}}/nV_{\text{dc}})|\sin 2\pi f t| \tag{1}$$

to generate an average output ac voltage of $\pm nV_{\text{dc}}m(t)/2$, where $V_{\text{ac}}\sin 2\pi f t$ is the desired output ac voltage, V_{dc} is the input dc voltage, and n is the transformer turns ratio. The ac-side devices unfold the high-frequency ac voltage to 60-Hz ac voltage. The devices M_{s3}–M_{s6} operate at 60 Hz with no switching loss. The devices M_{s4} and M_{s6} are kept ON for positive half-cycle, and the devices M_{s3} and M_{s5} are ON for negative half-cycle of the output ac current. The gate signals of the secondary side devices M_{s1} and M_{s2} are synchronized with the primary-side devices M_{p4} and M_{p2}, respectively. The detailed gate signals of all devices can be seen in Fig. 2. The converter operation in a switching cycle during positive polarity of output ac current is discussed here.

B. Converter Operation

1) Mode 1 [see Fig. 3(a)]: In this mode, the device M_{p1} is turned ON and M_{p2} is turned OFF impressing a voltage of $V_{\text{dc}}/2$ in the primary winding of T_1. At the secondary end, the diode D_{s1}, device M_{s6}, and body diode of M_{s5} conduct allowing the rise of output inductor current i_{ac}. The incremental change in i_{ac} is given by

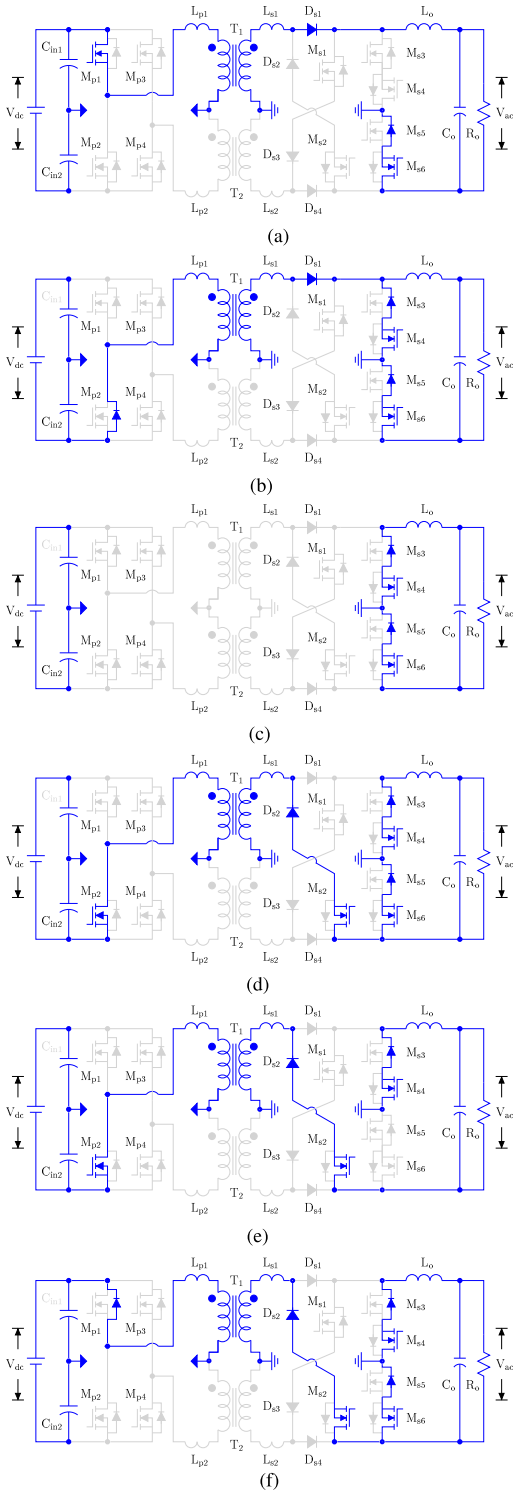

Fig. 3. Different operating modes of the proposed low switch count single-stage dc–ac converter. (a) Mode 1. (b) Mode 2(a). (c) Mode 2(b). (d) Mode 3(a). (e) Mode 3(b). (f) Mode 4.

$$\Delta i_{\text{ac}} = \frac{nV_{\text{dc}} - 2V_{\text{ac}} - 2(V_{f1} + V_{f2})}{2(L_o + L_{s1})}(\Delta t_1) \tag{2}$$

where V_{f1} is the body diode drop of the device M_{s5}, and V_{f2} is the diode D_{s1} voltage drop. The output capacitor of the device M_{s3} is charged to $nV_{\rm dc}/2$ and its body diode blocks this voltage.

2) Mode 2(a) [see Fig. 3(b)]: This transient state begins with the turn OFF of the device M_{p1} to introduce a zero state. The leakage inductor L_{p1} energy discharges the output capacitor of M_{p2} leading to a momentary turn ON of its body diode. In the secondary side, the inductor L_o energy discharges the output capacitor of the device M_{s3} leading to its body diode conduction. The transient voltage across the device M_{s3} can be simplified as

$$v_{s3}(t) = nV_{\rm dc}/2 - v_{Ls1}(t) - (i_{\rm ac}/C_{s3})(t) \tag{3}$$

where v_{Ls1} is the voltage across leakage inductor L_{s1}, and C_{s3} is the output capacitor of M_{s3}. The time taken to complete this transition can be written as

$$\Delta t_{2a}{}' = (nV_{\rm dc}/2 - v_{Ls1} - V_f)C_{s3}/i_{\rm ac} \tag{4}$$

where V_f is the body diode drop of the device M_{s3}. At the same time, L_{s2} energy is dissipated through the diode D_{s1}.

3) Mode 2(b) [see Fig. 3(c)]: This is a freewheeling/zero state, where the energy of L_{p1} and L_{s1} are fully dissipated. The diode D_{s1} experiences a soft turn OFF with no reverse recovery loss due to L_{s1}. The output ac current freewheels through M_{s4}, M_{s6} and body diodes of M_{s3} and M_{s5}. At this time, the devices M_{s3} and M_{s5} can also be turned ON to achieve synchronous rectification.

4) Mode 3(a) [see Fig. 3(d)]: At the end of zero interval, the device M_{s2} is turned ON first. It experiences zero current switching (ZCS) turn ON as there is no active voltage applied from the primary side, and the output ac current continues to freewheel. After this event, the device M_{p2} is turned ON impressing $-nV_{\rm dc}/2$ voltage across T_1. The current through L_{s1} rises. The output ac current continues to freewheel in the loop discussed in mode 2(b). In this mode, the transformer secondary voltage V_{s2} and output voltage of the cycloconverter $V_{{\rm in}v}$ are given by

$$V_{s2} = -nV_{\rm dc}/2, \text{and} \tag{5}$$

$$V_{{\rm in}v} \simeq -2V_f \approx 0. \tag{6}$$

5) Mode 3(b) [see Fig. 3(e)]: This mode begins when the leakage inductor L_{s1} current becomes equal to the output ac current $i_{\rm ac}$. As a result, the body diode of the device M_{s5} turns OFF naturally under ZCS. Its output capacitor is charged to $nV_{\rm dc}/2$ voltage and it blocks this voltage. This smooth energy transfer between the leakage inductor L_{s1} and the output inductor L_o provides natural commutation. Thus, eliminates the need for snubber capacitors. The power is transferred from the dc-to-ac side at the end of this commutation process.

6) Mode 4 [see Fig. 3(f)]: This mode is similar to mode 2, and it starts with turn OFF of the device M_{p2}. The energy of inductors L_{p1} and L_o discharges the output capacitors of M_{p1} and M_{s5}, respectively, causing the turn ON of their body diodes. The output ac current begins to freewheel through the devices M_{s4}, M_{s6} and body diodes of M_{s3}, M_{s5}. The current through D_{s2} and M_{s2} reduces with a slope of $V_{\rm ac}/L_{s1}$. Thus, the diode D_{s2} does not exhibit reverse recovery loss. The gate pulse of the device M_{s2} is revoked once the current through L_{s1} drops to zero providing ZCS OFF.

In summary, the devices M_{s3}–M_{s6} operate at 60 Hz contributing to only conduction loss. Their body diodes are soft-switched due to natural commutation. The diodes D_{s1} and D_{s2} and device M_{s2} also operate under ZCS. The devices M_{p3}, M_{p4}, M_{s1}, D_{s3}, and D_{s4}, and transformer T_2 stay idle during positive half-cycle. Thus, no loss, heat, and noise generation is involved with these components.

C. Soft Switching Design

1) Devices M_{s1} and M_{s2}: The devices M_{s1} and M_{s2} experience ZCS during both turn-ON and -OFF instants. As discussed in mode 3(a), the device M_{s2} is turned ON during freewheeling state irrespective of load condition. Thus, it does not see any device current transition resulting ZCS ON.

The device M_{s2} is turned OFF in mode 4. Its gate pulse is revoked only after the device current drops to zero naturally. This transition time is a function of the magnitude of the instantaneous device current, leakage inductor, and the device voltage as given in (7). This duration is maximum at the peak of output ac current. Considering the prototype parameters, the maximum limit of this duration is calculated as

$$t_{{\rm off},M_{s1,s2}} = \frac{2 \times L_{s1} \times \Delta i_{\rm ac}}{nV_{\rm dc}} = \frac{2 \times 4 \times 10^{-6} \times 10}{0.8 \times 300} = 333 \text{ ns}. \tag{7}$$

Thus, a minimum commutation interval of 350 ns is selected to ensure ZCS OFF at all load conditions (up to 1 kW) in the developed prototype. This discussion is also applicable to the device M_{s1}.

2) Devices M_{s3}–M_{s6}: These devices are ON for 50% duration of the power cycle. The switching takes place at zero crossing of the output ac current. Thus, these devices incur only conduction loss.

3) Diodes D_{s1}–D_{s4}: The diodes D_{s1}–D_{s4} always turn OFF during freewheeling states, where the diode current naturally transfers to the freewheeling branch formed by the devices M_{s3}–M_{s6}. The diode current transfer rate is governed by the leakage inductors L_{s1} and L_{s2}. This controlled decaying current provides negligible reverse recovery loss.

4) Devices M_{p1}–M_{p4}: The turn-ON zero voltage switching (ZVS) of the devices M_{p1}–M_{p4} is a function of modulation index, the primary-end leakage inductor value ($L_{p1,p2}$), and the power level. It is possible to achieve ZVS only at higher power level near peak of the output ac current, where the duty is large. In this scenario, the devices can be turned ON while their body diodes conduct providing ZVS ON. Fig. 4 depicts the possible ZVS ON range for the devices M_{p1}–M_{p4} plotted between the modulating signal and output ac current angle at different leakage inductor values at rated 1-kW power considering the developed prototype specifications.

D. Converter Control

Fig. 5 depicts the control block for the proposed single-stage dc–ac converter operating in the current control mode. The controller is implemented with the integration of a repetitive controller (RC), and a proportional–integral (PI) controller. The RC eliminates the periodic errors as it improves the present trial using the information from the previous trial. Thus, provides

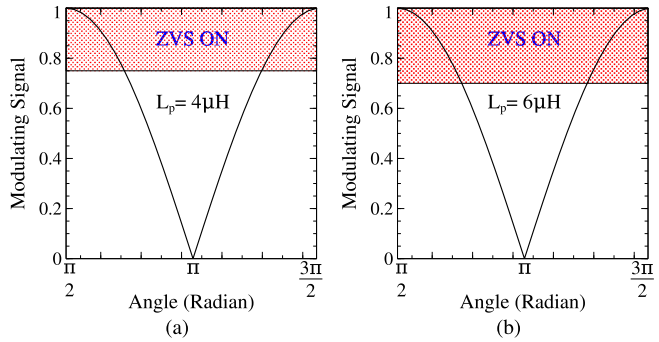

Fig. 4. ZVS ON range for the devices M_{p1}–M_{p4}. (a) $L_{p1,p2} = 4$ μH. (b) $L_{p1,p2} = 6$ μH.

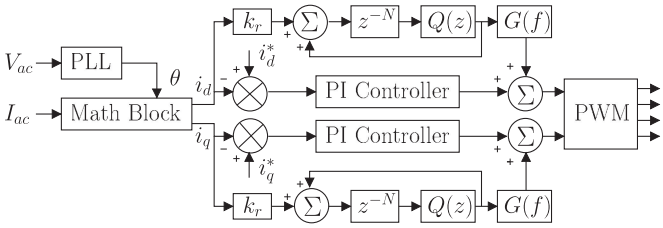

Fig. 5. Implemented control block diagram.

zero steady-state error tracking [10]. The repetitive controller $G_{\text{RC}}(z)$ with a phase lead compensation is given by

$$G_{\text{RC}}(z) = k_r \frac{z^{-N}Q(z)}{1 - z^{-N}Q(z)} G_f(z) \tag{8}$$

where k_r : RC gain, N : f_g/f_s and Q_z : first-order low-pass filter. The filter G_f increases closed-loop stability. The $G_{\text{RC}}(z)$ can be simplified as

$$G_{\text{RC}}(z) = k_r \frac{z^{-(f_g/f_s)}(\alpha_1 z^{-1} + \alpha_0 + \alpha_1 z)}{1 - z^{-(f_g/f_s)}(\alpha_1 z^{-1} + \alpha_0 + \alpha_1 z)} G_f(z) \tag{9}$$

where $2\alpha_1 + \alpha_0 = 1$, $\alpha_0 \geq 0$ and $\alpha_1 \geq 0$.

The output of RC is added with the current PI controllers, and used to generate PWM for the devices M_{p1}–M_{p4}. The gate pulses for M_{s1} and M_{s2} are synchronized with devices M_{p4} and M_{p2}, respectively. The gate pulses for the devices M_{s3}–M_{s6} are derived from the phase-locked loop information.

III. Experimental Results and Analysis

A 1-kW prototype is developed using 650-V SiC MOSFETs to validate the performance of the proposed single-stage isolated dc–ac converter. The dc-bus voltage is 300 V and the output ac voltage is 120 V, 60 Hz. Transformers are rated for 500 W each. Prototype specifications are listed in Table I.

TABLE I
Prototype Specifications

Parameters	Symbol	Value
Output power	P_o	1kW
Input voltage	V_{dc}	300V
RMS ac voltage	$V_{\text{ac,rms}}$	120V
AC voltage frequency	f	60Hz
Switching frequency	f_s	110kHz
Output inductor	L_o	480μH
Leakage inductor	$L_{p,s}$	4μH
Input capacitor	C_{in}	270μF
Components	**Value**	
SiC MOSFET	V_{DS} = 650 V, I_{D} = 27 A,	
CREE C3M0060065D	R_{DSon} = 60 mΩ, C_{oss} = 80 pF	
SiC Schottky Diode	V_{RRM} = 600 V, I_{F} = 24 A,	
CREE C3D08060A	V_{F} = 1.5 V, Q_{C} = 20 nC	

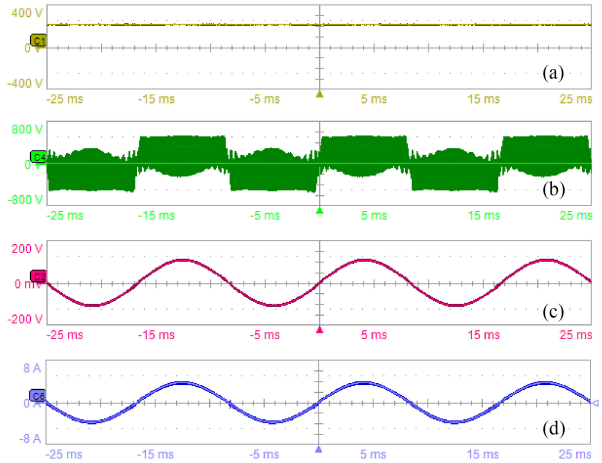

Fig. 6. Converter Performance-I. (a) Input dc voltage. (b) Cycloconverter output voltage. (c) Output ac voltage. (d) Output ac current.

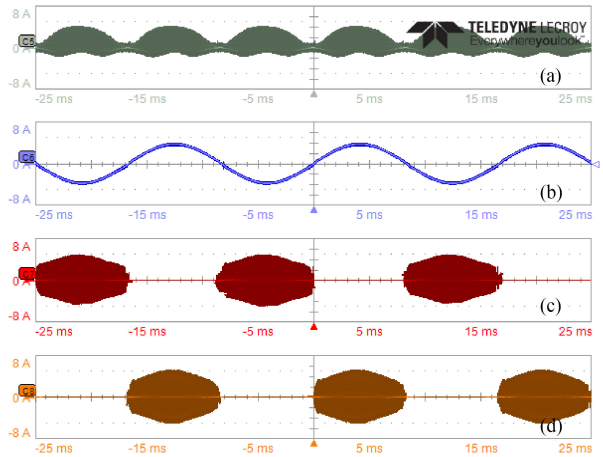

Fig. 7. Converter Performance-II. (a) Input dc current. (b) Output ac current. (c) Transformer T_2 current. (d) Transformer T_1 current.

A. Results

Fig. 6 shows the terminal characteristics of the proposed converter in steady state. The sine-modulated output voltage of the cycloconverter is depicted in plot 2. The output 60-Hz ac voltage and current waveforms are shown in plot 3 and 4, respectively. Various current waveforms are shown in Fig. 7. Plot 1 shows the input dc current and plot 2 depicts the output 60-Hz ac current. The transformer T_2 and T_1 currents are shown in plots 3 and 4, respectively. It is important to note here that the transformer T_1 is active only during the positive half-cycle of the output ac current. Similarly, the negative half-cycle is supported by the transformer T_2. These operating functions ensure

Fig. 8. ZCS turn-OFF switching performance for device M_{s2}. (a) Gate voltage. (b) Device current.

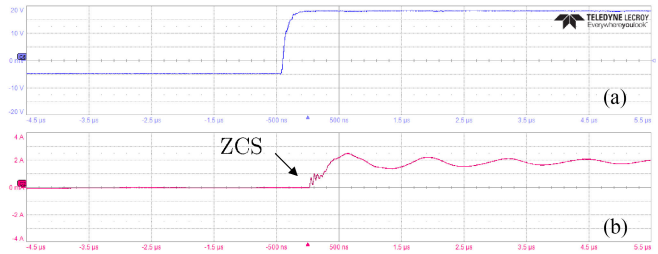

Fig. 9. ZCS turn-ON switching performance for device M_{s2}. (a) Gate voltage. (b) Device current.

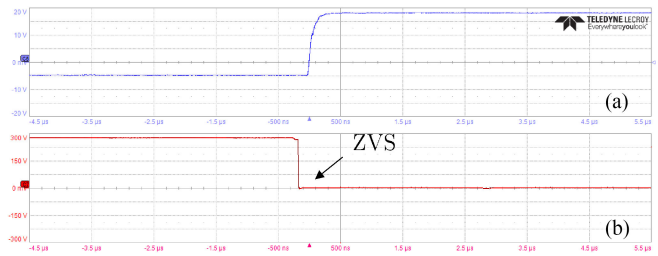

Fig. 10. Turn-ON SS performance for device M_{p1} at peak of output ac current. (a) Gate voltage. (b) Device voltage.

that the components are only active for 50% time. This action provides improved performance compared to conventional CCT converters as discussed ahead.

The SS performance of the device M_{s2} is depicted in Figs. 8 and 9. The gate pulse of the device M_{s2} is revoked after its current drops to zero naturally during mode 4 giving a ZCS OFF instant, as shown in Fig. 8. In mode 3(a), the output ac current freewheels through the devices $M_{s3}-M_{s6}$. In this instant, the device M_{s2} is turned ON providing ZCS response, as depicted in Fig. 9. The similar responses are also observed for device M_{s1} during both turn-ON and -OFF instants. The primary-side devices can experience ZVS near peak of the output ac current where the energy stored in the primary end leakage inductor is large. The ZVS turn ON of the device M_{p1} is depicted in Fig. 10.

B. Performance Analysis and Comparison

1) THD, Loss, and Efficiency Analysis: The output ac current THD is shown in Fig. 11(a), which is well within 2.5% at different loading conditions.

The proposed topology requires 4 diodes and 10 MOSFETs. However, it is equivalent to 2 diodes and 7 MOSFETs from

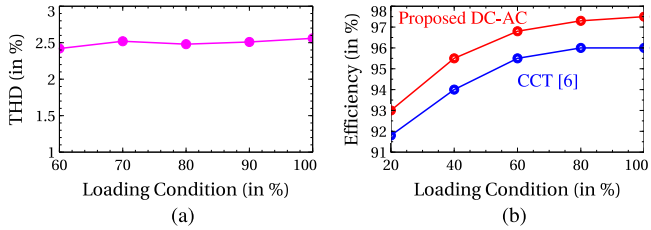

Fig. 11. (a) THD of the output ac current. (b) Efficiency comparison.

TABLE II
LOSS COMPARISON BETWEEN CCT AND PROPOSED TOPOLOGY AT 1 kW

Loss	CCT (in W)	Proposed (in W)
DC side conduction	2.2	1.6
DC side switching	3.5	2.5
Transformer	12.4	9.6
AC side switching	8.48	3.17
AC side conduction	8.05	7.08
Others	5.45	4.05
Total Loss	40.08W	28W
Efficiency	95.99%	97.2%

loss point of view. From the previous discussion, the MOSFETs $M_{s3}-M_{s6}$ operate over complete cycle. However, diodes D_{s1}, D_{s2} and MOSFET M_{s1} operate only in positive half-cycle. Similarly, D_{s3}, D_{s4}, and M_{s2} operate in negative half-cycle. Thus, they contribute to loss only for half of the 60-Hz cycle. So, if complete cycle is considered, the total loss is equivalent to the loss generated by two diodes and one MOSFET for this section. Similarly in the dc side, two MOSFETs are active only for half of the cycle. So, the total loss in a cycle for this section is equivalent to only two MOSFETs. If we account these phenomena, total loss generated in the proposed topology is equivalent to two diodes and seven MOSFETs, a total of nine switches. Thus, the low loss and high efficiency is achieved.

The loss break down of the proposed converter is compared with conventional 12 switch CCT topology operated with the switching scheme reported in [6]. The compared results can be seen in Table II. This loss break down information is collected from another prototype based on the CCT topology at same specifications that of the proposed topology. It can be noticed that the proposed topology provides an efficiency of 97.2% at 1-kW power. The efficiency comparison between different topologies is presented in Fig. 11(b).

2) Duty Cycle Loss: It is the phenomenon where the cycloconverter output remains zero though active voltage is supplied to the transformer. It happens in mode three during natural commutation process. The current through L_{s1} gradually increases when an active voltage is applied to the transformer T_1. At the same time, the output ac current continues to freewheel through the loop discussed in mode 2(b). In this instant, the cycloconverter output remains zero until L_{ks1} current becomes equal to the output ac current resulting loss in output voltage. Once these currents becomes equal, the body diode of M_{s5} gets reverse biased and the output voltage rises to $nV_{\rm dc}/2$.

This commutation duration in a switching cycle is given by

$$\Delta t_l = \frac{4 \times L_s |I_{\rm ac} \sin 2\pi f t|}{nV_{\rm dc}} \tag{10}$$

TABLE III
TOPOLOGY COMPARISON

Parameters	[15]	[6]	[13]	[8]	[11]	[12]	Proposed
MOSFET Count	8	12	12	16	12	14	10
Diode Count	5	-	-	3	-	4	4
Transformer	1	1	1	3	1	3	2
Switching Logic	HS	SS	SS/HS	SS	SS/HS	SS/HS	SS
Maximum Efficiency	-	96%	92%	96.6%	88.8%	94.2%	97.2%

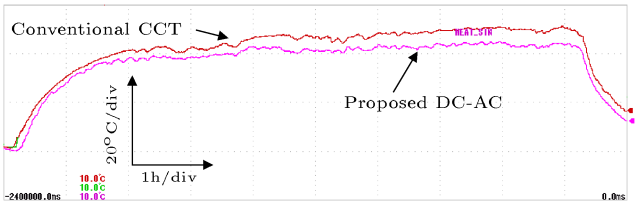

Fig. 12. Thermal comparison test results.

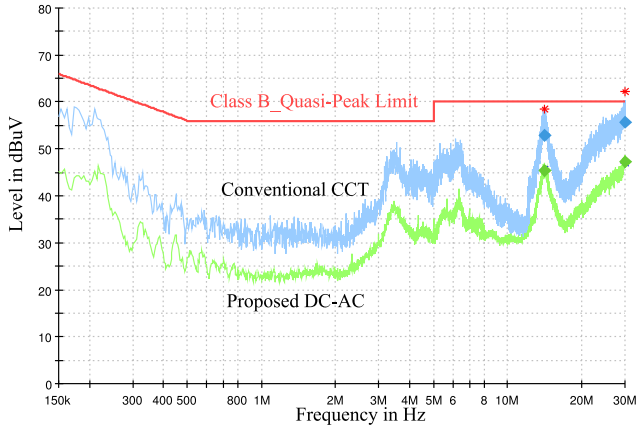

Fig. 13. CE comparison between CCT and proposed dc–ac.

with a reduction in average output voltage given by

$$V_g = V_{\rm ac}\sin 2\pi f t - 2 f_s n V_{\rm dc} \Delta t_l. \tag{11}$$

It can be noticed from (11) that this loss is directly proportional to the leakage inductor L_s value. Unlike conventional CCT with single transformer, the proposed converter uses two half-rated transformers, which require lesser turns and thinner wire gauge. Thus, can provide very low leakage inductance compared to a CCT transformer. The proposed converter reduces the duty cycle loss by 40% with smaller transformer at 1 kW.

3) Thermal Management: A detailed thermal analysis has been conducted on the proposed converter. Type-T thermocouple is placed on each devices to measure the individual case temperature using a Yokogawa data accusation system. It is then averaged to find the average device case temperature. This test is conducted over 5 h at room temperature of 25 ° C. Similar test is repeated on the prototype with traditional CCT topology. Fig. 12 depicts the thermal comparison results. It can be noticed that 10 ° C reduction is achieved by the proposed converter. This reduction in temperature is attributed to a 50% reduction in operating time of various devices as discussed earlier. This helps in heat sink size optimization.

4) EMI Performance: Fig. 13 depicts the conducted emission (CE) test results obtained from the proposed dc–ac converter and CCT converter with respect to class B quasi-peak limit at 1 kW. The same standard CLC-type EMI filter is used for both prototypes. The X and Y cap values are 1 μF and 4.7 nF, respectively. The common-mode choke is of 15 mH. An average 12-dBμV reduction in CE is achieved by the proposed dc–ac converter due to the reduction in number of switching instants. This helps in reducing EMI filter size.

5) Topology Comparison: The proposed topology is compared with other relevant single-stage dc–ac converter topologies, as listed in Table III. It can be noticed that it requires lesser number of MOSFETs operating in soft-switching (SS). The achieved efficiency is very competitive.

6) Cost and Development: The proposed converter requires 10 MOSFETs compared to 12 MOSFETs used in conventional CCT converters [6]. It is important to note here that the devices M_{s3}–M_{s6} are always ON for half the duration in a 60-Hz cycle exhibiting only conduction loss. Therefore, instead of high-cost SiC MOSFETs, low-cost CoolMOS can be selected. Also, the cost involved in the gate driver circuit is reduced as the MOSFET count is reduced by two in the proposed topology. The secondary-side diodes experience a slow decaying current during turn OFF. Thus, provides negligible reverse recovery loss. Therefore, low-cost ultrafast switching diodes can be selected instead of high-cost SiC Schottky diodes. Although this topology requires two transformers, they are only half rated. So, the cost and volume are not very high compared to single full power transformer. Another advantage of selecting two smaller transformers is that it provides better mechanical reliability than a single bulky transformer during vibration and shock, which is a standard test in UPS industry. In addition, it requires small volume heat sink, as the average operating temperature is reduced by 10 ° C shown in Fig. 12.

IV. CONCLUSION

This letter proposes a single-stage isolated dc–ac converter with a target of industrial implantation. It addresses the shortcomings of conventional single-stage CCT converters. The converter performance is evaluated in a 1-kW prototype. Compared to the conventional CCT, the MOSFET count is reduced by two. The duty cycle loss is reduced by 40%. The average device case temperature is reduced by 10 °C. It also provides a better CE response with a noise reduction of 12 dB·μV. The peak efficiency of the proposed converter is 97.2%. These advancements can help in developing a low-cost and reliable product for UPS applications.

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