Low Common-Mode Noise Full-Bridge *LLC* Resonant Converter With Balanced Resonant Tank

Keon-Woo Kim, *Student Member, IEEE*, Yeonho Jeong, *Member, IEEE*, Jae-Sang Kim, *Student Member, IEEE*, and Gun-Woo Moon, *Member, IEEE*

***Abstract*—This article proposes a low common-mode (CM) noise full-bridge *LLC* resonant converter with two balanced resonant tanks. In the proposed converter, each resonant inductor and capacitor is divided into two components with the same value. The CM current flowing through parasitic capacitors of the transformer is reduced due to the balanced resonant tank. Moreover, the CM noise can be significantly reduced by adjacently locating the primary and secondary layers with the same *dv/dt* characteristic. Therefore, the proposed converter decreases the CM noise generated from the planar transformer (PT) by the balanced resonant tank and proposed layer arrangement of PT and achieves a high power density with a decreased size of the electromagnetic interference filter. The validity of the proposed converter is verified by a 1.5-kW prototype with 400-V input and 270–420-V output.**

***Index Terms*—Common mode (CM) noise, planar transformer (PT), LLC resonant converter.**

I. Introduction

COMMON-MODE (CM) noise in power converters generates an electromagnetic interference (EMI), which can disrupt electronic devices, equipment, and systems [1]. In order to mitigate the EMI issue, the EMI filter, including the CM choke and *Y*-capacitor, is required. Despite the necessity of the EMI filter, it can be a burden of power density because the size of the EMI filter becomes larger as the level of CM noise becomes higher [2]. Therefore, a low CM noise is necessary for a high-power-density converter.

The CM noise is mostly caused by the CM current flowing through parasitic capacitors with high *dv/dt* nodes, such as the parasitic capacitors of MOSFETs and transformer [3]–[6]. Among them, the parasitic capacitors of the transformer present a high level of CM current. Especially, the planar transformer (PT) has a much larger parasitic capacitance comparing with the wire-wound transformer because the overlapped area of the layer in the PT is much wider. A large capacitance with large *dv/dt* difference between parasitic capacitors results in severe CM noise. Although the PT is an attractive solution for designing a small volume of magnetics, it leads to a large volume of the EMI filter. Thus, it is necessary to reduce the CM noise generated from the PT.

Various works for reducing the CM noise generated from the PT have been studied [7]–[24]. The first category is reducing the CM noise based on the circuit variation, such as winding cancellation, passive component cancellation, symmetrical circuit configuration, and so on [7]–[14]. The works in [7] and [8] utilize an additional transformer winding named antiphase winding for good CM noise attenuation, and previous research works in [9] and [10] achieve a low CM noise by adding passive components, such as the capacitor and inductor. Other approaches in [11]–[13] suggest the symmetrical circuit configuration, which can eliminate the CM noise current flowing through the parasitic capacitor of the transformer. Although they improve the EMI performance by canceling the CM current flowing through the parasitic capacitors of the transformer, additional components or windings degrade the power density of the converter. In [14], it gets a better CM noise attenuation by changing the location of the transformer and rectifier diodes. This scheme is simple because the additional components or windings are not required. However, methods [7]–[14] have limited improvement of CM noise reduction because they do not consider the CM noise generated from parasitic capacitors between each layer of the transformer. That CM noise is especially a critical factor of the PT compared with the wire-wound transformer because there are large parasitic capacitances between adjacent layers in the PT by the large overlapped area of layers.

The secondary category was focused on reducing the CM noise generated from the parasitic capacitor between the adjacent layers of the PT, and many works have been studied [15]–[24]. Previous works in [15]–[19] use the shielding layer between the primary and secondary layers to suppress the CM noise. However, extra windings for shielding should be added and they increase the winding area of the transformer. There is a large conduction loss in shielding layers due to the eddy current. Although Fei *et al.* [20] can relieve the conduction loss of the primary circuit by utilizing half of the shielding layer as the primary turn, it still requires the shielding layer for every space between primary and secondary windings. In [21]–[24], adjacent primary and secondary layers have the same *dv/dt* characteristic, and there is no CM current flowing through

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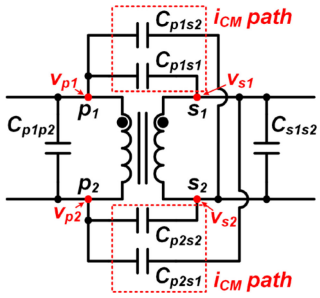

Fig. 1. Parasitic capacitor model of the transformer.

parasitic capacitors between layers. However, those schemes are adopted to the half-bridge *LLC* resonant converter, flyback converter, and forward converter. Thus, it is difficult to utilize them for medium-to-high power applications due to the large conduction loss in the primary-side circuit.

This article proposes a CM noise reduction method for the full-bridge (FB) *LLC* resonant converter, and it can be adopted for medium-to-high power applications, such as the electric vehicle system, due to a high voltage gain and small primary current [25], [26]. The proposed converter has a new circuit configuration and layer arrangement of the PT, and they can significantly reduce the CM noise. The resonant inductor and capacitor are equally divided into two components to make the symmetric circuit structure and have the equivalently same values with the conventional converter. So that, static points, which have zero *dv*/*dt* characteristic, on the primary and secondary side of the transformer can be generated. The primary and secondary layer can have the same *dv*/*dt* by proposing a layer arrangement for PT based on the proposed converter. As a result, the proposed two major key ideas, the balanced resonant tank and layer arrangement of the PT, can decrease the CM noise generated from the CM current flowing through parasitic capacitors in the PT and achieve high power density by reducing the size of the EMI filter.

The rest of this article is organized as follows. In Section II, the CM noise of the conventional and proposed FB *LLC* resonant converters according to each operational mode is explained. Section III suggests a layer arrangement of the transformer in the proposed converter. In Section IV, the proposed converter is verified by the experimental results of the prototype with 400-V input and 1.5-kW (270–420 V/3.57 A) output. Finally, Section V summarizes the effectiveness of the proposed converter with the conclusion.

II. CM Noise of FB *LLC* Resonant Converter According to the Operational Principle

A. CM Noise Characteristic in the Conventional Converter

The CM noise generated from the PT is caused by the CM current $i_{\rm CM}$, which is flowing through parasitic capacitors between primary and secondary layers. Fig. 1 shows a parasitic capacitor model of the transformer. If the transformer is constructed symmetrically, it can be assumed that $C_{p1s1} = C_{p2s2}$ and

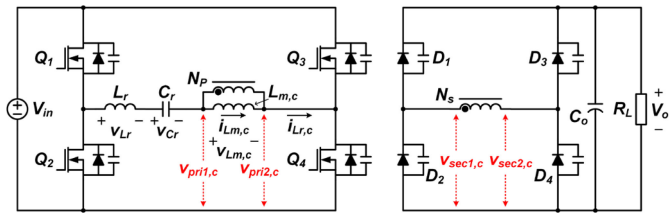

Fig. 2. Circuit diagram of the conventional converter.

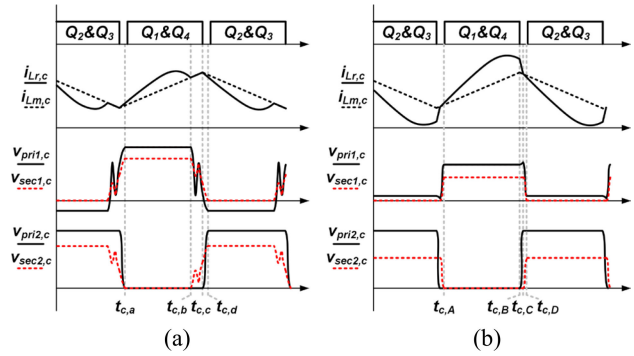

Fig. 3. Operational waveform of the conventional converter. (a) Under the below region. (b) Under the above region.

$C_{p1s2} = C_{p2s1}$, and $i_{\rm CM}$ can be expressed as follows [23]:

$$i_{\rm CM} = C_{p1s1}\left\{\left(\frac{dv_{p1}}{dt} - \frac{dv_{s1}}{dt}\right) + \left(\frac{dv_{p2}}{dt} - \frac{dv_{s2}}{dt}\right)\right\} + C_{p1s2}\left\{\left(\frac{dv_{p1}}{dt} - \frac{dv_{s2}}{dt}\right) + \left(\frac{dv_{p2}}{dt} - \frac{dv_{s1}}{dt}\right)\right\} \quad (1)$$

where C_{p1s1}, C_{p1s2}, C_{p2s1}, and C_{p2s2} are the parasitic capacitors between the primary and secondary side of the transformer, and v_{p1}, v_{p2}, v_{s1}, and v_{s2} are the voltage versus ground at the point p_1, p_2, s_1, and s_2, respectively, as shown in Fig. 1.

According to (1), $i_{\rm CM}$ is proportional to the *dv*/*dt* difference between the primary and secondary side terminals of the transformer. Thus, a small *dv*/*dt* difference is necessary for small $i_{\rm CM}$. In the case of parasitic capacitors between two different primary or secondary layers, there is no CM current between layers.

Fig. 2 shows a circuit diagram of the conventional FB *LLC* resonant converter. The turn-ON time of Q_1 is complementary to that of Q_2 with a dead time, and the same gate signals are applied to Q_3 and Q_4. The operating region in the *LLC* resonant converter can be divided into two regions, the below and above regions, depending on the operating switching frequency [28]. The below region means that the operating switching frequency is lower than the resonant frequency, and the above region is the opposite operation region, i.e., the operating switching frequency is higher than the resonant frequency. Fig. 3 shows the key operating waveforms of the conventional converter under below and above regions. The operation of the *LLC* resonant converter is divided based on [27] and the CM current of each mode will be discussed.

Fig. 4 shows an equivalent circuit at the primary and secondary-side circuit during both operations from $t_{c,a}$ to $t_{c,b}$

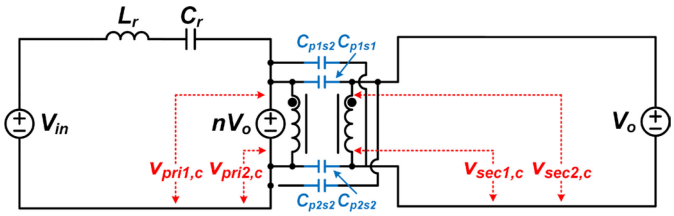

Fig. 4. Equivalent circuit of the conventional converter during the operation from $t_{c,a}$ to $t_{c,b}$ and from $t_{c,A}$ to $t_{c,B}$.

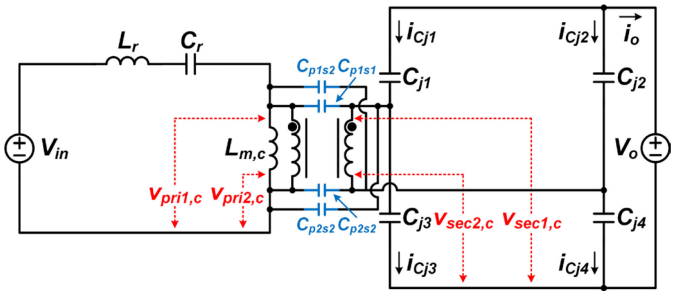

Fig. 5. Equivalent circuit of the conventional converter during the operation from $t_{c,b}$ to $t_{c,c}$.

and from $t_{c,A}$ to $t_{c,B}$. During these operations, the voltage across the magnetizing inductor $v_{Lm,c}$ is the turns-ratio of the transformer n times the output voltage V_o. Also, secondary diodes D_1 and D_4 are conducted. Therefore, the voltage potential versus ground at the terminals of the transformer in the conventional converter and their dv/dt characteristics can be calculated as follows:

$$v_{\mathrm{pri1},c} = \mathrm{n}V_o \tag{2}$$

$$v_{\mathrm{pri2},c} = 0 \tag{3}$$

$$v_{\mathrm{sec1},c} = V_o \tag{4}$$

$$v_{\mathrm{sec2},c} = 0 \tag{5}$$

$$\frac{dv_{\mathrm{pri1},c}}{dt} = \frac{dv_{\mathrm{pri2},c}}{dt} = \frac{dv_{\mathrm{sec1},c}}{dt} = \frac{dv_{\mathrm{sec2},c}}{dt} = 0 \tag{6}$$

where $v_{\mathrm{pri1},c}$ and $v_{\mathrm{pri2},c}$ are, respectively, the voltage potentials versus ground at the primary-side terminals of the transformer in the conventional converter, and $v_{\mathrm{sec1},c}$ and $v_{\mathrm{sec2},c}$ are, respectively, the voltage potentials versus ground at the secondary-side terminals of the transformer in the conventional converter.

From (1) and (6), the CM current of the conventional converter in Fig. 4 $i_{\mathrm{CM},c1}$ is zero.

Fig. 5 shows an equivalent circuit at the primary and secondary sides from $t_{c,b}$ to $t_{c,c}$. V_o is not reflected on the primary side because there is no current flowing through the secondary diode. Thus, the equivalent circuit at the primary side is composed of the resonant inductor L_r, resonant capacitor C_r, and magnetizing inductor $L_{m,c}$, and $v_{\mathrm{pri1},c}$, $v_{\mathrm{pri2},c}$ and dv/dt characteristics of the primary-side terminals can be expressed as follows:

$$v_{\mathrm{pri1},c} = v_{Lm,c} \tag{7}$$

$$\frac{dv_{\mathrm{pri1},c}}{dt} = \frac{dv_{Lm,c}}{dt} \tag{8}$$

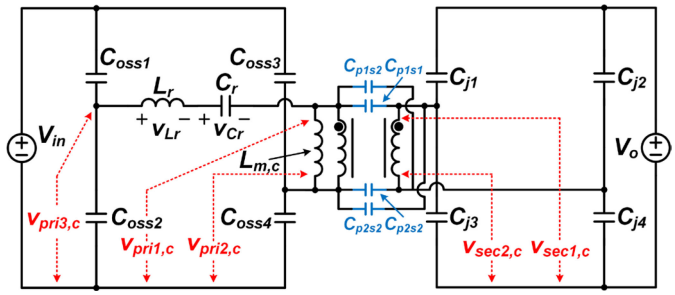

Fig. 6. Equivalent circuit of the conventional converter during the operation from $t_{c,B}$ to $t_{c,C}$.

$$v_{\mathrm{pri2},c} = \frac{dv_{\mathrm{pri2},c}}{dt} = 0. \tag{9}$$

Assuming the parasitic capacitors of secondary diodes C_{j1}, C_{j2}, C_{j3}, and C_{j4} are the same, the magnitude of the current flowing through the junction capacitor of rectifier diodes is the same, i.e., $i_{Cj1} = -i_{Cj2} = -i_{Cj3} = i_{Cj4}$ because the output current i_o is zero. Also, voltages across C_{j1} and C_{j4} are the same, and the voltage across C_{j2} and C_{j3} are the same. Thus, the relationship between $v_{\mathrm{sec1},c}$ and $v_{\mathrm{sec2},c}$ can be obtained as follows:

$$v_{\mathrm{sec1},c} + v_{\mathrm{sec2},c} = V_o \tag{10}$$

$$v_{\mathrm{sec1},c} - v_{\mathrm{sec2},c} = \frac{v_{Lm,c}}{\mathrm{n}}. \tag{11}$$

From (10) and (11), $v_{\mathrm{sec1},c}$, $v_{\mathrm{sec2},c}$, and dv/dt characteristic of the secondary-side terminals can be calculated as follows:

$$v_{\mathrm{sec1},c} = \frac{1}{2}\left(V_o + \frac{v_{Lm,c}}{\mathrm{n}}\right) \tag{12}$$

$$v_{\mathrm{sec2},c} = \frac{1}{2}\left(V_o - \frac{v_{Lm,c}}{\mathrm{n}}\right) \tag{13}$$

$$\frac{dv_{\mathrm{sec1},c}}{dt} = -\frac{dv_{\mathrm{sec2},c}}{dt} = \frac{1}{2\mathrm{n}}\frac{dv_{Lm,c}}{dt}. \tag{14}$$

Using (1), (6), and (14), the CM current during the operation in Fig. 5 $i_{\mathrm{CM},c2}$ can be calculated as follows:

$$i_{\mathrm{CM},c2} = \frac{dv_{Lm,c}}{dt}\left\{C_{p1s1}\left(1-\frac{1}{2\mathrm{n}}\right) + C_{p1s2}\left(1+\frac{1}{2\mathrm{n}}\right)\right\}. \tag{15}$$

Fig. 6 shows an equivalent circuit at the primary and secondary side from $t_{c,B}$ to $t_{c,C}$. During this operation, the primary switches are turned OFF, and the current flows through secondary diodes. The relationship between $v_{\mathrm{pri1},c}$, $v_{\mathrm{pri2},c}$, and $v_{\mathrm{pri3},c}$ can be obtained as follows:

$$v_{\mathrm{pri2},c} + v_{\mathrm{pri3},c} = V_{\mathrm{in}} \tag{16}$$

$$v_{\mathrm{pri1},c} - v_{\mathrm{pri2},c} = \mathrm{n}V_o \tag{17}$$

$$v_{\mathrm{pri3},c} - v_{\mathrm{pri1},c} = v_{Lr} + v_{Cr} \tag{18}$$

where v_{Lr} is the voltage across the L_r and v_{Cr} is the voltage across the C_r.

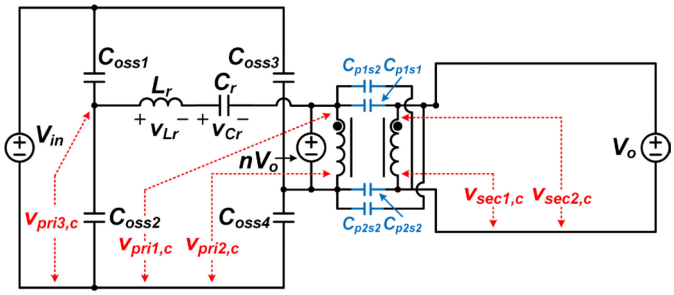

Fig. 7. Equivalent circuit of the conventional converter during both operations from $t_{c,c}$ to $t_{c,d}$ and from $t_{c,C}$ to $t_{c,D}$.

Using (16)–(18), $v_{\mathrm{pri1},c}$, $v_{\mathrm{pri2},c}$ and the *dv/dt* characteristic of primary-side terminals can be expressed as follows:

$$v_{\mathrm{pri1},c} = \frac{1}{2}\ (V_{\mathrm{in}} + \mathrm{n}V_o - v_{Lr} - v_{Cr}) \tag{19}$$

$$v_{\mathrm{pri2},c} = \frac{1}{2}\ (V_{\mathrm{in}} - \mathrm{n}V_o - v_{Lr} - v_{Cr}) \tag{20}$$

$$\frac{dv_{\mathrm{pri1},c}}{dt} = \frac{dv_{\mathrm{pri2},c}}{dt} = -\frac{1}{2}\left(\frac{dv_{Lr}}{dt} + \frac{dv_{Cr}}{dt}\right). \tag{21}$$

The equivalent circuit on the secondary side is the same as the secondary circuit in Fig. 5. Thus, *dv/dt* of $v_{\mathrm{sec1},c}$ and $v_{\mathrm{sec2},c}$ can be calculated from (14). Using (1), (14), and (21), the CM current during the operation in Fig. 6 $i_{\mathrm{CM},c3}$ can be calculated as follows:

$$i_{\mathrm{CM},c3} = -C_{p1s1}\left(\frac{dv_{Lr}}{dt} + \frac{dv_{Cr}}{dt} + \frac{1}{\mathrm{n}}\frac{dv_{Lm,c}}{dt}\right) - C_{p1s2}\left(\frac{dv_{Lr}}{dt} + \frac{dv_{Cr}}{dt} - \frac{1}{\mathrm{n}}\frac{dv_{Lm,c}}{dt}\right). \tag{22}$$

Fig. 7 shows an equivalent circuit at the primary and secondary sides from $t_{c,c}$ to $t_{c,d}$ and from $t_{c,C}$ to $t_{c,D}$. During these operations, primary switches are turned OFF, and the current does not flow through secondary diodes. The equivalent circuit at the primary side is similar to the primary circuit in Fig. 6, and $v_{\mathrm{pri1},c}$, $v_{\mathrm{pri2},c}$, and the *dv/dt* characteristic of primary-side terminals can be calculated as follows:

$$v_{\mathrm{pri1},c} = \frac{1}{2}\left\{V_{\mathrm{in}} - v_{Cr} + v_{Lm,c}\left(1 - \frac{L_r}{L_{m,c}}\right)\right\} \tag{23}$$

$$v_{\mathrm{pri2},c} = \frac{1}{2}\left\{V_{\mathrm{in}} - v_{Cr} - v_{Lm,c}\left(1 + \frac{L_r}{L_{m,c}}\right)\right\} \tag{24}$$

$$\frac{dv_{\mathrm{pri1},c}}{dt} = -\frac{1}{2}\left\{\frac{dv_{Cr}}{dt} - \frac{dv_{Lm,c}}{dt}\left(1 - \frac{L_r}{L_{m,c}}\right)\right\} \tag{25}$$

$$\frac{dv_{\mathrm{pri2},c}}{dt} = -\frac{1}{2}\left\{\frac{dv_{Cr}}{dt} + \frac{dv_{Lm,c}}{dt}\left(1 + \frac{L_r}{L_{m,c}}\right)\right\}. \tag{26}$$

The equivalent circuit of the secondary side is the same as the secondary circuit in Fig. 4. Therefore, *dv/dt* of $v_{\mathrm{sec1},c}$ and $v_{\mathrm{sec2},c}$ is zero according to (6). From (1), (6), (25), and (26), a CM current during the operation in Fig. 7, $i_{\mathrm{CM},c4}$, can be calculated as follows:

$$i_{\mathrm{CM},c4} = -C_{p1s1}\left\{\frac{dv_{Cr}}{dt} + \frac{dv_{Lm,c}}{dt}\left(1 - \frac{L_r}{L_{m,c}}\right)\right\} - C_{p1s2}\left\{\frac{dv_{Cr}}{dt} + \frac{dv_{Lm,c}}{dt}\left(1 + \frac{L_r}{L_{m,c}}\right)\right\}. \tag{27}$$

The secondary-side circuit of the conventional converter is symmetric based on the transformer. However, the primary-side circuit of the conventional converter is asymmetric. Thus, the *dv/dt* characteristics of primary and secondary-side terminals in the transformer are different, and it results in a large CM noise from the transformer.

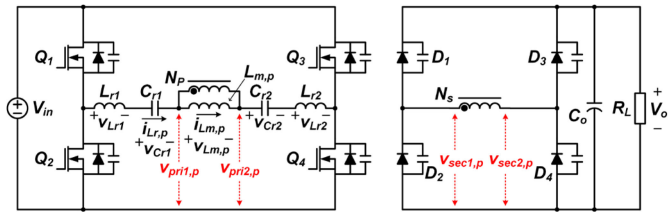

Fig. 8. Circuit diagram of the proposed converter.

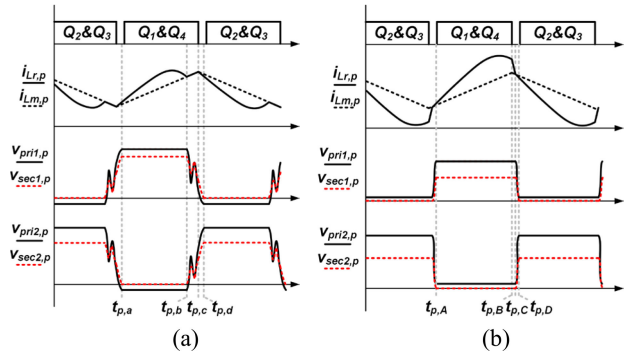

Fig. 9. Operational waveform of the proposed converter. (a) Under the below region. (b) Under the above region.

B. CM Noise Characteristic in the Proposed Converter

Fig. 8 shows a circuit diagram of the proposed converter. The gate signals of the proposed converter are the same as those of the conventional converter. The turns-ratio of the transformer is the same as that of the conventional converter. In the proposed converter, both resonant inductor and resonant capacitor are equally divided into two components to make a balanced resonant tank. In the real case, it is difficult to make exactly balanced resonant tanks due to the tolerance of components. In our prototype, L_{r1} and L_{r2} are integrated into the one core, and each resonant inductor is made up of windings on the side legs of the EE-shaped core. L_{r1} and L_{r2} are almost the same because half of the symmetrical EE-shaped core is applied as L_{r1} and L_{r2}, and windings made by printed circuit board (PCB) manufacture are identical. C_{r1} and C_{r2} can have the tolerance, which is commonly maximum 5%. Therefore, the CM noise of the proposed converter is mainly affected by the tolerance of the resonant capacitor. Since there are less tolerance components, such as 2%, 1%, and 0.5%, the voltage unbalance problem of

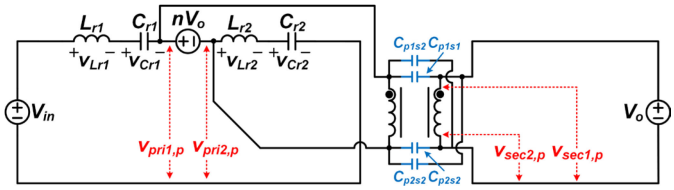

Fig. 10. Equivalent circuit of the proposed converter during both operations from $t_{p,a}$ to $t_{p,b}$ and from $t_{p,A}$ to $t_{p,B}$.

the capacitance tolerance can be solved by tightly managing the tolerance. Thus, it is analyzed with the assumption that the divided resonant tanks have the same component values, and the proposed converter has a smaller CM noise because the primary and secondary sides are symmetric based on the transformer. Fig. 9 shows the key operating waveforms of the proposed converter under below and above regions. The operation and equivalent circuit for the secondary side of the proposed converter are the same as those of the conventional converter. In this section, the CM current of the proposed converter for each mode will be discussed.

Fig. 10 shows an equivalent circuit from $t_{p,a}$ to $t_{p,b}$ and from $t_{p,A}$ to $t_{p,B}$. During these operations, the voltage across the magnetizing inductor $v_{Lm,p}$ is nV_o. L_{r1} is equal to L_{r2} and C_{r1} is equal to C_{r2} because they are equally divided. Thus, the relationship among the voltage across L_{r1} v_{Lr1}, the voltage across L_{r2} v_{Lr2}, the voltage across C_{r1} v_{Cr1}, and the voltage across C_{r2} v_{Cr2} can be calculated as follows:

$$v_{Lr1}+ v_{Cr1} = v_{Lr2} + v_{Cr2} = \frac{1}{2}\ (V_{\rm in}-{\rm n}V_o)\,. \tag{28}$$

The voltage potential versus ground at the primary-side terminals of the transformer in the proposed converter $v_{{\rm pri}1,p}$ and $v_{{\rm pri}2,p}$ can be calculated from (28). Thus, $v_{{\rm pri}1,p}$, $v_{{\rm pri}2,p}$, and their *dv/dt* characteristics can be calculated as follows:

$$v_{{\rm pri}1,p} = \frac{1}{2}\ (V_{\rm in}+{\rm n}V_o) \tag{29}$$

$$v_{{\rm pri}2,p} = \frac{1}{2}\ (V_{\rm in}-{\rm n}V_o) \tag{30}$$

$$\frac{dv_{{\rm pri}1,p}}{dt} = \frac{dv_{{\rm pri}2,p}}{dt} = 0. \tag{31}$$

The equivalent circuit of the secondary side is the same as the secondary circuit in Fig. 4. Therefore, voltage potentials versus ground at the secondary-side terminals of the transformer in the proposed converter $v_{{\rm sec}1,p}$ and $v_{{\rm sec}2,p}$ are zero according to (4) and (5), and *dv/dt* characteristics of $v_{{\rm sec}1,p}$ and $v_{{\rm sec}2,p}$ are also zero. Using (1), (6), and (31), the CM current during the operation in Fig. 10 $i_{{\rm CM},p1}$ is zero.

Fig. 11 shows an equivalent circuit from $t_{p,b}$ to $t_{p,c}$. The sum of v_{Lr1} and v_{Cr1} is the same as the sum of v_{Lr2} and v_{Cr2}. Therefore, $v_{{\rm pri}1,p}$, $v_{{\rm pri}2,p}$, and their *dv/dt* characteristics can be calculated as follows:

$$v_{{\rm pri}1,p} = \frac{1}{2}\ (V_{\rm in} + v_{Lm,p}) \tag{32}$$

$$v_{{\rm pri}2,p} = \frac{1}{2}\ (V_{\rm in} - v_{Lm,p}\ ) \tag{33}$$

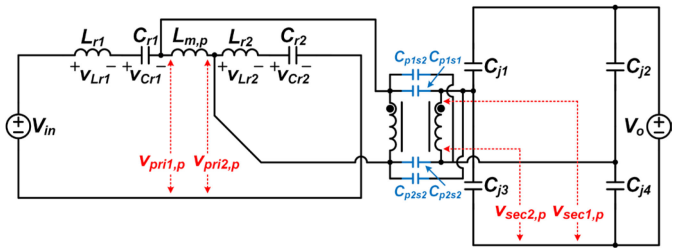

Fig. 11. Equivalent circuit of the proposed converter during the operation from $t_{p,b}$ to $t_{p,c}$.

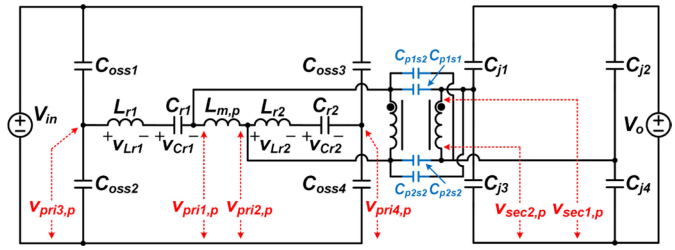

Fig. 12. Equivalent circuit of the proposed converter during the operation from $t_{p,B}$ to $t_{p,C}$.

$$\frac{dv_{{\rm pri}1,p}}{dt} = -\frac{dv_{{\rm pri}2,p}}{dt} = \frac{1}{2}\frac{dv_{Lm,p}}{dt} \tag{34}$$

where $v_{Lm,p}$ is the voltage across the $L_{m,p}$.

The equivalent circuit on the secondary side is the same as the secondary circuit in Fig. 5. Thus, *dv/dt* of $v_{{\rm sec}1,p}$ and $v_{{\rm sec}2,p}$ can be calculated by using (17) and (18), respectively. Using (2), (14), and (34), the CM current during the operation in Fig. 11 $i_{{\rm CM},p2}$ is zero.

Fig. 12 shows an equivalent circuit from $t_{p,B}$ to $t_{p,C}$. The equivalent circuit on the primary side is similar to the primary circuit in Fig. 6, and the sum of v_{Lr1} and v_{Cr1} is the same as the sum of v_{Lr2} and v_{Cr2}. Therefore, the relationship between $v_{{\rm pri}1,p}$, $v_{{\rm pri}2,p}$, $v_{{\rm pri}3,p}$, $v_{{\rm pri}4,p}$, and the *dv/dt* characteristics of $v_{{\rm pri}1,p}$ and $v_{{\rm pri}2,p}$ can be obtained as follows:

$$v_{{\rm pri}3,p}+ v_{{\rm pri}4,p} = V_{\rm in} \tag{35}$$

$$v_{{\rm pri}3,p}- v_{{\rm pri}1,p} = v_{{\rm pri}2,p}\ - v_{{\rm pri}4,p} \tag{36}$$

$$v_{{\rm pri}1,p} = \frac{1}{2}\ (V_{\rm in}+{\rm n}V_o) \tag{37}$$

$$v_{{\rm pri}2,p} = \frac{1}{2}\ (V_{\rm in}-{\rm n}V_o) \tag{38}$$

$$\frac{dv_{{\rm pri}1,p}}{dt} = \frac{dv_{{\rm pri}2,p}}{dt} = 0. \tag{39}$$

Based on the same equivalent circuit of the primary side in Fig. 4, the *dv/dt* characteristics of $v_{{\rm sec}1,p}$ and $v_{{\rm sec}2,p}$ are zero. From (1), (6), and (39), the CM current during the operation in Fig. 12 $i_{{\rm CM},p3}$ is zero.

Fig. 13 shows an equivalent circuit during both operations from $t_{p,c}$ to $t_{p,d}$ and from $t_{p,C}$ to $t_{p,D}$. The equivalent circuit on the primary side is similar to the primary circuit in Fig. 7, and the sum of v_{Lr1} and v_{Cr1} is the same as the sum of v_{Lr2} and v_{Cr2}. Thus, the relationship between $v_{{\rm pri}1,p}$, $v_{{\rm pri}2,p}$, $v_{{\rm pri}3,p}$, $v_{{\rm pri}4,p}$,

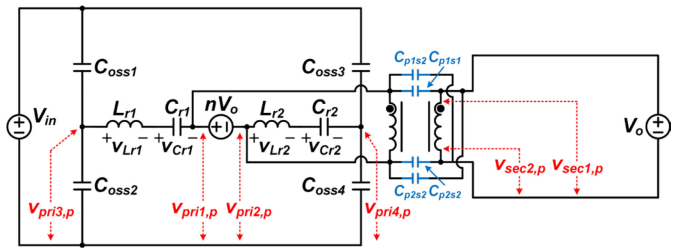

Fig. 13. Equivalent circuit of the proposed converter during the operation from $t_{p,c}$ to $t_{p,d}$ and from $t_{p,C}$ to $t_{p,D}$.

TABLE I
CM CURRENT COMPARISON UNDER BELOW REGION

time	*i_{CM} under below region*	
	prop.	*conv.*
t_a~t_b	0	0
t_b~t_c	0	$\frac{dv_{Lm}}{dt}\left\{C_{p1s1}\left(1-\frac{1}{2n}\right)+C_{p1s2}\left(1+\frac{1}{2n}\right)\right\}$
t_c~t_d	0	$-C_{p1s1}\left\{\frac{dv_{Lr}}{dt}+\frac{dv_{Lm}}{dt}\left(1-\frac{L_r}{L_m}\right)\right\}-C_{p1s2}\left\{\frac{dv_{Lr}}{dt}+\frac{dv_{Lm}}{dt}\left(1+\frac{L_r}{L_m}\right)\right\}$

TABLE II
CM CURRENT COMPARISON UNDER ABOVE REGION

time	*i_{CM} under above region*	
	prop.	*conv.*
t_A~t_B	0	0
t_B~t_C	0	$-C_{p1s1}\left(\frac{dv_{Lr}}{dt}+\frac{dv_{Cr}}{dt}+\frac{1}{n}\frac{dv_{Lm}}{dt}\right)-C_{p1s2}\left(\frac{dv_{Lr}}{dt}+\frac{dv_{Cr}}{dt}-\frac{1}{n}\frac{dv_{Lm}}{dt}\right)$
t_C~t_D	0	$-C_{p1s1}\left\{\frac{dv_{Lr}}{dt}+\frac{dv_{Lm}}{dt}\left(1-\frac{L_r}{L_m}\right)\right\}-C_{p1s2}\left\{\frac{dv_{Lr}}{dt}+\frac{dv_{Lm}}{dt}\left(1+\frac{L_r}{L_m}\right)\right\}$

and *dv*/*dt* characteristics of $v_{\mathrm{pri1},p}$ and $v_{\mathrm{pri2},p}$ can be obtained as follows:

$$v_{\mathrm{pri1},p}=\frac{1}{2}\left(V_{\mathrm{in}}+v_{Lm,p}\right) \tag{40}$$

$$v_{\mathrm{pri2},p}=\frac{1}{2}\left(V_{\mathrm{in}}-v_{Lm,p}\right) \tag{41}$$

$$\frac{dv_{\mathrm{pri1},p}}{dt}=-\frac{dv_{\mathrm{pri2},p}}{dt}=\frac{1}{2}v_{Lm,p}. \tag{42}$$

The equivalent circuit on the secondary side is the same as the secondary circuit in Fig. 5. Thus, *dv*/*dt* of $v_{\mathrm{sec1},p}$ and $v_{\mathrm{sec2},p}$ is zero according to (14). Using (1), (14), and (42), the CM current during the operation in Fig. 13 $i_{\mathrm{CM},p4}$ is zero.

The CM currents of the proposed converter are equal or smaller than those of the conventional converter in Section II-A under every operating condition, as listed in Tables I and II. Therefore, the CM noise in the proposed converter can be smaller than that in the conventional converter.

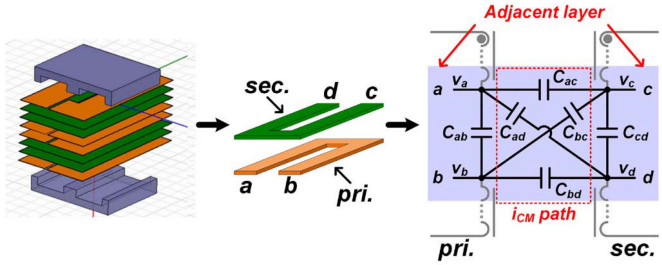

Fig. 14. Parasitic capacitor model of the planar transformer.

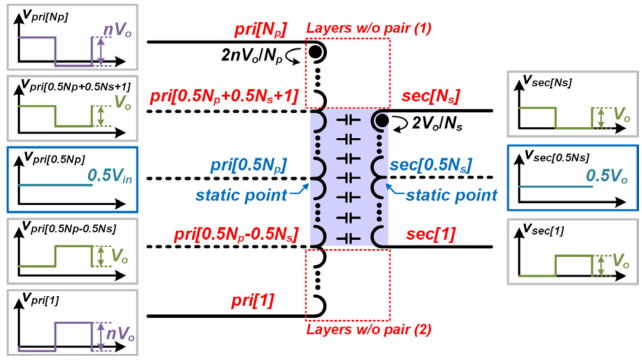

Fig. 15. Voltage waveforms at the primary and secondary layers of the transformer.

III. LAYER ARRANGEMENT OF PT IN THE PROPOSED CONVERTER

The proposed converter has a smaller CM current flowing through the parasitic capacitors in the transformer, according to the analysis in Section II. However, the parasitic capacitor model of the transformer in Fig. 1 does not include the effect of parasitic capacitors between each winding. In the PT, each layer of the transformer contains the primary or secondary winding, and there are large parasitic capacitances between adjacent layers, as shown in Fig. 14. Thus, parasitic capacitors should be considered to analyze the CM current in the transformer. The CM current between adjacent layers $i_{\mathrm{CM},L}$ is similar to (1). If the adjacent layers have the same number of turns and symmetric layout, parasitic capacitances can be assumed as the same value. Thus, $i_{\mathrm{CM},L}$ can be calculated as follows:

$$i_{\mathrm{CM},L}=\left(C_{ac}+C_{ad}\right)\left(\frac{dv_a}{dt}+\frac{dv_b}{dt}-\frac{dv_c}{dt}-\frac{dv_d}{dt}\right) \tag{43}$$

where C_{ac} and C_{ad} are the parasitic capacitors between adjacent primary and secondary layers in the transformer, and v_a, v_b, v_c, and v_d are the voltage versus ground at the point a, b, c, and d, respectively.

According to (43), if the *dv*/*dt* characteristics of the voltage potential versus ground of adjacent primary and secondary layers are the same, $i_{\mathrm{CM},L}$ is zero. Fig. 15 shows the voltage potential versus ground at the primary and secondary layers of the transformer. The voltages of the first layer and N_pth layer on the primary side change with the amplitude of nV_o based on $0.5V_{\mathrm{in}}$, and the amplitude changes by $2nV_o/N_p$ per turn. The voltage potential of the $0.5N_p$th layer on the primary side $v_{\mathrm{pri}[0.5\,Np]}$ becomes $0.5V_{\mathrm{in}}$. Thus, *dv*/*dt* of $v_{\mathrm{pri}[0.5\,Np]}$ is

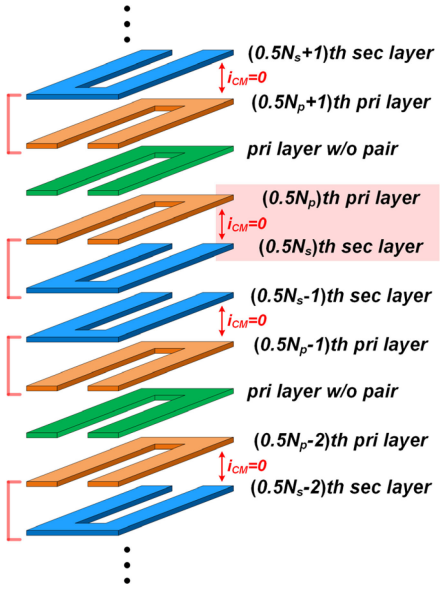

Fig. 16. Winding layout of the transformer in the proposed converter.

zero, which means the static point, as shown in Fig. 15. The voltages of the first layer and N_sth layer on the secondary side change with the amplitude of V_o on the basis of $0.5V_o$, and the amplitude changes by $2V_o/N_s$ per turn. The voltage potential of the $0.5N_s$th layer on the secondary side $v_{\mathrm{sec}[0.5\,Ns]}$ becomes $0.5V_o$. Therefore, the *dv*/*dt* characteristic of $v_{\mathrm{sec}[0.5\,Ns]}$ is zero, which means the static point, as shown in Fig. 15. There is no difference of *dv*/*dt* between the $0.5N_p$th layer of the primary side and $0.5N_s$th layer of the secondary side. The voltage–amplitude-variation per turn of both sides is the same because n is N_p/N_s. Therefore, the primary and secondary layers can have the same *dv*/*dt* characteristic if primary and secondary layers are overlapped one by one based on the $0.5N_p$th layer for the primary side and $0.5N_s$th layer for the secondary side, as shown in Fig. 16.

If N_p is equal to N_s, every primary and secondary layer has its pair. However, the layers without pair should be considered because N_p and N_s are normally different. This section will explain the case when N_p is larger than N_s. The layers without pair are green layers in Fig. 16, which are located between the primary layers that have their pair. There is no CM current flowing through those layers because the CM current does not flow between the parasitic capacitors of the same side of the transformer.

The conventional and proposed converters have 20 layers in the PT, 12 primary layers, and 8 secondary layers. The whole layer arrangements of the PT in the conventional and proposed converters are given in Table III. The transformer of the conventional converter is composed of the interleaved winding structure and it results in a large CM current between primary and secondary layers. Although the transformer of the proposed converter also has an interleaved winding structure, there is no CM current between primary and secondary layers because the adjacent layers have the same *dv*/*dt* characteristic.

TABLE III
WINDING LAYOUT OF TRANSFORMERS IN CONVENTIONAL AND PROPOSED CONVERTERS

Layers	*Conv.*	*Prop.*
20th	sec[1]	pri[11]
19th	pri[1]	pri[10]
18th	sec[2]	sec[8]
17th	pri[2]	sec[7]
16th	pri[3]	pri[9]
15th	sec[3]	pri[12]
14th	pri[4]	pri[8]
13th	pri[5]	sec[6]
12th	sec[4]	sec[5]
11th	pri[6]	pri[7]
10th	pri[7]	pri[1]
9th	sec[5]	pri[6]
8th	pri[8]	sec[4]
7th	pri[9]	sec[3]
6th	sec[6]	pri[5]
5th	pri[10]	pri[4]
4th	pri[11]	sec[2]
3rd	sec[7]	sec[1]
2nd	pri[12]	pri[3]
1st	sec[8]	pri[2]

pri[n]: the nth primary winding of the transformer. sec[m]: the mth secondary winding of the transformer.

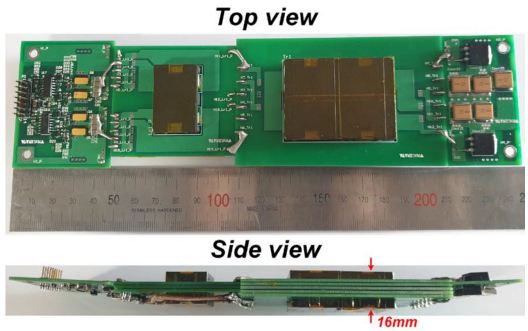

Fig. 17. Prototype of the proposed converter.

IV. EXPERIMENTAL RESULTS

Prototypes of both conventional and proposed converters are implemented with 1.5-kW FB *LLC* resonant converter, and the design specifications are as follows: input voltage is 400 V, output voltage is 270–420 V, and resonant frequency is 500 kHz. The prototype of the proposed converter is shown in Fig. 17 and the detailed component list of prototype converters is presented in Table IV. Each component is selected by considering the maximum voltage and current across components with a reasonable margin.

A. Voltage Waveforms of Prototype Converters

Fig. 18 shows the experimental waveforms of the conventional converter, and the voltage waveforms of the primary side $v_{\mathrm{pri,conv}}$, secondary side $v_{\mathrm{sec,conv}}$, and $i_{Lr,c}$ are presented. Two voltage waveforms show the voltage potential of two adjacent

TABLE IV
COMPONENT LIST OF CONVENTIONAL AND PROPOSED CONVERTERS

	Conventional converter	Proposed converter
Primary switches (Q_1, Q_2, Q_3, and Q_4)	GS66508T ($V_{ds,max}$ = 650 V and $I_{DS,avg}$ = 30 A)	
Transformers ($L_{m,c}$ and $L_{m,p}$)	ELP 38/8/25 * 2 (Material: N49. $L_{m,c}$ and $L_{m,p}$ =40 μH and turns-ratio= 12:8)	
Resonant inductors (L_r, L_{r1}, and L_{r2})	ELP 32/6/20 (Material: N49. L_r=11.2 μH)	ELP 32/6/20 (Material: N49. L_{r1} and L_{r2}=5.6 μH)
Resonant capacitors (C_r, C_{r1}, and C_{r2})	GRM32D7U3A222JW31L (C_r=8.8 nF, *Quantity*: 4)	GRM32D7U3A222JW31L (C_{r1} and C_{r2}=17.6 nF, *Quantity*: 8 and 8)
Rectifier diodes (D_1, D_2, D_3, and D_4)	SCS210AJ (V_R=650 V and I_F=10 A)	
CM choke ($L_{CM,conv}$ and $L_{CM,prop}$)	B64290L0082 (Material: N30, $L_{CM,conv}$=174 mH, 140turns)	B64290L0618 (Material: N30, $L_{CM,prop}$=5 mH, 34turns)
Y capacitor (C_Y)	B32529C8332J000 (C_Y=3300 pF)	

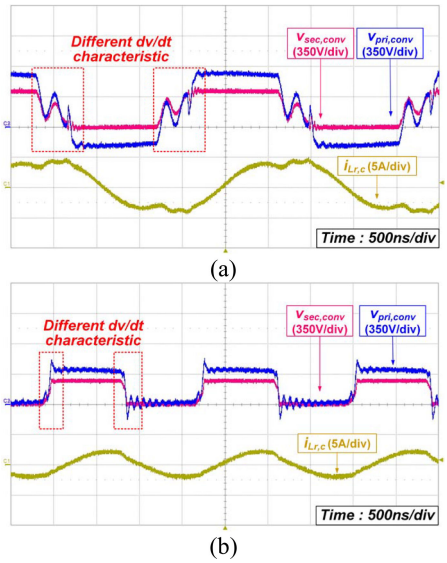

Fig. 18. Voltage waveforms of the conventional converter. (a) At $V_o = 420$ V. (b) At $V_o = 270$ V.

layers. Fig. 18(a) shows waveforms when V_o is 420 V and Fig. 18(b) presents the waveforms when V_o is 270 V. Both operations have the different *dv/dt* characteristic for the adjacent layers and it generates the large CM noise.

Fig. 19 presents the experimental waveforms of the proposed converter, and the voltage waveforms of the primary side $v_{\mathrm{pri,prop}}$, secondary side $v_{\mathrm{sec,prop}}$, and resonant inductor current $i_{Lr,p}$ are presented. Two voltage waveforms show the voltage potential of two adjacent layers. Fig. 19(a) shows waveforms when V_o is 420 V and Fig. 19(b) shows waveforms when V_o is 270 V. Both operations when V_o is 420 and 270 V have the same *dv/dt* characteristic for the adjacent layers, and it results in low CM noise.

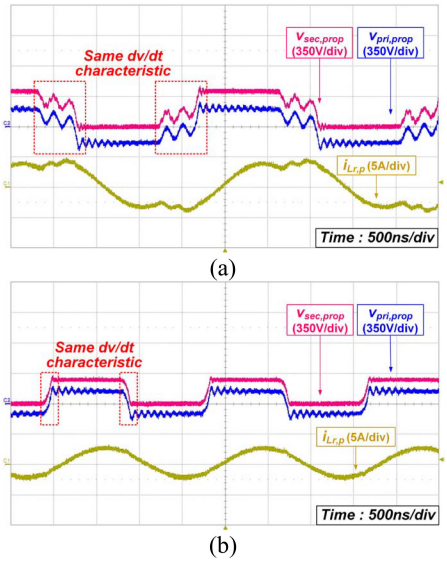

Fig. 19. Voltage waveforms of the proposed converter. (a) At $V_o = 420$ V. (b) At $V_o = 270$ V.

B. CM Noise of Conventional and Proposed Converter

CM noises are not only generated from parasitic capacitors of the transformer but also can be generated from parasitic capacitors between two phase-leg midpoints and protective earth C_{mid}. However, it is assumed that the CM noise generated from C_{mid} is very small because C_{mid} is generated between the heat sink and earth ground, and there is no heat sink in the prototype converter. Therefore, most of the CM noise differences between the conventional and proposed converter come from the variation of the circuit and layer arrangement of the PT.

Fig. 20 shows the measured CM noise of the conventional and proposed converter without the EMI filter. The CM noise is measured with the line impedance stabilization network named NNHV 8123 and spectrum analyzer named EA-300. In Fig. 20(a) and (c), the first peak locates around 500 kHz, which is the operating switching frequency when V_o is 270 V. In Fig. 20(b) and (d), the first peak locates around 340 kHz, which is the operating switching frequency when $V_o = 420$ V. Most of the peak values occurs at the multiples of each switching frequency. The CM noise peak of the proposed converter has a smaller value under almost every frequency range due to the balanced resonant tank and proposed winding layout. The CM noise at the fundamental frequency is increased according to the rise of V_o in the conventional converter. However, it is almost the same regardless of the V_o condition in the proposed converter because the *dv/dt* characteristic of adjacent layers in the transformer is almost the same under every occasion.

C. Design of the Resonant Tank

In the proposed converter, the design process of the resonant tank is the same as the conventional converter. The resonant tank is designed to have the same resonant frequency and voltage gain, and the resonant inductor and capacitor are divided into two equal components, respectively. $L_{r1} = L_{r2}$ and $C_{r1} = C_{r2}$ due to

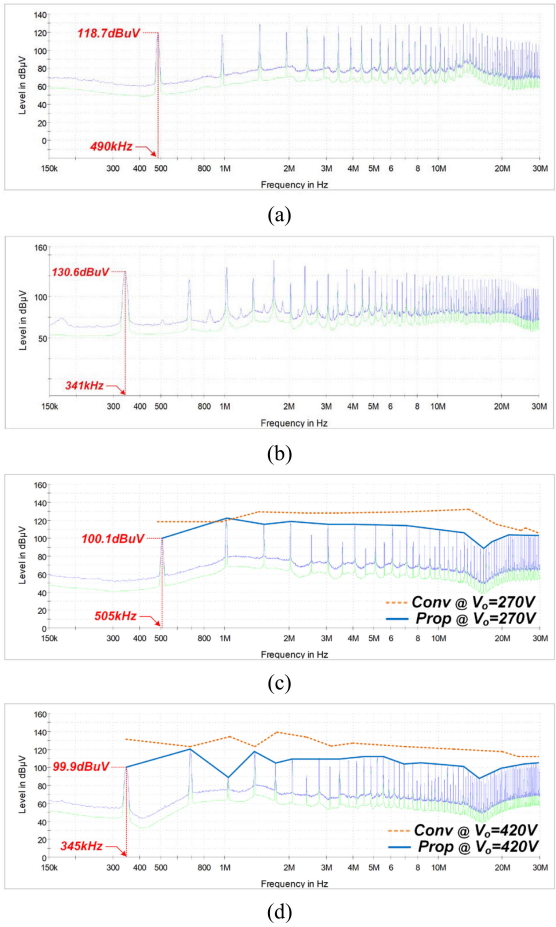

Fig. 20. CM noise of prototype converters. (a) Conventional converter at $V_o = 270$ V. (b) Conventional converter at $V_o = 420$ V. (c) Proposed converter at $V_o = 270$ V. (d) Proposed converter at $V_o = 420$ V.

the balanced resonant tank structure, and the total inductance of series-connected L_{r1} and L_{r2} is $2L_{r1}$, and the total capacitance of series-connected C_{r1} and C_{r2} is $0.5C_{r1}$. Thus, $L_{r1} = L_{r2} = 0.5L_r$ and $C_{r1} = C_{r2} = 2C_r$ for the same resonant frequency.

The voltage gain of the *LLC* resonant converter is obtained by using the fundamental harmonic approximation (FHA) [29]. Utilizing the FHA method, the voltage gain of the conventional converter M_c and that of the proposed converter M_p can be calculated as follows:

$$M_c = \frac{V_{o,c}^F}{V_{\text{in},c}^F} = \frac{1}{1+\frac{1}{k_c}\left(1-\frac{1}{F_c^2}\right)^2 + \left\{\left(F_c - \frac{1}{F_c}\right)Q_c\right\}} \tag{44}$$

$$M_p = \frac{V_{o,p}^F}{V_{\text{in},p}^F} = \frac{1}{1+\frac{1}{k_p}\left(1-\frac{1}{F_p^2}\right)^2 + \left\{\left(F_p - \frac{1}{F_p}\right)Q_c\right\}}. \tag{45}$$

where $V_{o,c}^F$ and $V_{\text{in},c}^F$ are the fundamental components of the V_o and V_{in} for the conventional converter, k_c is $L_{m,c}/L_r$, F_c is $f_s/f_{r,c}$, f_s is the switching frequency, $f_{r,c}$ is the resonant frequency of the conventional converter, $Q_c = (L_r/C_r)^{0.5}/R_{ac}$, R_{ac} is $8R_o n^2/\pi^2$, R_o is the output resistance, $V_{o,p}^F$ and $V_{\text{in},p}^F$ are the fundamental components of V_o and V_{in} for the proposed converter, k_p is $L_{m,p}/(2L_{r1})$, F_p is $f_s/f_{r,p}$, $f_{r,p}$ is the resonant frequency of the proposed converter, and $Q_p = (2L_{r1}/(0.5C_{r1}))^{0.5}/R_{ac}$.

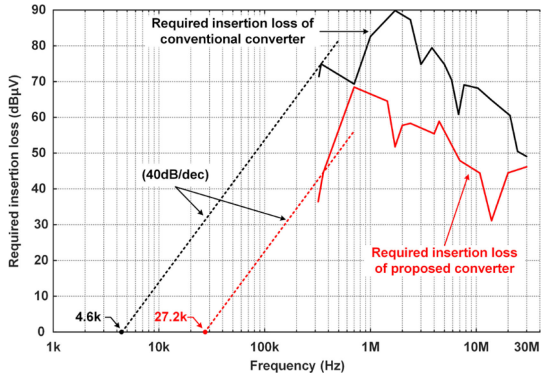

Fig. 21. Required insertion loss for the conventional and proposed converter.

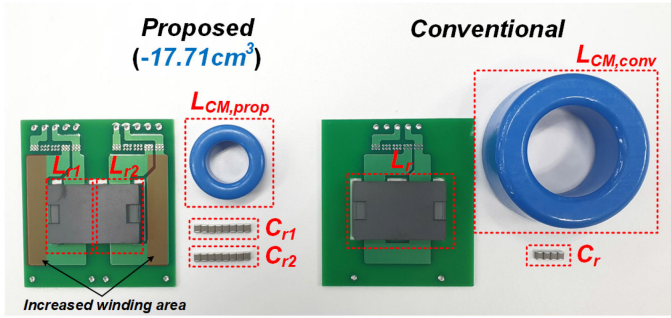

Fig. 22. Volume comparison of the resonant tank and CM inductor.

As aforementioned earlier, $L_{r1} = L_{r2} = 0.5L_r$ and $C_{r1} = C_{r2} = 2C_r$ for the same resonant tank, and it results in same M_c and M_p according to (44) and (45). The voltage across the resonant inductor in the proposed converter is half of that in the conventional converter. The effective cross-sectional area for the resonant inductor of the conventional converter $A_{e,c}$ and that of the proposed converter $A_{e,p}$ can be calculated as follows:

$$\text{A}_{e,p} = 0.5\ \text{A}_{e,c} = \frac{V_{Lr,p\_\text{peak}}}{4\text{N}_{Lr}B_{\max}f_{s,\min}} \tag{46}$$

where V_{Lr,p_peak} is the peak voltage across the resonant inductor in the proposed converter, $B_{\max}$ is the maximum flux density, and $f_{s,\min}$ is the minimum operating frequency.

The size of the resonant inductor of the proposed converter is half of that of the conventional converter. The total inductor size of the conventional and proposed converter is the same. As aforementioned, $C_{r1} = C_{r2} = 2C_r$ for the same voltage gain of the conventional and proposed converter. Each number of capacitors for C_{r1} and C_{r2} is doubled compared with that of C_r. Therefore, the total number of resonant capacitors becomes quadrupled in the proposed converter. Although the number of resonant capacitors becomes quadrupled in the proposed converter, they do not occupy a large area, as shown in Fig. 22.

D. Design of Expected EMI Filter

The EMI filter should be utilized to meet the EMI standard and the EMI filter is designed based on the EN55022B standard in this article. In [30], the required CM noise attenuation (required insertion loss) $V_{\text{req,CM}}$ is calculated as follows:

$$(V_{\text{req,CM}})_{\text{dB}} = (V_{\text{meas,CM}})_{\text{dB}} - (V_{\text{Limit}})_{\text{dB}} + 3\text{dB} \tag{47}$$

where $V_{\mathrm{meas,CM}}$ is the measured CM noise amplitude, V_{Limit} is the quasi-peak CM noise limit, and 3 dB is for a safety margin.

From (47), $V_{\mathrm{req,CM}}$ of the conventional and proposed converter when V_o is 420 V is presented in Fig. 21. From the EMI standard, the required CM noise limit is different according to the switching frequency and $V_{\mathrm{req,CM}}$ represents the required amount of the CM noise to be reduced to satisfy the EMI standard for each switching frequency. The case when V_o is 420 V is the worst occasion in terms of the CM noise because *dv*/*dt* of the voltage potential at each layer in the transformer becomes the largest. The corner frequencies of the conventional converter $f_{R,\mathrm{conv}}$ and the proposed converter $f_{R,\mathrm{prop}}$ can be obtained as follows:

$$V_{\mathrm{req,CM,conv}} = 40\log\left(\frac{f_{\mathrm{meas}}}{f_{R,\mathrm{conv}}}\right) \tag{48}$$

$$V_{\mathrm{req,CM,prop}} = 40\log\left(\frac{f_{\mathrm{meas}}}{f_{R,\mathrm{prop}}}\right) \tag{49}$$

where f_{meas} is the frequency at $V_{\mathrm{meas,CM}}$, $V_{\mathrm{req,CM,conv}}$ is the required CM noise attenuation of the conventional converter, and $V_{\mathrm{req,CM,prop}}$ is the required CM noise attenuation of the proposed converter.

From (48) and (49), $f_{R,\mathrm{conv}}$ and $f_{R,\mathrm{prop}}$ can be calculated as 4.6 and 27.2 kHz, as shown in Fig. 21, respectively. *LC* CM filter is composed of the CM choke and *Y* capacitor C_Y. C_Y is limited by the leakage current limits for safety requirements [21] and C_Y is designed with 3300 pF in this case. The CM choke of the conventional converter $L_{\mathrm{CM,conv}}$ and the proposed converter $L_{\mathrm{CM,prop}}$ can be calculated as follows:

$$L_{\mathrm{CM,conv}} = \frac{1}{2C_Y(2\pi f_{R,\mathrm{conv}})^2} \tag{50}$$

$$L_{\mathrm{CM,prop}} = \frac{1}{2C_Y(2\pi f_{R,\mathrm{prop}})^2} \tag{51}$$

Using (50) and (51), $L_{\mathrm{CM,conv}}$ is 174 mH and $L_{\mathrm{CM,prop}}$ is 5 mH. Based on the N30 material, the CM choke of the conventional converter can be designed with B64290L0082, whose volume is 23.56 cm^3, and that of the proposed converter can be applied as B64290L0618, whose volume is 3.08 cm^3. Therefore, the decreased volume is 20.48 cm^3, which means that the CM filter size of the proposed converter is reduced as 86.9% compared with that of the conventional converter. A comparison of the actual size of the resonant tank and CM choke in the conventional and proposed converter is shown in Fig. 23. Although the volume by the resonant capacitor and winding area of the resonant inductor is increased as 2.77 cm^3, the proposed converter can reduce the volume as much as 17.71 cm^3.

E. Measured Efficiency

The efficiency of the prototype converter is measured according to the variation of V_o, as shown in Fig. 23. The efficiency of the conventional converter without the CM filter is almost the same as that of the proposed converter because it uses almost the same components and switching frequency. The conventional converter uses a large CM choke with a large number of turns. As a result, the conventional converter with the CM filter decreases efficiency due to the large conduction loss of the CM choke. On the other hand, the proposed converter uses a small CM choke with a small number of turns. Thus, the measured efficiency of the proposed converter with the CM filter is almost the same as that of the proposed converter without the CM filter.

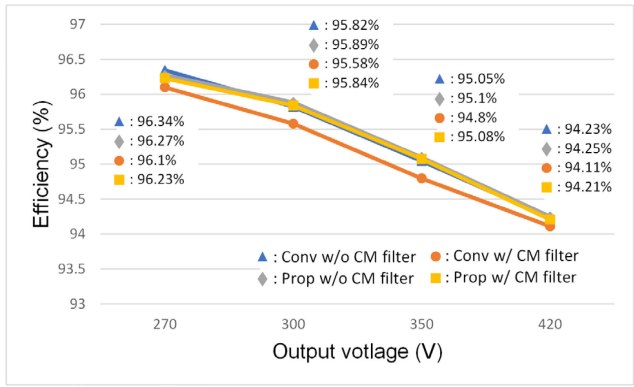

Fig. 23. Measured efficiency of the conventional and proposed converter.

V. Conclusion

In this article, a low CM noise FB *LLC* resonant converter having a balanced resonant tank is proposed. In the proposed converter, resonant inductances and capacitances in the balanced resonant tank are the same, i.e., $L_{r1} = L_{r2}$ and $C_{r1} = C_{r2}$, and the CM current flowing through the parasitic capacitors of the transformer becomes zero. Moreover, the CM noise generated from parasitic capacitors between the primary and secondary layers is decreased by locating primary and secondary layers adjacently with the same *dv*/*dt* characteristics. A 1.5-kW prototype of the FB *LLC* resonant converter is fabricated to verify the performance of the proposed converter. The CM noise of the proposed converter at the fundamental frequency is 30.7 dBμV smaller than that of the conventional converter when V_o is 420 V. Thus, the size of the EMI filter can be reduced by 83% for a single-stage *LC* CM filter and 59% for a multistage *LCLC* CM filter. As a result, the proposed converter can increase the power density for the FB *LLC* resonant converter by reducing the size of the EMI filter.

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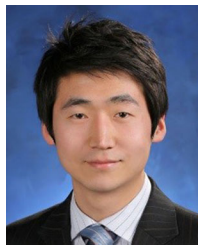

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