Fault Detection in a Hybrid Dickson DC–DC Converter for 48-V Automotive Applications

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***Abstract*— Autonomous driving features have introduced safety-critical processor modules. A 48-V network has been developed to enable efficient power distribution. A fault-tolerant high-voltage power management unit is required to ensure continuous power delivery to critical loads. This article compares the cost and efficiency penalty of accommodating the fault-tolerant capability in common dc–dc topologies. The comparison is verified using a 0.13-μm high-voltage automotive Bipolar-CMOS-DMOS SMARTMOS technology in a `Cadence` simulation environment. Besides, a quantitative reliability assessment of the single-phase and multiphase configurations is presented. This has led to the selection of the hybrid Dickson topology, which has the best electrical performance and comparable cost and reliability among all for high-conversion-ratio fault-tolerant 48-V automotive application. Moreover, this article presents a fast and robust short-circuit and open-circuit fault detection scheme for power switches and flying capacitors in a hybrid Dickson dc–dc converter. The detection method only observes the low-voltage switching node, which eliminates the challenges associated with high-voltage high-bandwidth sensing. The performance of the design has been verified using a multiphase 48-V-to-3.3-V 4-to-1 Dickson converter prototype. The measured results demonstrate that the short-circuit faults are detected within two switching cycles of 250 kHz, which is less than the 10-μs short-circuit immunity of commercial silicon devices.**

***Index Terms*—DC–DC power conversion, fault diagnosis, fault tolerance, switched capacitor circuits.**

I. Introduction

THERE is an ongoing shift toward autonomous driving systems in electric vehicles (EVs), with an expected annual market share of 85 million vehicles by 2035 [2]. In an autonomous system, a sudden failure in the power delivery path of any critical sensor or computing platform may cause a catastrophic accident. This highlights the need for a fault-tolerant power management unit (FTPMU). An FTPMU continues to deliver power to critical downstream subsystems in the event of a failure of some of its components, possibly with some performance restrictions rather than failing completely.

The increase in power demand associated with the expansion of autonomous driving systems and tightening emission regulations have pushed the conventional 12-V bus to its 3-kW maximum capacity [3]. This has led to the development of a complementary 48-V bus system in EVs [3]. The 48-V bus provides a tradeoff between reducing the power delivery conduction losses while meeting the safety-extra low-voltage requirements [4]. Transferring the higher power components to the secondary 48-V distribution network increases the system efficiency while reducing the load demand on the 12-V bus.

A high and wide input-voltage range of 24–60 V [5] necessitates a two-stage cascaded conversion system. The system is composed of a preregulator stage and postregulator stage, as shown in Fig. 1. The postregulator stage is implemented using low-voltage high figure of merit devices, capable of low-loss fast-switching behavior (in the range of megahertz), which satisfies stringent point-of-load transient response requirements. A conventional synchronous two-level converter as shown in Fig. 2(a) is commonly adopted in the postregulator stage. The preregulator stage enables efficient high-conversion-ratio power delivery. The design of a fault-tolerant preregulator stage is the main focus of this article. A high-voltage-conversion ratio at the preregulator stage presents an opportunity for hybrid

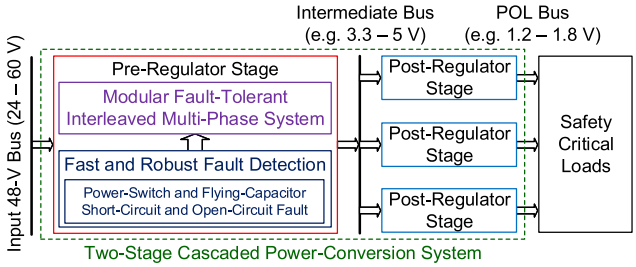

Fig. 1. High-level architecture of a two-stage cascaded power-conversion system.

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switched-capacitor (SC) converters [6]–[9]. Hybrid SC converters incorporate capacitors as the main energy storage elements, which offer relatively higher energy density compared to an inductor, resulting in higher power density [10].

The most common component failures in power converters are related to capacitors and semiconductor power switches, while failures associated with resistors and inductors are quite rare [11], [12]. The failure mechanisms in different capacitor types are presented in [13], which includes design defects, material wear-out, and out-of-bound operating conditions. Power-switch failures can be provoked by several intrinsic and/or extrinsic mechanisms such as the activation of the parasitic bipolar junction transistor, excessive thermal transients, and electrical overstresses [14]. The interaction of these failure mechanisms in both capacitors and power switches may result in open-circuit or short-circuit faults (SCFs), with the latter being the most severe [11]–[13].

The key goal of a fault-tolerant design is to intercept the propagation of a fault to avoid cascaded failures. A fault-tolerant scheme is generally composed of: 1) fault detection, which detects the occurrence of a failure; 2) fault isolation and containment, which confines the failure within a subsystem; and 3) fault compensation, which masks the effects of the failure on the system outputs [15], [16]. Fault compensation is commonly achieved through redundancy. There are two basic types of redundancy: 1) active redundancy, in which the redundant subsystems are operating and automatically overtake load for the failed unit; and 2) standby redundancy, in which the redundant subsystems are inactive and replace the failed unit upon a fault [16]. It should be noted that redundancy is not the only requirement for fault compensation, and further precautions, particularly from the control standpoint, are necessary to provide a seamless postfault operation [9].

Fault detection methods can be generally classified as: 1) device-based [17], [18]; and 2) system-based schemes [11], [12]. In device-based methods, the fault is diagnosed based on the parameter drifts caused by the degradation effects and/or dedicated embedded sensors in the device. On the other hand, system-based methods rely on system-level measurements to capture a unique fault feature. The employment of externally accessible measurements used in converter control makes this approach more desirable than device-based methods. However, the existence of an exclusive correlation between the failure modes and system characteristics is required for this approach.

Fault compensation and recovery necessitate the adoption of a multiphase configuration, which is a parallel set of subconverters. A multiphase system with one level redundancy is capable of maintaining continuous power delivery to downstream subsystems in case of a malfunction in any one of the phases. More importantly, the design must be capable of blocking the propagation of the fault to avoid cascading failures. Necessary provisions must be considered to enable isolation of the faulty phase from the rest of the system. Previous studies of FTPMUs have dealt with fault isolation by incorporating redundancy or a safety device such as fuse [19], [20]. However, doing so increases the cost or degrades the form-factor and potentially sacrifices efficiency, neither of which is acceptable in the automotive

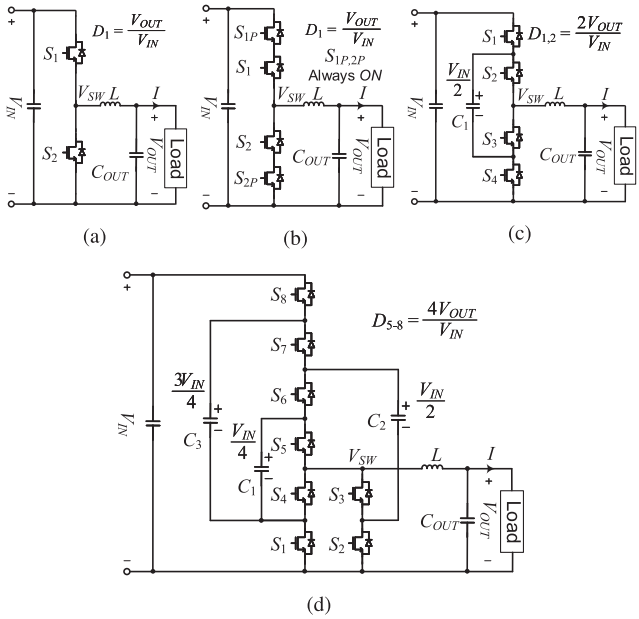

Fig. 2. Commonly used dc–dc topologies. (a) Conventional synchronous two-level converter. (b) Fault-tolerant two-level converter. (c) Three-level FCML converter. (d) 4-to-1 Dickson converter (nonfault-tolerant and fault-tolerant variants of the three-level FCML and 4-to-1 Dickson converters have the same architecture but with different power-switch voltage ratings) (V_{OUT}: output voltage, V_{IN}: input voltage, D_i: duty cycle of switch i, and I: load current).

industry. Furthermore, using a fuse is not an effective method to prevent the propagation of the fault in modern semiconductors due to the slow response time (in the millisecond range), while the short-circuit immunity of silicon power devices is in the microsecond range [21]. Consequently, a topology with inherent fault-blocking capability is desired while enabling efficient power delivery with high-voltage-conversion ratios. In other words, the system structure must prevent punch-through of the high-voltage input to the low-voltage output in an event of an SCF.

Fault-diagnosis methods presented in [19], [20], and [22]–[34] are mainly focused on conventional magnetics-based topologies. To date, [20] is the only study of fault diagnosis on a three-level flying-capacitor multilevel (FCML) converter, shown in Fig. 2(c). However, the detection method in [20] is based on sensing the floating flying-capacitor voltage, which requires high-voltage differential voltage measurement. Hybrid SC converter topologies operate based on a different operation principle and require SCF and open-circuit fault (OCF) diagnosis of both flying capacitors and power switches. Among all hybrid SC converters presented in the literature, the Dickson converter shown in Fig. 2(d) offers the best switch utilization [10] and therefore is selected for the fault studies conducted in this article. The hybrid Dickson topology can simultaneously tackle the fault-tolerant and high-conversion-ratio efficient power delivery challenges in future automotive applications.

A portion of this article was published in [1], where a system-based detection for SCFs and OCFs of the power switches and flying capacitors was demonstrated on a 4-to-1 hybrid SC Dickson converter, shown in Fig. 2(d). This article further

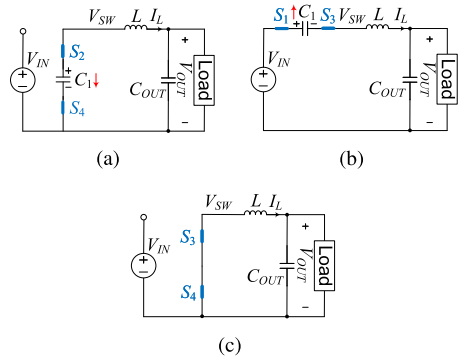

Fig. 3. Switching cycles of the three-level FCML converter. (a) State I. (b) State II. (c) State 0 (↑: charging and ↓: discharging).

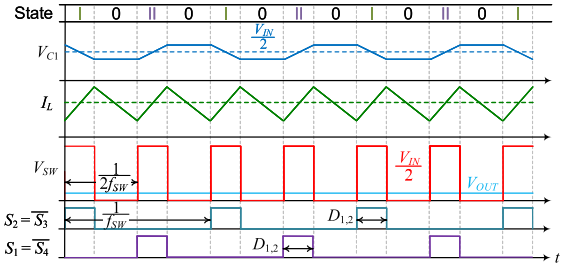

Fig. 4. Ideal key waveforms of the three-level FCML converter for a given inductance of L and switching frequency of f_{SW}.

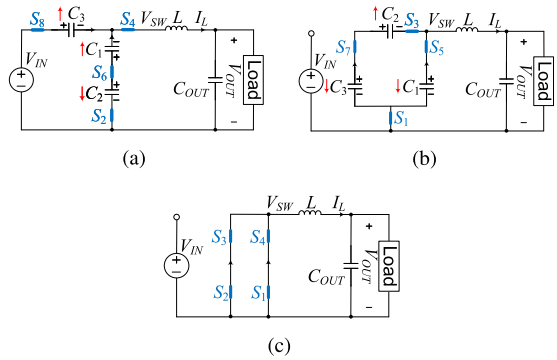

Fig. 5. Switching cycles of the 4-to-1 Dickson converter: (a) State I, (b) State II, and (c) State 0 (↑: charging and ↓: discharging).

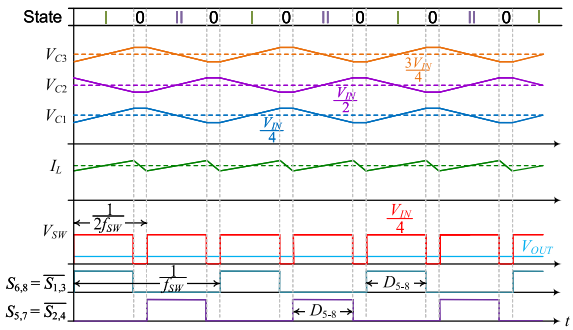

Fig. 6. Ideal key waveforms of the 4-to-1 Dickson converter for a given inductance of L and switching frequency of f_{SW}.

expands on [1] by investigating and comparing the performance of commonly used dc–dc topologies, shown in Fig. 2, as a potential candidate for future fault-tolerant 48-V automotive applications. A summary of the relevant topologies is provided in Section II. The required power-switch voltage ratings for a fault-tolerant design are studied in Section III. The effect of the fault-tolerant capability on the cost and efficiency of the design is evaluated in Section IV. This analysis is conducted based on a 0.13-μm high-voltage automotive Bipolar-CMOS-DMOS (BCD) SMARTMOS integration technology in a Cadence simulation environment. Moreover, a quantitative reliability assessment of the single-phase and multiphase converter configurations is presented in Section V. Following the discussions on the proposed fault detection scheme in Section VI, new extensive measurements on fault detection times including all possible fault scenarios have been performed and are presented in Section VII. Finally, Section VIII concludes the article.

II. Operation Principles of Three-Level FCML and 4-to-1 Dickson Converters

A. Three-Level FCML Converter

A K-level FCML converter is composed of $K-2$ flying capacitors and $2K-2$ power switches [35]. In a high-conversion-ratio application, for a given set of switching states, this architecture theoretically can provide output voltages in the range of 0 to $V_{IN}/(K-1)$. For a K-level FCML converter with the switching frequency of f_{SW}, a switching-node voltage of $V_{IN}/(K-1)$ can be provided by K-1 internal states, which results in an effective switching frequency of $f_{SW,EFF} = (K-1) \times f_{SW}$ at the switching node. Considering the 48-V two-stage power-conversion system shown in Fig. 1, this article investigates the three-level FCML converter shown in Fig. 2(c) as the preregulator stage. The corresponding switching states and ideal key waveforms are shown in Figs. 3 and 4, respectively. For a three-level FCML converter, a consecutive sequence of State I → State 0 → State II → State 0 results in a full switching cycle and, thus, the effective frequency, $f_{SW,EFF}$ at the switching node is $2 \times f_{SW}$. The discharging (State I) and charging (State II) interval is used to balance the flying-capacitor voltage. Moreover, State 0 is needed to maintain the volt-second product of the inductor and regulate the output voltage.

B. 4-to-1 Dickson Converter

A K-to-1 Dickson converter provides a maximum output voltage of V_{IN}/K and is composed of K-1 flying capacitors and K+4 power switches. Regardless of K, a switching-node voltage of V_{IN}/K can only be provided by two internal states, which results in an effective frequency of $f_{SW,EFF} = 2 \times f_{SW}$ at the switching node. Considering the input-voltage range of 24–60 V of the 48-V system and common intermediate voltages in the range of 3.3–5 V in a two-stage power-conversion system as shown in Fig. 1, this article assesses a 4-to-1 Dickson converter shown in Fig. 2(d) as the preregulator stage. The corresponding switching states and ideal key waveforms are shown in Figs. 5 and 6, respectively. A full switching cycle consists of alternative

TABLE I
POWER-SWITCH RATINGS OF A TWO-LEVEL CONVERTER

Component	RMS Current	Steady-State Voltage Rating	MOC ($\gamma = 1.5\times$)	AMR
S_1, S_{1P}	$\sqrt{D_1}\ I$	V_{IN}	$3V_{IN}/2$	V_{IN}
S_2, S_{2P}	$\sqrt{1-D_1}\ I$	V_{IN}	$3V_{IN}/2$	V_{IN}

TABLE II
POWER-SWITCH RATINGS OF A THREE-LEVEL CONVERTER

Component	RMS Current	Steady-State Voltage Rating	MOC ($\gamma = 1.5\times$)	AMR
S_1, S_2	$\sqrt{D_{1,2}/2}\ I$	$V_{IN}/2$	$3V_{IN}/4$	V_{IN}
S_3, S_4	$\sqrt{1-D_{1,2}/2}\ I$	$V_{IN}/2$	$3V_{IN}/4$	V_{IN}

TABLE III
POWER-SWITCH RATINGS OF A 4-TO-1 DICKSON CONVERTER

Component	RMS Current	Steady-State Voltage Rating	MOC ($\gamma = 1.5\times$)	AMR
S_8	$\sqrt{D_{5-8}/2}\ I/2$	$V_{IN}/4$	$3V_{IN}/8$	V_{IN}
S_7	$\sqrt{D_{5-8}/2}\ I/2$	$V_{IN}/2$	$3V_{IN}/4$	V_{IN}
S_6	$\sqrt{D_{5-8}/2}\ I/2$	$V_{IN}/2$	$3V_{IN}/4$	$3V_{IN}/4$
S_5	$\sqrt{D_{5-8}/2}\ I/2$	$V_{IN}/4$	$3V_{IN}/8$	$V_{IN}/2$
S_2, S_3	$\sqrt{1-D_{5-8}/2}\ I/2$	$V_{IN}/4$	$3V_{IN}/8$	$V_{IN}/2$
S_1, S_4	$\sqrt{1+D_{5-8}}\ I/2$	$V_{IN}/4$	$3V_{IN}/8$	$V_{IN}/2$

insertion of States I and II as shown in Fig. 5. At States I and II, even-numbered switches ($S_{2,4,6,8}$) and odd-numbered switches ($S_{1,3,5,7}$) are ON, respectively. At steady-state operation, flying-capacitor voltages V_{C1}, V_{C2}, and V_{C3} are $V_{\text{IN}}/4$, $V_{\text{IN}}/2$, and $3V_{\text{IN}}/4$, respectively [9]. As in any hybrid converter, State 0 is needed for volt-second product balancing of inductor.

III. POWER-SWITCH VOLTAGE RATINGS

The voltage ratings of a power switch can be described as: 1) maximum operation condition (MOC), which is the safe operating area of a power switch; and 2) absolute maximum rating (AMR), which should not be exceeded even for a short duration. Exceeding the AMR of a power MOSFET may lead to immediate and permanent device failure. To ensure lifetime reliability, the MOC rating of a power switch must cover the imposed voltages under the normal operating condition. This includes the repetitive ringing and overshoots during the normal operation, which, in this article, is taken into account by a safety-margin factor of $\gamma = 1.5\times$ of the steady-state blocking voltage. On the other hand, the fault conditions are not repetitive and the converter halts the operation upon detection of a fault. A fault scenario results in an abnormal circuit condition, which imposes different voltage stresses compared to a steady-state condition. Therefore, to ensure fault-blocking capability and avoid the propagation of a fault, the AMR of a power device must cover the electrical overvoltage stress imposed subject to a faulty condition. This article only considers a single-point failure of any of the power switches and flying capacitors. The current and voltage ratings of power switches under normal (MOC) and faulty (AMR) conditions for the topologies shown in Fig. 2 are summarized in Tables I–III.

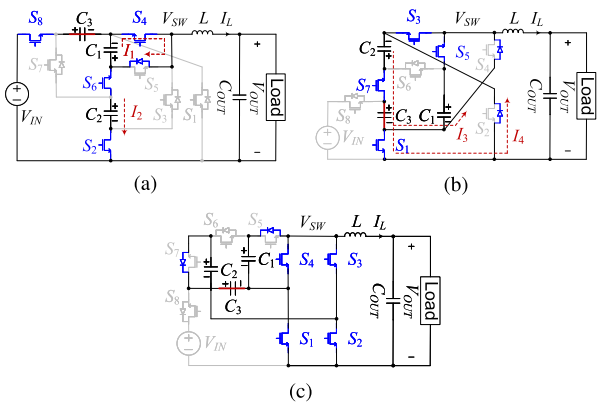

Fig. 7. Switching states of a 4-to-1 Dickson converter subject to a C_3 SCF. (a) State I. (b) State II. (c) State 0.

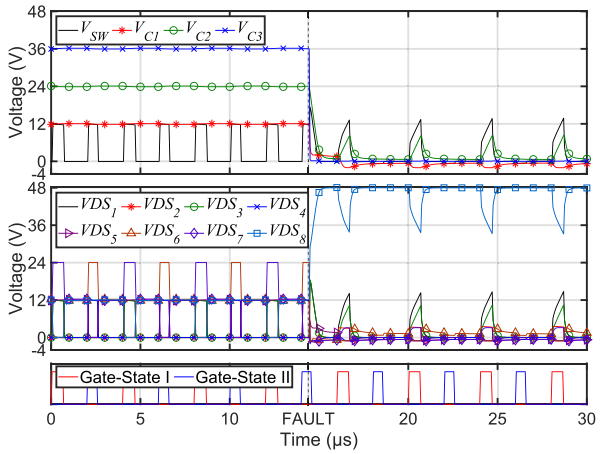

Fig. 8. Simulated behavior of a 4-to-1 Dickson converter subject to a persistent C_3 SCF without any fault detection ($V_{\text{IN}} = 48$ V, $V_{\text{OUT}} = 3.3$ V, $C_{1-3} = 4.7\,\mu$F, $L = 4.7\,\mu$F, $f_{SW} = 250$ kHz, and $I = 2$ A) (V_{Ci}: ith flying-capacitor voltage, V_{SW}: switching-node voltage, and $V\text{DS}_i$: drain-to-source voltage of power switch i).

Due to the existence of the parallel capacitive loops in a 4-to-1 Dickson converter, the circuit behavior subject to an SCF differs from what has been commonly seen in the conventional two-level and three-level FCML converters. Despite the SCF of flying capacitors which results in a malfunction in both States I and II, the SCF of power switches $S_{6,8}$ is only considered a failure in States II and 0, $S_{5,7}$ is only a failure in States I and 0, while $S_{1,3}$ and $S_{2,4}$ are a failure in States I and II, respectively.

As an example, the switching states of a 4-to-1 Dickson converter subject to a C_3 SCF are depicted in Fig. 7, in which the ON power switch S_i is drawn in blue and the OFF ones are grayed. The simulated behavior of a 4-to-1 Dickson converter subject to a persistent C_3 SCF without any fault detection is shown in Fig. 8. As it can be seen, upon the occurrence of the failure in State II, C_1 is immediately discharged through the body diode of S_6. Following that, S_6 is reversed biased by C_2 and remains OFF. Meanwhile, C_2 is discharged through $I_{3,4}$ current loops. In State I, the excessive drain-to-source voltage caused

by the absence of C_3 moves power devices S_2 and S_8 into the saturation region. Using the MOSFET square-law equation, the saturation current of a MOSFET I_{SAT} with ON-state resistance of R_{ON} can be estimated by

$$I_{\text{SAT}} = \frac{V_{\text{DRV}} - V_{\text{TH}}}{2 \times R_{\text{ON}}} \tag{1}$$

where V_{DRV} and V_{TH} are the MOSFET gate-drive and threshold voltages, respectively. The saturation current I_{SAT} dictates the fault current I_2 and passes through C_1 and C_2. Consequently, C_1 flips its polarity while it is clamped by the body diode of S_5 through the ON switch S_4. Meanwhile, C_2 is charged where its voltage change ΔV_{C2} can be estimated by

$$\Delta V_{C2} = \frac{I_2 \Delta T}{C_2} = \frac{I_{\text{SAT}} \Delta T}{C} \tag{2}$$

where ΔT is the duration of State I and C is the flying capacitance. In State 0, C_1 and C_2 discharge through the body diodes of S_5 and S_7, respectively. The exposed voltage stress on all power switches subject to a C_3 SCF can be inspected from Fig. 8. The other SCF scenarios can be investigated following the same principles and the summary of the observed required AMR voltages is tabulated in Table III.

The addition of the fault-tolerant feature may necessitate a different power-switch voltage rating. This effectively translates into an area or efficiency penalty, which can be used as a guideline for designing a fault-tolerant power stage as discussed in the following sections.

IV. Cost and Efficiency Penalty of the Fault-Tolerant Capability

A. Cost or Area Penalty of the Fault-Tolerant Capability at a Given Loss

To assess the area or cost penalty of the fault-tolerant capability, this article follows the same rationale and procedure presented in [35]. The GV^2 product of a power switch is used as an indicator of its on-chip active area, where G and V are the switch conductance and voltage rating, respectively. The switch conductance is sized corresponding to its rms current. In addition, it is assumed that a hybrid SC converter operates in the fast-switching-limit region, where the switch ON-state conductance determines the conduction losses. Moreover, in a nonfault-tolerant design, power switches are rated for MOC, while in a fault-tolerant power stage, devices are rated to the maximum of MOC and AMR based on Tables I–III. In each topology, the comparison of area or cost is used to represent the lumped effect of the fault-tolerant capability. To compare the relative area or cost of different topologies at a given loss, the conduction and switching losses are equalized among all topologies by design. This is achieved by adjusting the switch sizes to equalize the total conduction loss while the switching frequency and passive components are modified accordingly to match the switching loss and voltage/current ripples, respectively. The conventional synchronous buck converter shown in Fig. 2(a) is considered as the reference for the comparison. The relative conduction loss, area, and switching loss can be obtained using (3)–(5), respectively, where f_{SW} is the switching frequency and n is the total number of power switches

$$P_{\text{COND}} = \sum_{i=1}^{n} \frac{I_i^2}{G_i} \tag{3}$$

$$A \propto \sum_{i=1}^{n} G_i V_i^2 \tag{4}$$

$$P_{\text{SW}} \propto \sum_{i=1}^{n} G_i V_i^2 f_{\text{SW}}. \tag{5}$$

1) Conventional Two-Level Converter (2L): The relative switch conductance of a conventional two-level converter shown in Fig. 2(a), using their rms currents given in Table I, can be obtained as (6). Using (6) and the MOC ratings given in Table I, the conduction loss, area, and switching loss of a two-level converter are obtained as (7)–(9), respectively

$$\frac{G_{2,2L}}{G_{1,2L}} = \sqrt{\frac{1 - D_{2L}}{D_{2L}}} \tag{6}$$

$$P_{\text{COND},2L} = (D_{2L} + \sqrt{D_{2L}(1 - D_{2L})}) \frac{I^2}{G_{1,2L}} \tag{7}$$

$$A_{2L} \propto \frac{9}{4} \left(1 + \sqrt{\frac{1 - D_{2L}}{D_{2L}}}\right) G_{1,2L} V_{\text{IN}}^2 \tag{8}$$

$$P_{\text{SW},2L} \propto \frac{9}{4} \left(1 + \sqrt{\frac{1 - D_{2L}}{D_{2L}}}\right) G_{1,2L} V_{\text{IN}}^2 f_{\text{SW}}. \tag{9}$$

2) Fault-Tolerant Two-Level Converter (FT-2L): The conventional two-level converter shown in Fig. 2(a) can block SCF by adding protection switches, S_{1P} and S_{2P}, as shown in Fig. 2(b) [20]. S_{1P} and S_{2P} have the same rms current and voltage rating as S_1 and S_2, respectively. The protection switches are not involved in the switching states during the normal operation and are normally always ON. Using (3), the conduction loss of a fault-tolerant two-level converter is

$$P_{\text{COND,FT-2L}} = 2 \times (D_{2L} + \sqrt{D_{2L}(1 - D_{2L})}) \frac{I^2}{G_{1,FT-2L}}. \tag{10}$$

Matching the conduction loss of a fault-tolerant two-level converter with a conventional one obtained in (7), the switch conductance must satisfy

$$G_{1,\text{FT-2L}} = 2 \times G_{1,2L}. \tag{11}$$

Consequently, using (4) and (11), a fault-tolerant two-level converter area is proportional to

$$A_{\text{FT-2L}} \propto \frac{9}{2} \left(1 + \sqrt{\frac{1 - D_{2L}}{D_{2L}}}\right) G_{1,\text{FT-2L}} V_{\text{IN}}^2 \tag{12}$$

which compared to the area of a conventional two-level converter given in (8) is four times larger. Similarly, a fault-tolerant two-level converter must switch at half the frequency of a conventional one to achieve the same switching loss. Using the current ripple constraint given by

$$L = \frac{V_{\text{OUT}}(1 - D)}{f_{\text{SW}} \Delta I} \tag{13}$$

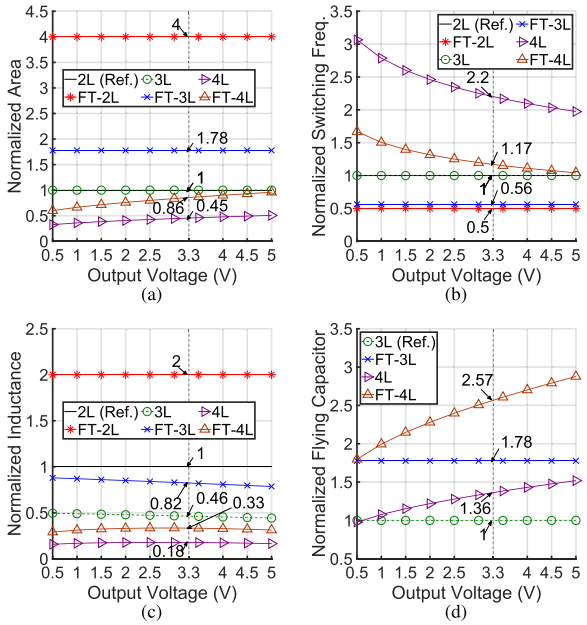

Fig. 9. Normalized parameter comparison of the understudy topologies for constant efficiency at the nominal input voltage of 48 V and different output voltages. (a) Total active area. (b) Switching frequency. (c) Inductance. (d) Total flying capacitor.

for a given current ripple of ΔI, a fault-tolerant two-level converter requires two times larger inductance to achieve the same efficiency.

3) Three-Level Converter (3L): Comparing Tables I and II shows that in a three-level converter, shown in Fig. 2(c), the MOC ratings are half of those of a two-level converter, shown in Fig. 2(a). Following the same procedure, the relative switch conductance and conduction loss of a three-level converter are given by (14) and (15), respectively

$$\frac{G_{3,3L}}{G_{1,3L}} = \sqrt{\frac{1-\frac{D_{3L}}{2}}{\frac{D_{3L}}{2}}}. \tag{14}$$

$$P_{\text{COND},3L} = (D_{3L} + \sqrt{D_{3L}(2-D_{3L})})\frac{I^2}{G_{1,3L}}. \tag{15}$$

Equalizing (15) with the conduction loss of a conventional two-level converter given in (7) gives

$$\frac{G_{1,3L}}{G_{1,2L}} = \frac{D_{3L} + \sqrt{D_{3L}(2-D_{3L})}}{D_{2L} + \sqrt{D_{2L}(1-D_{2L})}} \tag{16}$$

which enforces the same conditions as (11). Using (4), the area of a three-level converter is proportional to

$$A_{3L} \propto \frac{9}{8}\left(1 + \sqrt{\frac{1-\frac{D_{3L}}{2}}{\frac{D_{3L}}{2}}}\right) G_{1,3L} V_{\text{IN}}^2 \tag{17}$$

which results in an approximately the same semiconductor active area as that of a two-level converter. Following the same rationale, it is concluded that for the same switching loss, the three-level and two-level converters have approximately the same switching frequency. Although the switching frequency is the same, a three-level converter requires a smaller inductance as shown in Fig. 9. The flying-capacitor value C_F can be obtained using the voltage-ripple constraint as

$$C_F = \frac{I_C \times D}{2 f_{\text{SW}} \Delta V} \tag{18}$$

where I_C is the capacitor current and ΔV is the voltage ripple. Flying capacitance of a three-level FCML converter is used as the reference to compare other SC topologies.

4) Fault-Tolerant Three-Level Converter (FT-3L): As can be seen from Table II, to provide the fault-tolerant capability, all power devices must withstand the maximum input voltage. Although the corresponding switch conductance remains the same as (16), a higher voltage rating for fault blocking results in a larger area is given by

$$A_{\text{FT-3L}} \propto 2 \times \left(1 + \sqrt{\frac{1-\frac{D_{3L}}{2}}{\frac{D_{3L}}{2}}}\right) G_{1,3L} V_{,}^2. \tag{19}$$

Using (5), (13), and (18), the switching frequency, inductance and flying capacitor can be summarized as presented in Fig. 9.

5) 4-to-1 Dickson Converter (4L): In a 4-to-1 Dickson converter, in which the power-switch conductances are sized in accordance with their rms current, the conduction loss is

$$P_{\text{COND},4L} = \frac{1}{2}\left(D_{4L} + \sqrt{\frac{D_{4L}}{2}(1+D_{4L})} + \sqrt{\frac{D_{4L}}{2}\left(1-\frac{D_{4L}}{2}\right)}\right)\frac{I^2}{G_{8,4L}}. \tag{20}$$

By simplifying (20) and equalizing it to the conduction loss of a two-level converter, the relative switch conductance with respect to a conventional two-level converter is

$$\frac{G_{8,4L}}{G_{1,2L}} = \frac{\frac{1}{2}(D_{4L} + \sqrt{\frac{D_{4L}}{2}(1+D_{4L})} + \sqrt{\frac{D_{4L}}{2}(1-\frac{D_{4L}}{2})})}{D_{2L} + \sqrt{D_{2L}(1-D_{2L})}}. \tag{21}$$

Using (4), the area of a 4-to-1 Dickson converter is proportional to

$$A_{4L} \propto \frac{9}{64} \times \left(10 + 2\sqrt{\frac{1+D_{4L}}{\frac{D_{4L}}{2}}} + 2\sqrt{\frac{1-\frac{D_{4L}}{2}}{\frac{D_{4L}}{2}}}\right) G_{8,4L} V_{\text{IN}}^2. \tag{22}$$

Simplifying (22) and following the same approach, the area, switching frequency, inductance, and flying capacitors of a 4-to-1 Dickson converter can be obtained as presented in Fig. 9. It is assumed that all flying capacitors C_{1-3} are identical.

6) Fault-Tolerant 4-to-1 Dickson Converter (FT-4L): Considering a fault-tolerant 4-to-1 Dickson converter with the given AMR values in Table III, the area of a fault-tolerant 4-to-1 Dickson converter is proportional to

$$A_{\text{FT-4L}} \propto \left(\frac{45}{16} + \frac{1}{2}\sqrt{\frac{1+D_{4L}}{\frac{D_{4L}}{2}}} + \frac{1}{2}\sqrt{\frac{1-\frac{D_{4L}}{2}}{\frac{D_{4L}}{2}}}\right) G_{8,4L} V_{\text{IN}}^2. \tag{23}$$

As the device ratings have changed, to match the switching loss with a conventional two-level converter and make the same inductor current and flying-capacitor voltage ripples, the area,

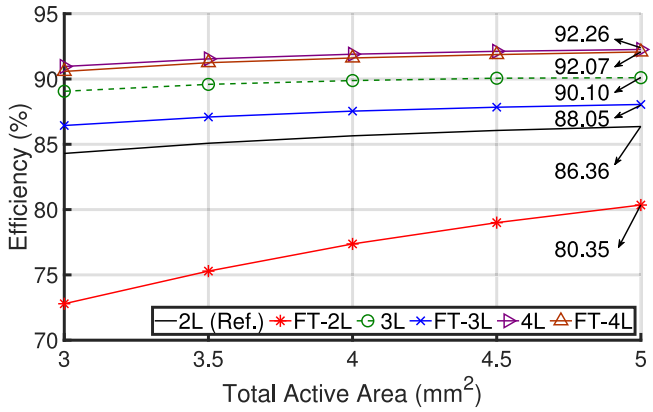

Fig. 10. Simulated optimum efficiency at a given total active area ($V_{\text{IN}} = 48$ V, $V_{\text{OUT}} = 3.3$ V, $P_{\text{SINGLE}} = 12$ W, and $f_{\text{SW}} = 250$ kHz).

switching frequency, inductance, and flying capacitors are obtained as presented in Fig. 9.

The fault-tolerant penalty of the commonly used dc–dc topologies shown in Fig. 2 is compared and summarized in Fig. 9. The maximum practical regulated output voltage of 5 V is dictated by the minimum operational input voltage of the 48-V system ($V_{\text{IN,MIN}} = 24$ V) and the maximum theoretical output voltage range of a 4-to-1 Dickson converter, which is $V_{\text{IN,MIN}}/4 = 24/4 = 6$ V. For each topology, the corresponding value of the duty cycle at the desired operating point can be obtained using the formulae provided in Fig. 2. Considering the nominal input voltage of 48 V and the output voltage of $V_{\text{OUT}} = 3.3$ V as a typical example of a two-stage cascaded power conversion system as shown in Fig. 1, a fault-tolerant 4-to-1 Dickson topology with SCF and OCF blocking capabilities occupies 14% less active device area and requires only 33% of inductance compared to a conventional two-level converter having the same efficiency at the given operating condition. Without loss of generality, this article further investigates the output voltage of 3.3 V as the targeted operating point while the provided analysis in Fig. 9 includes the whole range of output voltages.

B. Efficiency Penalty of The Fault-Tolerant Capability at a Given Area

To quantify the effect of the fault-tolerant capability on the power-stage efficiency at a given total active area, dc–dc topologies shown in Fig. 2 have been simulated in a 0.13-μm 90-V automotive BCD SMARTMOS technology in a `Cadence` environment. In each case, the power-switch sizes have been swept within a given total active area to optimize efficiency. The closest available voltage rating of the technology power switches to those presented in Tables I–III has been chosen for each topology. The simulated optimum efficiency under the nominal operating conditions at a given total active area is shown in Fig. 10. The calculated efficiency includes conduction, switching, and driver losses. The inductance values have been adjusted for each topology to achieve the same ripple current. The two-level, three-level, and 4-to-1 Dickson converters have output inductance of 12, 5.6, and 4.7 μH, respectively. As shown in Fig. 10, among all the understudy topologies, a 4-to-1 Dickson converter has the best efficiency at different active areas, while it suffers the least from the additional fault-tolerance feature. As an example, at 5-mm^2 total active area, the efficiency penalty of the fault-tolerant capability is about 0.2% and 2% for a 4-to-1 Dickson converter and three-level converter, respectively.

V. Reliability Assessment

The useful life period of a device is characterized by a constant failure rate and is the basis for most reliability engineering methods [16]. For a device with a constant failure rate of λ_i, the probability of not failing prior to time t is expressed by an exponential-distribution reliability function $R_i(t)$ as

$$R_i(t) = e^{-\lambda_i t}. \tag{24}$$

Based on the military handbook MIL-HDBK-217 [36], the failure rate of each device can be expressed in the form of

$$\lambda_i = \lambda_b \prod_{i=1}^{n} \pi_i \tag{25}$$

where λ_b is the base failure rate and n is the total number of failure factors π_i, which takes into account the ambient/junction temperature, voltage stress, application type, and quality factor [36]. For a phase configuration composed of M independent devices with a series reliability model, the system reliability $R_p(t)$ is

$$R_p(t) = e^{-\lambda_p t} = \prod_{i=1}^{M} R_i(t) \tag{26}$$

where

$$\lambda_p = \sum_{i=1}^{M} \lambda_i. \tag{27}$$

A quantitative assessment of the single-phase reliability for the understudy topologies, shown in Fig. 2, has been derived and is presented in Fig. 11(a). The analysis considers a single-phase output power of $P_{\text{SINGLE}} = 9$ W and a mission period of 10 years, which is a typical operational period in the automotive industry. The junction temperature of each topology T_J has been calculated as

$$T_J = T_A + R_{\text{CA}} \times P_{\text{LOSS}} \tag{28}$$

where T_A is the ambient temperature (25°C), R_{CA} is the case-to-ambient thermal resistance ([$p$er-mode=symbol]40°C W^{-1}), and P_{LOSS} is extrapolated from simulations at 5-mm^2 total active area as shown in Fig. 10. A 4.7-μF 100-V general-purpose ceramic capacitor has been considered for all flying capacitors. In addition, the input capacitor, output inductor, and output capacitor are common to all topologies and have not been included in this analysis. As shown in Fig. 11(a), as a single-phase converter, the conventional two-level topology [Fig. 2(a)] offers the best reliability within the targeted time interval, while a fault-tolerant two-level topology [Fig. 2(b)] offers the worst.

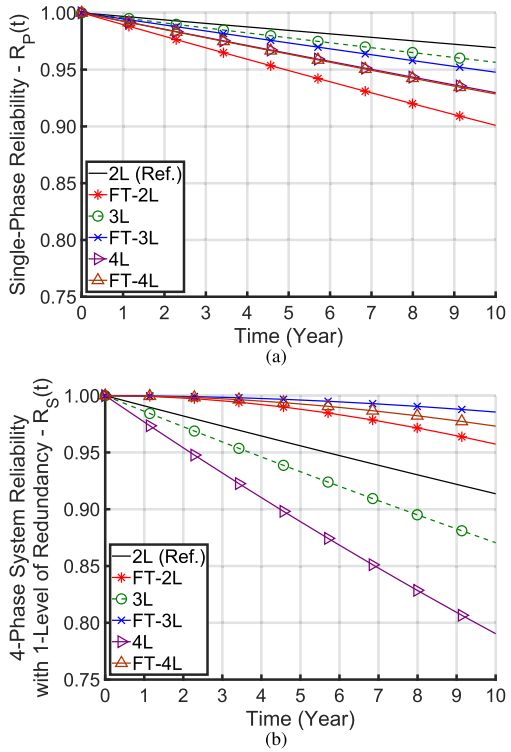

Fig. 11. Quantitative reliability analysis of (a) a single-phase converter and (b) 4-phase system with 1 level of redundancy, ($V_{\text{IN}} = 48$ V, $V_{\text{OUT}} = 3.3$ V, $f_{\text{SW}} = 250$ kHz, $P_{\text{SINGLE}} = 9$ W, and $P_{\text{MULTI}} = 36$ W).

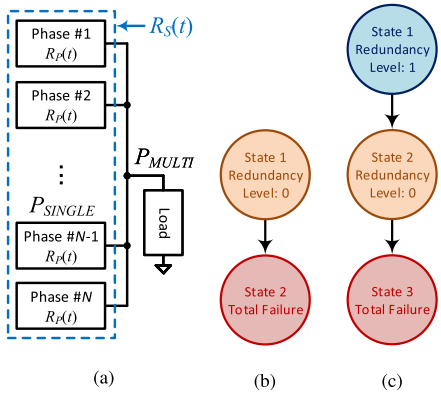

Fig. 12. (a) Multiphase system configuration, (b) reliability model of a nonfault-tolerant multiphase system, and (c) reliability model of a fault-tolerant multiphase system with 1-level of redundancy.

The reason behind this is the addition of the series protection switches, S_{1P} and S_{2P}, and considerably higher power loss of the fault-tolerant two-level converter compared to its nonfault-tolerant counterpart as presented in Fig. 10. Although the three-level FCML [Fig. 2(c)] and 4-to-1 Dickson [Fig. 2(d)] topologies have higher number of components, they represent a higher reliability value compared to the fault-tolerant two-level converter, thanks to their considerably better efficiency and thus lower T_J for a given total active area, as shown in Fig. 10.

Considering a fault-tolerant N-phase design with J-level of redundancy as shown in Fig. 12(a), in which each phase has the reliability of $R_p(t)$, the reliability of the whole multiphase system $R_s(t)$ is given by a series of additive binomial terms as

$$R_s(t) = \sum_{i=0}^{J} \binom{N}{N-i} R_p(t)^{(N-i)} (1 - R_p(t))^i. \tag{29}$$

The first level of redundancy provides the greatest gain in reliability and there is a diminishing gain as the number of redundant units increases [16]. The reliability of a nonfault-tolerant multiphase system is obtained by substituting $J = 0$ in (29). As compared to the reliability model of a nonfault-tolerant multiphase system shown in Fig. 12(b), a fault-tolerant multiphase configuration with one level of redundancy contains an additional intermediate state, which takes into account the fault-tolerance and redundancy aspects of the design as shown in Fig. 12(c). To demonstrate the benefits of a fault-tolerant multiphase design on the reliability, the overall system reliability of a 4-phase configuration with fixed output power of $P_{\text{MULTI}} = 36$ W is shown in Fig. 11(b). Upon the loss of any phase in a fault-tolerant design with 1-level redundancy, the output power of the remainder healthy phases is increased from 9 to 12 W to compensate for the absence of the failed phase. As shown in Fig. 11(a), although a single fault-tolerant two-level converter offered the worst reliability, its multiphase variant offers a better reliability value compared to a multiphase system composed of its nonfault-tolerant conventional counterpart. This improvement is accomplished through the addition of the fault-tolerant capability and one level of redundancy. Similarly, the fault-tolerant three-level FCML and fault-tolerant 4-to-1 Dickson multiphase configurations provide a better reliability value compared to their nonfault-tolerant counterparts.

VI. Fault Detection Method

A. Choice of Observation Node

The kirchhoffs voltage law (KVL) equations in States I and II are given by (31) and (33), respectively, where V_{IN} is the input voltage and V_{Ci} is the voltage across flying capacitor C_i. The voltages at the switching node are denoted as V_{SW1} and V_{SW2} during States I and II, respectively. During State 0, flying-capacitor voltages remain unchanged and are not considered in the analysis

$$\text{State I} : V_{\text{SW1}} = V_{\text{IN}} - V_{C3} = V_{C2} - V_{C1} \tag{30}$$

$$\rightarrow V_{\text{IN}} - V_{C2} = V_{C3} - V_{C1} \tag{31}$$

$$\text{State II} : V_{\text{SW2}} = V_{C3} - V_{C2} = V_{C1} \tag{32}$$

$$\rightarrow V_{C2} = V_{C3} - V_{C1}. \tag{33}$$

During steady-state operation, (31) and (33) are both satisfied and result in

$$V_{\text{IN}} - V_{C2} = V_{C2} \tag{34}$$

$$\rightarrow V_{C2} = \frac{V_{\text{IN}}}{2} \tag{35}$$

$$V_{C3} - V_{C1} = \frac{V_{\text{IN}}}{2}. \tag{36}$$

On one hand, (35) indicates that the steady-state operation of the circuit sets the average voltage of the flying capacitor

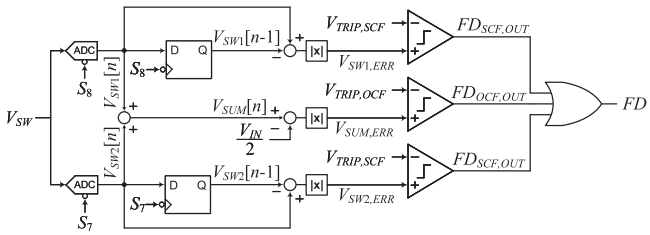

Fig. 13. Fault detection scheme (FD: fault detection).

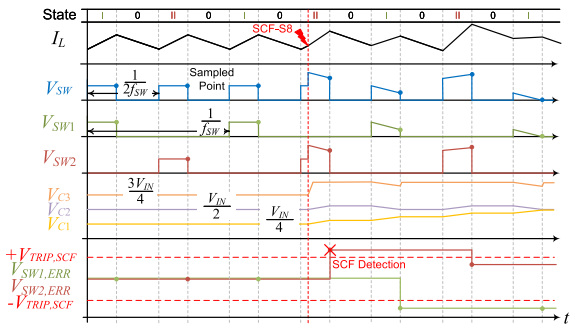

Fig. 14. Key waveforms of the SCF detection scheme (FD_{SCF}). Voltage deviations exceeding the threshold voltage $V_{TRIP,SCF}$ represent the occurrence of an SCF.

C_2 to $\frac{V_{IN}}{2}$. On the other hand, based on (36), the difference of V_{C3} and V_{C1} is set to $\frac{V_{IN}}{2}$, while the absolute average values of V_{C1} and V_{C3} are undetermined. In other words, (36) indicates that decrease/increase of the average value of V_{C1} results in decrease/increase of the average value of V_{C3} and vice versa. Consequently, the average voltage of flying capacitors C_1 and C_3 requires voltage balancing, while C_2 is automatically balanced by circuit operation. The optimum operating condition is achieved for equal switching-node voltages in States I and II. Based on (31) and (33), equalizing switching-node voltages, V_{SW1} and V_{SW2}, results in desired flying-capacitor voltages of $\frac{V_{IN}}{4}$ and $\frac{3V_{IN}}{4}$ for C_1 and C_3, respectively. In a fixed-frequency control scheme, the adjustment of the charging and discharging intervals, T_{ON1} and T_{ON2}, can be deployed to balance flying-capacitor voltages V_{C1} and V_{C3}.

The SCF or OCF of one of the power switches or flying capacitors invalidates the KVL equations given in (31) and (33). As a result, the flying-capacitor voltages differ from the desired values and, correspondingly, the switching-node voltages in States I and II deviate from the nominal value of $\frac{V_{IN}}{4}$. The proposed fault detection scheme in this article samples the switching-node voltage during States I and II intervals and derives an exclusive fault signature to detect SCF and OCF of the power devices and flying capacitors. The presented method is based on two detection algorithms, referred to as FD_{SCF} and FD_{OCF}, as shown in Fig 13. The detection algorithms FD_{SCF} and FD_{OCF} are used to diagnose the SCF and OCF, respectively.

B. SCF Detection

As shown in Figs. 13 and 14, the voltages at the switching node, $V_{SW1}[n]$ and $V_{SW2}[n]$, are sampled in each switching state

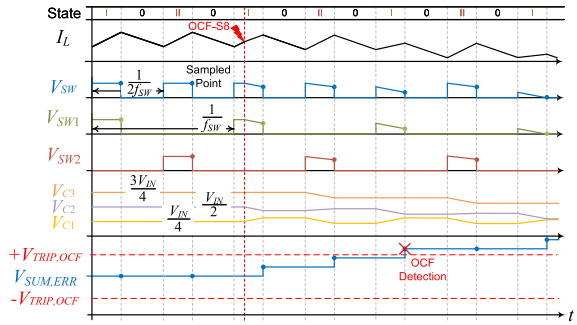

Fig. 15. Key waveforms of the OCF detection scheme (FD_{OCF}). Voltage deviations exceeding the threshold voltage $V_{TRIP,OCF}$ represent the occurrence of an OCF.

using control signals S_8 and S_7, respectively. The system also holds the previously sampled switching-node voltage from each switching state, referred to as $V_1[n-1]$ and $V_2[n-1]$. To detect the SCFs, the absolute deviation of the consecutive switching-node voltages in each switching state, $V_{SW1,ERR}$ and $V_{SW2,ERR}$ as expressed in (37) and (38), respectively, is monitored and compared with a predetermined threshold voltage $V_{TRIP,SCF}$. Small voltage deviations of consecutive samples indicate the healthy operation of the system, while voltage deviations exceeding the threshold voltage $V_{TRIP,SCF}$ represent the occurrence of an SCF in either power switches or flying capacitors

$$V_{SW1,ERR} = V_{SW1}[n] - V_{SW1}[n-1] \tag{37}$$

$$V_{SW2,ERR} = V_{SW2}[n] - V_{SW2}[n-1] \tag{38}$$

$$\left.\begin{aligned} V_{SW1,ERR} \geq V_{TRIP,SCF} \\ \text{OR} \\ V_{SW2,ERR} \geq V_{TRIP,SCF} \end{aligned}\right\} \Rightarrow FD_{SCF,OUT} = 1. \tag{39}$$

C. OCF Detection

Although an SCF results in an abrupt change of the switching-node voltages, OCFs are considerably less severe and result in slow voltage gradients on the switching-node voltages. The slow gradient of the switching-node voltages during OCFs leads to small voltage deviations, $V_{SW1,ERR}$ and $V_{SW2,ERR}$, which makes FD_{SCF} unable to detect these faults. To address this issue, the fault-detection scheme FD_{OCF}, shown in Figs. 13 and 15, is proposed for OCF diagnosis. Using (30), (32), and (35), the addition of the sampled switching-node voltages in States I and II, $V_{SW1}[n]$ and $V_{SW2}[n]$, results in (40), where V_{SUM} is the result of the summation

$$\begin{aligned} V_{SUM} &= V_{SW1}[n] + V_{SW2}[n] \\ &= \underbrace{V_{C2} - V_{C1}}_{\text{State I}} + \underbrace{V_{C1}}_{\text{State II}} = V_{C2} = \frac{V_{IN}}{2} \\ &= \underbrace{V_{C2} - V_{C1}}_{\text{State I}} + \underbrace{V_{C3} - V_{C2}}_{\text{State II}} = V_{C3} - V_{C1} = \frac{V_{IN}}{2}. \end{aligned} \tag{40}$$

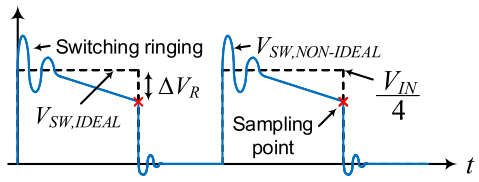

Fig. 16. Nonideal and ideal switching-node voltages.

As (40) indicates, the normal operation of the converter leads to V_{SUM} equal to $\frac{V_{\text{IN}}}{2}$. In this article, the deviation of the V_{SUM} from its nominal value is adopted as a unique signature to detect the OCF of power switching devices and flying capacitors. As shown in Fig. 13 and expressed in (41) and (42), the absolute difference of the summation result from $\frac{V_{\text{IN}}}{2}$ is monitored and compared with a predetermined threshold voltage $V_{\text{TRIP,OCF}}$. For deviations greater than $V_{\text{TRIP,OCF}}$, the output of the comparator $\text{FD}_{\text{OCF,OUT}}$ is asserted, indicating the occurrence of an OCF

$$V_{\text{SUM,ERR}} = V_{\text{SUM}}[n] - \frac{V_{\text{IN}}}{2} \tag{41}$$

$$V_{\text{SUM,ERR}} \geq V_{\text{TRIP,OCF}} \Rightarrow \text{FD}_{\text{OCF,OUT}} = 1. \tag{42}$$

The OCF of either power switches or flying capacitors disturbs the flying-capacitor voltage balancing and results in the deviation of (40) from its nominal value. As an example, while C_2 is being discharged in State I [Fig. 5(a)], a C_3 OCF prevents the charging of C_2 in State II [Fig. 5(b)] and consequently results in continuous gradual discharge of C_2. Similarly, a C_2 OCF translates into a continuous charge of C_3 in State I [Fig. 5(a)] and a continuous discharge of C_1 in State II [Fig. 5(b)], which results in the deviation of (40) from its nominal value.

D. Practical Considerations

In a practical system, the parasitic inductance of the commutation loop results in ringing of the switching-node voltage at the edge of the switching event, as shown in Fig. 16. To avoid a false fault detection by capturing the switching ringings, it is recommended to perform the sampling event on the falling edge of the switching signal as shown in Fig. 16. Moreover, a nonideal switching-node voltage $V_{\text{SW,NONIDEAL}}$ includes the resistive voltage drop ΔV_R as shown in Fig. 16. The ΔV_R is induced by the parasitic trace resistance and ON-state resistance of the power switches. While the difference equations (37) and (38) are not affected by ΔV_R, the sum equation (40) includes this voltage drop. The $V_{\text{TRIP,OCF}}$ must take this voltage drop into account to avoid false fault detection under the normal operating conditions. Consequently, $V_{\text{TRIP,OCF}}$ is practically needed to be chosen greater than $V_{\text{TRIP,SCF}}$.

In addition, using the voltage-ripple constraint given in (18), the flying-capacitor voltage ripple is designed to be a small fraction of the smallest flying-capacitor voltage V_{C1} and its effect on the switching-node voltage can be neglected. Furthermore, as expressed in (37)–(39), the SCF fault detection relies on the switching transitions (States I and II) and requires switching-node voltage samples from two switching cycles regardless of the switching period. As such, to avoid the cascaded failure of other devices due to the short-circuit inrush currents induced by an SCF, the switching frequency f_{SW} must satisfy

$$2 \times f_{\text{SW}} < \text{SCI} \tag{43}$$

where SCI is the short-circuit immunity time of the power switches. Considering $10\,\mu$s SCI of commercially available silicon devices [21], the minimum practical switching frequency is limited to 200 kHz.

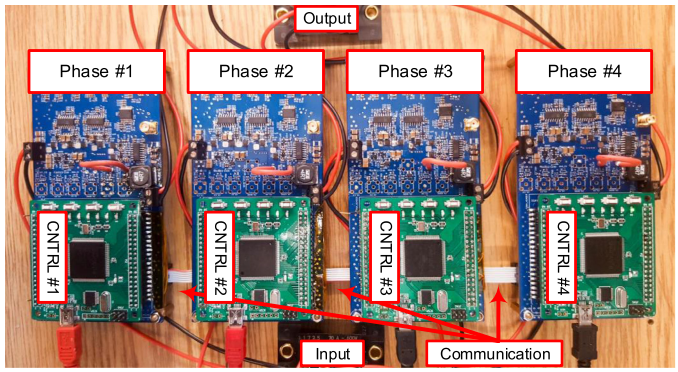

Fig. 17. Experimental setup. The printed-circuit board (PCB) includes additional circuitry to impose SCF and OCF on the flying capacitors.

TABLE IV
EXPERIMENTAL PARAMETERS

Parameter	Value	Unit
Single-phase nominal power, P_{SINGLE}	9	W
Input voltage, V_{IN}	24 - 60	V
Output voltage, V_{OUT}	3.3 $\pm$ 10%	V
Switching frequency, f_{SW}	250	kHz
Apparent Switching frequency, $2 \times f_{SW}$	500	kHz
Output inductance, L	3.3	µH
Output capacitance, C_{OUT}	40	µF
Flying capacitance, C_{1-3}	4.7	µF

VII. EXPERIMENTAL RESULTS

The performance of the proposed fault detection scheme has been verified using the experimental prototype shown in Fig. 17. The experimental parameters are listed in Table IV. This article employs the decentralized modular quasi-fixed-frequency (QFF) control scheme of a multiphase system presented in [9]. The QFF control scheme is based on the valley-current mode and ON-time control. The valley current and ON-time are used for output voltage and frequency regulations, respectively. The output voltage regulation loop is composed of a droop-based voltage loop and a hysteretic valley-current control. A droop-based voltage control enables decentralized balanced current distribution of the multiphase system through the insertion of a virtual resistance R_{DROOP} in the voltage regulation loop. The frequency control is accomplished by adjusting the ON-time

TABLE V
MEASURED SCF DETECTION TIMES (μS) ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, AND $P_{SINGLE} = 9$ W)

Component	SCF			
	State I	State 0_I	State II	State 0_{II}
S_8	2.72	2.12	1.8 (Fig. 18)	2.12
S_7	3.06	3.86	5.94	5.34
S_6	5.16	4.56	4.5	4.12
S_5	4.3	3.92	6.7	6.16
S_4	4.04	3.44	2.04	5.44
S_3	1.84	5.22	3.86	3.28
S_2	4.12	3.5	2.14	5.52
S_1	1.84	5.22	3.88	3.22
C_3	3.38	3.48	2.92	3.48
C_2	3.6	5.8 (Fig. 20)	4.12	3.34
C_1	3.94	3.66	5.44	4.72

TABLE VI
MEASURED OCF DETECTION TIMES (μS) ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, AND $P_{SINGLE} = 9$ W)

Component	OCF			
	State I	State 0_I	State II	State 0_{II}
S_8	55	69.4 (Fig. 19)	56.8	56.4
S_7	58.6	53.2	57	60.2
S_6	47	46.6	48.4	47.8
S_5	56.6	56	56.8	58
S_4*	22.6	25.8	24.4	23.5
S_3*	47.5	46.3	44.1	47.8
S_2*	45.1	48.8	47.4	46.9
S_1*	24.8	22.5	20.3	26.1
C_3	32.4	39.2	34.4	34
C_2	17.4	20.4 (Fig. 21)	18.8	18.6
C_1	30.2	33.2	31.8	31.6

Only OCF of S_{1-4} cannot be emulated on the experimental prototype due to the presence of body diodes. The presented results for S_{1-4} are obtained from a detailed simulation test.

of a full switching cycle through a digital phase-locked loop. As indicated by (35) and (36), V_{C2} is set to $V_{IN}/2$ by the circuit operation while the absolute average values of V_{C1} and V_{C3} is not constrained [9]. The flying-capacitor voltages V_{C1} and V_{C3} are controlled through State I (charging) and State II (discharging) intervals as shown in Figs. 5 and 6 [9]. Further details of the utilized control scheme can be found in [9]. The converter's digital control system has been implemented in one field-programmable gate arrays (FPGA) per phase. The performance of the fault detection scheme is studied on a single-phase system, while the fault-blocking capability and postfault operation of the design are demonstrated on a multiphase system. The multiphase system has been designed with one level of redundancy and is capable of full load power delivery in the absence of any one of the phases.

A. SCF and OCF Detection

The SCF and OCF of power switches have been emulated by forcing the gating signal ON or OFF, respectively, independent of the controller input. To emulate the failure of a flying capacitor, an optically controlled solid-state relay has been utilized. The threshold voltages, $V_{TRIP,SCF}$ and $V_{TRIP,OCF}$, are adjustable and have been set to 2 and 4 V, respectively, in this article. The measured SCF and OCF fault detection times are summarized in Tables V and VI. The measured SCF detection times are within two switching cycles ($2 \times 1/250$ kHz $= 8$ μs), which is less than 10-μs short-circuit immunity of commercial silicon devices [21].

For the sake of brevity, the measured results for SCF and OCF of only S_8 and C_2 are presented. To evaluate the performance of the SCF detection scheme, power switch S_8, as an example of a high-side device, has been subjected to an SCF during State II. As shown in Fig. 18, the SCF is detected within 1.8 μs, shown by the fault indicator signal, $FD_{SCF,OUT}$. Note that the SCF detection time is less than the SC capability of the commercial silicon power devices, which is required to be more than 10 μs [21]. To isolate the faulty converter, all the gating signals have been blocked upon detection of the fault. The effectiveness of the proposed OCF detection scheme FD_{OCF} has been assessed by applying an OCF to power switch S_8 during State 0_I. The

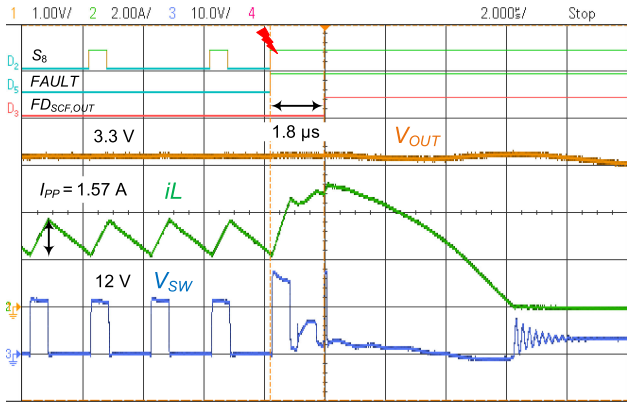

Fig. 18. Measured response for S_8 SCF detection at State II within 1.8 μs ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, and $P_{SINGLE} = 9$ W).

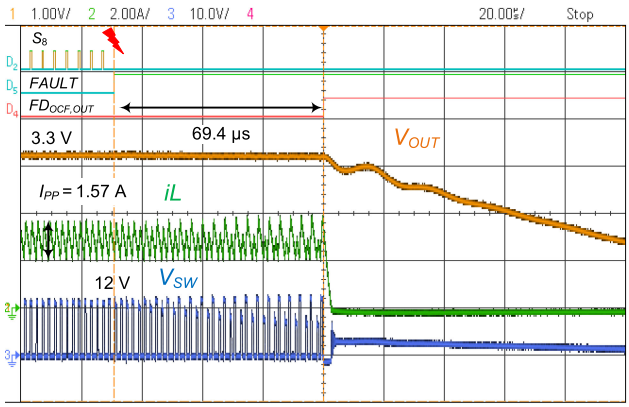

Fig. 19. Measured response for S_8 OCF detection at State 0_I within 69.4 μs ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, and $P_{SINGLE} = 9$ W).

measured results shown in Fig. 19 indicate that the emulated OCF is detected within 69.4 μs of the fault. Note that the OCF detection takes longer than the SCF detection as the flying capacitors are discharged slowly, which reduces the severity of the fault, and the need for a faster reaction as opposed to an SCF.

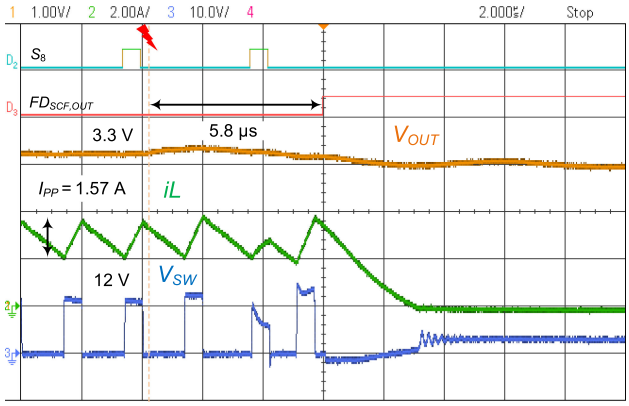

Fig. 20. Measured response for C_2 SCF detection at State 0_I within 5.8 μs ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, and $P_{SINGLE} = 9$ W).

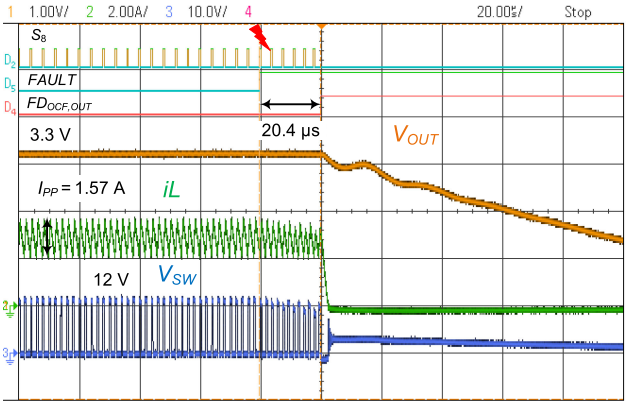

Fig. 21. Measured response for C_2 OCF detection at State 0_I within 20.4 μs ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, and $P_{SINGLE} = 9$ W).

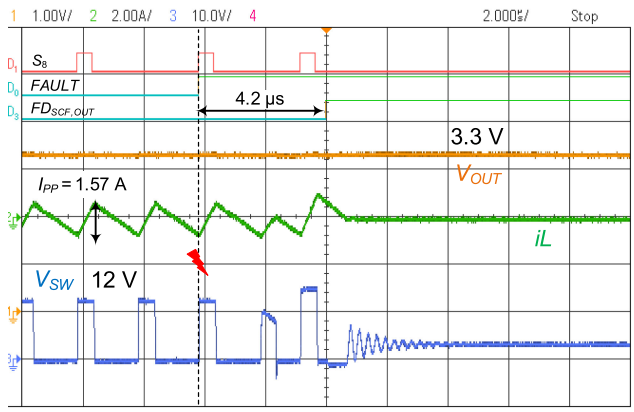

Fig. 22. Measured response for S_4 SCF detection at State I within 4.2 μs ($V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, and $P_{SINGLE} = 0$—no load).

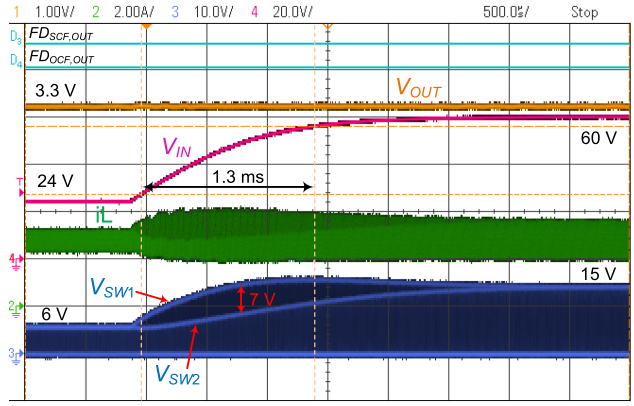

Fig. 23. Measured response for step-up input-voltage transient from 24 to 60 V in 1.3 ms ($V_{OUT} = 3.3$ V and $P_{SINGLE} = 9$ W).

The fault is detected as the absolute difference of the summation result, $V_{SUM,ERR}$ exceeds the predetermined threshold voltage, $V_{TRIP,OCF}$.

To study the system behavior subject to the short failure of a flying capacitor, C_2 has been subjected to an SCF as shown in Fig. 20. In State I, the SCF of C_2 shorts the C_1 top-plate to ground and, correspondingly, results in a negative voltage on the C_3 bottom-plate. As a consequence, C_3 is charged rapidly while C_1 is discharged. In State II, C_1 and C_3 are in parallel, resulting in a charge exchange between the two flying capacitors. The circuit configurations during the fault lead to very high inrush currents, which emphasizes the importance of a fast fault detection scheme. As shown in Fig. 20, the applied failure results in abrupt changes of the switching-node voltage. The measured results confirm the successful detection of the failure within 5.8 μs. To demonstrate the detection of a flying-capacitor OCF, the flying capacitor C_2 has been subjected to an OCF failure as shown in Fig. 21. In State I, only C_3 is charged due to the OCF of C_2, while in State II, only C_1 is discharged. As a result, the switching-node voltage declines gradually after the fault. As shown in Fig. 21, the proposed fault detection method captures the occurrence of the fault within 20.4 μs.

The measured response of the fault detection scheme under a no-load condition is shown in Fig. 22. As it can be seen, an S_4 SCF occurs at the beginning of State I and results in a change of the subsequent switching-node voltages. The proposed scheme has successfully detected the fault and blocked the converter within 4.2 μs.

B. Immunity to Transients

To demonstrate the immunity of the proposed detection scheme to input-voltage transients, a step-up transient from 24 to 60 V in 1.3 ms has been applied [5]. As shown in Fig. 23, a relatively large (~7 V) voltage deviation of switching-node voltages, V_{SW1} and V_{SW2}, is observed during the transient until the flying-capacitor voltages are rebalanced to their optimum levels. However, as shown in Fig. 23, fault indicator signals, $FD_{SCF,OUT}$ and $FD_{OCF,OUT}$, remain low, which confirm the immunity of the proposed scheme to the input voltage transients. The fault detection immunity subject to a load transient is evaluated as shown in Fig. 24. Despite an input-voltage transient that resulted in a temporary deviation of the flying-capacitor voltages, during a load step, the switching-node voltage is not exposed to a large variation. Subsequently, the error signals, $V_{SW1,ERR}$, $V_{SW2,ERR}$, and $V_{SUM,ERR}$ do not exceed the fault detection threshold voltages, $V_{TRIP,SCF}$ and $V_{TRIP,OCF}$, which verifies the immunity of the detection schemes subject to a load transient.

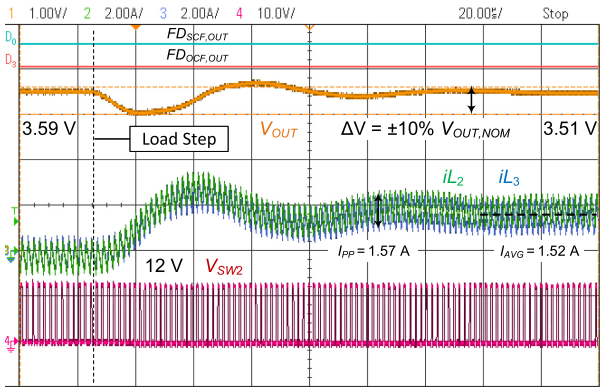

Fig. 24. Measured response of the closed-loop 3-phase system subject to a load step from no load to 16 W—due to the limitation of four analog channels, only $iL_{2,3}$ are shown ($V_{\text{IN}} = 48$ V, V_{OUT} at no load $= 3.6$ V, and $R_{\text{DROOP}} = 55\,\text{m}\Omega$).

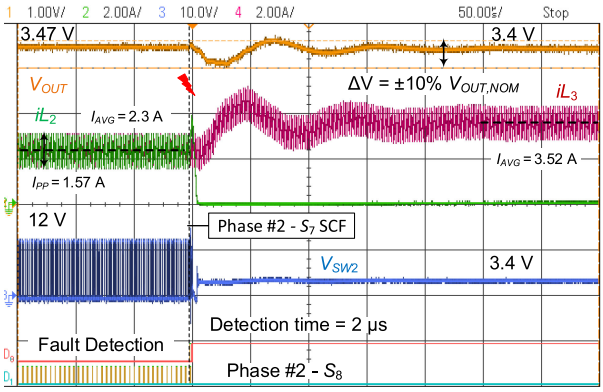

Fig. 25. Measured response of the closed-loop 3-phase system subject to the failure of Phase $\#2 - S_7$ SCF—due to the limitation of four analog channels, only $iL_{2,3}$ are shown ($V_{\text{IN}} = 48$ V, V_{OUT} at no load $= 3.6$ V, $R_{\text{DROOP}} = 55\,\text{m}\Omega$, and $P_{\text{MULTI}} = 24$ W).

C. Fault-Tolerant Operation of the Multiphase System

The fault-tolerant operation of a 3-phase system is shown in Fig. 25. Before the occurrence of any failure, each phase is delivering 8-W power. In this test, Phase $\#2$ has been subjected to an S_7 SCF. Upon the detection of the failure within 2 μs (fault detection stage), Phase $\#2$ has blocked all its gating signals to avoid the propagation of the failure to the remainder of the system (fault isolation and containment stage). The remainder of the system has automatically redeemed the absence of Phase $\#2$ by increasing their output power from 8 to 12 W (fault compensation stage). As shown in Fig. 25, the design enables continuous power delivery to the load regardless of the failure of any phase, while providing balanced current sharing and acceptable voltage regulation.

VIII. Conclusion

The comparison of common dc–dc topologies has revealed that the 4-to-1 hybrid Dickson converter provides the best electrical performance, while it offers comparable cost and reliability with fault tolerance for a multiphase configuration with one level of redundancy in high-conversion-ratio 48-V automotive applications. The measured results verify that the proposed fault detection criteria, which are based on the single ground-referenced measurement of the switching-node voltage, enable a fast and reliable means for detecting SCF and OCF of power devices and flying capacitors in a 4-to-1 hybrid Dickson converter. Particularly, SCFs are detected within two switching cycles ($2 \times 1/250$ kHz $= 8$ μs), which prevents the possibility of cascading failures due to the very high inrush currents. The presented analysis and fault detection scheme facilitate the implementation of a FTPMU for future autonomous driving systems.

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