Letters

Double Half-Bridge Submodule-Based Modular Multilevel Converters With Reduced Voltage Sensors

Chengkai Liu, Fujin Deng, *Senior Member, IEEE*, Qingsong Wang, *Senior Member, IEEE*, Yanbo Wang, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Zheng Wang, *Senior Member, IEEE*

***Abstract*—The half-bridge (HB) submodule (SM) based MMC requires a large number of sensors to measure capacitor voltages. In this letter, a double half-bridge (DHB) SM-based MMC is proposed, where each SM consists of two HBs. But only one voltage sensor is equipped in each DHB-SM for the capacitor voltage estimation, which is connected between the positive poles of two capacitors in the DHB-SM. A capacitor voltage estimation method is also proposed, which can estimate capacitor voltages in the proposed MMC with only a half number of voltage sensors in comparison with HB-SM-based MMCs. A DHB-SM-based three-phase MMC is simulated with power systems computer aided design/electromagnetic transients including DC (PSCAD/EMTDC) and a DHB-SM-based single-phase MMC prototype is built in the laboratory. Both the simulation and experimental results confirm the effectiveness of the proposed method.**

***Index Terms*—Half bridge (HB), modular multilevel converters (MMCs), submodule (SM), voltage sensor.**

I. Introduction

THE modular multilevel converters (MMCs) have received great interest from both academic and industry due to its advantages, such as easy construction, flexibility in converter design, excellent output voltage, and high efficiency [1]–[5].

In the conventional half-bridge (HB)-submodule (SM)-based MMCs, a large number of sensors are equipped to measure the capacitor voltages, where the number of the voltage sensor is the same to that of the SM [6]. Recently, a number of studies are focused on reducing voltage sensors in MMCs, which can be divided into three categories: software-based methods, hardware-based methods, and fix pattern-based methods.

In software-based methods, the SM capacitor voltages are estimated through the system dynamics along with a number of extra sensors. The individual capacitor voltages can be estimated with the weighted recursive least square algorithm [7] or Kalman filter [8], where extra voltage sensors are equipped to measure the arm voltages. Similarly, an adaptive linear neuron algorithm is used in [9], where the voltages on the arm inductors are measured by extra voltage sensors. In [10], the output voltages of SM groups are measured by sensors and the capacitor voltages can be obtained when only one SM is activated in the SM group. A capacitor voltage estimation with capacitance self-updating based on the grouping measurement is presented in [11], which increases the accuracy of the voltage estimation. Even no extra sensors are applied, the capacitor voltages can be estimated with adaptive observers [12] or Kalman filters [13]. The main limitations of the software-based methods are as follows. First, the computational burden is explosively increased along with the increase of the number of SMs, which limits its application to MMCs with a small number of SMs. Second, high-voltage sensors or sensors with high galvanic isolation voltage are required.

In hardware-based methods, extra semiconductor devices are equipped to balance the SM capacitor voltages. A diode-clamp MMC with SM voltage self-balancing ability is presented in [14], where two adjacent capacitors can be paralleled through the clamping diode. To limit the balancing current, small inductors are connected in series with the clamping diodes in a diode-clamp MMC-based STATCOM [15] and a diode-clamp MMC-based dc transformer [16]. In [17], additional two diodes are used for symmetrical HB-SM to achieve a sensorless voltage balance. A semi-full-bridge SM is presented in [18], where two capacitors can be connected in parallel through the conducted insulated gate bipolar transistors. In [19], a reduced series/parallel module is presented for the cascaded multilevel converter, which can be configured in series, bypassed, or in parallel to balance all capacitor voltages in a sensorless manner. The number of voltage sensors can be reduced by the hardware-based methods, which also reduce the communication burden and computational burden in regards to the voltage balancing controls (VBCs) [20]. However, the limitations of the hardware-based methods are evident. First, the balancing current would be large when the voltage deviation between two paralleled capacitors is large, especially during the startup process, which requires semiconductor devices with big capability. Second, extra devices not only lead to extra losses but it will also increase the costs.

In the fix pattern-based methods, the SMs are switched into a fixed pattern that the power absorbed by each SM is equal. A fix pulse pattern with harmonic elimination is presented in [21], where the stored energy in each SM remains stable. A hierarchical permutation cyclic coding method can evenly distribute the switching gate signals among the SMs [22] and the SM capacitor voltages can be balanced in a wide range of switching frequencies. A *Y*-matrix modulation method is presented in [23], where MMCs can achieve self-voltage balancing without measurements and feedback controls. However, in practical systems, the power losses of SMs can be various due to manufacturing errors [24] or different leakage resistances in the valve tower [25]. The fixed pattern-based methods cannot ensure an exact voltage balancing.

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Chengkai Liu, Qingsong Wang, and Zheng Wang are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: lckisafish@163.com; qswang@seu.edu.cn; zwang@seu.edu.cn).

Fujin Deng is with the Jiangsu Key Laboratory of Smart Grid Technology and Equipment, School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: fdeng@seu.edu.cn).

Yanbo Wang and Frede Blaabjerg are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: ywa@et.aau.dk; fbl@et.aau.dk).

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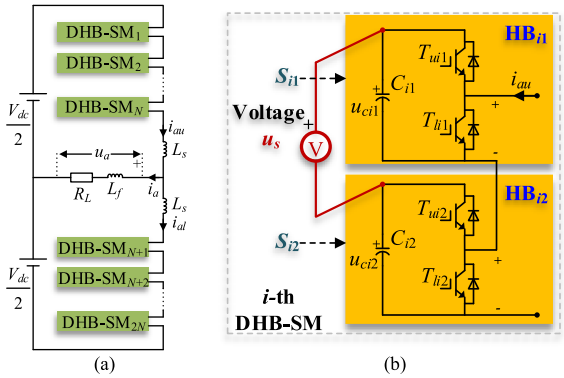


Fig. 1. (a) Single-phase DHB-SM-based MMC. (b) Topology of the *i*th DHB-SM.

TABLE I
SWITCHING STATES OF HB_{ij}

S_{ij}	T_{uij}	T_{lij}	i_{au}	u_{cij}
1	on	off	Positive	Increase
			Negative	Decrease
0	off	on	Positive	Unchange
			Negative	

This letter proposes a double HB (DHB) SM-based MMC, where only a voltage sensor is equipped between the positive poles of two capacitors in each DHB-SM. In addition, the corresponding capacitor voltage estimation method is also proposed for each DHB-SM with a simple algorithm. The proposed DHB-SM-based MMC only requires a half number of voltage sensors in comparison with the conventional HB-SM-based MMC [6].

The rest of this letter is organized as follows. The proposed DHB-SM-based MMCs and capacitor voltage estimation methods are presented in Sections II and III, respectively. The simulation and experimental studies are presented in Sections IV and V, respectively. Finally, the conclusion is drawn in Section VI.

II. Proposed DHB-SM-Based MMCs

A single-phase DHB-SM-based MMC is shown in Fig. 1(a), which consists of an upper arm and a lower arm. Each arm consists of N identical DHB SMs and an inductor L_s. Fig. 1(b) shows the ith ($i = 1, 2 \ldots, N$) DHB-SM in the upper arm, which is composed of two HBs (HB_{i1} and HB_{i2}) connected in series. The HB_{ij} ($j = 1, 2$) consists of two switches (T_{uij}, T_{lij}) and one capacitor C_{ij}, which are controlled by the switching function S_{ij}, as listed in Table I. When $S_{ij} = 1$, T_{uij} is ON and T_{lij} is OFF. Here, the capacitor C_{ij} is inserted into the arm and capacitor voltage u_{cij} is increased with the positive arm current and decreased with the negative arm current. When $S_{ij} = 0$, T_{uij} is OFF and T_{lij} is ON. The capacitor C_{ij} is bypassed from the arm and u_{cij} is unchanged.

One thing to mention is that only one voltage sensor is used between the positive poles of two capacitors in each DHB-SM to estimate capacitor C_{i1}'s voltage and C_{i2}'s voltage, which will be discussed more in Section III.

III. Proposed Capacitor Voltage Estimation Method for DHB-SMs-Based MMCs

A. Sensor's Measurement Voltage

In the ith DHB-SM, as shown in Fig. 1(b), only one voltage sensor is equipped to estimate capacitor voltage u_{ci1} and u_{ci2}. The measurement voltage u_s obtained from the sensor depends on the S_{i2} corresponding to HB_{i2}, as listed in Table II.

TABLE II
RELATIONSHIP BETWEEN S_{i2} AND u_s

S_{i2}	u_s
1	u_{ci1}
0	u_{ci1} - u_{ci2}

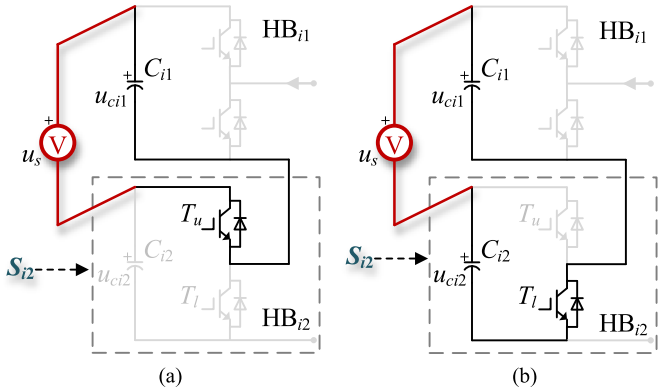


Fig. 2. Sensor voltage u_s corresponding to S_{i2} of HB_{i2}. (a) $S_{i2} = 1$. (b) $S_{i2} = 0$.

1) *$S_{i2} = 1$:* The sensor is connected in parallel with the C_{i1}, as depicted in Fig. 2(a). Here, $u_s = u_{ci1}$.
2) *$S_{i2} = 0$:* The negative poles of C_1 and C_2 are connected together, as depicted in Fig. 2(b). Here, the u_s equals the voltage deviation Δu_{ci} between C_{i1}'s voltage u_{ci1} and C_{i2}'s voltage u_{ci2}, as $u_s = \Delta u_{ci} = u_{ci1} - u_{ci2}$.

B. Proposed Capacitor Voltage Estimation Method

Based on the above-mentioned analysis, a capacitor voltage estimation method is proposed. Fig. 3 shows the proposed capacitor voltage estimation method for the ith DHB-SM in the upper arm. In Fig. 3(a), the SM individual VBC method [26], including VBC and voltage average control (VAC), is employed for the MMC. With the ac-side voltage reference u_a^*, estimated capacitor voltage $\hat{u}_{ci1}$ and $\hat{u}_{ci2}$, and average capacitor voltage u_{c_ave} in the phase, the reference signals y_{i1} and y_{i2} can be produced and compared with two carriers to generate the switching functions S_{i1} and S_{i2} for the HB_{i1} and HB_{i2} in the ith DHB-SM, respectively, which can ensure the capacitor voltage balancing in the MMC and it is close to the rated SM capacitor voltage u_{c0} as

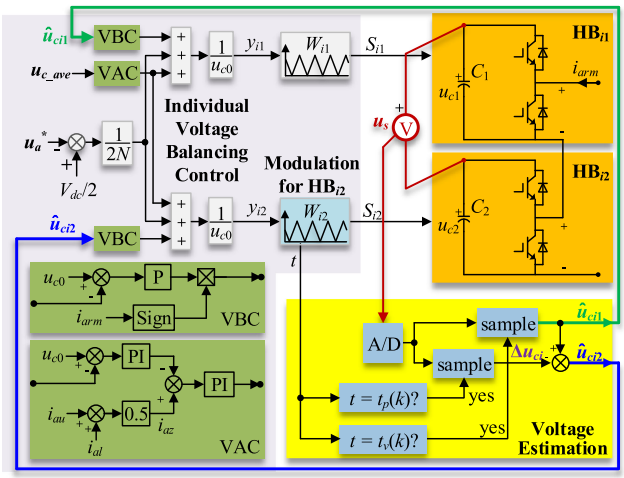
$$u_{c0} = V_{\rm dc}/(2N). \tag{1}$$

In Fig. 3, the average capacitor voltage u_{c_ave} is

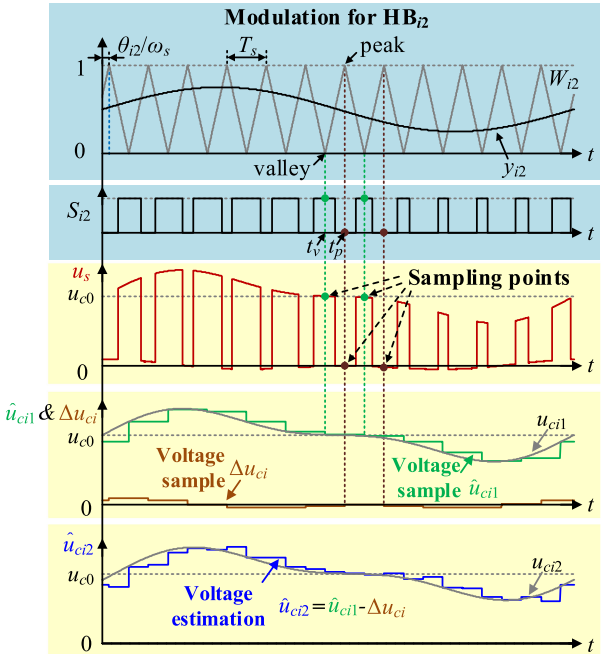
$$u_{c\_ave} = \sum_{i=1}^{2N} (\hat{u}_{ci1} + \hat{u}_{ci2})/(4N). \tag{2}$$

In the MMC, the phase-shifted carrier (PSC)-based pulsewidth modulation (PWM) technique is adopted. The $2N$ isosceles triangle carriers with the phase-shifted angle of π/N are employed for SMs in the upper arm, where the carrier period is T_s and angular frequency is $\omega_s = 2\pi/T_s$. In Fig. 3(a), the initial phase angle of carrier W_{i2} for the HB_{i2} in the ith DHB-SM is

$$\theta_{i2} = (2i - 1) \cdot \pi/N. \tag{3}$$



(a)



(b)

Fig. 3. Proposed capacitor voltage estimation method. (a) Capacitor voltage estimation for the ith DHB-SM. (b) Proposed synchronous sampling.

TABLE III
RELATIONSHIP AMONG t, W_{i2}, AND S_{i2}

t	W_{i2}	S_{i2}
$t_v(k)$=[(2i-1)/(2N)+k+1/2]·T_s	Valley	1
$t_p(k)$=[(2i-1)/(2N)+k]·T_s	Peak	0

Fig. 3(b) shows the detailed modulation for the HB$_{i2}$. The S_{i2} is generated based on the y_{i2} and W_{i2} as $S_{i2} = 1$, if $y_{i2} > W_{i2}$ and $S_{i2} = 0$, if $y_{i2} < W_{i2}$.

As a result, Table III can be easily obtained as follows.

1) $S_{i2} = 1$ at the valley of W_{i2} and this instant is

$$t_v(k) = \frac{\theta_{i2}}{\omega_s} + \left(k + \frac{1}{2}\right) \cdot T_s = \left(\frac{2i-1}{2N} + k + \frac{1}{2}\right) \cdot T_s, (k = 0, 1, 2 \ldots). \quad (4)$$

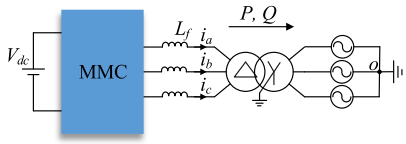


Fig. 4. Diagram of the simulated system.

TABLE IV
PARAMETERS FOR SIMULATED SYSTEM

Parameter	Value
Rated power (MW)	20
DC link voltage V_{dc} (kV)	24
Rated frequency (Hz)	50
Grid line-to-line voltage	33 kV
Transformer voltage rating	12 kV/33 kV
Rated capacitor voltage u_{c0} (kV)	1
SM capacitance (mF)	15
Arm inductance L_s (mH)	4
Filter inductance L_f (mH)	1
Carrier frequency $1/T_s$ (Hz)	110

2) $S_{i2} = 0$ at the peak of W_{i2} and this instant is

$$t_p(k) = \frac{\theta_{i2}}{\omega_s} + k \cdot T_s = \left(\frac{2i-1}{2N} + k\right) \cdot T_s, (k = 0, 1, 2 \ldots). \quad (5)$$

Based on Tables II and III, the capacitor voltage u_{ci1} of C_{i1} and u_{ci2} of C_{i2} can be sampled and estimated from the sensor voltage u_s, where the sampling of the sensor voltage u_s and the estimation of capacitor voltage are synchronized with the carrier W_{i2} for HB$_{i2}$, as follows.

1) The estimation of voltage $\hat{u}_{ci1}$ for C_{i1}: $\hat{u}_{ci1}$ is periodically sampled from sensor voltage u_s at the time $t_v(k)$ with a period of T_s, as shown in Fig. 3(b), given as

$$\hat{u}_{ci1} = u_s(t)|_{t=t_v(k)}. \quad (6)$$

2) The estimation of voltage $\hat{u}_{ci2}$ for C_{i2}: The voltage deviation Δu_c is periodically sampled from sensor voltage u_s at the time $t_p(k)$ with a period of T_s, as shown in Fig. 3(b), as

$$\Delta u_{ci} = u_s(t)|_{t=t_p(k)}. \quad (7)$$

As a result, the $\hat{u}_{ci2}$ can be estimated as

$$\hat{u}_{ci2} = \hat{u}_{ci1} - \Delta u_{ci}. \quad (8)$$

IV. SIMULATION STUDIES

To verify the effectiveness of the proposed method, a three-phase DHB-SM-based MMC (12 DHB SMs per arm) is simulated with power systems computer aided design /electromagnetic transients including DC, while a three-phase HB-SM-based MMC (24 HB SMs per arm) is also simulated for the comparison. The diagram of the simulated system is shown in Fig. 4 and the system parameters are listed in Table IV. Initially, the active power P and the reactive power Q are regulated at 18 MW and 0 MVar, respectively. At 2.5 s, P is reduced to 9 MW in a step and Q is not changed.

A. Case I: DHB-SM-Based MMC

Figs. 5–7 show the performance of the proposed DHB-SM-based MMC. Fig. 5 shows the ac-side current i_a, i_b, and i_c. Fig. 6(a) shows the estimated capacitor voltage $\hat{u}_{c11}$ and capacitor voltage u_{c11} for C_{11}

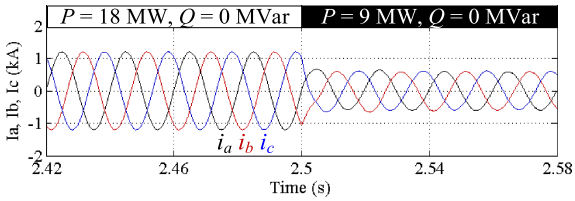


Fig. 5. AC-side current i_a, i_b, and i_c of DHB-SM-based MMC.

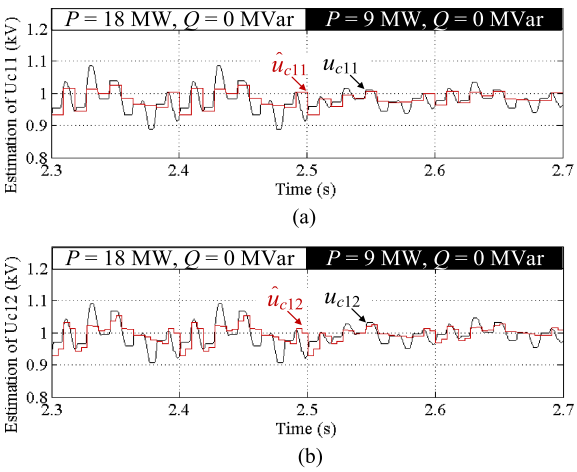


Fig. 6. Voltage estimation. (a) Estimated voltage $\hat{u}_{c11}$ and capacitor voltage u_{c11} for HB_{11} in DHB-SM_1 in the upper arm of phase *A*. (b) Estimated voltage $\hat{u}_{c12}$ and capacitor voltage u_{c12} for HB_{12} in DHB-SM_1 in the upper arm of phase *A*.

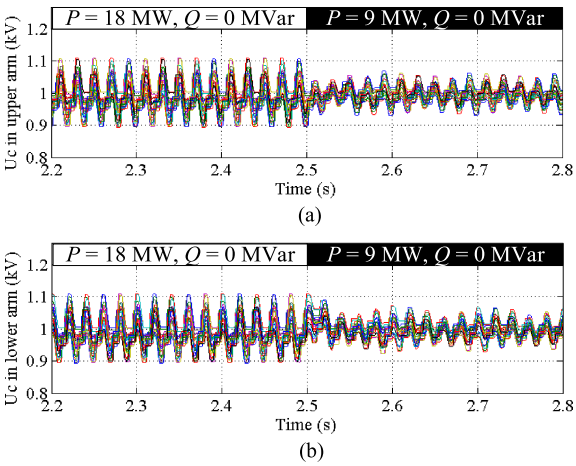


Fig. 7. Capacitor voltages in DHB-SM-based MMC. (a) DHB-SM_1–DHB-SM_{12} in the upper arm of phase *A*. (b) DHB-SM_{13}–DHB-SM_{24} in the lower arm of phase *A*.

in HB_{11} of DHB-SM_1 in the upper arm of phase *A*. Fig. 6(b) shows the estimated capacitor voltage $\hat{u}_{c12}$ and capacitor voltages u_{c12} for C_{12} in HB_{12} of DHB-SM_1. It can be observed that the estimated $\hat{u}_{c11}$ and $\hat{u}_{c12}$ are coinciding with u_{c11} and u_{c12}, respectively.

Fig. 7(a) shows the capacitor voltages in DHB-SM_1–DHB-SM_{12} in the upper arm of phase *A*, while Fig. 7(b) shows the capacitor voltages in DHB-SM_{13}–DHB-SM_{24} in the lower arm of phase *A*. It can be observed that the capacitor voltages can be well balanced at such a low switching frequency.

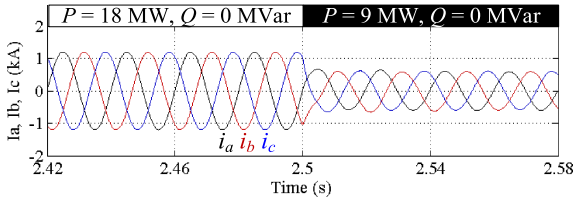


Fig. 8. AC-side current i_a, i_b, and i_c of HB-SM-based MMC.

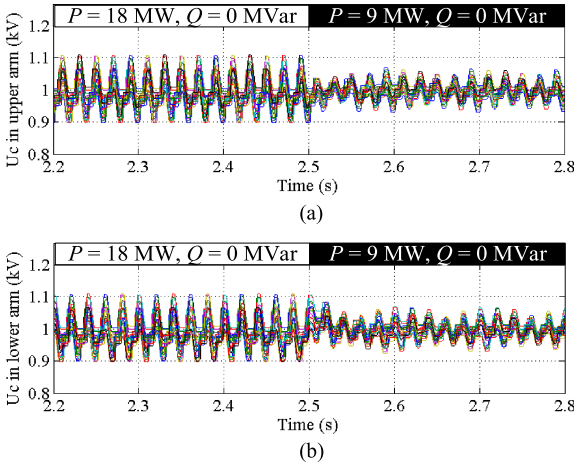


Fig. 9. Capacitor voltages in HB-SM-based MMC. (a) HB-SM_1–HB-SM_{24} in the upper arm of phase *A*. (b) HB-SM_{25}–HB-SM_{48} in the lower arm of phase *A*.

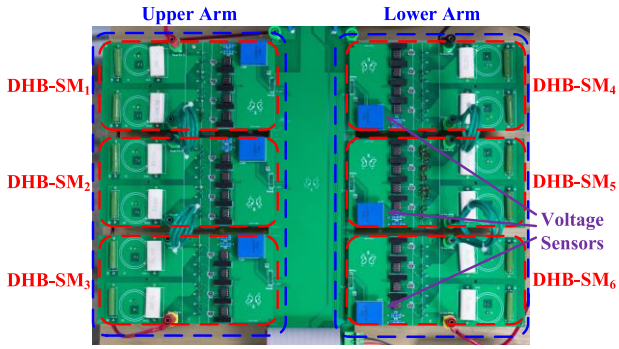


Fig. 10. Photograph of the experimental setup.

B. Case II: HB-SM-Based MMC

Fig. 8 shows the ac-side current i_a, i_b, and i_c of the HB-SM-based MMC. In comparison with Fig. 5, the current performance of the DHB-SM-based MMC is almost the same as that of the HB-SM-based MMC.

Fig. 9(a) shows the capacitor voltages in HB-SM_1–HB-SM_{24} in the upper arm of phase *A*. Fig. 9(b) shows the capacitor voltages in HB-SM_{25}–HB-SM_{48} in the lower arm of phase *A*. In comparison with Fig. 7, the capacitor voltage performance of the proposed DHB-SM-based MMC is also similar to that of the HB-SM-based MMC.

V. Experimental Studies

A single-phase DHB-SM-based MMC prototype, as shown in Fig. 1(a), is built in the laboratory. Fig. 10 shows a photograph of the experimental setup. The dc power supply SGA600/8 supports the dc link of the MMC. The IXFK48N36P is used as the switch/diode in

TABLE V
PARAMETERS FOR EXPERIMENTAL SYSTEM

Parameter	Value
DC link voltage V_{dc} (V)	300
Rated frequency (Hz)	50
Number of DHB-SM per arm N	3
Rated capacitor voltage u_{c0} (V)	50
SM capacitance (mF)	3.9
Arm inductance L_s (mH)	1.8
Filter inductance L_f (mH)	1.8
Load resistance R_L (Ω)	10
Carrier frequency $1/T_s$ (Hz)	400

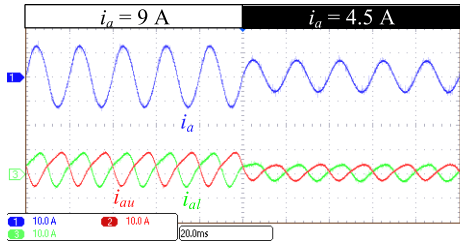


Fig. 11. AC-side current i_a, upper arm current i_{au}, and lower arm current i_{al}.

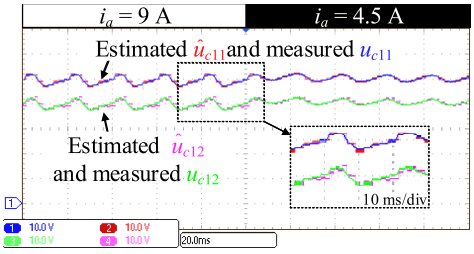


Fig. 12. Estimated voltage $\hat{u}_{c11}$ and measured voltage u_{c11} for HB_{11} in $DHB\text{-}SM_1$ in the upper arm. Estimated voltage $\hat{u}_{c12}$ and measured voltage u_{c12} for HB_{12} in $DHB\text{-}SM_1$ in the upper arm.

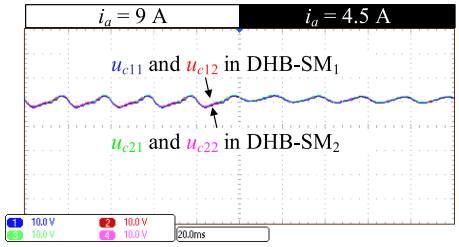


Fig. 13. Capacitor voltages for $DHB\text{-}SM_1$ and $DHB\text{-}SM_2$ in the upper arm.

each DHB-SM. The ac-side current control and VAC are implemented in a digital signal processor controller TMS32F28335. The voltage estimation, VBC, and PSC-PWM are implemented in the FPGA device XC6SLX25. The system parameters are listed in Table V.

Figs. 11–14 show the performance of the proposed MMC, where the ac-side current i_a is changed from 9 to 4.5 A in a step. Fig. 11 shows i_a, upper arm current i_{au}, and lower arm current i_{al}.

Fig. 12 shows the estimated capacitor voltage $\hat{u}_{c11}$ and measured capacitor voltages u_{c11} for C_{11} in HB_{11} of $DHB\text{-}SM_1$ as well as the estimated capacitor voltage $\hat{u}_{c12}$ and measured capacitor voltages u_{c12} for C_{12} in HB_{12} of $DHB\text{-}SM_1$, where the estimated capacitor voltages are output by the digital–analog converter and recorded by the

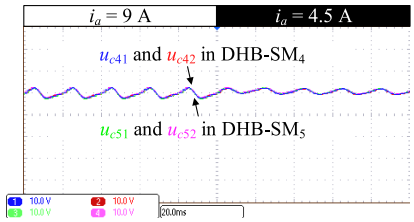


Fig. 14. Capacitor voltages for $DHB\text{-}SM_4$ and $DHB\text{-}SM_5$ in the lower arm.

oscilloscope. It can be observed that the estimated $\hat{u}_{c11}$ and $\hat{u}_{c12}$ are coinciding with the measured u_{c11} and u_{c12}, respectively.

Fig. 13 shows the measured capacitor voltages u_{c11} and u_{c12} in $DHB\text{-}SM_1$ and measured capacitor voltages u_{c21} and u_{c22} in $DHB\text{-}SM_2$ in the upper arm. Fig. 14 shows measured capacitor voltages u_{c41} and u_{c42} in $DHB\text{-}SM_4$ and measured capacitor voltages u_{c51} and u_{c52} in $DHB\text{-}SM_5$ in the lower arm. It can be observed that the capacitor voltages in the proposed MMC can be well balanced with the estimated capacitor voltages in the proposed method.

VI. CONCLUSION

This letter proposes a DHB-SM for MMCs, where only one voltage sensor is equipped in each DHB-SM to measure the voltage between the positive poles of two capacitors. The voltage estimation method is also proposed based on the sampled voltages at the peak and valley of the carriers. The proposed MMC reduces the number of voltage sensors to half in comparison with the conventional HB-SM-based MMC. The simulation and experimental results confirm the effectiveness of the proposed DHB-SM-based MMC and capacitor voltage estimation method.

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