Digital Predictive Current-Mode Control of Three-Level Flying Capacitor Buck Converters

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***Abstract*—This article investigates the use of digital predictive current-mode control (DPCMC) in dc–dc three-level flying capacitor (3LFC) buck converters. In particular, stability and flying capacitor (FC) balancing properties of predictive *peak*, *average*, and *valley* current-mode controllers are studied when operated in single- and multisampled modes. A variant of the multisampled DPCMC obtained through a *fast-update* of the duty cycle command is also disclosed and analyzed. Results indicate that single-sampled DPCMC is always stable, and that fast-update approaches can strongly improve the converter dynamic response. Multisampled controllers are also shown to be inherently more robust than single-sampled ones against timing mismatches in the control signals, resulting in a smaller FC voltage imbalance. The analysis is validated in simulation and experimentally on a 500 kHz, 12–1.5 V, 500 mA 3LFC buck case study.**

***Index Terms*—Current-mode control, dc–dc multilevel converters, digital predictive control.**

I. Introduction

ORIGINALLY introduced in the context of high-voltage power conversion applications [1], multilevel converters are gaining attention for dc–dc low-voltage applications such as low-power consumer and automotive electronics due to several advantages they offer in terms of inductance and output capacitance reduction, improved voltage stresses, and, overall, better opportunities for on-chip or on-package integration of the converter [2]–[8]. The inductance reduction typically enabled by multilevel converters also has direct beneficial effects on the converter dynamic capabilities, especially when exploited in combination with fast control techniques such as predictive control laws and time-optimal approaches.

All main advantages of multilevel converters are more or less directly tied to the requirement that the intermediate voltage levels remain regulated at specific values. In a three-level converter, for instance, the intermediate voltage must be held at one half of the input voltage V_g. Whenever these voltage levels are held by flying capacitors (FCs)—this being the most common situation—the even more serious issue of stability arises, as these voltages may or may not be affected by drift phenomena, depending on how FC voltages interact with the specific controller implemented around the converter. For example, a straightforward implementation of an analog peak current-mode controller in a three-level flying capacitor buck converter (3LFC) can be shown to be inherently unstable [4].

Several analog and digital control techniques have been disclosed, which, in general, may or may not need dedicated FC voltage sensing circuitry and active balancing loops to ensure FC voltage stability [5], [6], [9]–[15]. Furthermore, multilevel converters are known to exhibit balancing and controllability issues at very specific conversion ratios [10], [16].

Digital predictive current-mode control (DPCMC) is an attractive control strategy because of its inherent speed and simplicity [17], [18]. Although DPCMC has been extensively studied for basic dc–dc topologies, its reliable application to multilevel converters is still subject to the constraint that the FC voltage(s) remain stable and balanced. Understanding the interaction between the predictive control law and the FC voltage dynamics is, therefore, crucial to the implementation of fast digital current control loops in multilevel converters, justifying a dedicated study.

This article investigates the stability and balancing properties of *peak*, *average*, and *valley* DPCMC to 3LFC buck converters, considering both single- and multisampled implementations. In the single-sampled DPCMC, the inductor current is sampled at the same rate as the physical switching rate of the power devices. In the multisampled DPCMC (MS-DPCMC), the inductor current is sampled at twice the switching rate of the devices. A *fast-update* variation of the multisampled approach, in which the duty cycle is updated *immediately after the sampling event*, is also disclosed and analyzed. Extending results previously reported in [19] and [20], this article details an analysis approach for FC voltage stability suitable whenever the traditional small-ripple approximation (SRA) approach fails. Results indicate that all single-sampled controllers are unconditionally stable and can, therefore, be implemented with no dedicated FC stabilizing provisions. Furthermore, the fast-update multisampled approach can strongly improve the converter dynamic response. This article also highlights the different FC voltage balancing properties of the various predictive controllers in presence of mismatches in the control signals, proving that multisampled controllers are inherently more robust and can exhibit self-balancing features. Furthermore, this article clarifies the robustness of the controller

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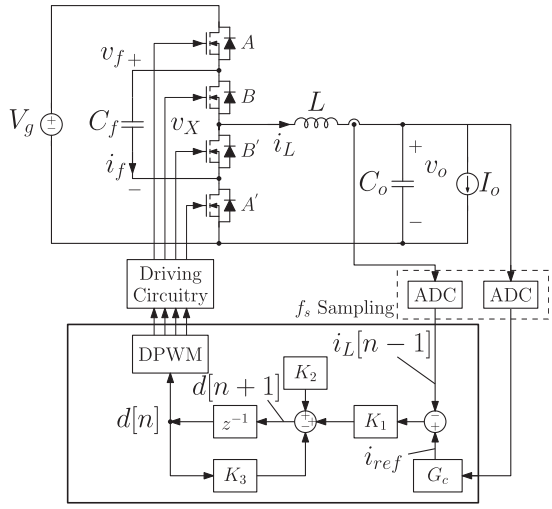


Fig. 1. Generic block diagram of a 3LFC buck converter with a single-sampled digital predictive current-mode controller.

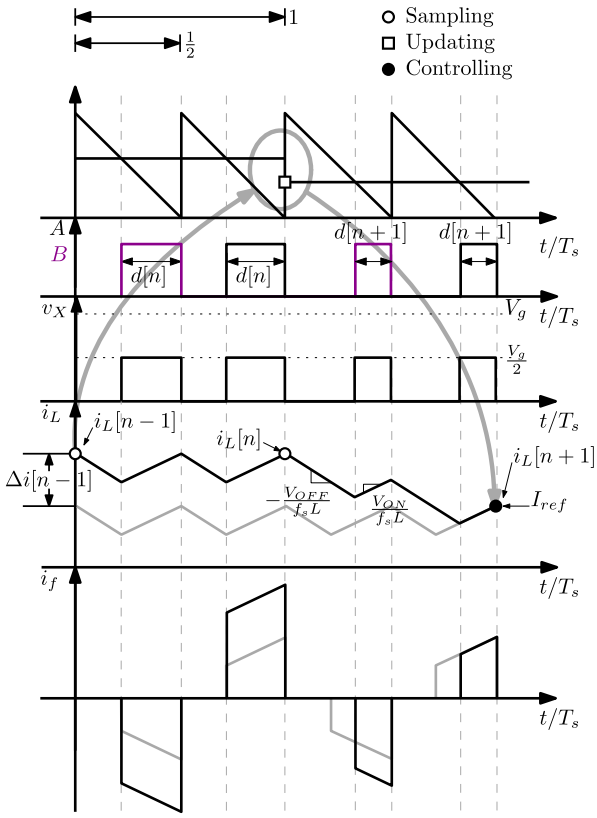


Fig. 2. Operation of the single-sampled *peak* DPCMC controller with an LE carrier for $M < 0.5$.

for nonnominal values of the converter parameters and includes new simulation and experimental results.

The rest of this article is organized as follows. Section II discusses the control equations and inductor current stability of single-sampled peak DPCMC, while Section III is devoted to investigating the stability of the FC voltage. Section IV generalizes the approach to the cases of single-sampled average and valley controllers. Multisampled *peak* DPCMC is investigated in Section V, while Section VI covers the multisampled average and valley cases, concluding with a comprehensive summary of the stability properties of all controllers. Results are validated in simulation and experimentally on a 500 kHz, 12–1.5 V, 500 mA 3LFC buck case study. Section VII reports the main simulation results, along with a Monte Carlo analysis of the sensitivity of the various controllers with respect to control signal timing mismatches. Experimental results are disclosed in Section VIII.

II. Single-Sampled Peak DPCMC

In single-sampled DPCMC, the inductor current is sampled at the same rate as the physical switching rate of the power devices. A general block diagram of a DPCMC-controlled 3LFC buck converter is illustrated in Fig. 1. Expressions of the coefficients K_1, K_2, and K_3 depend on the specific type of DPCMC—i.e., whether peak, valley, or average current control is considered.

Operation of single-sampled *peak* DPCMC based on a leading-edge (LE) carrier [17] is illustrated in Fig. 2. From top to bottom, the figure sketches the modulating signal along with the LE carrier, the pulsewidth modulation (PWM) commands A and B, the switching node voltage v_X, the inductor current i_L, and the FC current i_f. The time axis is normalized with respect to the switching period T_s. The figure exemplifies how an initial perturbation of the inductor current peak value, $\Delta i_L[n-1] \triangleq i_L[n-1] - I_{\rm ref}$, is corrected according to the predictive control equation. Assuming that the FC voltage is balanced at $V_f = V_g/2$, the value $i_L[n+1]$ of the inductor current at the controlling point can be written in terms of the sampled current $i_L[n-1]$, the inductor current slopes, and the two duty cycles $d[n]$ and $d[n+1]$

$$i_L[n+1] = i_L[n-1] - \frac{V_{\rm OFF}}{f_sL}(1-2d[n]) + 2\frac{V_{\rm ON}}{f_sL}d[n] + \\ - \frac{V_{\rm OFF}}{f_sL}(1-2d[n+1]) + 2\frac{V_{\rm ON}}{f_sL}d[n+1] \quad (1)$$

where $V_{\rm ON}$ and $V_{\rm OFF}$ are the voltages across the inductor during ON and OFF phases, respectively. Assuming, for the time being, that the voltage conversion ratio $M \triangleq V_o/V_g$ is less than 0.5, one has

$$V_{\rm ON} = \frac{V_g}{2} - V_o = \frac{V_g}{2}(1-2\,M) \\ V_{\rm OFF} = V_o = MV_g. \quad (2)$$

From (1), by imposing that the new duty cycle $d[n+1]$ makes the peak current $i_L[n+1]$ equal to $I_{\rm ref}$, one can solve for $d[n+1]$ and obtain the control equation

$$d[n+1] = \frac{f_sL}{V_g}(I_{\rm ref} - i_L[n-1]) + 2M - d[n]. \quad (3)$$

It is simple to show that the same control equation (3) holds for $M > 0.5$ as well [19]. Based on the above result and in reference to Fig. 1, for peak DPCMC, one has $K_1 = f_sL/V_g$, $K_2 = 2M$, and $K_3 = 1$.

In order to assess the static stability of the inductor current, it is necessary to evaluate the time-domain evolution of the

discrete sequence Δi representing the evolution of the inductor current perturbation in response to an initial condition [17]. Considering the perturbed waveforms sketched in Fig. 2, the current perturbation at the end of the $n+1$ cycle can be written as

$$\Delta i[n+1] = \Delta i[n-1] + \frac{2d[n+1]}{f_s L}(V_{\rm OFF} + V_{\rm ON}) - \frac{V_{\rm OFF}}{f_s L}. \tag{4}$$

By replacing $d[n+1]$ with (3), one obtains

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = 0. \tag{5}$$

Perturbation $\Delta i[n+1]$ is zero independently of the value $\Delta i[n-1]$ and of the operating point. Such a result, which can also be proven for the $M > 0.5$ case, confirms the static stability of the inductor current and that, as expected, the peak value of the inductor current is regulated in a dead-beat fashion.

III. Stability of the FC Voltage

Stability of the FC voltage is crucial for the correct operation of the 3LFC buck converter and must be verified by means of an *ad-hoc* analysis [4], [11], [21]. The first approach here reported, based on the SRA for both the FC and output voltages, predicts a marginal stability for the FC voltage of all single-sampled predictive controllers. The SRA assumption does not, therefore, allow to assess the actual stability character of the control. Failure of this simplified approach justifies the use of a computer-assisted analysis, which predicts asymptotic stability of the FC voltage.

A. Failure of the SRA Method

Assume that the FC voltage is initially unbalanced, i.e., $V_f = \frac{V_g}{2} + \hat{v}_f = \frac{V_g}{2}(1+\hat{v}_N)$. The switching node, the FC current, and the inductor current in this hypothetical unbalanced steady-state condition are shown in Fig. 3. Note that the switching node no longer swings between 0 and $V_g/2$, and that the inductor current waveform has a period equal to T_s.

With the assumption that the dynamics of the average FC voltage is much slower than the inductor current dynamics, stability of the FC voltage is determined by the sign of the average FC current I_f being *discordant* with respect to the sign of the FC voltage perturbation $\hat{v}_N$, i.e., a positive $\hat{v}_N$ should induce a *discharge* of the FC, and vice versa. Small-signal wise, this means that FC voltage stability is characterized by a *negative* value of the (normalized) quantity

$$\lambda \triangleq \left.\frac{\partial \tilde{I}_f}{\partial \hat{v}_N}\right|_{\hat{v}_N=0} \tag{6}$$

with

$$\tilde{I}_f \triangleq \frac{2R_o}{V_g} I_f \qquad \left(R_o \triangleq \frac{V_o}{I_o}\right). \tag{7}$$

For the 3LFC buck, the voltage conversion ratio can be written, in general, as

$$M \triangleq \frac{V_o}{V_g} = \frac{D_1 + D_2}{2} + \frac{\hat{v}_N}{2}(D_1 - D_2) \tag{8}$$

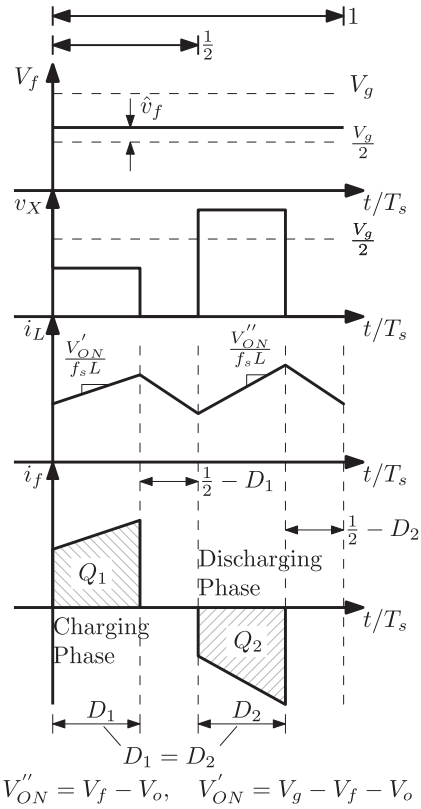


Fig. 3. Single-sampled *peak* DPCMC with LE carrier: main waveforms in presence of an unbalanced FC voltage.

where D_1 and D_2 are the duty cycles associated with the charging and discharging phases, respectively, as indicated in Fig. 3. Since the single-sampled DPCMC forces D_1 and D_2 to be equal, the voltage conversion ratio does not depend on the value of $\hat{v}_N$, i.e., $M = D_1 = D_2 = D$, as in the balanced condition.

In reference to Fig. 3, under the traditional small-ripple approximation for both v_f and v_o, the average FC current can be written as difference between charges Q_1 and Q_2

$$I_f \triangleq \frac{1}{T_s}\int_t^{t+T_s} i_f(\tau)d\tau = Q_1 - |Q_2|\,. \tag{9}$$

Both Q_1 and $|Q_2|$ can be written as a function of the average FC voltage perturbation $\hat{v}_N$:

$$Q_1 = \frac{D}{2}\left[2I_{\rm pk} - \frac{2\,MV_g}{f_s L}(1-D) + \frac{V_g}{2f_s L}(1-2M-\hat{v}_N)\right] \tag{10}$$

$$|Q_2| = \frac{D}{2}\left[2I_{\rm pk} - \frac{V_g}{2f_s L}(1-2M+\hat{v}_N)\right] \tag{11}$$

where $I_{\rm pk} = I_o + \frac{V_g}{4f_s L}(1-2M)D$.

By substituting (10) and (11) into (9), the average FC current is found as

$$I_f = \frac{V_g}{2f_s L} D\,(M-D)\,. \tag{12}$$

Since, as anticipated, $D_1 = D_2 = D = M$, the above result implies that

$$I_f = 0 \quad \Rightarrow \quad \lambda = 0 \tag{13}$$

i.e., the FC voltage is marginally stable. A similar result is found for $M > 0.5$ [19].

This result, derived under the SRA for both v_f and v_o, does not predict the fact—documented in Sections VII and VIII—that the FC voltage is, indeed, stable.

Failure of the SRA-based approach in capturing the actual stability character of the system is consistent with recent findings reported in [22] with regard to odd-level converters operating open loop. It must be observed, however, that the scenario here considered includes the closed-loop effects of the DPCMC controller. It is also important to stress that the SRA-based approach does not necessarily fail when applied to other types of predictive controllers, and it will be successfully applied in Section V to prove the stability for peak and valley MS-DPCMC. In these cases, the SRA-based approach represents a simple and accurate approach to determine a closed-form expression of λ.

B. More Accurate FC Voltage Stability Analysis

In this section, the SRA hypothesis on v_o is removed, and the average FC current is calculated for a lossless 3LFC buck by including the effect of the output voltage ripple on $i_f(t)$. The following analysis is based on a state-space model approach and is developed upon the basic simplifying assumption that the switching instants as well as the state vector at $t = 0$ are the same as the ones obtained with the SRA-based analysis. As before, the FC is replaced with an ideal unbalanced dc voltage source $V_f = \frac{V_g}{2}(1 + \hat{v}_N)$.

To keep the problem in a normalized form, define the state vector as

$$\tilde{v}_o(\tilde{t}) \triangleq \frac{2v_o(\tilde{t}T_s)}{V_g}$$
$$\tilde{i}_L(\tilde{t}) \triangleq \frac{2R_o i_L(\tilde{t}T_s)}{V_g} \tag{14}$$

with $\tilde{t} \triangleq t/T_s$. The steady-state solution is obtained by solving the four linear systems corresponding to the four topological states, whose waveforms are sketched in Fig. 3

$$\begin{cases} \dot{\boldsymbol{x}}_i = \boldsymbol{A} \cdot \boldsymbol{x}_i + \boldsymbol{B}_i \cdot u_i \\ \boldsymbol{x}_{o_i} = \boldsymbol{C}_i \end{cases} \tag{15}$$

where index $i = 1, \ldots, 4$ indicates the topological state. Vector $\boldsymbol{x}_{o_i}$ represents the initial condition for topological state i. Values of the constants $\boldsymbol{C}_i$ are calculated by imposing the continuity of the state vector at the switching instants and the overall periodicity of the sought solution.

State matrix $\boldsymbol{A}$ is the same for all four topological states and can be put in the normalized form

$$\boldsymbol{A} = \begin{pmatrix} -2\pi\dfrac{f_N}{Q} & 2\pi\dfrac{f_N}{Q} \\ -2\pi f_N Q & 0 \end{pmatrix} \tag{16}$$

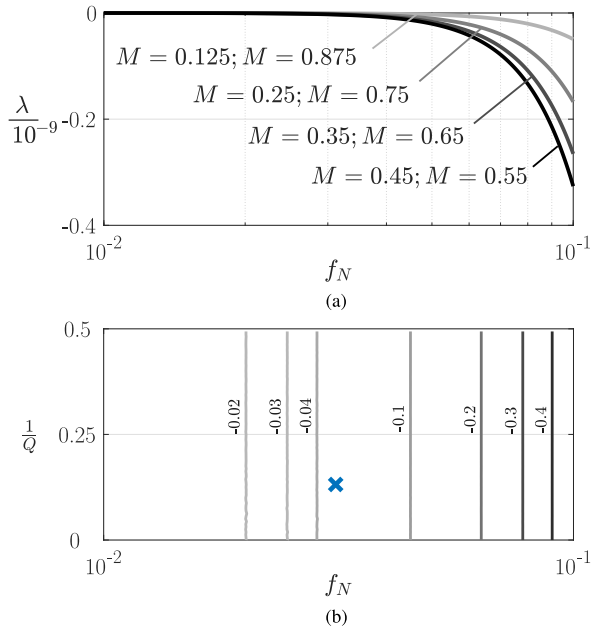


Fig. 4. (a) Stability parameter λ as a function of the normalized resonant frequency f_N for different values of M ($Q \approx 8$). (b) Contour plots of $\lambda(f_N, Q)$ for $M = 0.125$. The cross refers to the case study 3LFC prototype later presented.

where f_N and Q are normalized constants defined by

$$f_N \triangleq \frac{f_o}{f_s}, \qquad Q \triangleq R_o\sqrt{\frac{C_o}{L}}. \tag{17}$$

Expressions of u_i and $\boldsymbol{B}_i$ are

$$u_1 = 1 - \hat{v}_N;\ u_2 = u_4 = 0;\ u_3 = 1 + \hat{v}_N \tag{18}$$

$$\boldsymbol{B_1} = \boldsymbol{B_3} = \begin{pmatrix} 0 \\ 2\pi f_N Q \end{pmatrix};\ \boldsymbol{B_2} = \boldsymbol{B_4} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}. \tag{19}$$

Solution of the above equations has been obtained in closed form with the aid of Mathematica. Once the time-domain evolution of the state vector is obtained, the average value $\tilde{I}_f(M, \hat{v}_N, f_N, Q)$ of the FC current is evaluated. Finally, the expression of $\lambda(M, f_N, Q)$ is calculated by differentiation following the definition (6).

A closed-form expression of λ is unfortunately too complex to be reported here. Behavior of λ is, therefore, studied graphically. Fig. 4(a) shows λ versus f_N for various values of M. To generate the plot, a fixed value $Q \approx 8$ is used, which corresponds to the full-load quality factor of the case study converter later considered for simulation and experimental verification. As seen in the plot, λ is always negative regardless of f_N or M, confirming the asymptotic stability of the FC voltage. Furthermore, one has

$$\lim_{f_N \to 0} \lambda = 0. \tag{20}$$

This result is compatible with the simplified SRA-based analysis developed earlier, in that the better the condition $f_o \ll f_s$ is satisfied, the more justified the SRA approximation is.

A more general view of $\lambda(M, f_N, Q)$ is provided by the contour plots reported in Fig. 4(b). The plot reports λ for values of f_N between 0.01 and 0.1, and for values of Q comprised

between 2 and $+\infty$. Note that the y-axis is defined as $1/Q$ in order to explicitly depict the open-circuit condition $Q \to +\infty$. To generate the plot, $M = 0.125$ is chosen, which corresponds to the case study 3LFC converter later presented. The corresponding point of such case study on the plane is indicated by a cross. The contour plot of Fig. 4(b) confirms that λ is negative for all values of f_N and Q and is consistent with Fig. 4(a) with regard to the behavior of λ as f_N decreases. Furthermore, the contour plot confirms open-circuit stability for the DPCMC controller, in that all contour lines remain strictly negative as $1/Q$ approaches zero. These considerations hold for other values of M, for which the contour plots are qualitatively similar.

IV. Extension to Single-Sampled Average and Valley DPCMC

The DPCMC technique can be formulated for average or valley current control as well [17], [20]. Furthermore, each type of control can be paired with a specific choice of the PWM carrier, yielding many different cases. Among all possible pairings, of specific interest are those which allow for a dead-beat control of the sampled current. These are: 1) the *peak* DPCMC with LE carrier already examined and illustrated in Fig. 2; 2) the *valley* DPCMC with a trailing-edge (TE) carrier illustrated in Fig. 5(a); and 3) the *average* DPCMC with trailing triangle-edge (TTE) carrier illustrated in Fig. 5(b) [17], [20]. In these three cases, both sampling and controlling points refer to the same inductor current value, this being the peak, the valley, or the average: as a consequence, forcing the controlled current to the desired set point in a single step amounts to null the regulation error in a dead-beat fashion, immediately reaching steady state. Static stability of the inductor current is, therefore, guaranteed by construction.

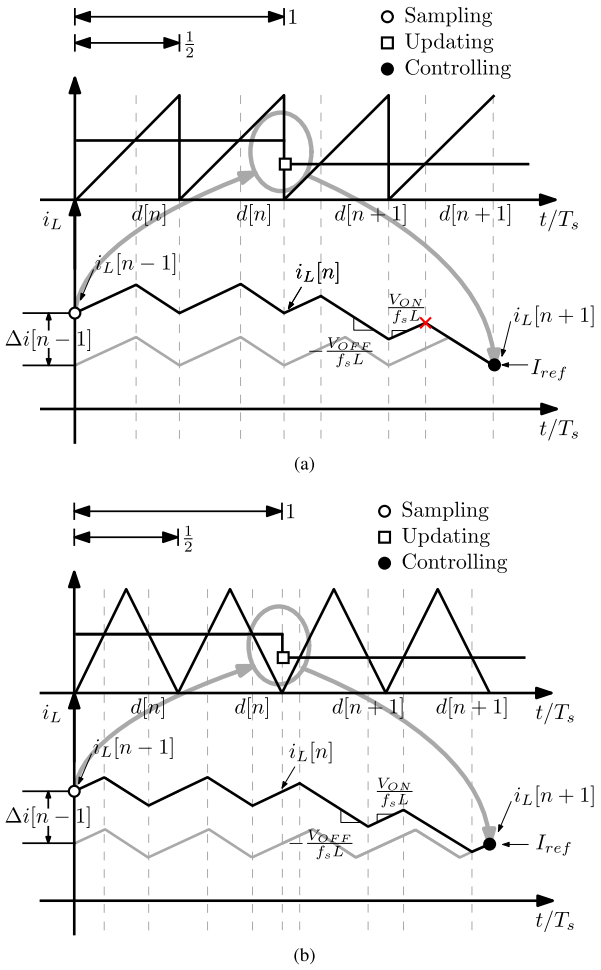


Fig. 5. Operation of (a) valley DPCMC with TE carrier for $M < 0.5$ and (b) average DPCMC with TTE carrier for $M < 0.5$.

A. Single-Sampling Valley DPCMC

The valley DPCMC with a TE carrier operation is exemplified in Fig. 5(a) for $M < 0.5$. As in the case of peak DPCMC, the current is dead-beat regulated after two switching cycles following the sampling instant.

Using Fig. 5(a) as a reference, the following general equation can be easily derived:

$$i_L[n+1] = i_L[n-1] + 2\frac{V_{\rm ON}}{f_sL}d[n] - \frac{V_{\rm OFF}}{f_sL}(1-2d[n]) + 2\frac{V_{\rm ON}}{f_sL}d[n+1] - \frac{V_{\rm OFF}}{f_sL}(1-2d[n+1]). \tag{21}$$

By solving for $d[n+1]$ so that $i_L[n+1] = I_{\rm ref}$, the control equation for valley DPCMC is

$$d[n+1] = \frac{f_sL}{V_g}(I_{\rm ref} - i_L[n-1]) + 2M - d[n]. \tag{22}$$

In order to prove the inductor current static stability, the time-domain evolution of $\Delta i[n]$ in response to an initial perturbation is evaluated

$$\Delta i[n+1] = \Delta i[n-1] + \frac{2d[n+1]}{f_sL}(V_{\rm OFF} + V_{\rm ON}) - \frac{V_{\rm OFF}}{f_sL}. \tag{23}$$

By replacing $d[n+1]$ with (22), one obtains

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = 0. \tag{24}$$

Static stability of the inductor current is, therefore, confirmed, and the valley value of the inductor current is regulated in a dead-beat fashion.

B. Single-Sampling Average DPCMC

Operation of the average DPCMC for $M < 0.5$ is exemplified in Fig. 5(b). Note that the average DPCMC here is set to control the midpoint of the triangular inductor current waveform rather than the quantity $\frac{1}{T_s}\int_t^{t+T_s} i_L(\tau)d\tau$ as done, for instance, in [17].

For average DPCMC, results (22)–(24) are the same as those obtained for peak DPCMC, a fact descending from the particular pairing between the carrier type and the controller type, as stated at the beginning of this section.

The control equations and static stability properties of the inductor current remain the same also for $M > 0.5$ when the aforementioned combinations between the carrier and the controller are considered. This generalization also applies to FC voltage stability properties. Particularly, for single-sampled valley and average DPCMC, the results obtained in Section III hold with no modification.

C. Other Pairings Between Control Type and Carrier Type

To exemplify how stability properties may change by changing the pairing between the controller type and the carrier type, consider the single-sampled peak DPCMC with a TE, rather than LE, carrier. Fig. 5(a), already used to describe the valley control case, can be taken as a reference for this case as well: the sampling point remains located at the beginning of the $(n-1)$th switching cycle, while the controlling instant, highlighted with a cross, is now located at the peak inductor current during the nth switching cycle.

Following the developed methodology, the control equation is, for $M < 0.5$,

$$d[n+1] = \frac{f_s L}{V_g}\left(\frac{I_{\text{ref}} - i_L[n-1]}{1-M}\right) + - \frac{d[n]}{1-M} + \frac{3}{2}\frac{M}{1-M}. \tag{25}$$

The perturbed current can be shown to evolve according to the equation

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = \frac{M}{1-M}. \tag{26}$$

Such quantity is inside the unit circle but not at the origin, implying that the sampled inductor current, although remaining stable and free of subharmonic oscillations, is no longer regulated in a dead-beat fashion. Furthermore, derivation of the predictive control law for $M > 0.5$ would yield a different equation than (25): the TE+peak DPCMC pairing between the carrier and the variable under control loses the symmetry between the $M < 0.5$ and $M > 0.5$ cases, leading to different predictive control laws depending on the value of M. This is another motivation to restrain the focus of the analysis to just the three pairings outlined at the beginning of this section, for which the predictive control law is unique.

V. Multisampled Peak DPCMC

In an N-level FC dc–dc converter operating at a switching frequency f_s, the output filter is excited with an effective switching rate equal to $(N-1)f_s$, a fact that opens up to the possibility of implementing a multisampled version of the DPCMC (MS-DPCMC) and, as a consequence, to significantly extend the bandwidth of the control loop. Following the development of the single-sampled case, the discussion on MS-DPCMC will start from the peak current control case. Results for the other types of controllers will be discussed subsequently.

As proven in this section, implementation of multisampled peak DPCMC as a straightforward extension of the single-sampled case is inherently unstable as long as $M < 0.5$ and would require some form of active stabilization. A stable variant of the peak MS-DPCMC through a *fast-update* of the duty cycle command is presented in the next section. The proposed fast-update multisampled peak DPCMC extends the dynamic capabilities of the converter and does not require dedicated sensing and circuitry for FC voltage stabilization.

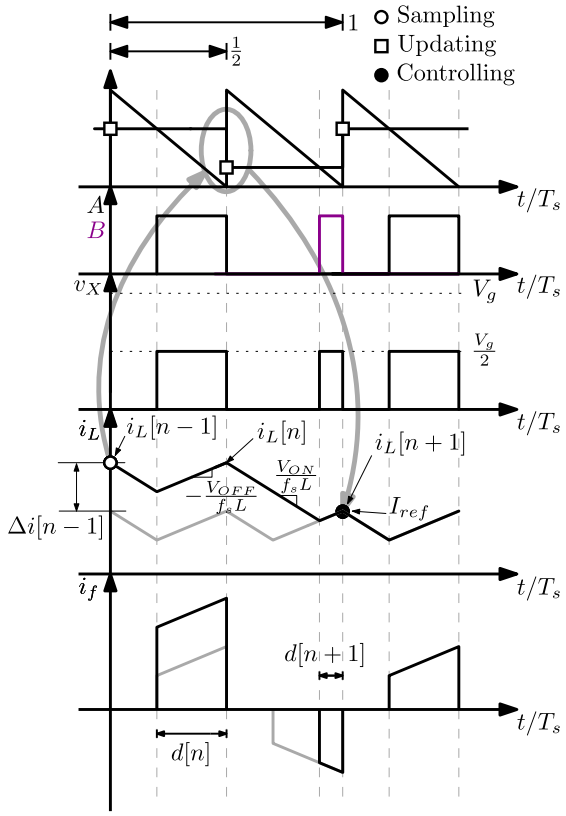


Fig. 6. Operation of the multisampled *peak* DPCMC with an LE carrier.

A. Multisampled Peak DPCMC

The implementation of peak MS-DPCMC for the 3LFC buck requires to sample/update the inductor current *twice* per switching period. Fig. 6 exemplifies the case of multisampled peak current-mode control based on an LE PWM carrier. Using the same approach as in the single-sampled case, the following control equation is derived:

$$d[n+1] = \frac{2f_s L}{V_g}\left(I_{\text{ref}} - i_L[n-1]\right) + 2M - d[n]. \tag{27}$$

The time evolution of the perturbed current is still provided by (5). As expected, the inductor current is regulated in a dead-beat fashion over a time interval equal to T_s.

With respect to the FC current, the main difference between Figs. 3 and 6 lies in the values of the duty cycles during the charging and discharging phases of the FC. As already discussed, in the single-sampled DPCMC, the two duty cycles are always equal within a given switching period T_s. Conversely, in the MS-DPCMC they are not, and such difference has a strong impact on the stability of the average FC voltage.

As anticipated at the end of Section III-A, the simple SRA-based approach is here sufficient to analyze the stability of the controller. Assuming that FC voltage is unbalanced, i.e., $V_f = \frac{V_g}{2} + \hat{v}_f = \frac{V_g}{2}(1 + \hat{v}_N)$, expression of λ can be shown to be

$$\lambda = 4\, M^2 \left(2 + \frac{3}{k}\right) \tag{28}$$

where

$$k \triangleq \frac{2 f_s L I_o}{V_o}. \tag{29}$$

The stability parameter λ is, therefore, positive: although the discussed version of the MS-DPCMC is a seemingly straightforward modification of the single-sampled approach to a sampling period equal to $T_s/2$, interaction between the predictive control law and the FC dynamics now results in an unstable FC voltage.

B. Fast-Update Multisampled Peak DPCMC

Fig. 7(a) shows the 3LFC buck converter with a proposed modification of the peak MS-DPCMC, here referred to as fast-update MS-DPCMC. Operation of the controller is exemplified in Fig. 7(b) for peak current-mode control with an LE carrier. The key point is that $d[n]$ is updated *immediately after the sampling event*—in practice, as soon as the digital controller has calculated the new duty cycle value. In Fig. 7(b), the duty cycle update occurs Δt_{calc} seconds after the sampling event. Observe that, while this type of control action is usually not possible using a microcontroller-based platform, it poses little technical difficulties in the context of custom hardwired digital controllers targeted by this article [23].

With the same approach used for (3), the control equation for the fast-update implementation can be derived as

$$d[n] = \frac{2 f_s L}{V_g} \left(I_{\text{ref}} - i_L[n-1]\right) + M. \tag{30}$$

It can be shown that the evolution of the peak current perturbation is still governed by a dead-beat relationship.

Stability of the FC voltage can be studied using the SRA-based approach. From the fast-update predictive control law (30), and assuming that the FC voltage is unbalanced with a small perturbation $\hat{v}_N$ defined as usual, a first-order Taylor expansion of the average FC current yields

$$I_f \simeq -4\, M I_o \left(\frac{1}{2} + M^2 \frac{V_g}{4 f_s L I_o}\right) \hat{v}_N. \tag{31}$$

Using the definitions (6), (7), and (29), the expression of λ becomes

$$\lambda = -4\, M^2 \left(1 + \frac{M}{k}\right). \tag{32}$$

Stability parameter λ is always negative, indicating that the FC voltage is unconditionally stable.

C. Remarks on Duty Cycle Constraints in the Fast-Update MS-DPCMC

Since, in the fast-update MS-DPCMC, the duty cycle is updated Δt_{calc} seconds into the switching period, duty cycles

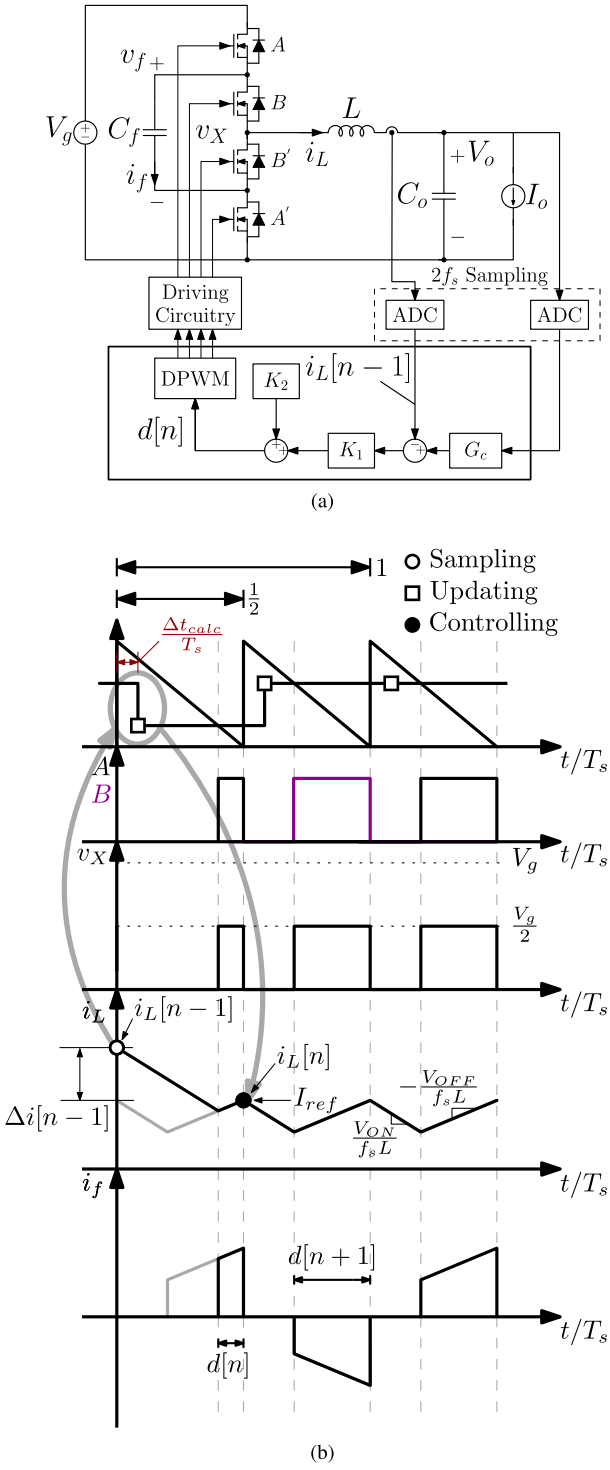


Fig. 7. (a) Generic block diagram of a 3LFC buck with fast-update MS-DPCMC. (b) Operation of fast-update multisampled *peak* DPCMC with an LE carrier.

$d[n]$ larger than $1 - \Delta t_{\text{calc}}/T_s$ cannot be correctly generated by the LE PWM. It is, therefore, necessary to provide an upper saturation to the duty cycle command equal to

$$D_{\max} = 1 - \frac{\Delta t_{\text{calc}}}{T_s}. \tag{33}$$

TABLE I
EXPRESSIONS OF λ AND FC VOLTAGE STABILITY PROPERTIES FOR PEAK, VALLEY, AND AVERAGE DPCMC ($k \triangleq 2f_sLI_o/V_o$)

		peak DPCMC+LE carrier	*valley* DPCMC+TE carrier	*average* DPCMC+TTE carrier
single-sampled	$0 < M < 1$	$\lambda = 0$ (stable)	$\lambda = 0$ (stable)	$\lambda = 0$ (stable)
multi-sampled	$M < 0.5$	$\lambda = 4M^2\left(2+\frac{3}{k}\right)$ (unstable)	$\lambda = 4M^2\left(2+\frac{(1-2M)}{k}\right)$ (unstable)	$\lambda = 0$ (stable)
	$M > 0.5$	$\lambda = -4M(1-M)\left(1+\frac{(M-1)^2}{Mk}\right)$ (stable)	$\lambda = -4M(1-M)\left(1-\frac{(M-1)^2}{Mk}\right)$ (conditionally stable)	$\lambda = 0$ (stable)
fast-update	$M < 0.5$	$\lambda = -4M^2\left(1+\frac{M}{k}\right)$ (stable)	$\lambda = -4M^2\left(1-\frac{M}{k}\right)$ (conditionally stable)	$\lambda = 0$ (stable)
	$M > 0.5$	$\lambda = 4M(1-M)\left(1+\frac{(M-1)^2}{2Mk}\right)$ (unstable)	$\lambda = -4M(1-M)\left(\frac{(M-1)^2}{Mk}-1\right)$ (conditionally stable)	$\lambda = 0$ (stable)

Such a saturation limit does not pose practical problems as long as $\Delta t_{\text{calc}} \ll T_s$. Similar considerations hold for the other analyzed cases.

VI. EXTENSION TO AVERAGE AND VALLEY MS-DPCMC

A multisampled predictive control equation can be derived for the *valley* and the *average* controllers, in both the traditional and fast-update forms.

Following the discussion in Section IV regarding the possible pairings between the controller type and the PWM carrier, the discussion will only focus on those cases that can yield a unique control law and a dead-beat regulation of the sampled inductor current: these are peak DPCMC with LE carrier, valley DPCMC with TE carrier, and average DPCMC with TTE carrier. In all these cases, the same control equations already derived for peak MS-DPCMC are obtained, with identical dead-beat dynamic properties as far as the inductor current is concerned. Conversely, FC voltage stability properties strongly depend on the controller type and the DPWM carrier used. As discussed before, this is evaluated by studying the sign of the stability parameter λ.

Expressions of λ under the SRA for the three types of controllers are reported in Table I. Table I provides a comprehensive summary of the stability properties of single-sampled and MS-DPCMC, and represents the main contribution of this article.

For the single-sampled cases, the SRA analysis predicts a marginally stable FC voltage ($\lambda = 0$). As discussed in Section III-B, by removing the SRA hypothesis, one finds that λ is always negative regardless of the values of M and k. In practice, single-sampled peak, valley, and average DPCMCs are always stable.

For the multisampled cases, the situation is much more heterogeneous. Stability of peak and valley MS-DPCMC is affected by both M and k. For $M < 0.5$, both controllers have an unstable FC voltage; for $M > 0.5$, peak MS-DPCMC is unconditionally stable, while valley MS-DPCMC is stable under the condition

$$\frac{2+k-\sqrt{k^2+4\,k}}{2} < M < \frac{2+k+\sqrt{k^2+4\,k}}{2}.$$

Observe that valley MS-DPCMC is not open-circuit stable.

For the fast-update MS-DPCMC, the situation is as follows. For $M < 0.5$, peak fast-update MS-DPCMC leads to an unconditionally stable operation, as already discussed in Section V-B, while the controller in unstable for $M > 0.5$. For valley fast-update MS-DPCMC, one has conditional stability expressed by $M < k$ if $M < 0.5$. The controller is, therefore, open-circuit unstable. When $M > 0.5$, stability condition becomes

$$M < \frac{2+k-\sqrt{k^2+4\,k}}{2} \;\vee\; M > \frac{2+k+\sqrt{k^2+4\,k}}{2}.$$

With regard to average MS-DPCMC, the SRA-based approach yields $\lambda = 0$ in both the multisampled and fast-update cases. Removal of the SRA according to the approach described in Section III-B is, therefore, necessary. Interestingly, the calculation of λ yields exactly the same results as the single-sampled case, and therefore the same plots of Fig. 4(a) and (b), confirming controller stability.

The reason why, for average current control, the same λ is found for both single-sampled and multisampled controllers, is that the unbalanced steady-state waveforms of the two situations are identical. In fact, duty cycles D_1 and D_2 of the charging and discharging phases remain equal to each other in the multisampled case even if $\hat{v}_N \neq 0$, due to the TTE modulation. Consequently, the calculation of I_f for the multisampled case is analytically identical to the single-sampled one. In conclusion, average DPCMC is always unconditionally stable regardless of its single-sampled, multisampled, or fast-update implementation.

A. Summary

The following general remarks can be drawn from the above analysis and from the results reported in Table I.

1) Single-sampled peak, valley, or average always guarantee FC voltage stability.
2) Multisampled average DPCMC also guarantees FC voltage stability. In particular, the fast-update option strongly improves the dynamic capabilities of the converter.
3) Multisampled peak DPCMC implemented using the fast-update approach is always stable for $M < 0.5$. Although stability is not achieved throughout the entire range of M, this option is nonetheless extremely interesting in a number of relevant cases—e.g., automotive scenarios—in which M is already constrained to be small by the application.

TABLE II
PARAMETERS OF THE 3LFC BUCK CONVERTER CASE STUDY

Converter parameters	
Input voltage V_g	12 V
Output voltage V_o	1.5 V
Output current I_o	500 mA
Filter inductance L	6.5 µH
Filter capacitance C_o	50 µF
Flying capacitance C_f	20 µF
Switching frequency	500 kHz
Voltage loop bandwidth and phase margin	
Single-sampled DPCMC	$f_s/18$, 50°
Multi-sampled DPCMC	$f_s/13$, 50°
Fast-update, multi-sampled DPCMC	$f_s/6$, 50° ($\Delta t_{calc} = 50$ ns)

VII. SIMULATION ANALYSIS

For the purpose of investigating the discussed DPCMC control approaches, a 500 kHz, 12–1.5 V, 500 mA 3LFC buck case study is considered. Converter parameters are summarized in Table II. The voltage loop is compensated in order to achieve the same phase margin in both the single-sampled and multisampled cases and by maximizing the loop gain crossover frequency subject to that constraint.

The case study converter is simulated in the MATLAB/Simulink/PLECS environment. In the simulation analysis presented below, a uniformly distributed $\pm 25\%$ tolerance is systematically included in the switch ON resistances. Neither stability nor appreciable balancing issues are observed in any of the DPCMC controllers under investigation. As for the sensitivity of DPCMC controllers to timing mismatches in the control signals, a dedicated Monte Carlo analysis is performed and described in Section VII-B.

A. Dynamics and FC Voltage Stability

Simulated waveforms illustrating the transient response of single-sampled peak DPCMC to a 500 mA-to-0 A load step is shown in Fig. 8. The simulation confirms that the average FC voltage remains stable at $V_g/2$ throughout the transient.

Fig. 9 reports the corresponding simulated response for the fast-update multisampled peak DPCMC. As expected, the fast-update MS-DPCMC achieves a much faster dynamics and smaller overshoot with respect to the single-sampled implementation. Furthermore, in both cases, the FC voltage remains stable throughout the transient, in agreement with the theoretical findings.

To further validate the FC voltage stability achieved by the fast-update approach, the system response to an abrupt (step-like) FC voltage perturbation is simulated and reported in Fig. 10. In the simulation model, the FC is suddenly put in series with a constant voltage source, and the total voltage across the voltage source + FC is then monitored throughout the subsequent transient. Although such abrupt variation is rather unrealistic in practice, it nonetheless represents a good simulation test to

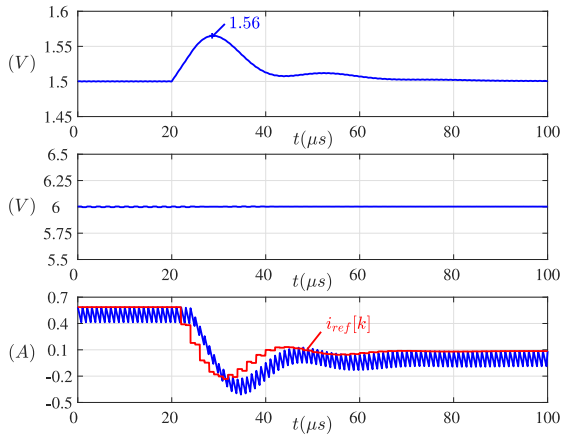


Fig. 8. Single-sampled *peak* DPCMC with LE carrier: simulated response to a 500 mA-to-0 A load step. (Top) output voltage, (middle) FC voltage, and (bottom) inductor current and reference current.

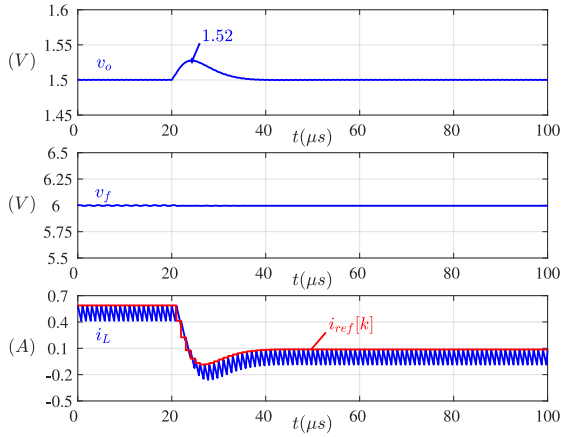


Fig. 9. Fast-update multisampled peak DPCMC with LE carrier: simulated response to a 500 mA-to-0 A load step. (top) output voltage; (middle) FC voltage; and (bottom) inductor current and reference current.

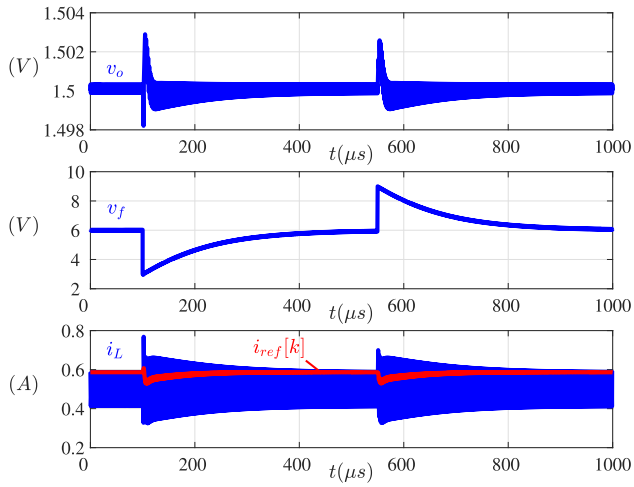


Fig. 10. Fast-update multisampled *peak* DPCMC with LE carrier: simulated response to an abrupt FC voltage perturbation $V_f = 0.5V_g \rightarrow 0.25V_g$ and $V_f = 0.5V_g \rightarrow 0.75V_g$: (top) output voltage v_o; (middle) instantaneous FC voltage v_f; and (bottom) inductor current i_L and current loop reference signal i_{ref}.

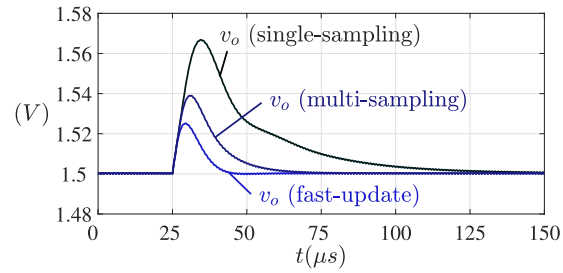


Fig. 11. Simulated output voltage response to a 500 mA-to-0 A load step for average DPCMC; comparison between the single-sampled, multisampled, and fast-update multisampled cases.

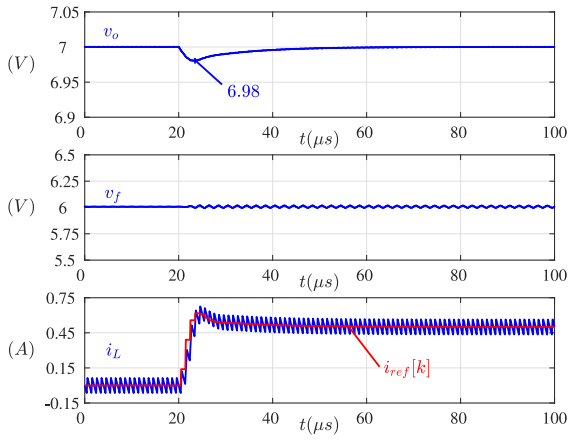


Fig. 12. Fast-update multisampled average DPCMC with TTE carrier: simulated response to a $0 \rightarrow 500$mA load step, for $M > 0.5$: (top) output voltage; (middle) FC voltage; and (bottom) inductor current and reference current.

assess the conclusions of the theoretical section. Waveforms in Fig. 10 indeed confirm that the average FC voltage asymptotically converges back to the initial value even in such extreme case.

Fig. 11 reports a comparison between the transient responses of single-sampled, multisampled, and fast-update multisampled average DPCMC controllers to a 500 mA-to-0 A load step. Although, in this case, all three techniques can be implemented without any FC stability issue, the dynamic performances are obviously different. As expected, the fast-update implementation is faster and produces a smaller overshoot in the output voltage response.

Fig. 12 reports the closed-loop response of the fast-update multisampled average DPCMC to a 0 A-to-500 mA load-step variation. In order to test the inductor current and the FC voltage stability for the operating conditions $M > 0.5$, the average output voltage is regulated at $V_o = 7$ V. The test confirms that the fast-update average MS-DPCMC guarantees stability of both the inductor current and FC voltage, in agreement with the developed theory.

B. DPCMC Sensitivity to Timing Mismatches

In order to assess the impact of timing mismatches in the control signals on FC voltage balancing, a Monte Carlo simulation is carried out. In each simulation run, a uniformly distributed

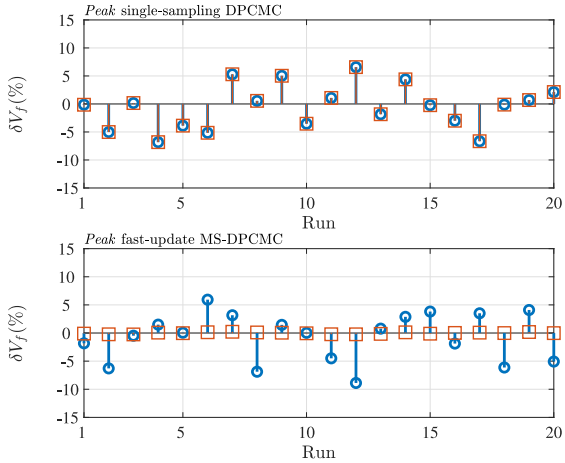


Fig. 13. Open-loop (circles) versus closed-loop (squares) Monte Carlo simulation of (top) single-sampled peak DPCMC and (bottom) fast-update multisampled peak DPCMC.

$\pm 5\%$ variation of the gate driver propagation delay is randomly generated. Simulations are performed both closed loop and open loop, with the open-loop modulating signal of the DPWM adjusted to produce, in steady state, the nominal output voltage $V_o = 1.5$V. After each simulation run, the relative steady-state imbalance

$$\delta V_f \triangleq \frac{V_f - V_g/2}{V_g/2} \tag{34}$$

is recorded.

Fig. 13 reports the simulation results for peak DPCMC, comparing the single-sampled case with the fast-update multisampled case. As seen in the figure, sensitivity of the single-sampled peak DPCMC is identical to the open-loop condition. In other words, no inherent balancing action is produced by the single-sampled controller in presence of significant timing mismatches. This has been found to be the case for all single-sampled controllers (peak, valley, and average).

The fast-update multisampled peak case is, in contrast, significantly different, in that the closed-loop sensitivity is strikingly smaller than the open-loop one, and the open-loop imbalance is almost entirely corrected by the multisampled controller: the residual FC voltage imbalance δV_f for the fast-update MS-DPCMC is less than 0.3% for all simulation runs illustrated in Fig. 13.

Such an inherent self-balancing feature of the fast-update peak DPCMC can be justified by the fact that multisampled controllers are intrinsically capable of producing different duty cycles D_1 and D_2 within the same switching period. In presence of a timing mismatch of the control signals, the system reaches a steady state in which D_1 and D_2 are slightly different and partially compensate for the open-loop FC voltage imbalance. This condition is simply not possible with any of the single-sampled controllers here discussed, which force $D_1 = D_2$ by construction. Significant self-balancing capabilities have been verified for peak and valley controllers in all the stable multisampled or fast-update multisampled cases reported in Table I.

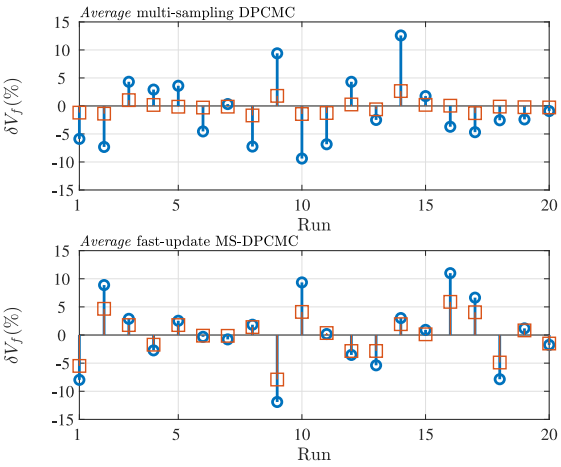


Fig. 14. Open-loop (circles) versus closed-loop (squares) Monte Carlo simulation of (top) multisampled average DPCMC and (bottom) fast-update multisampled average DPCMC.

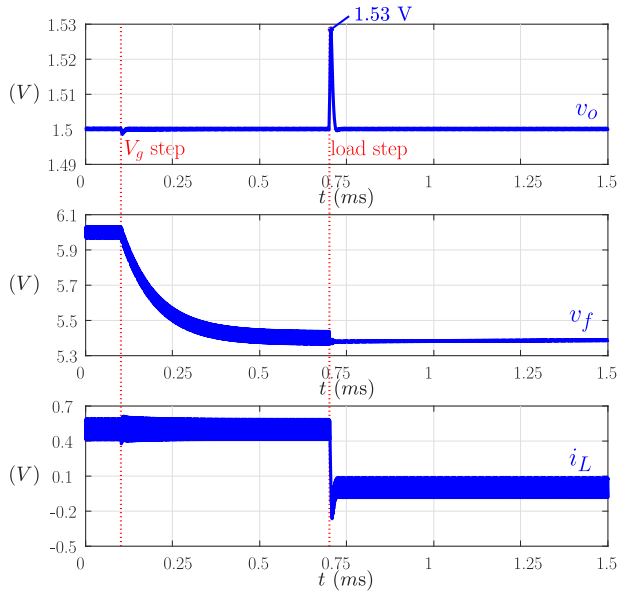


Fig. 15. Fast-update multisampled peak DPCMC with LE carrier: simulated response to a 12 V-to-10.8 V input voltage step followed by a 500 mA-to-0 A load step. (Top) output voltage, (middle) FC voltage, and (bottom) inductor current.

Monte Carlo analysis and comparison between the multisampled and fast-update multisampled average DPCMCs is shown in Fig. 14. As seen, multisampled average controllers also exhibit some degree of self-balancing, although less marked than the peak or valley cases, and with the multisampled case being slightly more robust than the fast-update one: the worst case FC voltage imbalance δV_f is always less than 2.6% in the former and less than 6% in the latter. Nonetheless, the closed-loop imbalance is strongly improved over the open-loop condition in all cases.

Results presented in this section can be summarized as follows.

1) Single-sampled DPCMC techniques exhibit a closed-loop sensitivity to timing mismatches, which is identical to that of the open-loop converter.
2) When stable, multisampled peak and valley DPCMC (either in their simple or fast-update forms) exhibit strong self-balancing capabilities, resulting in a marked improvement of the converter sensitivity to timing mismatches over the open-loop condition.
3) Multisampled average DPCMC also exhibits self-balancing properties, although to a lesser extent than their peak or valley counterparts, and with the regular multisampled implementation being slightly less sensitive than the fast-update one.

C. Robustness With Respect to the Converter Parameters

The predictive control equations discussed in this article depend on the converter parameters V_g, M, and L—a fact shared by other predictive controllers previously reported [17] and which deserves a dedicated discussion.

One preliminary comment is that, in the integrated applications targeted by this study, a package pin is routinely reserved for input voltage sensing, as testified in several commercial integrated circuits datasheets [24]–[26]. Therefore, the assumption that the information on V_g is available to the controller is consistent with the state of the art of commercial products. Furthermore, in the multilevel converters considered in this article, one has $M = D$, i.e., the voltage conversion ratio is equal to the duty cycle, a signal always available inside the digital controller. Also note that an estimate of V_g can also be numerically obtained as V_o/M, eliminating the need for input voltage sensing altogether at the expense of a slight increase in hardware complexity. Overall, presence of V_g and M in the predictive control laws do not pose significant technical challenges to the application of DPCMC because all equations can be digitally implemented using measured or online-estimated coefficients.

Nonetheless, a simulation-based analysis is here presented assuming that variations of V_g occur without a corresponding adjustment or recalculation of the predictive law coefficients. Fig. 15 shows a simulation where the input voltage V_g changes quickly from 12 to 10.8 V. Subsequently, the load current steps from 500 mA to 0 A. After the input voltage step, the FC voltage settles to the new balanced value, confirming that the controller is still able to guarantee a stable operation. After the load step, the overshoot of the output voltage v_o is slightly larger than the overshoot in Fig. 9, while the response time is practically unchanged.

With regard to the robustness of DPCMC against variations in L, Fig. 16 reports closed-loop simulation results for the fast-update peak MS-DPCMC assuming variations of the filter inductance with respect to the nominal value $L_{\rm nom}$ used in the predictive equations. In all cases, the closed-loop response to a 500 mA-to-0 A load step is stable and the performances are almost unchanged.

These results confirm that the fast-update peak MS-DPCMC operates normally while continuing to guarantee stability for both inductor current and FC voltage even in the presence of

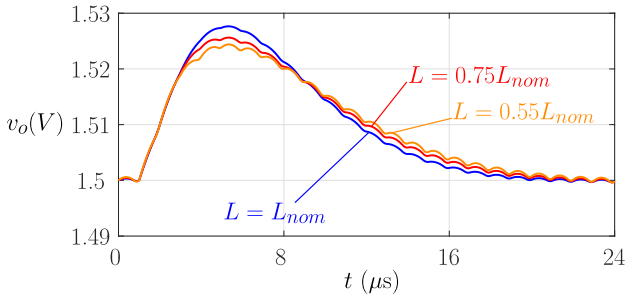


Fig. 16. Fast-update multisampled *peak* DPCMC with LE carrier: simulated output voltage response to a 500 mA-to-0 A load step with nominal and nonnominal inductance values.

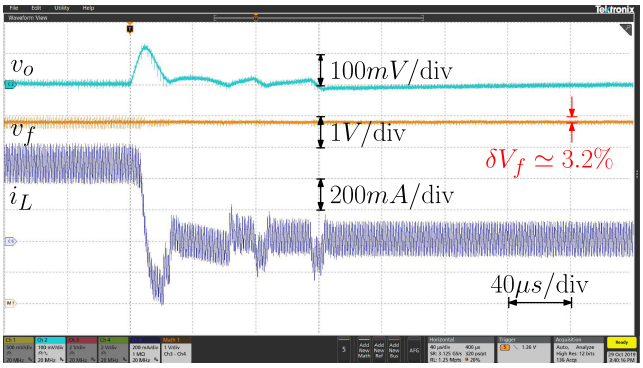


Fig. 17. Experimental response of single-sampled peak DPCMC to a $500\text{mA} \rightarrow 0$ load step. Output voltage v_o (ac-coupled): 100 mV/div; FC voltage v_f: 1 V/div; and inductor current i_L: 200 mA/div.

inductance and input voltage values deviating with respect to the nominal values. Same robustness holds for peak single-sampling and multisampling DPCMC as well as for average and valley controllers.

VIII. Experimental Results

A custom prototype of the case study 3LFC buck converter described in Table II is built and tested. The digital controller is VHDL-coded and synthesized on a commercial field-programmable gate array board interfaced with the 3LFC prototype. In the experimental measurements, no attempt is made to correct or compensate timing mismatches naturally present in the prototype.

The experimental response of the single-sampled *peak* DPCMC to a 500 mA-to-0 A load-step variation is reported in Fig. 17. As predicted theoretically and by the simulations, the average FC voltage remains stable throughout the transient.

The same transient response is illustrated in Fig. 18 for the fast-update peak MS-DPCMC, illustrating a faster dynamics compared to the peak single-sampled DPCMC while still maintaining a stable FC voltage. Note that the small FC voltage imbalance visible in Fig. 17 is essentially eliminated in Fig. 18, in agreement with the discussion carried out in Section VII-B.

Fig. 19 reports the closed-loop response of the fast-update multisampled average DPCMC to 500 mA-to-0 A load-step

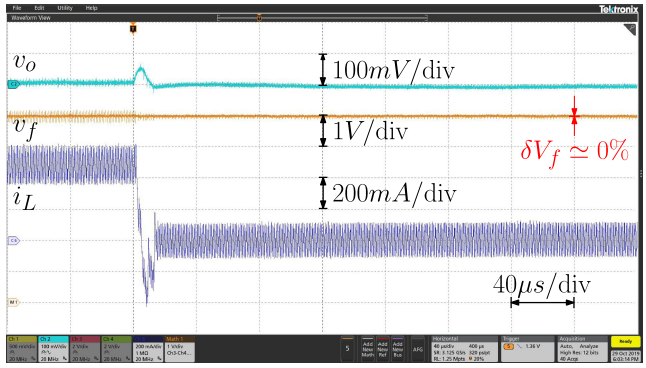


Fig. 18. Experimental response of fast-update multisampled peak DPCMC to a $500\text{mA} \rightarrow 0$ load step. Output voltage v_o (ac-coupled): 100 mV/div; FC voltage v_f: 1 V/div; and inductor current i_L: 200 mA/div.

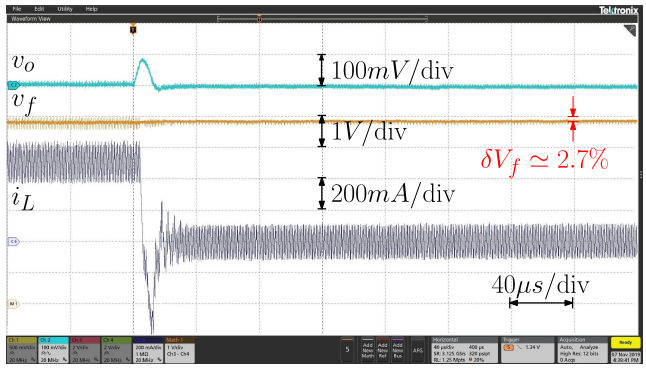


Fig. 19. Experimental response of fast-update multisampled average DPCMC to a $500\text{mA} \rightarrow 0$ load step. Output voltage v_o (ac-coupled): 100 mV/div; FC voltage v_f: 1 V/div; and inductor current i_L: 200 mA/div.

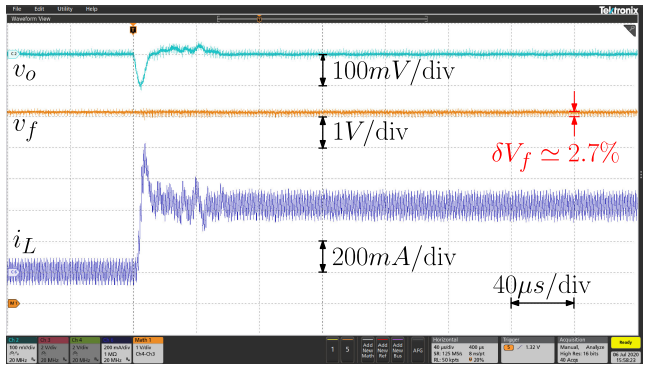
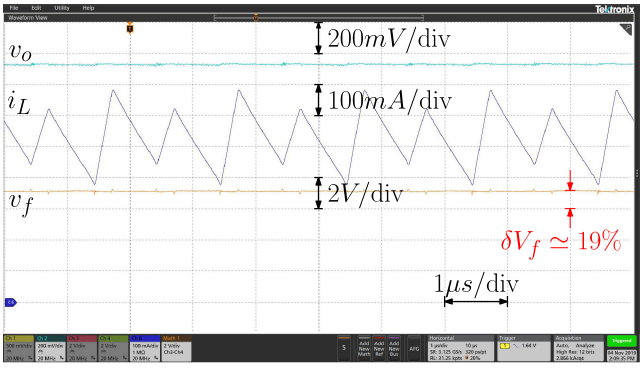


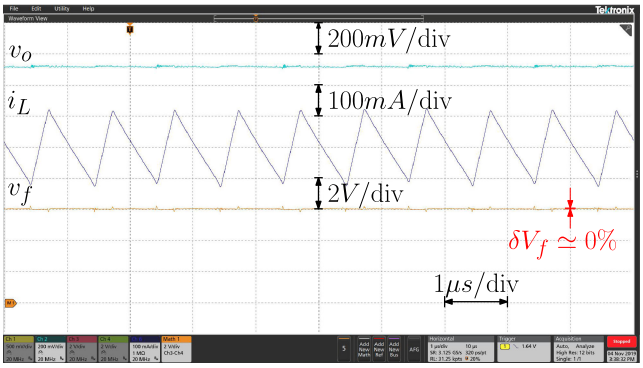
Fig. 20. Experimental response of fast-update multisampled average DPCMC to a $500\text{mA} \rightarrow 0$ load step and for $M = 7/12$. Output voltage v_o (ac-coupled): 100 mV/div; FC voltage v_f: 1 V/div; and inductor current i_L: 200 mA/div.

variation. Main conclusions regarding FC voltage stability and dynamic capabilities of the controller are verified.

Unlike the fast-update multisampled peak DPCMC, fast-update multisampled average DPCMC control is predicted to be stable for $M > 0.5$ as well. The experimental test reported in Fig. 20 documents the closed-loop response of the fast-update multisampled average DPCMC to a 0 A-to-500 mA load-step variation for $V_o = 7\text{V}$. Main conclusions regarding FC voltage



(a)



(b)

Fig. 21. Experimental comparison between (top) open-loop and (bottom) closed-loop FC voltage imbalance with fast-update multisampled peak DPCM in presence of an intentional timing mismatch of the control signals. Output voltage v_o: 200 mV/div; FC voltage v_f: 2 V/div; and inductor current i_L: 100 mA/div.

stability and dynamic capabilities of the controller are, therefore, experimentally verified for both $M < 0.5$ and $M > 0.5$ cases.

To better validate the conclusions drawn in Section VII-B regarding the self-balancing properties of multisampled controllers, an intentional timing mismatch is introduced in the control signals in order to produce a large open-loop FC voltage imbalance and compare it with the closed-loop situation. Such intentional mismatch is obtained by adding a turn-ON delay of switch B [see Fig. 7(a)] and causes the duration of the discharging phase of the FC to be reduced by 2.5 ns. As a result, the measured open-loop FC voltage imbalance becomes $\delta V_f = 19.5\%$ ($V_f = 7.17\text{V}$).

Fig. 21(a) and (b), respectively, reports the experimental open-loop and closed-loop situation for the fast-update multisampled *peak* DPCMC in presence of such intentional mismatch. The multisampled controller almost fully eliminates the open-loop imbalance: measured average FC voltage in the closed-loop condition is $V_f = 6.01\text{V}$, corresponding to a residual imbalance of $\delta V_f = 0.17\%$.

Fig. 22 shows a load-step transient similar to the one proposed in Fig. 18 but with a nonnominal input voltage $V_g = 10.8\text{V}$ and with no recalculation of the predictive law coefficients. The experimental average FC voltage correctly settles to the balanced value $10.8\text{V}/2 = 5.4\text{V}$. The dynamics of the inductor current is very similar to the nominal condition, and no stability issues are seen.

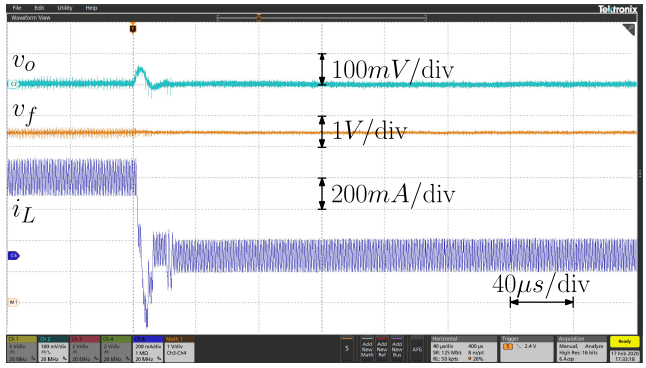


Fig. 22. Experimental response of fast-update multisampled peak DPCMC to a $500\text{mA} \rightarrow 0$ load step for nonnominal value of the input voltage $V_g = 10.8\text{V}$. Output voltage v_o (ac-coupled): 100 mV/div; FC voltage v_f: 1 V/div; and inductor current i_L: 200 mA/div.

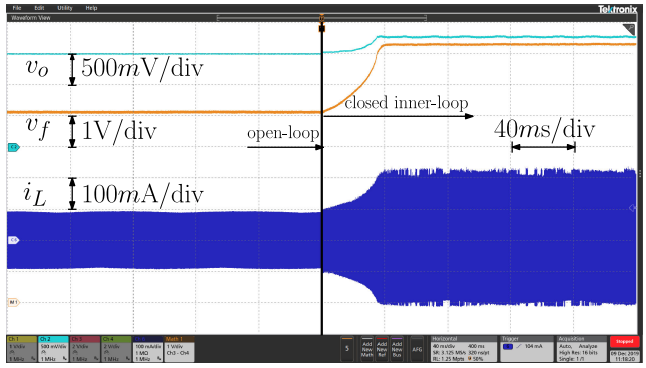


Fig. 23. Experimental open-circuit response of fast-update multisampled valley DPCMC when the inner current loop is suddenly closed from an initially open-loop condition. Output voltage v_o: 500 mV/div; FC voltage v_f: 1 V/div; inductor current i_L: 100 mA/div.

Open-circuit instability theoretically predicted for multisampled *valley* controllers is verified in Fig. 23. Specifically, the figure reports the experimental behavior of fast-update valley MS-DPCMC when, starting from an initially open-loop situation, the inner inductor current loop is suddenly closed. In the measurement, the converter operates in open-circuit conditions. Theoretical instability predicted in Table I is confirmed by the onset of FC voltage runaway as soon as the DPCMC loop is closed.

IX. Conclusion

This article investigates the use of digital predictive peak, valley, and average current-mode control in dc–dc 3LFCs. Single-sampled and multisampled implementations are considered, including a fast-update variation of the multisampled controller in which the duty cycle command is updated as soon as the control calculations are performed. Stability of the inductor current and of the FC voltage are analyzed in all cases, and a simulation investigation of the controller sensitivities to timing mismatches in the control signals is reported.

Single-sampled peak, valley, or average DPCMC can always be reliably implemented with no stability issues for the inductor current nor the FC voltage. Furthermore, average DPCMC is

unconditionally stable regardless of its single-sampled, multi-sampled, or fast-update implementation. For the average and the peak cases, the fast-update option leads to a significant control bandwidth extension over the single-sampled approach.

While single-sampled controllers do not exhibit improved sensitivity to timing mismatches in the control signals over the open-loop condition, all multisampled implementation present some degree of self-balancing, with peak and valley controllers capable of significantly correcting the open-loop imbalance.

Simulation and experimental results are presented for a 500 kHz, 12–1.5 V, 500 mA 3LFC buck case study.

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