Comparison of DAB and *LLC* DC–DC Converters in High-Step-Down Fixed-Conversion-Ratio (DCX) Applications

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***Abstract*—This article compares the dual active bridge (DAB) and *LLC* converter topologies when utilized in a high-step-down fixed-conversion-ratio application, such as the dc–dc stage in laptop and LED TV adapters. Multiple candidate topologies for this application are compared, motivating the selection of the DAB and the *LLC* for further investigation. The two converters are first compared using first-order insights, and then using a detailed analytical design methodology focused on zero-voltage switching. Fundamental tradeoffs between conduction and switching losses are analyzed, predicting that the DAB converter should achieve higher efficiency at heavy loads due to lower conduction losses, while the *LLC* converter should achieve higher efficiency at lighter loads due to lower switching losses. To validate these predictions, design examples are developed for a 1-MHz 400–20 V 330-W application, and experimental prototypes for both converters are built based on these designs. Measured results match well with the predictions. The DAB prototype achieves a peak efficiency of 94.9% at full load, corresponding to a 27% reduction in losses compared to the *LLC* prototype.**

***Index Terms*—Design with optimal tradeoff between switching and conduction losses, fixed conversion ratio (DCX) converters, high-step-down dc–dc converters, high-efficiency and high power density converters, zero voltage switching (ZVS).**

I. Introduction

OFFLINE power supplies rated for hundreds of watts and providing high step-down, including adapters for gaming laptops and LED TVs [1]–[3], and datacenter power distribution systems [4]–[8], typically employ a two-stage architecture with a front-end power-factor correction (PFC) ac–dc stage followed by an isolated step-down dc–dc stage, as shown in Fig. 1. The PFC stage generates a well-regulated intermediate bus voltage (typically 400 V for universal input applications) and the dc–dc stage converts it down to the load voltage (for, e.g., 20 V for laptop adapter applications). Designing this isolated dc–dc converter to provide a fixed conversion ratio [like a dc transformer, or fixed-conversion-ratio (DCX)] allows it to be optimized for high efficiency. In addition, this converter must maintain high power density to comply with increasingly stringent area and height constraints in consumer electronics and datacenter applications. Suitable high-density solutions have been enabled by the emergence of wide-bandgap devices, together with the use of soft-switching topologies, which allow the isolated dc–dc stage to operate efficiently at high switching frequencies [9]–[12].

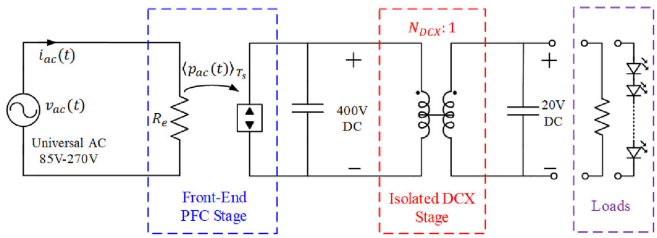

Fig. 1. Typical two-stage ac–dc power delivery architecture, comprising a front-end PFC stage, an energy buffering capacitor and an isolated DCX dc–dc stage.

Two popular choices for high-step-down isolated DCX converters are the dual active bridge (DAB) converter and the *LLC* resonant converter [11]–[21]. These converters share many desirable characteristics, including the design flexibility to achieve zero-voltage switching (ZVS) over a wide load range, easy-to-implement control strategies (frequency control for *LLC*, phase-shift control for DAB), and a relatively low component count. Among the two topologies, the *LLC* converter offers an advantage in control, since the secondary-side devices can be driven synchronously without the need for communication across the isolation barrier [22]–[24]. On the other hand, the DAB converter can potentially deliver higher efficiencies due to lower rms and circulating currents [16], [25]. The relative merits of DAB and *LLC* converters [along with other isolated topologies suitable for high step-down, e.g., phase-shifted full-bridge (PSFB)] have been extensively studied for higher power applications ($\geq$1 kW) [25]–[28]. At these power levels, the switching frequency is relatively low ($<$100 kHz) and ZVS is not always vital to achieving high efficiency [25]. However, for

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the lower power levels (100 W−1 kW) and higher switching frequencies (>500 kHz) targeted in this article, zero-voltage switching is critical to the converter's performance.

This article presents a comparison between DAB and *LLC* converters for a high-step-down fixed-conversion-ratio DCX application, wherein power density requirements necessitate high-frequency operation. First, a brief overview of isolated dc–dc topologies suitable for such an application is provided to motivate the selection of the DAB and *LLC* converters. Following this, an analytical comparison between the two converters is performed—initially based on first-order insights and then using a ZVS-oriented design methodology—to establish their relative merits. This analysis concludes that the DAB converter is likely to achieve higher efficiency at heavy loads, while the *LLC* converter is likely to be more efficient at lighter loads. These predictions are validated using 1-MHz 400–20 V 330-W prototypes of the DAB and *LLC* converters. The DAB converter prototype achieves 94.9% efficiency at full load, corresponding to 27% lower losses than the *LLC* converter prototype.

The remainder of this article is organized as follows. Section II compares and downselects suitable topologies for a high-frequency high-step-down DCX application. Section III presents fundamental insights into the relative merits of DAB and *LLC* converters. A more detailed comparison including ZVS transitions is performed in Section IV. Section V uses the preceding analysis to develop design examples for both converters. Section VI presents experimental results to validate the theoretical comparison. Finally, Section VII summarizes and concludes this article.

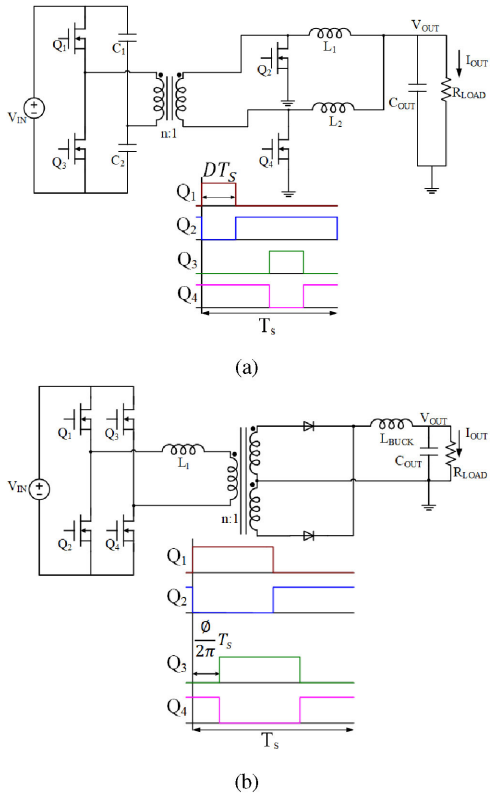


Fig. 2. Isolated dc–dc converter topologies suitable for voltage step-down. (a) Duty-cycle controlled half-bridge converter with current doubler rectifier. (b) PSFB converter.

II. Alternative Topologies

At power levels below ∼200 W, low component count and simple control make flyback and forward converters the most popular choices for high-step-down isolated power conversion [29]–[31]. However, the basic versions of these topologies suffer from relatively high device stresses, and additional components are typically needed to lower device stresses and efficiently achieve large step down at higher power levels [32]. For power levels higher than ∼200 W, bridge type converters are typically preferred [33], [34].

The simplest such converter is the duty-ratio controlled half-bridge converter [35], a version of which with a current-doubler rectifier is shown in Fig. 2(a). The half-bridge converter can share its large step-down burden between duty ratio and transformer turns ratio. However, it does not lend itself well to high-frequency operation (and, hence, high power density) due to its inability to incorporate circuit parasitics such as transformer leakage inductance, and because its inverter devices are hard switched.

Another topology suitable for high-step-down is the PSFB converter, shown with a center-tapped rectifier in Fig. 2(b). Here, the step-down burden is shared between the transformer turns ratio and the phase-shift between the two legs of the full-bridge inverter. The PSFB converter can achieve ZVS of its inverter devices for a limited load range, but the leading inverter leg (passive to active transition) loses ZVS at light loads [36], necessitating a relatively low switching frequency. This, combined with the use of an additional magnetic component in the form of the output filter inductor, limits the power densities achievable with this topology. Furthermore, this particular topology with diode rectification, also suffers from substantial secondary-side ringing due to resonance between the tank inductance and the parasitic switch-node capacitance during diode turn OFF, necessitating additional snubber circuits to maintain reliable operation, further increasing the volume of the converter [37].

Two isolated topologies better suited for high-frequency operation are the DAB converter and the *LLC* converter, shown in Fig. 3(a) and (b), respectively. Compared to the PSFB converter, the DAB and *LLC* converters (when appropriately designed) can achieve soft-switching over a wider load range with reduced circulating currents. Note that the efficiency of DAB and *LLC* converters falls off rather rapidly when the conversion ratio changes from its optimal value of $V_{\mathrm{IN}}/V_{\mathrm{OUT}} = 2n$ [38], [39]. This study is limited to a fixed conversion-ratio application, and hence, is unaffected by this drawback.

In summary, among the topologies considered previously, the DAB and *LLC* converters are the most suitable alternatives for high-power-density high-step-down DCX applications in the >200 W power range, and are selected for further investigation. Salient features of the bridge-type converter topologies compared in this section are summarized in Table I.

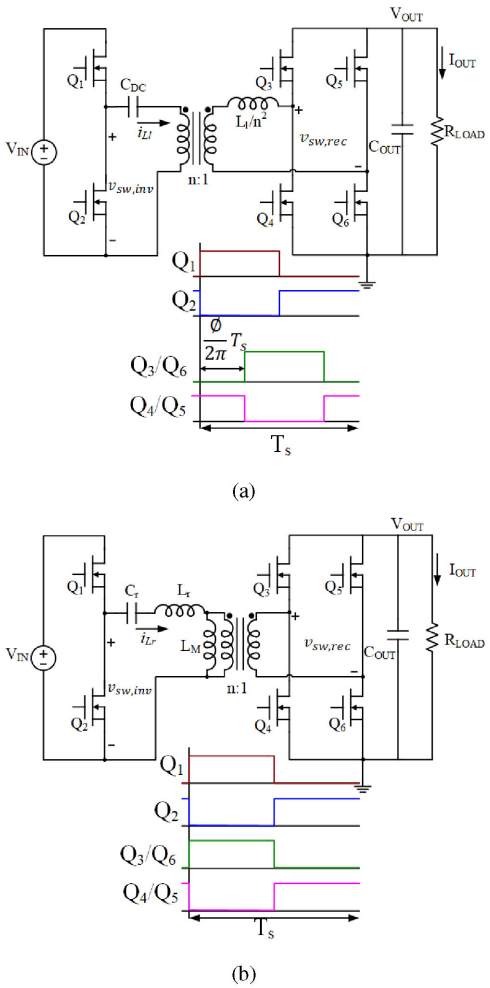


Fig. 3. Isolated dc–dc converter topologies suitable for voltage step-down and high-frequency operation. (a) Dual active bridge converter. (b) *LLC* converter.

TABLE I
COMPARISON OF STATE-OF-THE-ART BRIDGE-TYPE CONVERTER TOPOLOGIES FOR HIGH-STEP-DOWN ISOLATED DCX CONVERTERS

Topology	Number of high voltage devices	Soft switching	Output DC Inductor(s)	Control
Isolated half bridge (Fig. 2(a))	2	No	Yes	Duty cycle control
Phase shifted full bridge (Fig. 2(b))	4	Yes	Yes	Phase shift control
LLC (Fig. 3(a))	2	Yes	No	Frequency control
DAB (Fig. 3(b))	2	Yes	No	Phase shift control

III. FIRST-ORDER COMPARISON OF DAB AND *LLC* CONVERTERS

As can be seen from Fig. 3, the DAB and *LLC* converters are structurally very similar. Both comprise a high-frequency inverter and rectifier, interfaced by an *LC* tank and a transformer. The inverter is selected to be a half-bridge and the rectifier a full-bridge to obtain an effective step-down of two, allowing the turns ratio of the transformer—which provides the bulk of the step-down—to be reduced. Despite the structural similarity, the two converters differ greatly in design and operation. In the DAB converter, the capacitor of the *LC* tank is large and serves the purpose of dc blocking; therefore, at the converter's switching frequency the DAB tank is purely inductive. On the other hand, in the *LLC* converter the capacitor is small and resonates with the inductor at (or close to) the switching frequency; hence, the *LLC* tank has an arbitrary small impedance at the converter's switching frequency. Another distinction between the two converters is in the transformer's construction and magnetizing inductance. In the DAB converter, the transformer is gapless and the magnetizing inductance is large, whereas in the *LLC* converter the transformer is gapped, resulting in a smaller magnetizing inductance. This has important implications in terms of soft-switching: since its gapless transformer stores very little energy, the DAB converter utilizes the energy stored in its inductor L_l (which can in some designs be the leakage inductance of the transformer) to discharge the inverter output capacitance and achieve ZVS. This energy is purely determined by the load current; hence, ZVS can be lost below a certain load as determined by the value of L_l. In contrast, the *LLC* converter utilizes the energy stored in its transformer's magnetizing inductance to achieve ZVS. Therefore, given a certain output voltage, once the magnetizing inductance is designed to achieve ZVS, it is maintained for all loads. These ZVS considerations will be analyzed in detail in Section IV. Since both the DAB and *LLC* converters are capable of achieving ZVS, conduction losses and core losses in the magnetic structures are the major sources of loss, particularly at medium to high loads. Transformer core losses in both converters are identical due to the same volt-seconds being applied. Inductor winding and core losses both depend on the tank currents, a fundamental understanding of which is developed next.

A. DAB Converter

It is assumed that the DAB converter switches at a fixed frequency and each device operates with 50% duty ratio. Output voltage is regulated using single phase-shift control [13], [14], i.e., by controlling the phase-shift between the inverter and the leading leg of the rectifier, as illustrated in Fig. 4. Here, v_1 and v_2 correspond to the inverter output voltage $v_{\text{sw,inv}}$ and the primary-referred rectifier input voltage $nv_{\text{sw,rec}}$, respectively. When the transformer turns ratio is selected to be $n = V_{\text{IN}}/2V_{\text{OUT}}$, the DAB tank current takes a trapezoidal shape (neglecting ZVS transitions, which add a sinusoidal fragment to the current and will be addressed in the following section). As shown in Fig. 4, the phase-shift ϕ controls the peak value of tank current, and hence, the converter's output current (which is the secondary-referred, rectified, and averaged version of the tank current). The rated output current can be expressed in terms of the maximum phase-shift ϕ_{max} as [21], [40]

$$I_{\text{OUT}} = nI_{Ll,\text{pk}}\left(1 - \frac{\phi_{\text{max}}}{\pi}\right) \tag{1}$$

where $I_{Ll,\text{pk}}$ is the peak value of the primary-referred tank current when delivering rated output current. The tank inductance

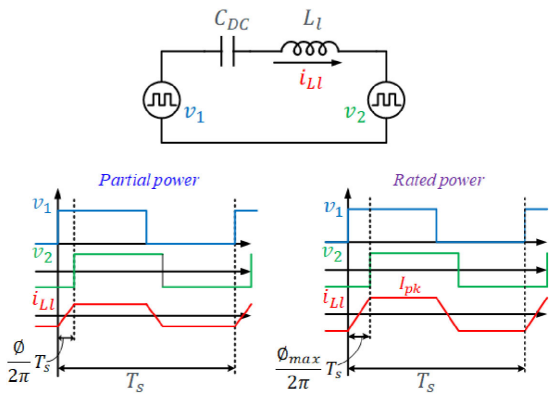


Fig. 4. Operation of DAB converter: equivalent circuit model (top), and idealized switch node voltage and tank current waveforms at partial and rated power levels (bottom).

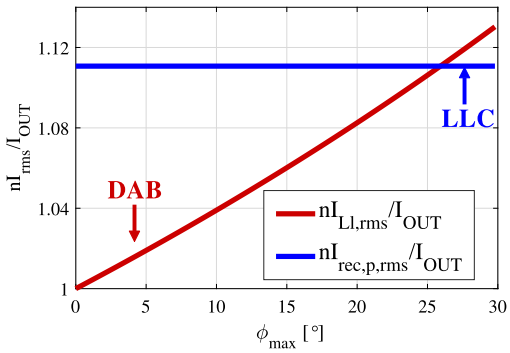


Fig. 5. Comparison of normalized rms tank currents in DAB (red) and *LLC* (blue) converters, as a function of the maximum phase-shift ($\phi_{\max}$) of the DAB converter, neglecting ZVS transitions.

required to deliver rated output current with $\phi = \phi_{\max}$ is given by [21], [40]

$$L_l = \frac{V_{\text{IN}}\phi_{\max} n(1 - \frac{\phi_{\max}}{\pi})}{4\pi f_s I_{\text{OUT}}} \tag{2}$$

where f_s is the converter switching frequency. It should be noted that the maximum phase-shift $\phi_{\max}$ is a design choice. Different selected values for $\phi_{\max}$ will result in different required values for L_l.

Once $\phi_{\max}$ and L_l are determined, the rms value of the DAB converter's tank current when delivering rated output current can be found as

$$I_{Ll,\text{rms}} = I_{Ll,\text{pk}}\sqrt{1 - \frac{2\phi_{\max}}{3\pi}}$$

$$\Rightarrow I_{Ll,\text{rms}} = \frac{I_{\text{OUT}}}{n(1 - \frac{\phi_{\max}}{\pi})}\sqrt{1 - \frac{2\phi_{\max}}{3\pi}}. \tag{3}$$

The rms tank current $I_{Ll,\text{rms}}$, normalized with respect to the rated output current I_{OUT}, is plotted as a function of the maximum phase-shift $\phi_{\max}$ in Fig. 5. For each value of $\phi_{\max}$, the tank inductance is computed using (2) and the normalized rms current is obtained from (3). The rms current is a monotonically increasing function of $\phi_{\max}$.

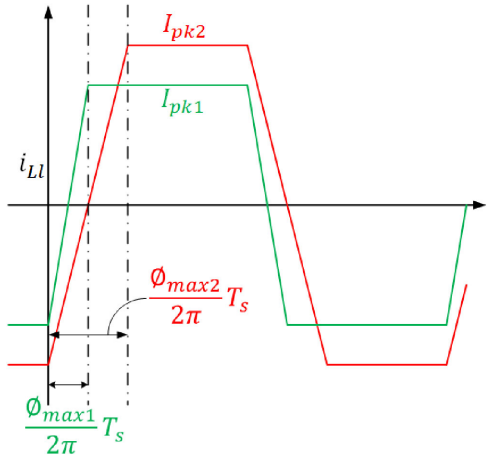


Fig. 6. Impact of two different maximum phase-shifts ($\phi_{\max 1} < \phi_{\max 2}$) on the waveshape of the DAB converter tank current, for the same output current.

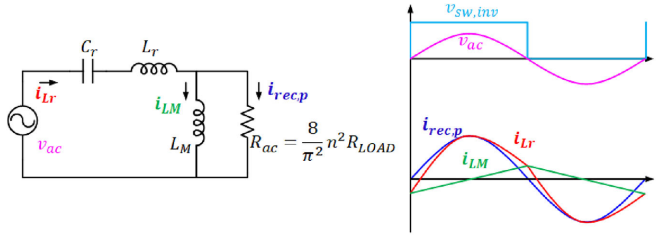


Fig. 7. Operation of *LLC* converter: equivalent circuit model (left), and idealized voltage and current waveforms (right).

This can be intuitively understood from Fig. 6, which shows the DAB tank current for two different values of $\phi_{\max}$, and for the same output current. As can be seen, for the larger value of $\phi_{\max}$, the current spends a longer time transitioning from its negative peak to its positive peak, resulting in higher peaks, and hence, a higher rms value.

B. LLC Converter

Fig. 7 shows equivalent circuit of the *LLC* converter under fundamental-frequency approximation [41], with $v_{\text{ac}} = (v_{\text{sw,inv}} - \frac{V_{\text{IN}}}{2})$ being the ac component of the inverter output voltage $v_{\text{sw,inv}}$, and the load resistor representing the equivalent resistance presented by the rectifier. When operated at the resonant frequency of L_r and C_r, the *LLC* converter behaves as a voltage source and achieves perfect load regulation if the input voltage is constant. In a practical scenario, narrowband frequency variation may be required to compensate for converter losses, component tolerances, and aging effects. With $n = \frac{V_{\text{IN}}}{2V_{\text{OUT}}}$, the equivalent circuit of Fig. 7 can be solved to express the rms value of the primary-referred rectifier input current ($i_{\text{rec},p}$ in Fig. 7) as

$$I_{\text{rec},p,\text{pk}} = \frac{\pi}{2n} I_{\text{OUT}} \Rightarrow I_{\text{rec},p,\text{rms}} = \frac{\pi}{2\sqrt{2}n} I_{\text{OUT}}. \tag{4}$$

As shown in Fig. 7, the *LLC* converter's tank current i_{Lr}, is the sum of the current given by (4) and the transformer

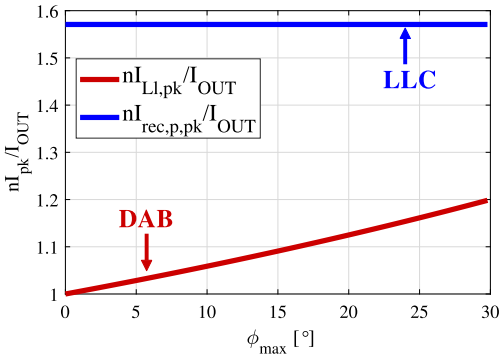


Fig. 8. Comparison of normalized peak tank currents in DAB (red) and *LLC* (blue) converters as a function of the maximum phase-shift (ϕ_{max}) of the DAB converter, neglecting ZVS transitions.

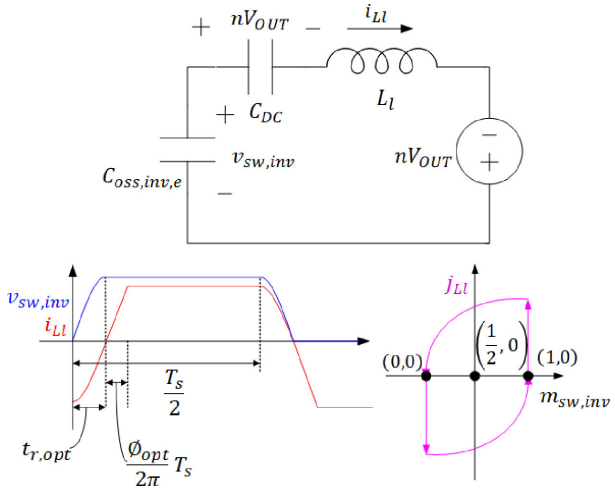


Fig. 9. ZVS transition in DAB converter: equivalent circuit model (top), and switch-node voltage and tank current (bottom) in time domain and on a normalized state-plane with base voltage V_{IN} and characteristic impedance $\sqrt{L_l/C_{oss,inv,e}}$.

magnetizing current. To simplify this analysis and draw insights, the transformer magnetizing current (which enables ZVS) is neglected in this section. Hence, the rms current in the *LLC* tank can be approximated by the expression given in (4). As can be seen, this current is independent of the tank component values and is fixed, given a rated output current I_{OUT}.

C. Comparison

The rms currents in the DAB and *LLC* tanks can now be compared. Since the DAB tank current is trapezoidal, it should follow that its rms value is lower than that of the *LLC* tank current, which is sinusoidal. However, from the fundamental-frequency perspective, the *LLC* tank with its resonating inductance and capacitance presents a resistive load to its inverter (neglecting the relatively small inductive component introduced by the magnetizing inductance); while the DAB tank presents a substantially inductive load to its inverter. The resultant phase lag between the DAB inverter's output voltage and current (proportional to the phase-shift ϕ) introduces circulating currents with associated losses. In order to still reap the benefit of trapezoidal current, the DAB converter must be designed with a relatively low maximum phase-shift ϕ_{max}. This is confirmed in Fig. 5, which compares the normalized rms currents in the DAB and *LLC* tanks, obtained from (3) and (4), respectively. The DAB rms current is lower than its *LLC* counterpart for all values of $\phi_{max} < 26°$. Hence, under the approximations made in this section and assuming the same switches and similar magnetics designs, a low phase-shift DAB converter is expected to have lower conduction losses than an *LLC* converter.

Inductor core losses can be addressed through a similar analysis of peak tank currents. Normalized peak currents for the two converters evaluated using (1) and (4) are plotted in Fig. 8. The DAB tank has lower peak current across the entire range of phase-shifts considered. Assuming similar inductor design and construction in the two converters, peak currents are a reasonable indicator of core losses. Hence, the DAB converter is also expected to have lower inductor core losses than the *LLC* converter.

The analysis presented previously derives first-order insights while neglecting ZVS transitions, which can significantly impact the operation and waveforms of both DAB and *LLC* converters [16], [39]. Hence, to better inform the conclusions drawn here, ZVS considerations are addressed next.

IV. ZVS-Inclusive Design and Comparison of DAB and *LLC* Converters

In order to achieve high efficiency and minimize thermal management needs, MHz-frequency converters must achieve ZVS. This is critical for high-input-voltage, medium-power applications, even with the smaller parasitic capacitances enabled by wide-bandgap devices. For example, consider a half-bridge inverter switching at 1 MHz, where the high-side device is hard-switched across 400 V. With a typical high-voltage GaN device [42], this amounts to a turn-ON switching loss (excluding V-I overlap) of ∼20 W, which, for <1 kW applications, is prohibitive from both the efficiency and thermal management viewpoints. Since this work focuses on step-down applications with relatively low output voltages and relatively high output currents, ZVS of rectifier devices is easier to achieve. Hence, in the following, ZVS considerations are discussed only for the inverter.

A. DAB Converter

In the DAB converter, ZVS is achieved when the inverter output capacitance is discharged through resonance with the tank inductance L_l [12], [16], [21]. As shown in Fig. 9, at the beginning of the ZVS transition, the tank current is at a peak value that is determined by the load current. The tank inductance then resonates with the inverter output capacitance, and the tank current reduces as the capacitance discharges. The scenario shown in Fig. 9 represents optimal ZVS: the tank current reaches zero at the same instant at which the inverter output capacitance is fully discharged, meaning that the tank current carries just enough energy for ZVS. Less energy would lead to hard

switching; more energy would lead to higher circulating current, which would then necessitate higher tank current (and, hence, losses) for the same power delivery. To achieve the optimal ZVS scenario of Fig. 9, the resonant transition period must equal one quarter of the resonant period [21], i.e.,

$$t_{r,\text{opt}} = \frac{1}{4f_{\text{res}}} = \frac{\pi}{2}\sqrt{L_l C_{oss,\text{inv},e}} \tag{5}$$

Here, $C_{\text{oss,inv},e}$ is the effective output capacitance of the inverter, which includes the energy-equivalent output capacitance of the two inverter devices [43], and other parasitic capacitances such as those originating from printed circuit board (PCB) layout and transformer windings; and f_{res} is the resonant frequency of the tank inductance and the inverter output capacitance. This optimal ZVS condition translates to a unique design of the DAB converter, in which the tank inductance and phase shift are given, respectively, by

$$L_{l,\text{opt}} = \frac{1}{\left[\frac{I_{\text{OUT,opt}}}{nV_{\text{IN}}\sqrt{C_{\text{oss,inv},e}}} + (3+\pi)f_s\sqrt{C_{\text{oss,inv},e}}\right]^2} \tag{6}$$

$$\phi_{\text{opt}} = \pi\left[1-(2+\pi)\sqrt{L_{l,\text{opt}}C_{\text{oss,inv},e}}f_s\right] - \sqrt{\pi^2[1-(2+\pi)\sqrt{L_{l,\text{opt}}C_{\text{oss,inv},e}}f_s]^2 - \frac{4\pi^2 f_s I_{\text{OUT,opt}} L_{l,\text{opt}}}{nV_{\text{IN}}}}. \tag{7}$$

These expressions are obtained by relating the phase shift and tank inductance to the output current of the DAB converter under the optimal ZVS condition, assuming instantaneous secondary side ZVS transitions, as described in Appendix A. Incorporating effects of secondary side ZVS transitions prohibit closed form design equations for the tank inductance [21]. The term $I_{\text{OUT,opt}}$ in (6) and (7) is a design choice, representing the output current level for which it is desired to achieve optimal ZVS; and ϕ_{opt} is the phase-shift corresponding to this output current. When a DAB converter is designed according to (6) and (7), it will achieve partial soft-switching while delivering output currents lower than $I_{\text{OUT,opt}}$, and achieve ZVS with circulating tank current while delivering output currents higher than $I_{\text{OUT,opt}}$. The value chosen for $I_{\text{OUT,opt}}$ impacts the DAB converter's efficiency profile over its load range, by altering the tradeoff between switching and conduction losses. A smaller value of $I_{\text{OUT,opt}}$ enables ZVS over a larger load range down from rated load, and hence, lower switching losses, but at the cost of higher circulating current over this range, and hence, higher conduction losses. A feasible range for $I_{\text{OUT,opt}}$ can be obtained from practical considerations. For example, to achieve a reasonably high efficiency, the resonant transition period during which ZVS is achieved but negligible power is transferred to the output, should be a small fraction of the switching period [21]. This can be expressed in terms of the resonant transition frequency f_{res} and switching frequency f_s as

$$F = \frac{f_s}{f_{\text{res}}} = \frac{f_s}{1/(2\pi\sqrt{L_{l,\text{opt}}C_{\text{oss,inv},e}})} \ll 1. \tag{8}$$

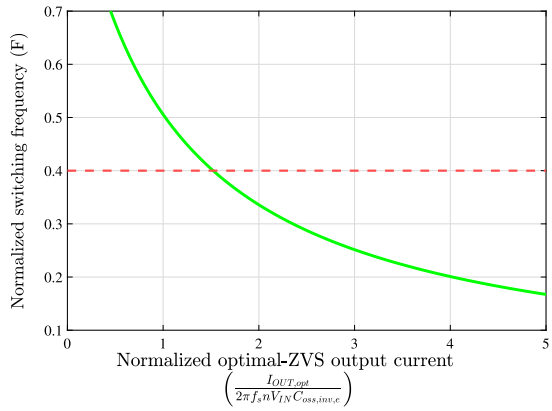


Fig. 10. Normalized switching frequency of the DAB converter as a function of its normalized output current, for an optimal-ZVS design.

An alternative expression for this frequency ratio can be obtained by rearranging (6) as

$$F = \frac{1}{\frac{3+\pi}{2\pi} + \frac{I_{\text{OUT,opt}}}{2\pi f_s n V_{\text{IN}} C_{\text{oss,inv},e}}}. \tag{9}$$

Fig. 10 shows how the choice of the optimal-ZVS output current $I_{\text{OUT,opt}}$ impacts the frequency ratio F. As can be seen, in order to limit the frequency ratio below a practical value (for example, $F = 0.4$, which, from (5) and (8), corresponds to the resonant transition period $t_{r,\text{opt}}$ taking up one-tenth of the switching period), $I_{\text{OUT,opt}}$ needs to be higher than a certain value. Note that $I_{\text{OUT,opt}}$ is normalized in Fig. 10 with respect to the product of the angular switching frequency, transformer turns ratio, input voltage, and inverter output capacitance. Therefore, once these parameters are determined, Fig. 10 can be used to determine a feasible range for $I_{\text{OUT,opt}}$. A loss model can, then, be utilized to determine the value of $I_{\text{OUT,opt}}$ within this range that produces a satisfactory efficiency profile over the converter's load range.

In the optimal-ZVS design given by (6) and (7), the rms value of the DAB tank current can be expressed as

$$I_{Ll,\text{rms,opt}} = I_{Ll,\text{pk,opt}}\sqrt{1-\frac{\phi_{\text{opt}}}{2\pi}\left(\frac{\pi}{2}+\frac{4}{3}\right)} = \frac{I_{\text{OUT,opt}}}{n}\frac{\sqrt{1-\frac{\phi_{\text{opt}}}{2\pi}(\frac{\pi}{2}+\frac{4}{3})}}{1-\frac{\phi_{\text{opt}}}{2\pi}(3+\pi)}. \tag{10}$$

This expression is derived in Appendix A. The normalized rms current ($nI_{Ll,\text{rms,opt}}/I_{\text{OUT,opt}}$) is plotted as a function of the optimal-ZVS phase shift ϕ_{opt} in Fig. 11, where ϕ_{opt} is varied across the shown range by varying the inverter's effective output capacitance $C_{\text{oss,inv},e}$. As can be seen, the rms current increases monotonically with ϕ_{opt}. This behavior can be understood from Fig. 12, which shows the dependence of the optimal tank inductance $L_{l,\text{opt}}$ and ϕ_{opt} on $C_{\text{oss,inv},e}$, computed using (6) and (7), respectively. Fig. 12(a) shows that the optimal inductance increases monotonically with the inverter output capacitance, which is expected since a larger output capacitance demands

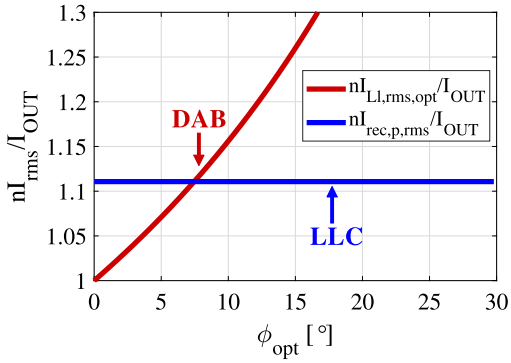
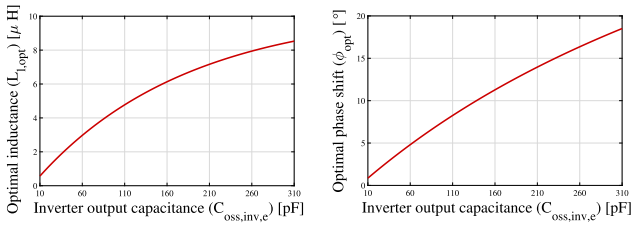


Fig. 11. ZVS-inclusive comparison of normalized rms tank currents in DAB (red) and *LLC* (blue) converters, as a function of the optimal-ZVS phase-shift (ϕ_{opt}) of the DAB converter.



(a) (b)

Fig. 12. Variation in: (a) optimal-ZVS tank inductance $L_{l,\text{opt}}$ and (b) optimal-ZVS phase shift (ϕ_{opt}) with the effective inverter output capacitance $C_{\text{oss,inv},e}$ of the DAB converter, for $f_s = 1$ MHz, $V_{\text{IN}} = 400$ V, $n = 10$, and $I_{\text{OUT,opt}} = 16.5$ A.

greater energy (and hence, larger inductance) to be discharged. Fig. 12(b) shows that the optimal phase-shift also increases monotonically with the inverter output capacitance. This is because, the larger the output capacitance, the larger the required tank inductance, and in turn, the longer the time (and hence, the larger the phase-shift) needed to ramp the tank current up to its peak value. From this it is clear that increasing ϕ_{opt} in Fig. 11 is equivalent to increasing $C_{\text{oss,inv},e}$, which increases the current required to achieve ZVS, and hence, the tank rms current.

B. LLC Converter

ZVS transitions in the *LLC* converter are fundamentally different from those in the DAB converter, because ZVS is facilitated not by the tank inductance but rather by the transformer's magnetizing inductance. Due to the square-wave voltage imposed on the transformer, the magnetizing current (i_{LM}) takes a triangular shape, with a peak value given by [22], [39]:

$$I_{LM,\text{pk}} = \frac{V_{\text{IN}}}{8L_M f_s}. \tag{11}$$

Since the magnetizing inductance is relatively large, the magnetizing current can be assumed to be constant at the abovementioned peak value during the inverter and rectifier commutation transitions, which happen simultaneously. During these transitions the peak magnetizing current discharges the effective output capacitances of the inverter and the rectifier. The magnetizing inductance required to achieve ZVS can be expressed as [11]

$$L_M = \frac{t_{\text{ZVS}}}{16 f_s (C_{\text{oss,inv},q} + \frac{C_{\text{oss,rec},q}}{n^2})}. \tag{12}$$

Here $C_{\text{oss,inv},q}$ and $C_{\text{oss,rec},q}$ are the effective output capacitances of the inverter and rectifier, respectively, including the charge-equivalent output capacitance of the devices and other parasitic capacitances; and t_{ZVS} is the total time duration over which the inverter and rectifier ZVS transitions take place. Note that since the current discharging the capacitances is assumed to be constant, charge-equivalent capacitances are relevant for the *LLC* converter, as opposed to the DAB converter, where energy-equivalent capacitances are relevant [43]. The *LLC* magnetizing inductance can be determined from (12) after selecting a reasonable value for the ZVS duration t_{ZVS}. *Prima facie*, it appears that by selecting a large value for t_{ZVS}, one can have a larger magnetizing inductance, and hence, relatively low magnetizing current and associated losses. However, if t_{ZVS} is too large, the magnetizing current is no longer constant during the ZVS transition, and in some cases ZVS may even be lost, as will be shown in Section VI. Furthermore, as in the DAB converter, efficiency considerations dictate that the ZVS duration in the *LLC* converter should also be a small fraction of the switching period [11].

With the ZVS duration and magnetizing inductance appropriately selected from (12), the *LLC* converter can achieve ZVS across its entire load range. This is in sharp constrast to the DAB converter, which can only achieve partial soft-switching at light loads (i.e., at output current levels lower than the optimal-ZVS current $I_{\text{OUT,opt}}$).

As shown in Fig. 7, the triangular magnetizing current of the *LLC* converter is 90° phase-shifted with respect to the rectifier input current, which is assumed to be sinusoidal. The rms value of the *LLC* tank current, which is the sum of the magnetizing current and the primary-reflected rectifier input current, is given by

$$I_{Lr,\text{rms}} = \sqrt{\frac{\pi^2}{8n^2} I_{\text{OUT}}^2 + \frac{I_{LM,\text{pk}}^2}{3}} = \sqrt{\frac{\pi^2}{8n^2} I_{\text{OUT}}^2 + \frac{V_{\text{IN}}^2}{192 L_M^2 f_s^2}}. \tag{13}$$

C. Comparison

Since the magnetizing current is independent of the converter's output current, the *LLC* tank rms current cannot be normalized with respect to the output current. However, a conservative comparison with the DAB converter can still be performed by neglecting the *LLC* magnetizing current and normalizing the remaining portion of the *LLC* tank current [i.e., (13) with $I_{LM,\text{pk}}$ set to zero, which reduces to (4)]. This comparison is shown in Fig. 11. As a reminder, the x-axis of Fig. 11—the DAB optimal phase shift—is a monotonically increasing function of the inverter output capacitance; hence, Fig. 11 indicates that for inverter output capacitances that allow the DAB optimal phase-shift to be small ($<7°$), the DAB tank has lower rms current than the *LLC* tank. Also note that with the *LLC* magnetizing

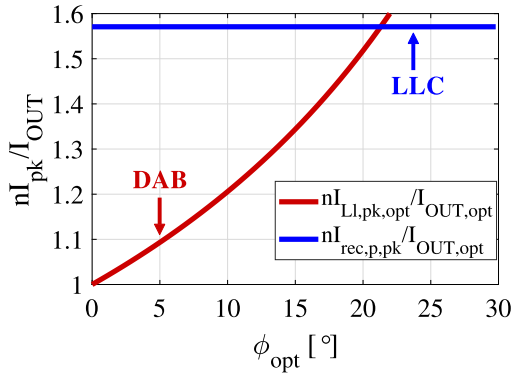


Fig. 13. ZVS-inclusive comparison of normalized peak tank currents in DAB (red) and *LLC* (blue) converters as a function of the optimal-ZVS phase-shift (ϕ_{opt}) of the DAB converter.

current included, the DAB tank will have lower rms current up to a higher phase-shift.

A similar comparison of normalized peak tank currents is shown in Fig. 13, wherein the peak current expressions for the DAB and *LLC* converters are taken from (10) and (4), respectively. It can be seen from Fig. 13 that the DAB converter has much lower peak tank currents for a large range of optimal phase-shifts. Note that this comparison assumes that the *LLC* magnetizing current is small enough not to change the peak tank current. If the magnetizing current does increase the *LLC* peak current (as it can in many designs), the comparison in Fig. 13 will become more favorable for the DAB converter.

The abovementioned ZVS-inclusive comparison of rms and peak tank currents further supports the conclusion that for a DCX application, low phase-shift designs of the DAB converter have lower conduction losses and inductor core losses than the *LLC* converter. However, the DAB converter has higher switching losses at output currents below the optimal-ZVS current. Hence, the DAB converter is expected to have higher efficiency than the *LLC* converter for medium to heavy loads, where conduction and inductor core losses typically dominate, and lower efficiency for lighter loads, where switching losses are the major loss contributors. This prediction will be experimentally validated in Section VI.

It should be noted that several strategies have been proposed to improve the light-load efficiency of the DAB converter by extending its ZVS range. In one such approach, an air gap is inserted in the DAB transformer and its magnetizing inductance is utilized for ZVS, similar to the *LLC* converter [44], [45]. Such approaches can be beneficial, provided their additional circulating currents do not outweigh the above-outlined conduction and inductor core loss benefits of the DAB converter.

V. Design Examples

In this section, the methodology of Section IV is used to design DAB and *LLC* converters for a large-step-down isolated DCX application, whose specifications are summarized in Table II. These specifications are suitable for the dc–dc stage of laptop adapters and LED TV backlight drivers. An overall step-down

TABLE II
Large-Step-Down DCX Design Specifications

Input Voltage (V_{IN})	400 V
Output Voltage (V_{OUT})	20 V
Rated Output Power (P_{OUT})	330 W
Rated Load Current (I_{OUT})	16.5 A
Switching frequency (f_s)	1 MHz

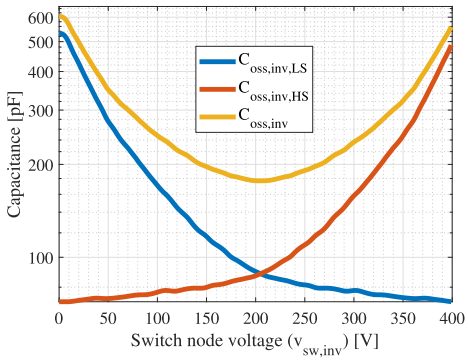


Fig. 14. Voltage dependent nonlinear switch node capacitance ($C_{\text{oss,inv}}$) of the low-side and high-side LMG3410R070 GaN devices ($C_{\text{oss,inv,LS}}$ and $C_{\text{oss,inv,HS}}$), and the sum of the two capacitances ($C_{\text{oss,inv}}$).

of 20:1 is required, out of which 2:1 step-down is provided by the half-bridge inverter, and the remaining 10:1 step-down is provided by the transformer. The designs developed here also form the basis for the prototypes shown in Section VI. The switching frequency is selected to be 1 MHz in order for these prototypes to achieve high power density.

A. DAB Design Example

The first step in designing the DAB converter is to accurately estimate the effective output capacitance seen at the inverter switch-node ($C_{\text{oss,inv},e}$). For simplicity, it is assumed that this capacitance mainly comprises the output capacitance of the inverter devices. The inverter is constructed from Texas Instruments' LMG3410R070 600-V 70-mΩ GaN devices, the nonlinear (voltage-dependent) capacitance of which is illustrated in Fig. 14. The capacitance $C_{\text{oss,inv}}$ in Fig. 14 is the sum of the nonlinear output capacitances of the high-side and low-side devices ($C_{\text{oss,inv,HS}}$ and $C_{\text{oss,inv,LS}}$, respectively). The effective "energy-equivalent" linear output capacitance of the inverter, which is used in the DAB design equations of Section IV, can be expressed in terms of $C_{\text{oss,inv}}$ as [43], [46]

$$C_{\text{oss,inv},e} = \frac{2}{V_{\text{IN}}^2}\int_0^{V_{\text{IN}}} C_{\text{oss,inv}}(v_{\text{sw,inv}})v_{\text{sw,inv}}dv_{\text{sw,inv}} = \frac{2}{V_{\text{IN}}}\int_0^{V_{\text{IN}}} C_{\text{oss,inv,LS}}(v_{\text{sw,inv}})dv_{\text{sw,inv}}. \quad (14)$$

Using (14) and the data from Fig. 14, with $V_{\text{IN}} = 400$ V, the effective output capacitance $C_{\text{oss,inv},e}$ for the LMG3410R070-based inverter is estimated to be ∼275 pF.

The second step is to select the optimal-ZVS output current $I_{\text{OUT,opt}}$. As discussed in Section IV, a feasible range for $I_{\text{OUT,opt}}$ can be determined using (9). With F smaller than 0.4 (which

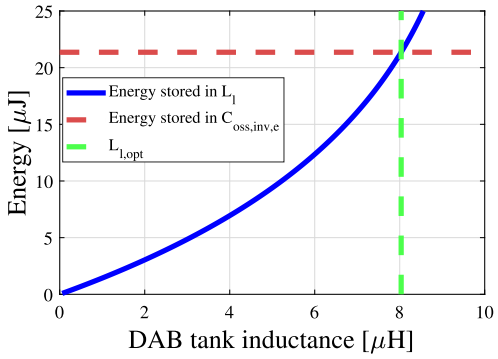


Fig. 15. Energy stored in the DAB tank inductor at the low-side and high-side device turn-OFF instants, as a function of its inductance, for $f_s = 1$ MHz, $V_{\text{IN}} = 400$ V, $n = 10$, $I_{\text{OUT,opt}} = 16.5$ A, and $C_{\text{oss,inv},e} = 275$ pF.

corresponds to the resonant transition period being less than one-tenth of the switching period), and with $f_s = 1$ MHz, $n = 10$, $V_{\text{IN}} = 400$ V, and $C_{\text{oss,inv},e} = 275$ pF, (9) requires $I_{\text{OUT,opt}}$ to be larger than 10.5 A. In this design example, $I_{\text{OUT,opt}}$ is selected to be equal to the rated load current of 16.5 A. The motivation here is to maximize efficiency by achieving optimal ZVS at rated load, where the converter in the applications considered here needs to operate most efficiently due to thermal constraints. A lower value of $I_{\text{OUT,opt}}$ would still ensure ZVS at rated load, but at the cost of higher circulating currents, and hence, lower efficiency. The third step is to determine the DAB tank inductance required for optimal ZVS, $L_{l,\text{opt}}$, which is obtained from (6) to be 8 μH. The optimality of $L_{l,\text{opt}}$ is visualized for this design example in Fig. 15, which shows that with an inductance of 8 μH, the tank inductor carries just enough energy at the beginning of the dead time to fully discharge the effective inverter output capacitance $C_{\text{oss,inv},e}$. The time required for this optimal ZVS transition is $t_{r,\text{opt}} = 74$ ns; to minimize reverse conduction, the DAB dead time is kept close to this value. Next, the phase-shift associated with this design is obtained from (7) to be $\phi_{\text{opt}} = 16.7°$. The above-described ZVS-oriented methodology for the DAB converter is illustrated by means of a flowchart in Fig. 16(a).

Finally, the rectifier is constructed from EPC2023 30-V, 1.5-mΩ GaN devices. Due to their low ON-resistance, these devices facilitate low conduction losses on the high-current side of the converter. Furthermore, achieving ZVS of these devices is straightforward and almost instantaneous due to the relatively low output voltage.

Design examples for the *LLC* converter are presented next, following which, transformer designs for both converters will be discussed and subsequently the converter designs compared.

B. LLC Design Examples

Following the methodology of Section IV, the *LLC* converter's design begins by selecting a ZVS duration t_{ZVS} (i.e., the dead time), from which the magnetizing inductance L_M can be determined using (12). To illustrate the tradeoffs involved, two designs are pursued, one with t_{ZVS} larger than, and the other smaller than, one-tenth of the switching period. For the

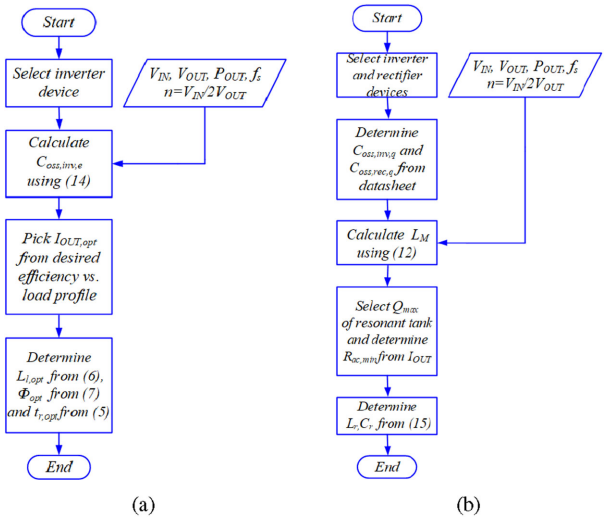


Fig. 16. Flowchart illustrating ZVS-oriented design methodology. (a) DAB converter. (b) *LLC* converter.

first design ($t_{\text{ZVS}} = 150$ ns), the magnetizing inductance L_M comes to be 30 μH, and for the second design ($t_{\text{ZVS}} = 80$ ns), L_M comes out to be 16 μH. Hereafter, these designs are referred to as the high-L_M design and the low-L_M design, respectively. The high-L_M design features low magnetizing current, resulting in lower conduction losses, and also requires a smaller air-gap, resulting in lower fringing-field induced losses. However, the low magnetizing current necessitates a longer ZVS transition, during which negligible output power is supplied.

The next step is to determine the resonant tank elements L_r and C_r, by selecting the maximum loaded quality factor of the tank, given by [11], [39]

$$Q_{\text{max}} = \frac{1}{2\pi f_s C_r R_{\text{ac,min}}}$$
$$f_p = \frac{1}{2\pi\sqrt{(L_M + L_r)C_r}}; f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (15)$$

Here, $R_{\text{ac,min}} = \frac{8n^2 V_{\text{OUT}}}{\pi^2 I_{\text{OUT}}}$ is the effective resistance presented by the rectifier at rated load. Similar to the high-L_M and low-L_M designs demonstrated previously, high-Q and low-Q designs are also performed. For the high-Q design ($Q_{\text{max}} = 0.24$), $L_r = 4$ μH and $C_r = 8$ nF; and for the low-Q design ($Q_{\text{max}} = 0.06$), $L_r = 1$ μH, and $C_r = 28$ nF. One benefit of the high-Q design is that it reduces the frequency variation required for regulation [47]. Another benefit is that it results in a fairly sinusoidal tank current with relatively low peak and rms values. However, the high-Q design requires a relatively large tank inductance, which can offset these benefits and lead to higher losses. Hence, to compensate, the high-Q design is paired with the lower peak magnetizing current high-L_M design. Similarly, the low-Q design ($Q_{\text{max}} = 0.06$) is paired with the higher peak magnetizing current low-L_M design. This design methodology of the *LLC* converter is visualised using a flowchart in Fig. 16(b).

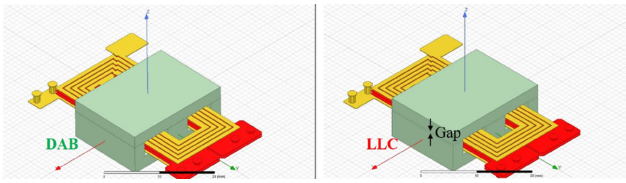


Fig. 17. HFSS models (isometric view) of the ungapped DAB transformer (left) and the gapped *LLC* transformer (right). Apart from the gap, the transformers are identical in construction.

TABLE III
10:1 TRANSFORMER DESIGN DETAILS

PCB stackup	4 layers, 3 oz.
Windings	10 primary turns (layer 1; 1-5 turns, layer 4; 6-10 turns), 1 secondary turn (paralleled in layer 2 and 3)
Core Geometry	EILP 22 (22 X 16 X 8.5)
Core material	TDK N49
Length of Airgap	DAB : 0 mm High L_M, high-Q LLC : 0.18 mm Low L_M, low-Q LLC : 0.4 mm

TABLE IV
DESIGN SUMMARY

Topology	Design of tank	Dead time interval (ns)	Tank Currents (Amps)
DAB	$L_{l,opt}$=8 μH	$t_{d,DAB}$= $t_{r,opt}$=74	$I_{Ll,rms,opt}$=2.13, $I_{Ll,pk,opt}$=2.3
High-L_M, high-Q LLC	L_r=4 μH, C_r=8 nF, L_M= 30 μH	$t_{d,LLC}$= t_{ZVS}=150	$I_{rec,p,rms}$=1.83, $I_{LM,pk}$=1.67, $I_{Lr,rms}$=2.07, $I_{Lr,pk}$=2.9
Low-L_M, low-Q LLC	L_r=1 μH, C_r=28 nF, L_M=16 μH	$t_{d,LLC}$= t_{ZVS}=80	$I_{rec,p,rms}$=1.83, $I_{LM,pk}$=3.12, $I_{Lr,rms}$=2.57, $I_{Lr,pk}$=3.63

C. Transformer Designs

To increase power density, the 10:1 transformers of the DAB and *LLC* converters are implemented as planar structures with PCB-integrated windings. These transformers are modeled using 3-D finite-element analysis in Ansys HFSS, as shown in Fig. 17. The DAB transformer is designed with no air-gap, while the air gaps in the two *LLC* designs are tuned in HFSS to obtain the required magnetizing inductances. Windings losses are estimated using the frequency-dependent impedance matrices extracted from HFSS [48], and core losses are estimated using improved generalized Steinmetz equation (iGSE) [49] (more details are provided in Appendix B). Details of the transformer constructions are provided and design is described in Table III. With these designs, the transformers achieve a power density of 1800 W/in^3.

D. Design Summary

The DAB and *LLC* designs are summarized in Table IV. In line with the theoretical predictions of Section IV, the DAB converter has lower rms and peak currents than both *LLC* designs. Another distinction between the DAB and *LLC* designs brought out by Table IV is that, although the ZVS-facilitating current in the low-Q *LLC* design (i.e., the peak magnetizing current) is higher than its counterpart (the peak tank current) in the DAB design, the low-Q *LLC* design needs a longer ZVS transition period (or dead time). This is because unlike in the DAB converter where the peak tank current discharges the inverter and rectifier output capacitances at different times, in the *LLC* converter the magnetizing current has to discharge the inverter and rectifier capacitances at the same time, resulting in a longer transition period. The following section describes the prototypes implemented from the designs developed previously, and compares their measured performance.

TABLE V
400–20 V, ISOLATED 330-W PROTOTYPE DETAILS

High voltage inverter (Q_1 and Q_2)	Texas Instruments' LMG3410R070 EVM daughter card
Low voltage devices (Q_3-Q_6)	EPC 2023, 30 V, 1.45 mΩ
Low voltage half bridge gate driver	Texas Instruments' LMG1210
Microcontroller (PWM signals)	TMS320F28379D

VI. EXPERIMENTAL RESULTS

A DAB converter prototype and two *LLC* converter prototypes conforming to the design examples of Section V are built and tested for a DCX application with 400-V input voltage, 20-V output voltage, and 330-W rated output power. The components common to all three prototypes are listed in Table V. The following sections present the measured results.

A. DAB Results

A photograph of the DAB converter prototype is shown in Fig. 18(a). Fig. 18(b) shows the planar transformer with the secondary-side PCB interconnects made from loops of multistrand wire. These loops realize most of the DAB tank inductance. Note that the DAB inductor is realized on the transformer's secondary side (which can be done due to the large magnetizing inductance). Hence, the required inductance is only $L_{l,\text{opt}}/n^2 = 80$ nH, about 70 nH of which comes from the loops, and the remaining portion from the leakage inductance of the transformer.

Measured switch-node voltages and tank current waveforms of the DAB converter while delivering its rated power of 330 W are shown in Fig. 19. The ZVS transition period and phase-shift are labeled. It can be seen that the inverter achieves near-optimal ZVS, since the tank current approaches zero at the time instant when the inverter switch-node voltage completes its transition; hence, minimizing circulating currents. This validates the optimal-ZVS design methodology of Section IV. The rectifier switch-node voltage in Fig. 19 exhibits substantial ringing. This is because although the energy in the tank inductor is just enough for achieving inverter ZVS, it is much higher than that required for rectifier ZVS. This results in residual energy being stored in the rectifier power loop parasitic inductances, causing high-frequency ringing after the rectifier commutates. This ringing has detrimental effects on electromagnetic interference, efficiency, and reliability, and can be reduced using an optimized PCB layout, lower package-inductance devices,

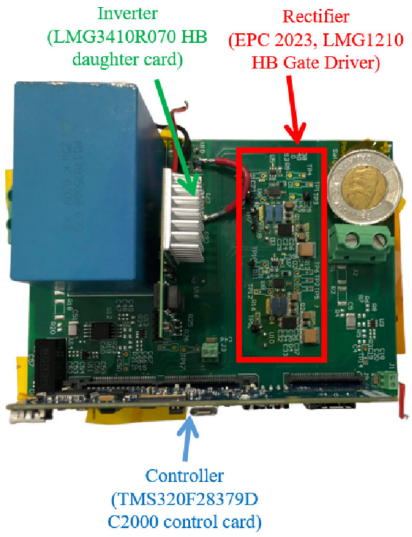


Fig. 18. Photographs of the DAB converter prototype. (a) Power stage. (b) Planar transformer.

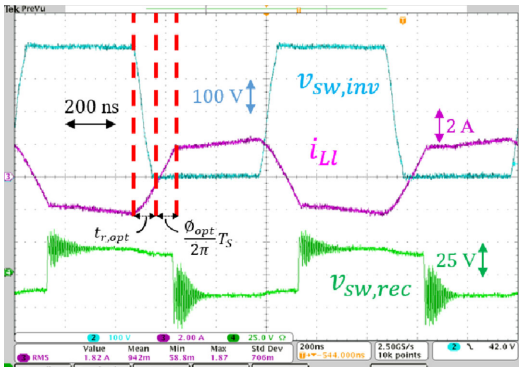


Fig. 19. Measured switch-node voltages and tank current of the DAB converter prototype operating at its rated power of 330 W.

and/or modulation schemes that reduce the rectifier turn-OFF current [21], [50].

Fig. 20 shows the measured efficiency of the DAB converter prototype for four different loads. When operating at full load (330 W), the phase-shift is maintained at ϕ_{opt}, and is reduced as the load decreases to keep the output voltage regulated at 20 V. As expected, the converter achieves its maximum efficiency of

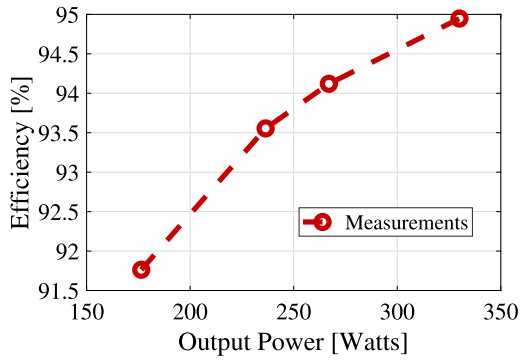


Fig. 20. Measured efficiency of the DAB converter prototype.

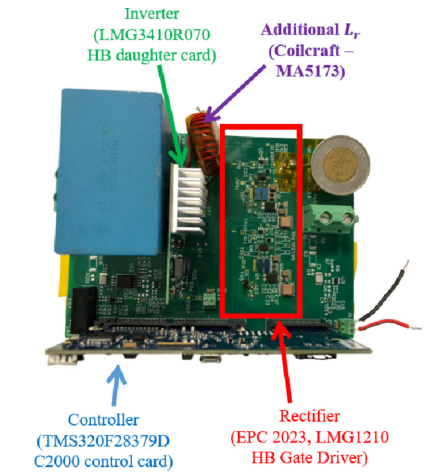
94.9% at full load, where it achieves optimal inverter ZVS. At lighter loads, partial soft-switching leads to reduced efficiencies. This efficiency profile is well-suited for laptop adapter and backlight driver applications, wherein full-load operation is most prevalent, and hence, due to thermal considerations, the associated efficiency is prioritized. Furthermore, in these applications the converter can be operated in burst mode to maintain flatter efficiency across load variation. For applications where burst-mode operation is unsuitable and light-load efficiency is of greater importance, the value of the optimal-ZVS output current $I_{\text{OUT,opt}}$ can be selected to be lower than the rated output current, as discussed in Section IV.

B. LLC Results

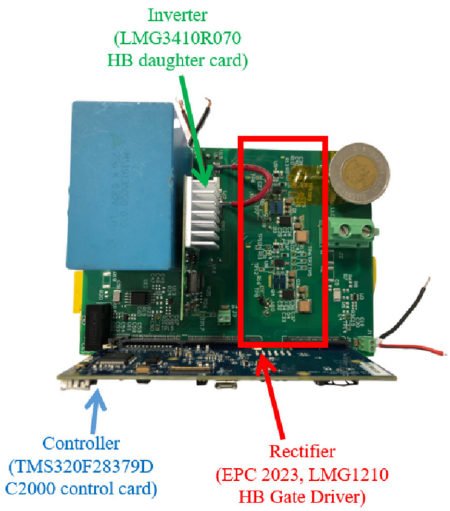
Photographs of the high-Q and low-Q *LLC* converter prototypes are shown in Fig. 21(a) and (b), respectively. As can be seen, the high-Q prototype utilizes a discrete off-the-shelf inductor (Coilcraft MA5173). This inductor realizes three quarters of the required tank inductance, and the remaining portion is realized from the leakage inductance of the transformer. In the low-Q prototype, the entire tank inductance comes from the transformer's leakage inductance, which is advantageous in terms of both efficiency and cost. The transformer used in both the high-Q and low-Q prototypes is shown in Fig. 21(c).

Fig. 22 shows measured waveforms of the switch-node voltages and tank current of the high-Q prototype. It can be seen that despite a substantial dead-time (140 ns), the inverter is only able to achieve partial soft-switching. This is because the magnetizing current falls due to resonance between the magnetizing inductance and the inverter and rectifier switch-node capacitances, and hence, does not have sufficient energy to fully discharge the inverter capacitance, as mentioned in Section IV-B. The corresponding waveforms for the low-Q design are shown in Fig. 23. Here, the inverter is able to achieve ZVS, since the lower magnetizing inductance allows the magnetizing current at the beginning of the resonant transition (i.e., the peak magnetizing current) to be higher. The higher magnetizing current is also evident from the tank current assuming a more triangular shape.

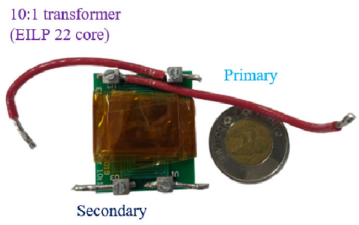
Fig. 24 shows the measured efficiencies of the high-Q and low-Q prototypes. As can be seen, the low-Q prototype maintains a higher and flatter efficiency across the load range, with



(a)



(b)



(c)

Fig. 21. Photographs of the *LLC* converter prototypes. (a) Power stage of high-Q prototype. (b) Power stage of low-Q prototype. (c) Planar transformer used in both prototypes.

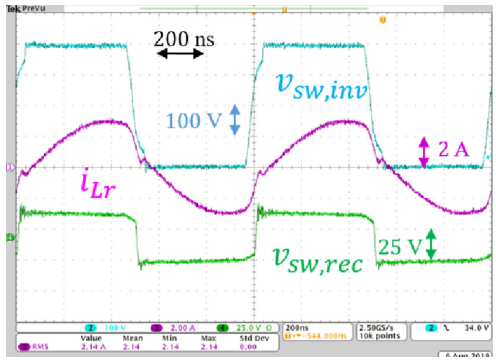


Fig. 22. Measured switch-node voltages and tank current of the high-Q *LLC* converter prototype operating at its rated power of 330 W.

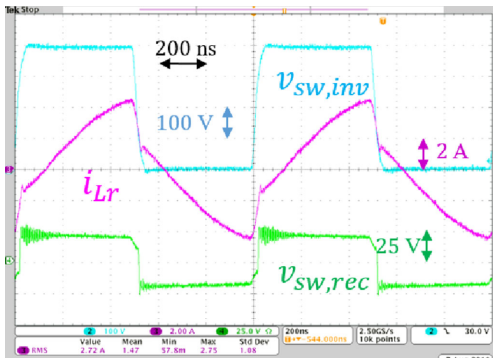


Fig. 23. Measured switch-node voltages and tank current of the low-Q *LLC* converter prototype operating at its rated power of 330 W.

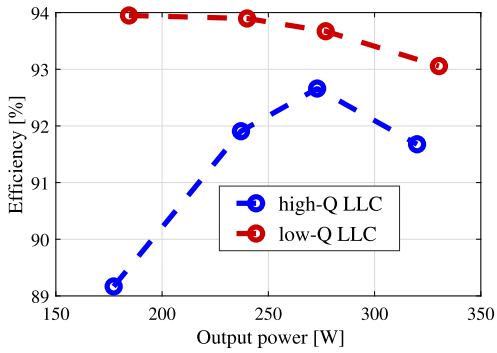


Fig. 24. Measured efficiency of high-L_m, high-Q (blue) and low-L_m, low-Q (red) *LLC* converter prototypes.

substantial benefits at light load. This is due to the high-Q converter suffering from partial soft-switching and core losses in its additional discrete inductor L_r.

C. Comparison

Measured efficiencies of the DAB and low-Q *LLC* prototypes are compared in Fig. 25. As was predicted in Section IV, the DAB converter achieves higher efficiency at full load, while the low-Q *LLC* converter achieves higher efficiency at lighter loads. At full load (330 W) the DAB converter achieves 94.9% efficiency, while the *LLC* converter achieves 93.1% efficiency. This translates to a 27% reduction is losses, and hence, a substantial reduction in thermal management size and cost. It was mentioned in Section IV that the DAB converter suffers from lower efficiency at lighter loads (i.e., at output currents lower than $I_{\mathrm{OUT,opt}}$) due to loss of ZVS, while the *LLC* converter can maintain ZVS across the load range. This is also experimentally validated in Fig. 26. Finally, loss breakdowns of the

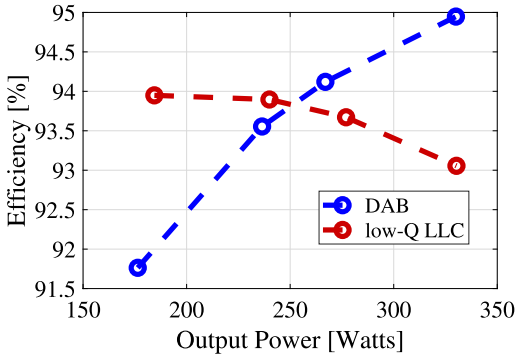
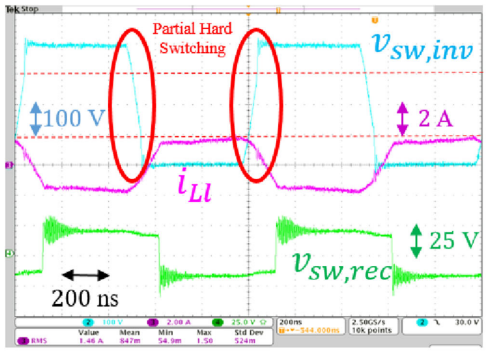
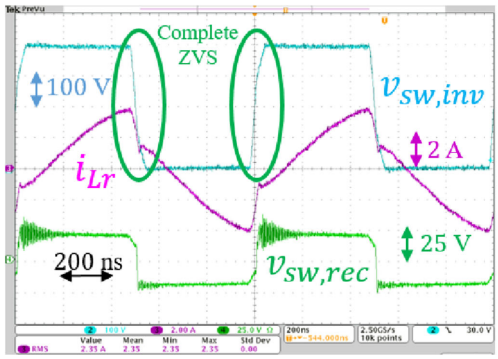


Fig. 25. Comparison of the measured efficiencies of the DAB and low-Q *LLC* converter prototypes.



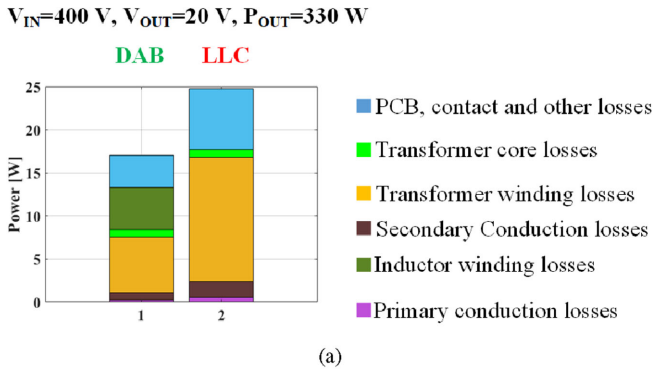
(a)



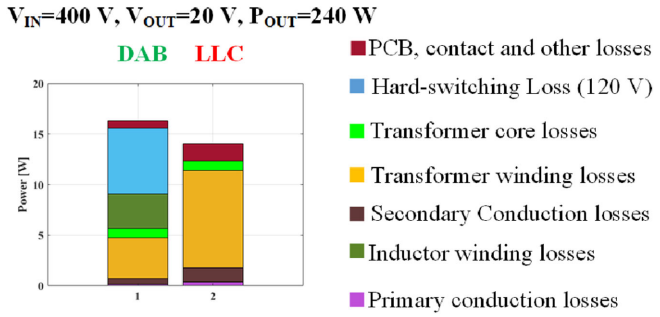
(b)

Fig. 26. Measured switch-node voltages and tank current. (a) DAB converter. (b) Low-Q *LLC* converter prototypes, with both prototypes operating at a partial power level of 240 W.

DAB and low-Q *LLC* prototypes at full load and at a lighter load are shown in Fig. 27(a) and (b), respectively; reinforcing the conclusion that at full load the DAB losses are lower due to lower conduction and winding losses, while at partial load, the *LLC* losses are lower due to partial hard-switching losses in the DAB converter. It should be noted here that since the DAB tank current is trapezoidal with part-linear, part-sinusoidal transitions, its harmonic content is substantial. Therefore, the DAB winding losses shown in Fig. 27 include the impact of higher order harmonics, as discussed in Appendix B.



(a)



(b)

Fig. 27. Loss breakdown comparisons of the DAB and low-Q *LLC* converter prototypes, when operating at (a) rated power (330 W) and (b) partial power (240 W).

VII. Conclusion

This article presents a fundamental comparison of two popular converter topologies—the DAB and the *LLC*—when employed in a high-step-down DCX application. It is shown that despite structural similarities, the two converters differ greatly in function, particularly with regard to their tank currents and ZVS operation. These differences lead to differing tradeoffs between conduction and switching losses, as a result of which the DAB converter outperforms the *LLC* converter at heavy loads, and vice versa at lighter loads. The comparison is first performed analytically using a ZVS-focused design methodology for the two converters, then numerically reinforced with design examples, and finally experimentally validated in a 400-V input, 20-V output, 330-W application. The DAB converter prototype is shown to achieve a peak efficiency of 94.9% at full load, translating to a 27% loss reduction compared to the *LLC* converter prototype. Based on these results, the DAB converter is the preferred solution for high-step-down DCX applications where heavy-load operation is prioritized.

Appendix A
Design Equations for Optimal-ZVS Design of DAB Converter

This appendix derives expressions for the tank inductance, maximum phase-shift and rms tank current in optimal-ZVS design of the DAB converter, given in (6), (7), and (10), respectively. The DAB tank current waveform corresponds to the

optimal-ZVS operation shown in Fig. 9. During each half of the switching period, this waveform can be decomposed into two linear segments and one sinusoidal segment, given by

$$i_{Ll}(t) = \begin{cases} -I_{Ll,\text{pk,opt}} \cos(2\pi f_{\text{res}} t), & 0 \le t \le t_{r,\text{opt}} \\ \dfrac{I_{Ll,\text{pk,opt}} 2\pi f_s}{\phi_{\text{opt}}}(t - t_{r,\text{opt}}), & t_{r,\text{opt}} \le t \le t_{r,\text{opt}} + \dfrac{\phi_{\text{opt}}}{2\pi f_s} \\ I_{Ll,\text{pk,opt}}, & t_{r,\text{opt}} + \dfrac{\phi_{\text{opt}}}{2\pi f_s} \le t \le \dfrac{T_s}{2} \end{cases} \tag{16}$$

where the peak tank current $I_{Ll,\text{pk,opt}}$ can be related to the input voltage, the tank inductance, and the phase-shift as

$$I_{Ll,\text{pk,opt}} = \frac{V_{\text{IN}} \phi_{\text{opt}}}{2\pi f_s L_l}. \tag{17}$$

Equating the primary-referred average output current to the switching-period average of (16) gives

$$\frac{I_{\text{OUT,opt}}}{n} = \frac{V_{\text{IN}} \phi_{\text{opt}}}{2\pi f_s L_l} \left(1 - \frac{2t_{r,\text{opt}}}{T_s}\left(1 + \frac{2}{\pi}\right) - \frac{\phi_{\text{opt}}}{2\pi}\right) \tag{18}$$

To facilitate optimal ZVS, the stored energy in the inductor at the beginning of the resonant transition needs to be equal to the energy of the energy stored in the effective inverter output capacitance $C_{\text{oss,inv},e}$, i.e.,

$$\frac{1}{2} L_{l,\text{opt}} I_{\text{pk}}^2 = \frac{1}{2} C_{\text{oss,inv},e} V_{\text{IN}}^2. \tag{19}$$

Equations (17)–(19) can be solved to obtain (6) and (7).

The rms tank current in an optimal-ZVS DAB design can be found using (16) as

$$I_{Ll,\text{rms,opt}} = I_{Ll,\text{pk,opt}} \sqrt{\left(1 - t_{r,\text{opt}} f_s - \frac{2\phi_{\text{opt}}}{3\pi}\right)}. \tag{20}$$

Substituting $t_{r,\text{opt}} = \phi_{\text{opt}}/4f_s$ in (20) and simplifying it using (17) and (18) produces

$$\frac{\dfrac{I_{Ll,\text{rms,opt}}}{I_{\text{OUT,opt}}}}{n} = \frac{\sqrt{1 - \frac{\phi_{\text{opt}}}{2\pi}\left(\frac{\pi}{2} + \frac{4}{3}\right)}}{1 - \frac{\phi_{\text{opt}}}{2\pi}(3 + \pi)}. \tag{21}$$

APPENDIX B
LOSS MODELING OF TRANSFORMER

This appendix provides the loss models used to estimate winding and core losses in the high frequency transformers of the DAB and *LLC* converter prototypes.

A. Winding Losses

The transformer models shown in Fig. 17 are simulated in Ansys HFSS, and their frequency-dependent impedance matrices are obtained in the form [48]

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} R_{11}(\omega) + j\omega L_{11} & R_{12}(\omega) + j\omega L_{12} \\ R_{12}(\omega) + j\omega L_{12} & R_{22}(\omega) + j\omega L_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{22}$$

where ω is the angular frequency corresponding to each harmonic of interest. The winding losses can then be computed as [48]

$$P_{\text{winding}} = I_{\text{rms}}^2(\omega) \left(R_{11}(\omega) - 2\sqrt{\frac{L_{11}}{L_{22}}} R_{12}(\omega) + \frac{L_{11}}{L_{22}} R_{22}(\omega)\right) \tag{23}$$

where $I_{\text{rms}}(\omega)$ is the rms value of the harmonic component. For the DAB converter this computation is performed up to the seventh harmonic of the switching frequency, and all the harmonic contributions are added together. For the *LLC* converter only the fundamental harmonic is considered, since the *LLC* tank current is predominantly sinusoidal.

B. Core Losses

Core losses are modeled using the iGSE [49]. The volt-seconds of the transformer are determined by a square wave of amplitude V_{OUT} applied across the transformer secondary, for both the DAB and *LLC* converters. The Steinmetz parameters of the core material (TDK N49) are obtained by curve fitting the core loss data provided in the manufacturer's datasheet [51] as

$$k_{fe} = 1.4423 \text{ W/m}^3; \alpha = 1.445; \beta = 2.663. \tag{24}$$

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