Analytical Characterization of CM and DM Performance of Three-Phase Voltage-Source Inverters Under Various PWM Patterns

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***Abstract*—The need for analytical models and tools to investigate common-mode (CM) and differential-mode (DM) signals in motor drive systems is evident in previous literature, which focuses on simulations and experiments. In this article, an analytical model of CM voltage (CMV) for various pulsewidth modulation (PWM) schemes is presented as a double Fourier integral (DFI) and the DM current (DMI) is described by mathematical equations. The model is applied to different modulation schemes such as space vector PWM, two types of discontinuous PWM, and active zero state PWM (AZSPWM) for two-level and three-level multiphase inverters. The impact of these four modulation schemes on the CMV and DMI is comprehensively compared across varying modulation indices. The DFI model shows that while AZSPWM has the lowest CMV around the switching frequency, it has increased sideband CMV. However, it still yields the best total CMV reduction overall. An SiC inverter is built to experimentally validate the analytical model with a range of switching frequencies of 10–40 kHz. In this system, a high-resolution field-programmable gate array (FPGA) is used to implement the control algorithm and assess the impact of control bandwidth on CMV and DMI.**

***Index Terms*—Common-mode (CM) voltage, control bandwidth (CBW), double Fourier integral (DFI) analysis, field-programmable gate array (FPGA), permanent magnet synchronous motor (PMSM), SiC.**

I. Introduction

A THREE-PHASE voltage source inverter (VSI) is commonly used in ac motor drive systems, such as electric vehicles (EVs) using permanent magnet synchronous motors (PMSMs) or induction motors [1]. A conventional two-level, three-phase inverter-fed motor drive system containing six switches (S_1–S_6) with two complementary switches in the same leg is shown in Fig. 1. The motor case and the middle point of the dc-link are typically grounded to the chassis for safety [2]. Between the ac neutral point and grounding chassis, the parasitic capacitor (C_s) and the cable to ground parasitic capacitors will provide the path for the common-mode (CM) current (CMI). This will cause insulation failure, greatly shorten the motor lifespan and cause significant EMI problems. To make the situation worse, wide bandgap (WBG) devices such as SiC MOSFETs are more commonly being used in motor drive systems. Their superior switching performance results in high CM voltage (CMV) by introducing a high switching frequency (f_s) and high dv/dt [3] [4].

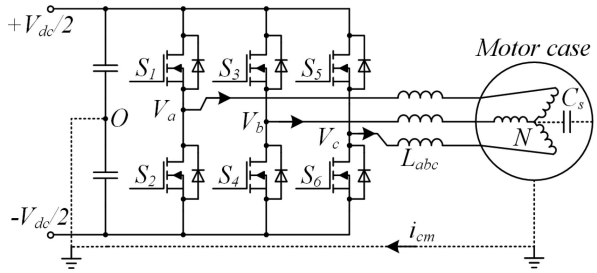

Fig. 1. Three-phase two-level VSI motor drive system.

The CMV, i.e., the potential of the ac neutral point of the load with respect to the middle-point of the dc-link, is expressed as [5]

$$V_{CM} = (V_{aO} + V_{bO} + V_{cO})/3 \tag{1}$$

V_{aO}, V_{bO}, and V_{cO} are the inverter phase voltage, i.e., the voltage difference between the leg output voltage (V_a, V_b and V_c) and the middle-point voltage potential of the dc-link V_O, as shown in Fig. 1.

Fig. 2(a) shows the three-phase gate pulses and corresponding CMV for conventional center-aligned continuous space vector pulsewidth modulation (SVPWM), with the peak of the CMV varying between $\pm V_{dc}/2$. The fast Fourier transform (FFT) of the CMV generated with SVPWM has shown that the main components of the CMV are concentrated at the switching frequency [6]. As WBG devices are perceived as the future substitute for Si devices in medium- and low-voltage applications due to their low conduction and switching losses, the high switching frequency and switching speed will amplify the CM noise, which is already significant in motor drives [7], [8]. Therefore, the

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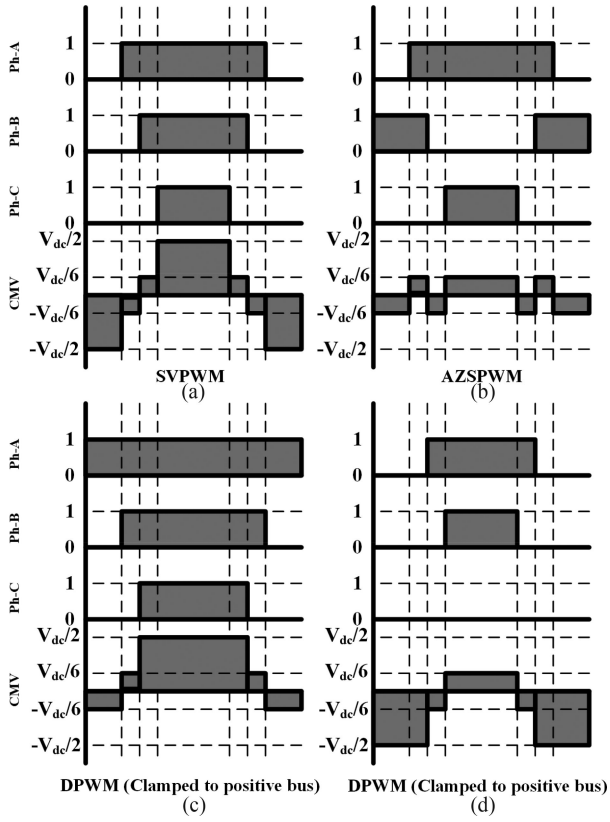

Fig. 2. Various SVM pulse pattern and corresponding CMV distribution. (a) SVPWM. (b) AZSPWM. (c) DPWM-positive bus clamping. (d) DPWM-negative bus clamping.

reduction of the CMV main components is critical in motor drive applications. To achieve this goal, either a bulky CM filter must be equipped, which offsets the merits of WBG devices by enlarging the system footprint, or other methods to reduce CMV in the modulation must be adopted such as active zero state PWM (AZSPWM) or one of two discontinuous PWM (DPWM) methods, DPWM1 and DPWMMin, illustrated in Fig. 2(b)–(d) [9]–[12].

Prior literature has empirically or experimentally shown that AZSPWM has a lower CMV than conventional SVPWM [13], but the side effects of AZSPWM have not been formulated [14] with regard to the potential CMV reduction limits caused by the increasing sideband components [15] and the higher phase current total harmonic distortion (THD) due to larger winding current ripple. Even the previous literature has observed such limit, without an analytical model it is hard to show the overall pros and cons of various PWMs, especially when their performance is highly dependent on the modulation index. An analytical model of CMV and phase-current ripple, instead of a simulation-based model, is highly demanded to optimize the performance of the overall motor drive system, which is the focus of this article.

Another trend in the EV domain is the increasing adoption of higher-resolution microcontrollers, such as field-programmable gate arrays (FPGAs). With their unique parallel computation capability, FPGAs can update the duty cycle every switching period [16], yielding a sampling or control frequency (f_c) equal to the switching frequency (f_s). This finely tunes the PWM patterns resulting in lower current THD. However, little research work has been performed on its effect on CMV reduction.

The rest of this article is organized as follows. In Sections II and III, the CMV and differential-mode (DM) current (DMI) of the four different PWM methods shown in Fig. 2 are compared to each other through theoretical analysis and simulation. Section IV gives the experimental verification of CM reduction performance with a hardware test bench consisting of a 400-V/30-kW SiC inverter switched up to 40 kHz and a resolver typed PMSM controlled by a Xilinx FPGA. Furthermore, Section V discusses how control bandwidth (CBW) affects CM and DM performance, and Section VI extends the analysis to a three-level NPC inverter. Finally, Section VII concludes the article.

II. CMV Analysis for Different PWM Patterns

As shown in Fig. 2(a), conventional center-aligned SVPWM results in the CMV with a peak of $\pm V_{dc}/2$. For AZSPWM, pulses are inversely aligned with the medium-length duty cycle of the three phases. This modulation scheme avoids the adoption of zero vectors, which reduces the peak of CMV to $\pm V_{dc}/6$. DPWM1 and DPWMMin also reduce the CMV by shaving the peak to either $+V_{dc}/2$ or $-V_{dc}/2$ in each switching cycle, as shown in Fig. 2(c) and (d). Nevertheless, all these space vector modulation (SVM) methods listed in Fig. 2 are the combination of SPWM and an injected third-order CM modulation signal [17]. The main difference between different PWM patterns lies in the corresponding CM modulation signals. Fig. 3(a)–(d) shows the modulation signal and CM modulation signal for SVPWM, DPWM1, and DPWMMin at high (0.8) and low (0.2) modulation index (M) scenarios, respectively.

Equation (2) gives the modulation index of SVM. Note that there are still some other modulation methods having the CMV reduction capability, for instance, remote-state PWM and near-state PWM (NSPWM). These two PWM schemes have limited dc-bus-voltage utilization, e.g., 0.61–0.907 for NSPWM and <0.58 for RSPWM. Therefore, these PWM methods will not be discussed here

$$M = \frac{\text{Modulation Amplitude}}{\text{Carrier Amplituder}} * \frac{2}{\sqrt{3}}. \tag{2}$$

When running at the same speed and torque, all four PWMs have the same fundamental frequency. However, their CM modulation signals result in different CMV distributions. The FFT result of the CM modulation signals, as shown in Fig. 4, indicates that DPWM will bring higher CMV in lower modulation indices. In this simulation, the fundamental frequency (f_0) was set to 50 Hz. DPWMMin draws high CMV within the frequency range of 0–3f_0 and DPWM1 draws high CMV in the frequency of $>3f_0$. This is particularly true when the modulation index is low, as validated in Fig. 7, where $M = 0.2$.

Fig. 5(a)–(d) shows the CMV spectrum of SVPWM, AZSPWM, DPWM1, and DPWMMin at high modulation index (0.8) and low modulation index (0.2) with the zoomed-in view at the switching frequency point, respectively. The fundamental frequency is 50 Hz (f_0), $f_s = 10$ kHz, and the dc-link voltage is 150 V. Several conclusions can be drawn.

1) In the low-frequency range ($<3f_0$), DPWMMin has a higher CMV than others. For the frequency of $3f_0$–f_s,

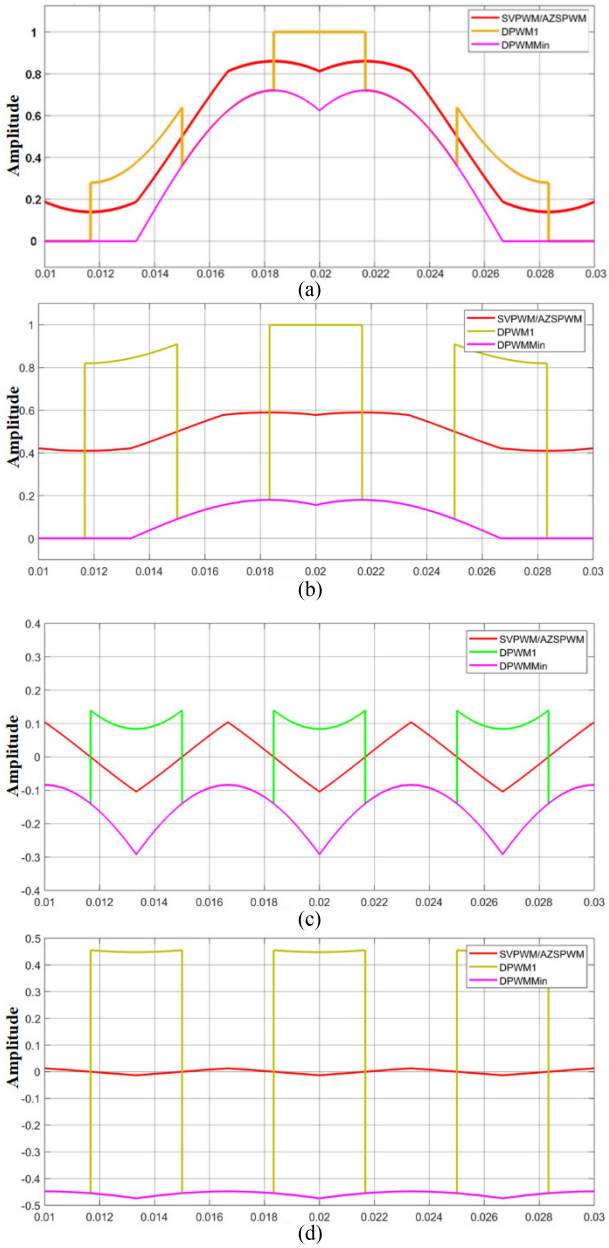

Fig. 3. Modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin (a) @M = 0.8, (b) @M = 0.2. CM modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin. (c) @M = 0.8. (d) @M = 0.2.

DPWM1 always has a higher CMV. These can be explained by FFT analysis shown in Fig. 5.

2) SVPWM and AZSPWM have almost the same performance excluding the carrier harmonics (integer numbers of f_s). At f_s, AZSPWM reduces the CMV sharply compared with SVPWM. However, the sideband near f_s for AZPWM increases, which cannot be explained by the FFT analysis shown in Fig. 6 and 7. The existence of such sideband CMV questions whether AZSPWM has the best CMV reduction.

It is essential to use a low-frequency modulation waveform to compare with a high-frequency carrier waveform in any PWM method. The phase leg outputs a series of pulses switching between upper and lower dc bus, which not only have the fundamental component but also incorporate a series of unwanted harmonics due to switching processes [18]. Double Fourier integral (DFI) analysis is a mathematical tool that can provide analytical solutions to precisely identify harmonic components of a PWM signal. In inverter applications, assume that the target function ($f(t)$) is the voltage between the middle point of the phase leg and the middle point of the dc bus. $f(t)$ is obviously a cyclic signal related to both $x(t)$ and $y(t)$ with period $= 2\pi$. Here, $x(t) = \omega_s t + \theta_s$ and $y(t) = \omega_0 t + \theta_0$, representing the time variation of the high-frequency modulating wave and low-frequency modulated wave, respectively. By doing the DFI analysis on the PWM waveform, $f(t)$ can be expanded as

$$
\begin{aligned}
&f(x,y) \\
&= \frac{A_{00}}{2} + \sum_{n=1}^{\infty} \{A_{0n}\cos[n(\omega_0 t+\theta_0)] + B_{0n}\sin[n(\omega_0 t+\theta_0)]\} \\
&\quad + \sum_{n=1}^{\infty} \{A_{m0}\cos[m(\omega_s t+\theta_s)] + B_{m0}\sin[m(\omega_s t+\theta_s)]\} \\
&\quad + \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \{A_{mn}\cos[m(\omega_s t+\theta_s) + n(\omega_0 t+\theta_0)] \\
&\quad + B_{mn}\sin[m(\omega_s t+\theta_s) + n(\omega_0 t+\theta_0)]\} \qquad (3)
\end{aligned}
$$

where m is the carrier index variable, n is the baseband index variable, and

$$
\begin{aligned}
A_{mn} &= \frac{1}{4\pi}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\cos(mx+ny)\,dxdyB_{mn} \\
&= \frac{1}{4\pi}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\sin(mx+ny)\,dxdy. \qquad (4)
\end{aligned}
$$

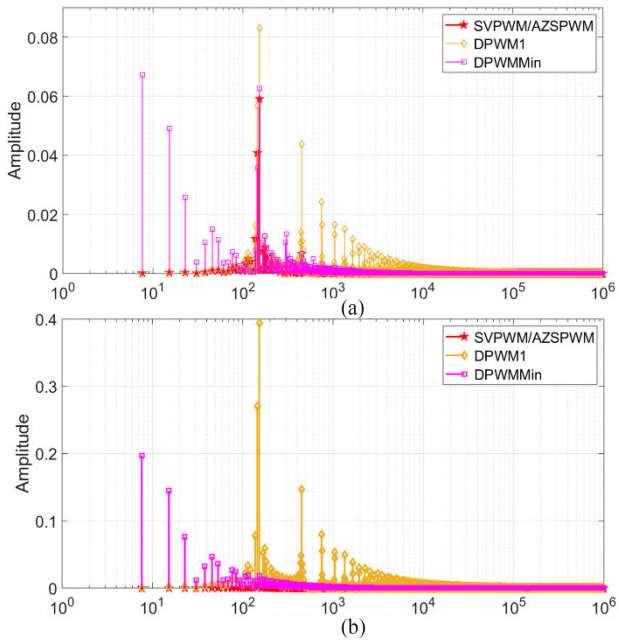

Fig. 4. FFT result for CM modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin. (a) @M = 0.8. (b) @M = 0.2.

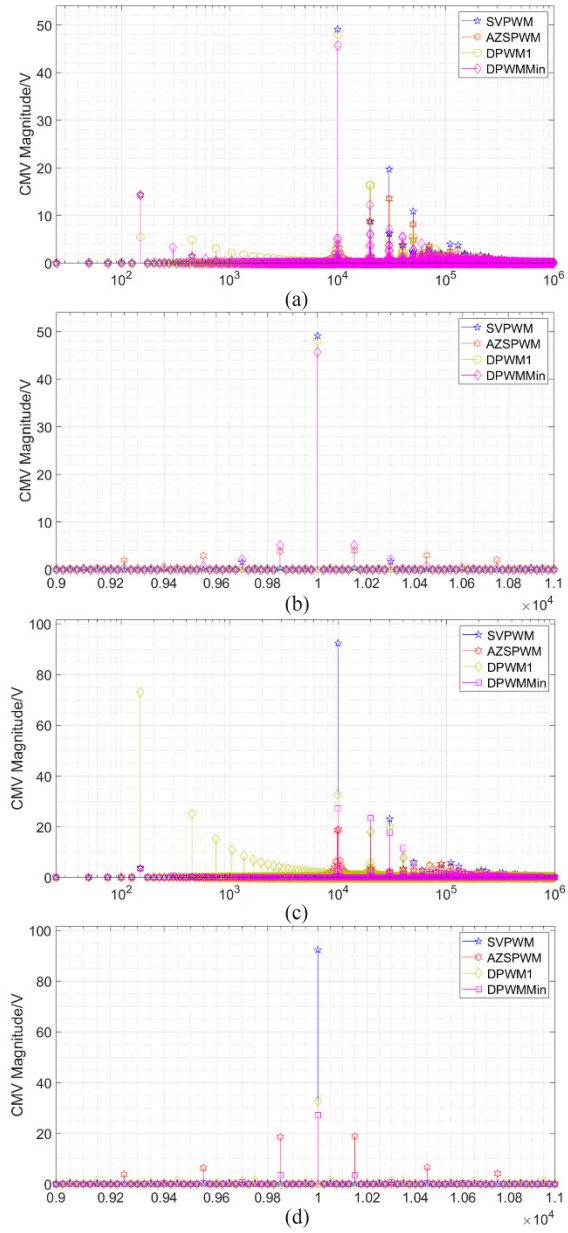

Fig. 5. CMV spectrum of SVPWM, AZSPWM, DPWM1, and DPWMMin (a) @M = 0.8. Wide frequency range (b) @M = 0.8. Zoomed-in view @f_s (c) @M = 0.2. Wide frequency range (d) @M = 0.2. Zoomed-in view @f_s.

Equation (3) divides the target function into four parts. The first term corresponds to the dc offset of the PWM waveform. Its existence depends on the reference point, which can be chosen as the lower dc bus or middle point of the dc bus. The second term represents the components of the fundamental frequency and its baseband harmonics. The third item represents the carrier wave harmonics, which are high-frequency components such as f_s, $2f_s$, and $3f_s$. The final double summation term is the entire group of all possible frequencies that appear as groups around the carrier harmonics frequencies. For example, $f_s \pm f_0$, $f_s \pm 2f_0$, $2f_s \pm 3f_0$, etc. The high-frequency components and the sideband group are the main objects to be analyzed.

For specific PWM schemes, according to (3) and (4), the Fourier coefficients A_{mn} and B_{mn} should be determined through

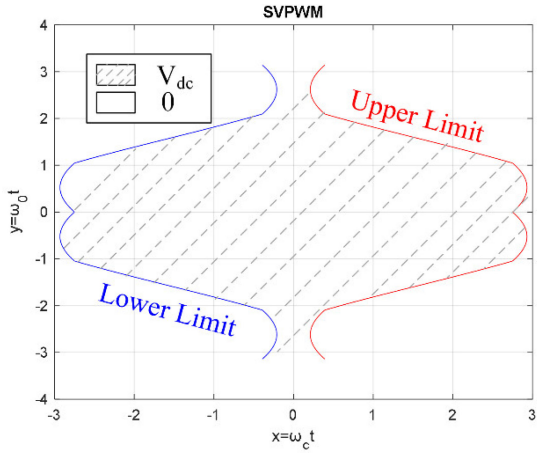

Fig. 6. DFI integral bounds for SVPWM.

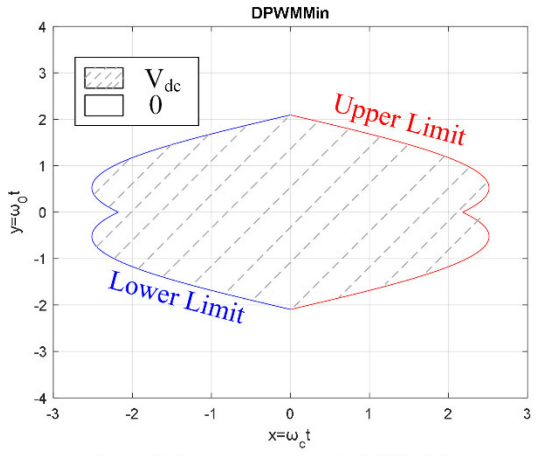

Fig. 7. DFI integral bounds for DPWMMin.

DFI. For the conventional SVPWM, the integral bounds follow the shape of corresponding modulation waveforms. Figs. 6 and 7 show the integral bounds for SVPWM and DPWMMin, both at full modulation index within one periodical area $(-\pi, \pi)$.

Theoretically, AZSPWM will share the same modulation waveform to SVPWM. The only difference is, in order to inversely align the medium-length duty in half of the six sectors, PWM pulses need to be shifted by half of the switching period. Therefore, an equivalent DFI model specifically for AZSPWM is built, as shown in Fig. 8. Assume the PWM duty cycle is D. Logically, to shift this PWM by 180°, the first step is to generate another PWM with the duty cycle equal to 1-D. By reversing the polarity of the newly generated PWM, the 180°-shifted PWM is obtained.

According to the logic operation derived above, the integral bounds of AZSPWM are redrawn in Fig. 9

$$A_{mn} + jB_{mn} = \int_{-\pi}^{-\frac{2\pi}{3}} \int_{-\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right)}^{\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right)} e^{j(mx+ny)}dxdy + \int_{-\frac{2\pi}{3}}^{-\frac{\pi}{3}} \int_{-\frac{\pi}{2}\left(1+\frac{3}{2}M\cos(y)\right)}^{\frac{\pi}{2}\left(1+\frac{3}{2}M\cos(y)\right)} e^{j(mx+ny)}dxdy$$

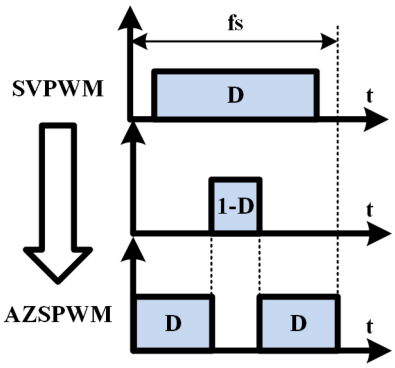

Fig. 8. AZSPWM generation logic.

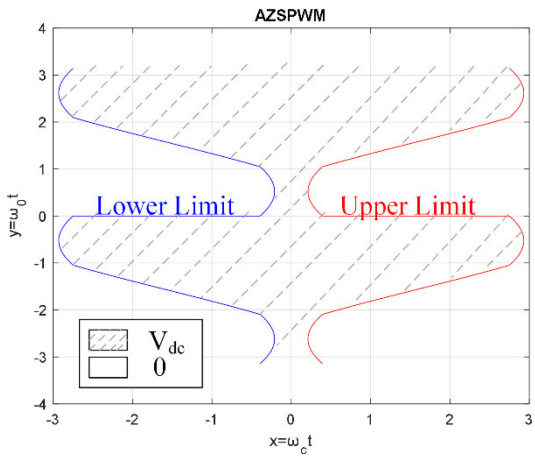

Fig. 9. DFI integral bounds for AZSPWM.

$$
\begin{aligned}
&+\int_{-\frac{\pi}{3}}^{0}\int_{-\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right)}^{\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right)} e^{j(mx+ny)}dxdy\\
&+\int_{0}^{\frac{\pi}{3}}\int_{\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{5\pi}{6}\right)\right)}^{-\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{5\pi}{6}\right)\right)} e^{j(mx+ny)}dxdy\\
&+\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}}\int_{\frac{\pi}{2}\left(1+\frac{3}{2}M\cos(y+\pi)\right)}^{-\frac{\pi}{2}\left(1+\frac{3}{2}M\cos(y+\pi)\right)} e^{j(mx+ny)}dxdy\\
&+\int_{\frac{2\pi}{3}}^{\pi}\int_{\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{5\pi}{6}\right)\right)}^{-\frac{\pi}{2}\left(1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{5\pi}{6}\right)\right)} e^{j(mx+ny)}dxdy \qquad (5)
\end{aligned}
$$

$$V_{ao} = |A_{mn} + jB_{mn}| * \frac{V_{dc}}{2\pi^2} \qquad (6)$$

$$V_{CM} = \frac{V_{ao} * \left(1 + 2\cos\left(2n * \frac{2\pi}{3}\right)\right)}{3}. \qquad (7)$$

It is worth noting that only flipping the integral bounds in Fig. 9 is not enough. During the integration, the upper and lower limits of the related section should also be swapped according to the AZSPWM generation logic in Fig. 8. Hence, the DFI model for AZSPWM is generated as (5)–(7). By substituting different *m* and *n*, the carrier harmonics and sideband components can be calculated.

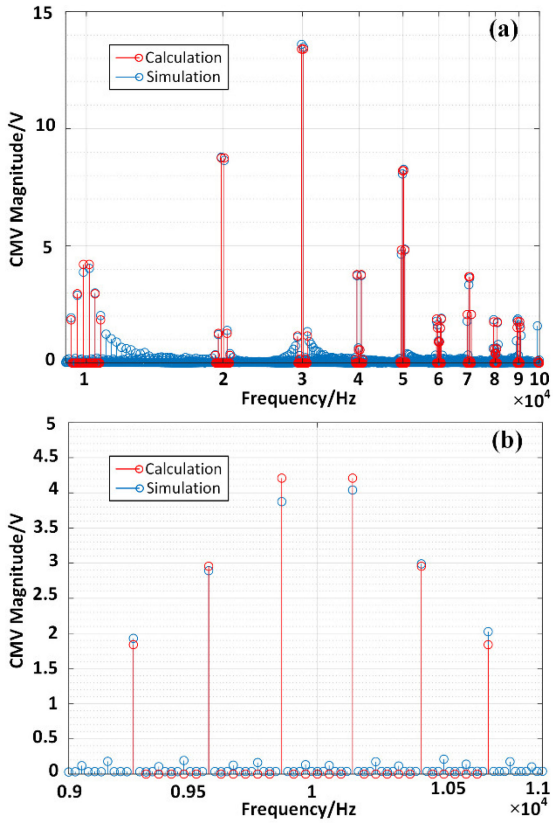

Fig. 10. Comparison of DFI result and simulation. (a) Wide frequency range. (b) Zoomed-in view @f_s.

The calculation and simulation are based on a 50-Hz fundamental frequency, 10-kHz switching frequency, 150-V dc bus voltage, and 0.8 modulation index. As Fig. 10(a) shows, the calculated carrier harmonics and the sideband component of both phase voltage and CMV are very close to the simulated result. Note that for computation, only the $f_s \pm 15f_0$ sideband harmonics around switching frequency are plotted. Fig. 10(b) shows the zoomed-in view of the range around the switching frequency (10 kHz). It can be observed that AZSPWM almost eliminates the CMV component at the switching frequency, but inevitably causes the sideband components to increase.

The CMV spectrum gives a visual impression on how the CMV is distributed. However, in reality, the CM energy (CME) distribution, especially the CME in a certain frequency range, rather than the CME at a specific frequency point is more important. To analyze CME, the square sum of each component within a certain frequency range is calculated as

$$f(x,y) = \sum_{\boldsymbol{f}=\boldsymbol{f}_c-nf_0}^{f_c+nf_0} \left(V_{\mathrm{CM}}(\boldsymbol{f})\right)^2 \qquad (8)$$

where n is the integer that defines the frequency range around f_c. Z_{CM} is the impedance of the CM path.

With (5)–(8), the CME distribution could be plotted as Fig. 11. AZSPWM reduces CME drastically at all operational ranges. However, at a low modulation index near f_s, DPWM1 and DPWMMin are not necessarily worse than AZSPWM. As the modulation index goes lower, the CM performance of DPWMMin and AZSPWM becomes comparable around f_s.

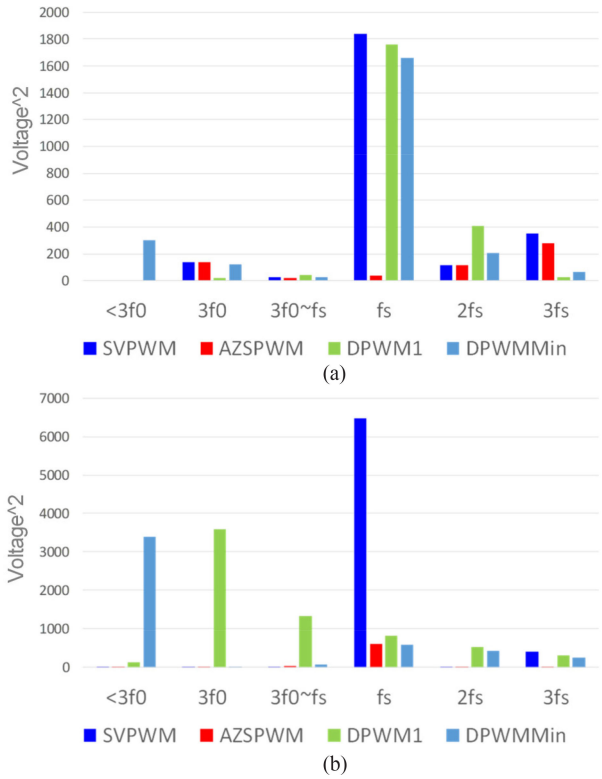

Fig. 11. CME distribution: (a) M = 0.8; and (b) M = 0.2.

TABLE I
THREE-PHASE CURRENT THD

MODULATION INDEX	SVPWM	AZSPWM	DPWM1	DPWMMIN
0.2	5.49%	37.46%	11.27%	10.62%
0.8	2.95%	5.84%	3.96%	4.02%

Considering the very-low-frequency, CMV has little impact on the motor CMI, in terms of the CME.

1) High M: SVPWM > DPWM1 > DPWMMin > AZSPWM.
2) Low M: SVPWM > DPWM1 ≈ DPWMMin ≈ AZSPWM.

A general procedure of DFI analysis for CMV can be summarized as shown in Fig. 12.

III. DM CURRENT RIPPLE ANALYSIS

The simulated three-phase current of the inverter for low (0.2) and high (0.8) modulation index is shown in Fig. 13. Here, $f_0 = 50$ Hz, $f_s = 10$ kHz, and the dc bus voltage is 150 V. The corresponding current THD is listed in Table I, which indicates AZSPWM always, has the highest DMI THD, though it has the best CMV reduction, especially for a low modulation index. As modulation increases, THD for AZSPWM goes down.

Therefore, the analytical model of the phase-current ripple is also needed. Since AZSPWM inversely aligns the pulse with the medium-length duty cycle, it results in a higher voltage drop across the winding inductance, which yields higher di/dt at the zero-crossing section. To analytically investigate the current

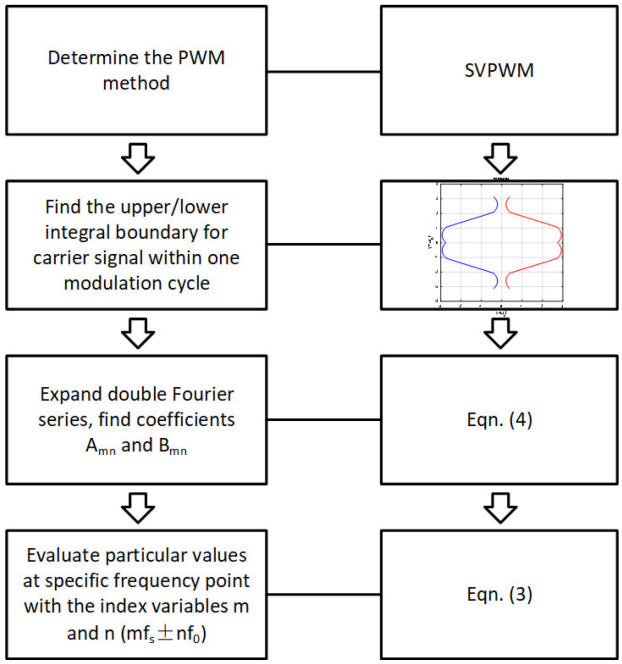

Fig. 12. General procedure of DFI analysis for CMV.

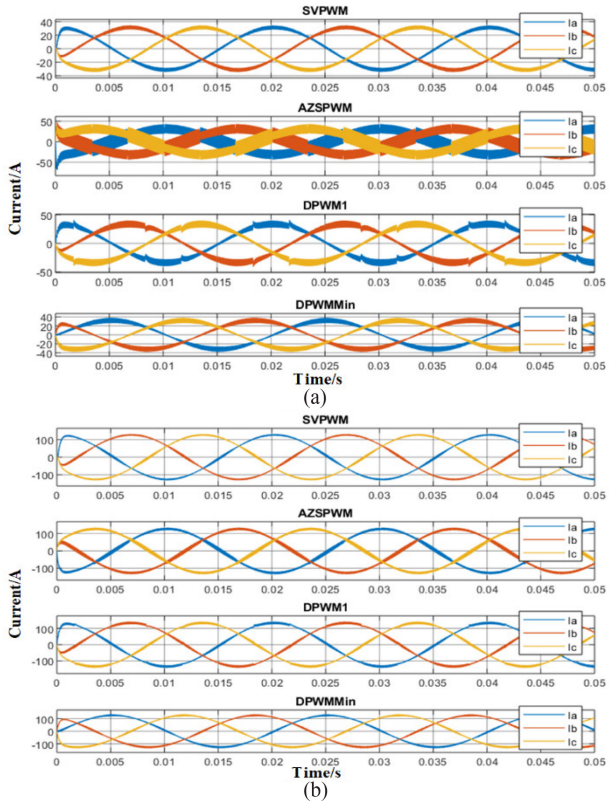

Fig. 13. Three-phase current waveform: (a) @M = 0.2; and (b) @M = 0.8.

ripple induced by different PWM schemes, the current ripple prediction is needed.

The prediction is based on the equivalent circuit for each space vector, as shown in Fig. 14 during the zero vector (000). The current slope can then be derived through KVL and KCL. Table II lists the current slope under different space vectors [19],

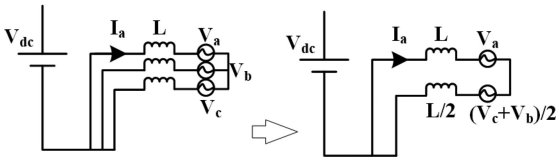

Fig. 14. Equivalent circuit for current ripple prediction.

TABLE II
CURRENT SLOPE UNDER DIFFERENT SPACE VECTORS

Space Vector	Current Slope
000/111	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a)$
100	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a - 2)$
110	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a + 2)$
001	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a - 1)$
010	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a - 1)$
011	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a - 2)$
101	$\frac{V_{dc}}{3L}(D_b + D_c - 2D_a + 1)$

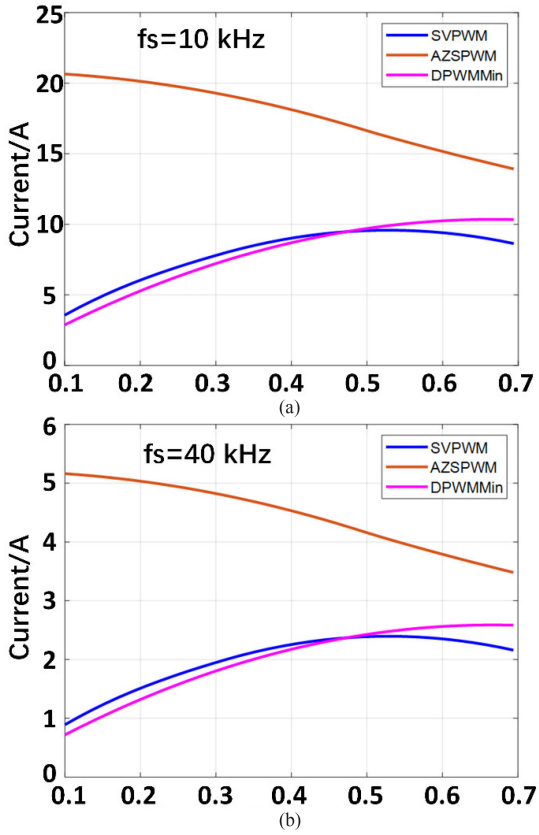

Fig. 15. Current ripple versus modulation index: (a) $f_s = 10$ kHz; and (b) $f_s = 10$ kHz.

[20], in which D_a represents phase A's duty cycle, D_b represents phase B's duty cycle, and D_c represents phase C's duty cycle.

With the current ripple prediction method, the reason why AZSPWM has a larger current ripple can be explained. According to the simulation result in Fig. 15, the largest ripple current for AZSPWM happens at each zero-crossing part, which is located in Sectors 2 and 5. The segments with a negative slope are 010 and 011, according to Table II. The predicted current ripple is

$$\Delta I = \frac{V_{dc}}{3L}(D_b + D_c - 2D_a - 2)\,D_c T_s + 2\frac{V_{dc}}{3L}(D_b + D_c - 2D_a - 1)\left(\frac{1 - D_a - D_c}{2}\right)T_s. \tag{9}$$

Fig. 16 shows the current ripple prediction in Sector 1. The actual ripple current is determined by the dc-link voltage, motor armature inductance, switching frequency, and instantaneous duty cycle. On the right-hand side of Fig. 16, the simulated ripple behavior is aligned with the prediction.

Assume the switching frequency is 10 kHz, the fundamental frequency is 120 Hz and the armature inductance is 120 μH. According to (9), the maximum ripple of any PWM scheme can be calculated with respect to different modulation index. Fig. 16 shows the predicted current ripple amplitude as the modulation index varies from 0.1 to 0.7 for SVPWM, AZSPWM, and DPWMMin, respectively. With the modulation index increasing, the current ripple of AZSPWM decreases, while for SVPWM and DPWMMin the current ripple increases. However, even the smallest current ripple of AZSPWM is still greater than the highest value of SVPWM or DPWMMin applies. This turns out to be one significant drawback of AZSPWM.

By doing the same current prediction in all sectors for different PWM schemes, the current ripple behavior can be compared to a different modulation index. The prediction result is shown in Fig. 17(a)–(c). It is observed that, as the modulation index increases, the current ripple of SVPWM and DPWMMin will also increase while dropping for AZSPWM. Furthermore, at the same modulation index, AZSPWM always generates the highest current ripple, followed by DPWMMin, and SVPWM shows the lowest current ripple.

Fig. 17(d) shows a direct comparison of the CM- and DM-performance of SVPWM, AZSPWM, and DPWMMin. It can be found that in the low-modulation index range, the current THD of AZSPWM is significantly higher than SVPWM and DPWMMin. In the medium and high-modulation zone, the corresponding CME of AZSPWM is significantly lower than other PWMs, though its DM current THD is still worse than others.

IV. EXPERIMENTAL RESULTS

An FPGA-controlled SiC inverter is designed to set up a motor drive test bench. The designed inverter is rated at 30 kW with a 400-V dc link voltage. The CMI measurement relies on the line impedance stabilization network (LISN). The overall system layout is shown in Fig. 18(a). LISN provides a stable and normalized source impedance (50 Ω in this test) for CM measurement and prevents the external noise from the source side [21]. The measured CM current is sent to the EMI analyzer through the power combiner, which allows the CM component to pass while suppressing the DM component. The test bench is shown in Fig. 18(b). The FPGA controller communicates with the host computer through Ethernet. The whole system sits on a

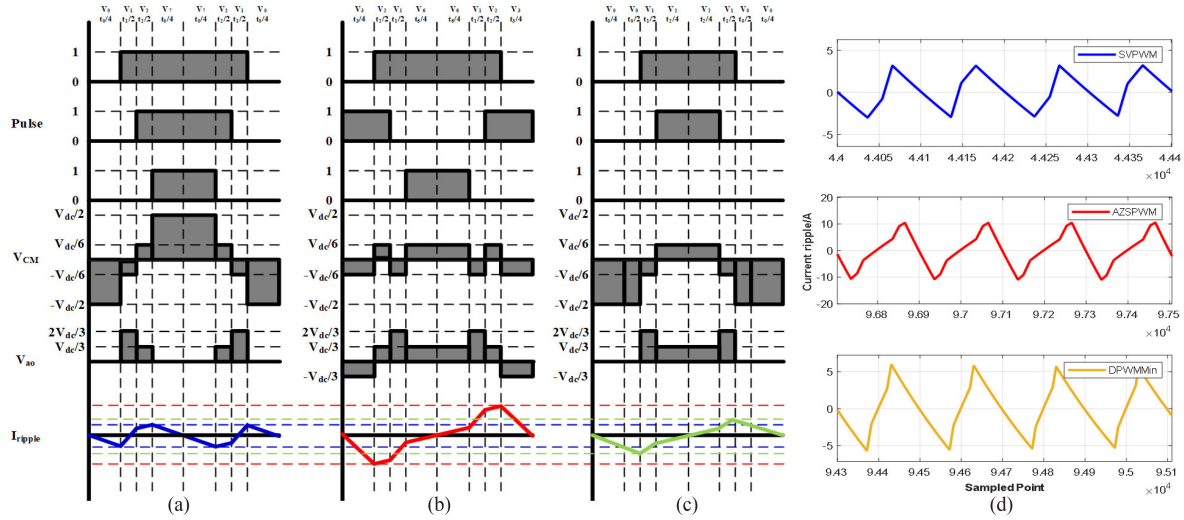

Fig. 16. DM current ripple at various PWMs. (a) SVPWM. (b) AZSPWM. (c) DPWMMin. (d) Current ripple versus PWM pattern.

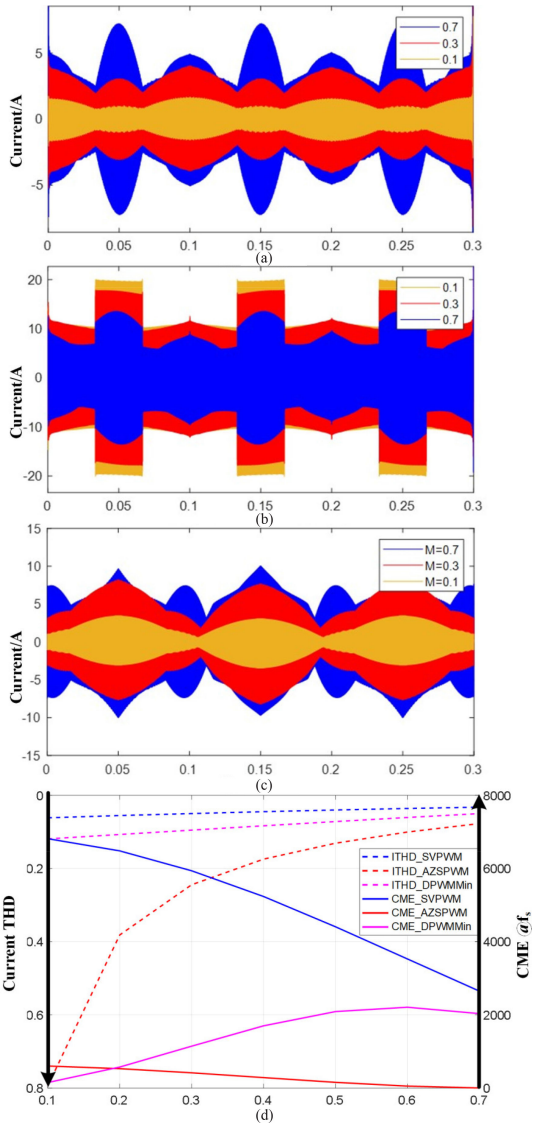

Fig. 17. (a) Current ripple prediction for SVPWM. (b) Current ripple prediction for AZSPWM. (c) Current ripple prediction for DPWMMin. (d) CM- & DM-performance comparison for various PWM methods.

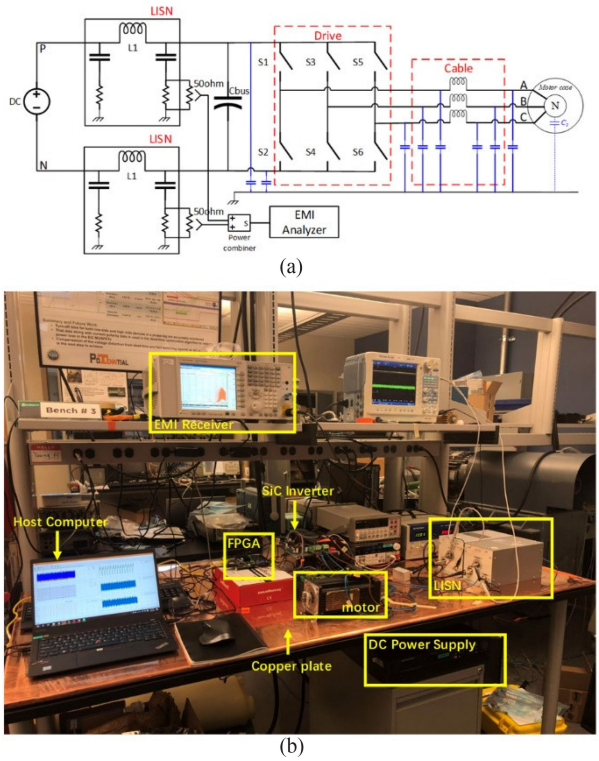

Fig. 18. Test bench setup. (a) Diagram for CM measurement in the motor drive system. (b) Test equipment.

copper grounding plate, where the inverter heatsink, motor case, and LISN are grounded.

By switching different PWM schemes at low speed (300 r/min), which is the low-modulation-index (0.2) case, the CMV measurement is collected and plotted, as shown in Fig. 19(a). The zoomed-in view at the switching frequency is shown in Fig. 19(b).

As seen in Fig. 20, at the switching frequency, SVPWM has the highest CM component by translating the CMV decibel plot to the CMI amplitude spectrum; DPWM1 and DPWMMin have lower CM components, and AZPWM has the lowest CM

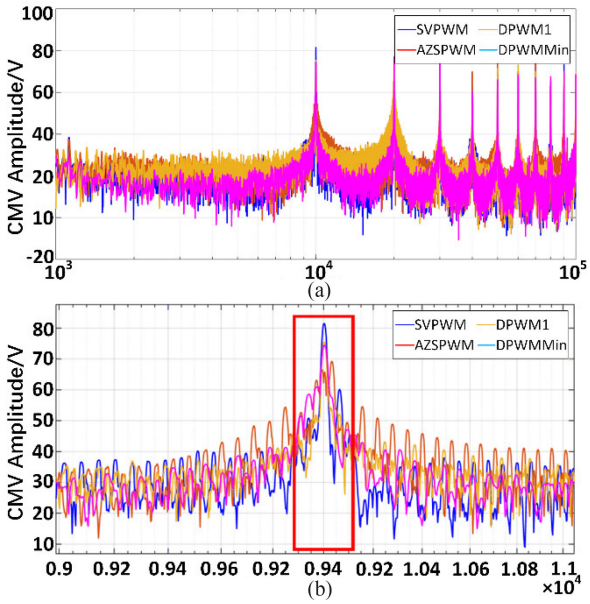

Fig. 19. CMV measurement. (a) Wide frequency range. (b) Zoomed-in view @f_s.

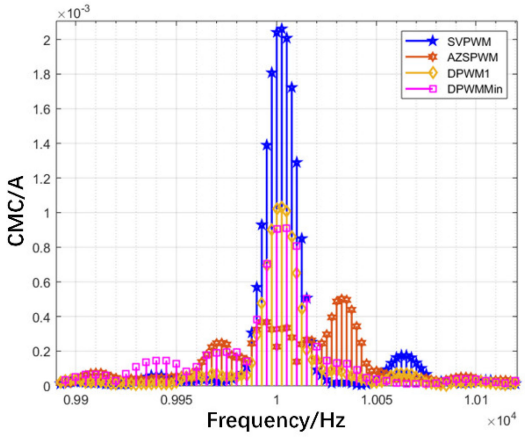

Fig. 20. CM current spectrum @f_s.

current—even though its CM component on the sideband rises up compared to other PWM schemes. This observed behavior at the switching frequency is aligned with the simulation result.

Note that the modulation index in this test is very low (0.2). At f_s, AZSPWM has the best CMV reduction performance. However, in terms of the spectrum near f_s ($f_s \pm 500$ Hz) of AZSPWM and DPWMMin, the CMV reduction performance is comparable, the lowest among all PWM schemes. DPWM1 is in the middle, and SVPWM has the highest CMV. This also confirms that at a low modulation index, the CM reduction performance of AZSPWM and DPWMMin are close, predicted in Fig. 11.

The CM current for each PWM method at different switching frequencies is also measured, as shown in Fig. 21. At a specific switching frequency, the peak value of CM components increases with the switching frequency. Fig. 22 shows that the CM current increase as switch frequency increases. This leads to the bulky design of the CM filter as the switching frequency

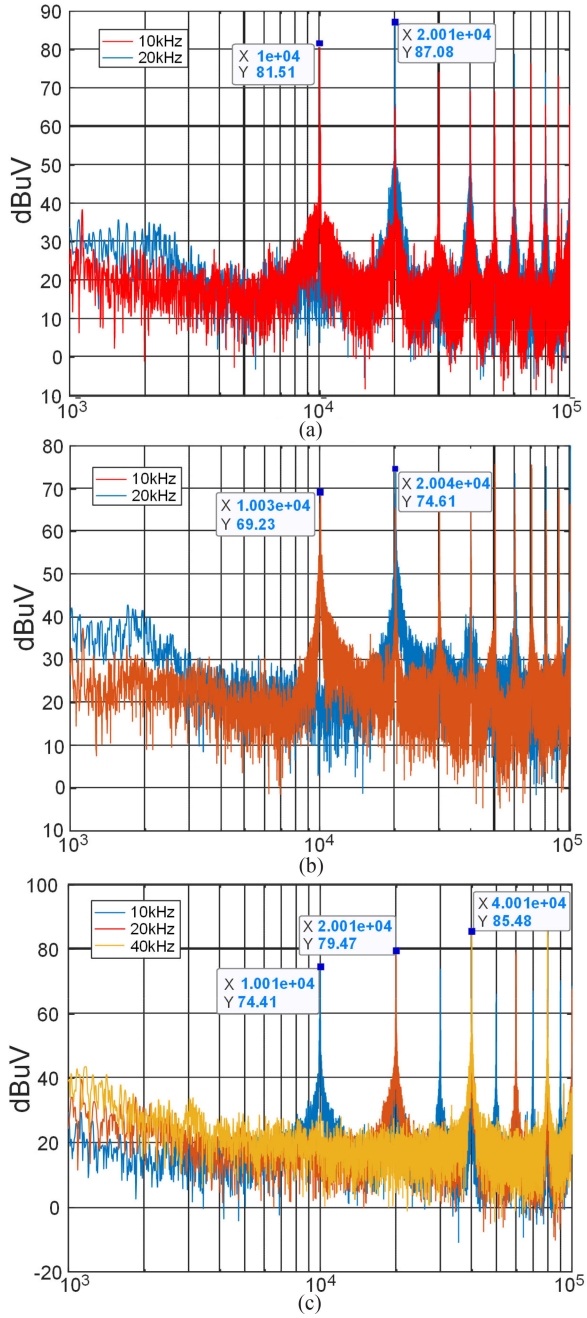

Fig. 21. CMV spectrum with respect to different switching frequency. (a) SVPWM. (b) AZSPWM. (c) DPWMMin.

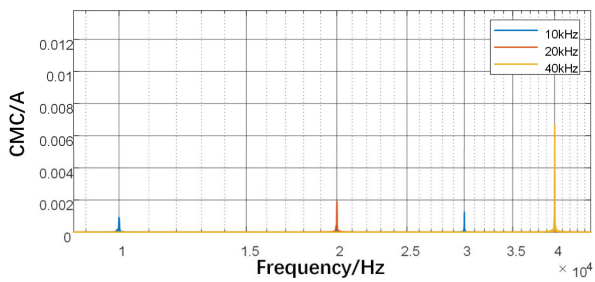

Fig. 22. CM current spectrum with respect to different switching frequency @DPWMMin.

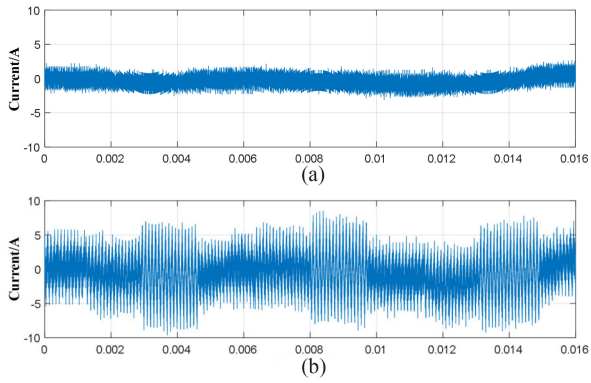

Fig. 23. Current ripple experimental result @M = 0.4. (a) SVPWM. (b) AZSPWM.

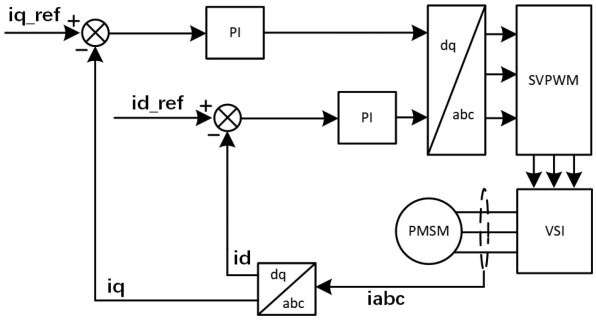

Fig. 24. Field oriented control block diagram.

increases, which is the main challenge when adopting WBG devices.

As for the impact on the DM signal, the current ripple has been captured in Fig. 23, when implementing SVPWM and AZSPWM at the same modulation index (0.4). For AZSPWM, the modulated current ripple could be 2–5 times of that modulated by SVPWM. Combined with the conclusions obtained in this section, this indicates that even though it indicated the AZSPWM reduces the CMV, it does increase the DM current. These ripples not only cause extra loss, but also generate acoustic noise when the switching frequency is below 20 kHz.

V. Impact of Control Frequency on CM and DM Signals

As the switching frequency of WBG devices is gradually pushed to a higher level to maximize the potential of SiC devices, the high control frequency, i.e., high CBW becomes more and more important. In this article, all the control logic is realized through Xilinx System Generator blocks and fixed-point arithmetic with high precision (32-bit) multiplications. The HDL code can be automatically generated as soon as the simulation in MATLAB/Simulink environment is verified. Then the generated HDL bitstream can be directly implemented to the Xilinx 7000-series FPGA chip to achieve field-oriented control, with the control diagram shown in Fig. 24. Note the traditional microprocessor executes the control algorithm in serial sequence, which limits the overall system processing efficiency and yields a low control frequency, i.e., $f_c \ll f_s$. In FPGAs, all the control logic is implemented in parallel, which means it can update the PWM every clock cycle, i.e., $f_c = f_s$. Its impact on CM and DM performance has rarely been mentioned in the previous research work, which is the subject of this section.

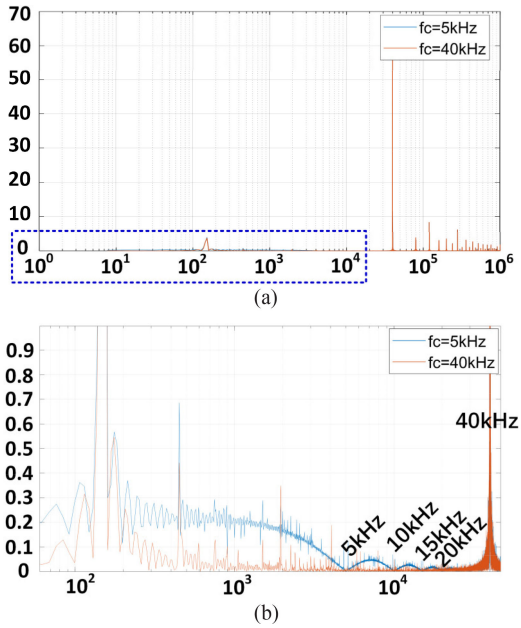

Fig. 25. (a) CM spectrum @$f_s = 40$ kHz with respect to different CBW ($f_c = 1/8f_s$, simulation). (b) Zoomed-in view.

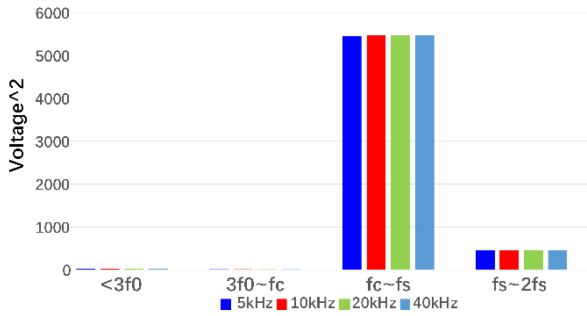

Fig. 26. CME distribution with respect to different f_c (simulation).

A. CBW Impact on CM Signal

Assume in a SiC inverter, $f_s = 40$ kHz and $f_0 = 50$ Hz. To investigate the impact of f_c, the author purposely set $f_c = 1/8f_s$, $1/4f_s$, and $1/2f_s$, which means to update the PWM duty cycle every 2, 4, and 8 switching periods, respectively. Fig. 25 gives the CMV FFT result when $f_c = 40$ kHz, $f_c = 1/8f_s = 5$ kHz. A zoomed-in view shows that for $f < f_s$, the CMV with low f_c is always higher than the curve with full CBW, except at some notched frequency pointe ($n*f_c$). However, overall, there is no significant CME difference.

By calculating the CME distribution, as shown in Fig. 26, the conclusion is as follows.

1) f_c will affect CMI at the frequency range $<f_s$, but the impact is minor.
2) CMI at the switching frequency point is still dominant, regardless of f_c.

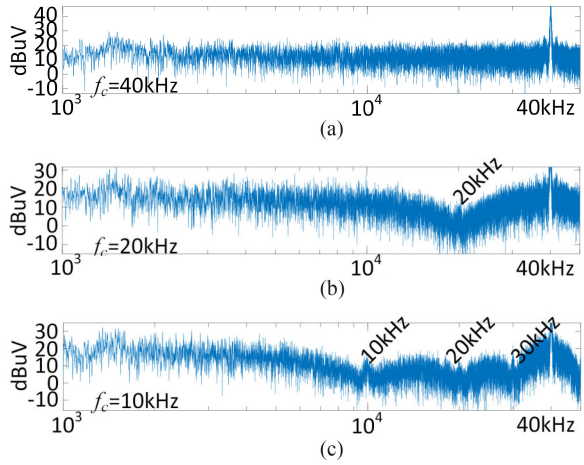

Fig. 27. Measured CMV spectrum with respect to different CBW. (a) 40 kHz. (b) 20 kHz. (c) 10 kHz.

TABLE III
THREE-PHASE CURRENT THD WITH DIFFERENT $f_c - f_0$ PAIR

CBW (f_C)	5 kHz	10 kHz	20 kHz	40 kHz
THD(f_0=500 Hz)	3.525%	2.45%	1.798%	1.775%
THD(f_0=1 kHz)	9.175%	3.339%	3.026%	2.581%

Therefore, f_c does not contribute to the CM reduction. This conclusion is confirmed by measurements in Fig. 27. In these measurements, the CM component is at $f = \mathrm{n}{*}f_c$ notches in the low-frequency range matching well with simulation results. The dominant part is still at $f = f_s$.

B. CBW Impact on DM Current

The PWM updating frequency will lower the resolution of the output waveform. For a 40 kHz inverter, set $f_c = 1/8f_s$, $1/4f_s$, $1/2f_s$, respectively. The spectrum of the DM current is compared in Fig. 28.

For each case, the DM components at $\mathrm{n}{*}f_c$ will appear as long as $f_c{\neq}f_s$. For $f_c = f_s$ case, the simulated current THD is 1.775%. As f_c decreases, the current THD increases. Table III shows the THD simulation result with various f_c at $f_0 = 500$ Hz and 1 kHz, respectively. The conclusion is as follows.

1) The influence that f_c brings to the DM signal is more obvious. Since the modulation signal changes along f_c, the resolution drops as $f_c < f_s$, which affects the shape of the output current.
2) For $f_c \neq f_s$, the spectrum has high components not only at f_0 and f_s, but also at $n{*}f_c$.
3) The lower fc, the higher DM current THD.
4) FPGA with the high CBW will benefit DM more than CM.

To validate the impact of using FPGA, the CM current at different f_c is collected. The inverter switching frequency is 40 kHz. f_c is set to 40 kHz, 20 kHz, and 10 kHz, respectively. The CM current spectrum is plotted in Fig. 29(a). Fig. 29(b) provides a zoomed-in view for the CM current spectrum at the switching frequency point (40 kHz). It shows that no matter what the control frequency is, there is almost no difference in the CM current, i.e., the control frequency does not affect the CME.

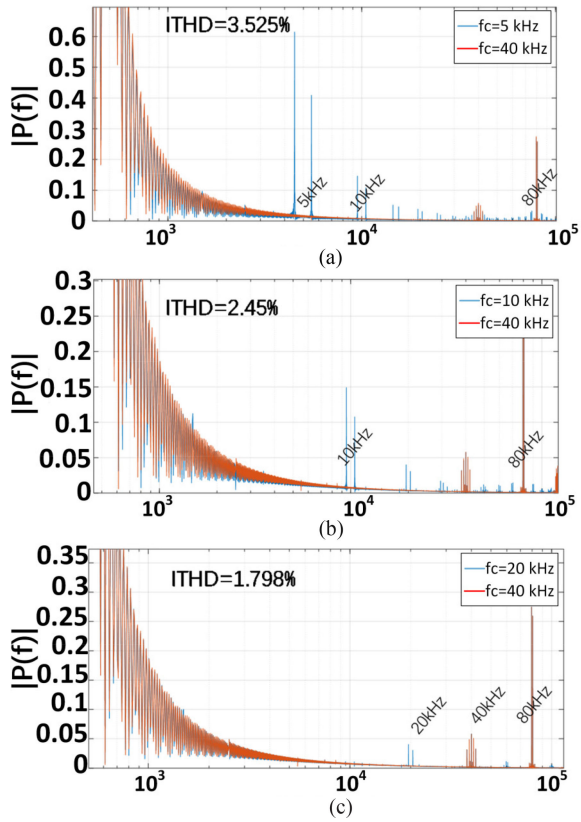

Fig. 28. DM signal spectrum of the three-phase current (simulation) comparison with different CBW. (a) $f_c = 1/8f_s$. (b) $f_c = 1/4f_s$. (c) $f_c = 1/2f_s$.

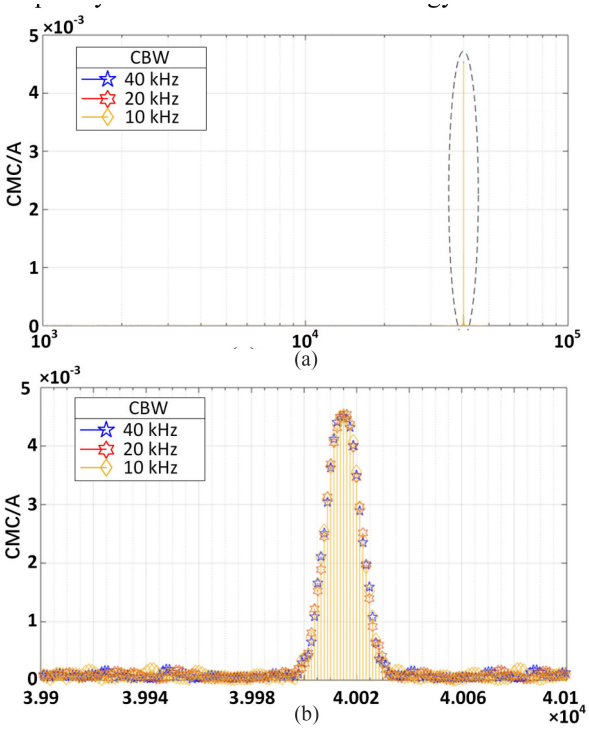

Fig. 29. Measured CM current spectrum with different CBW. (a) Wide frequency range. (b) Zoomed-in view @f_s.

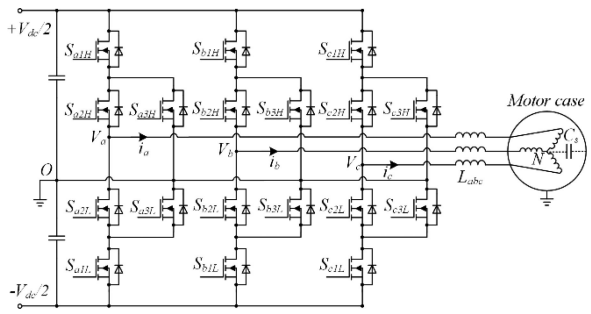

Fig. 30. Three-phase three-level ANPC inverter motor drive system.

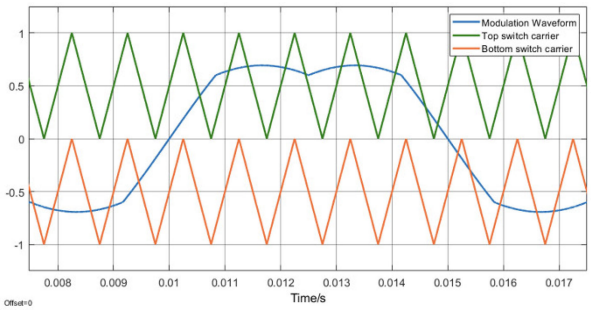

Fig. 31. 3L-ANPC SVPWM modulation waveform.

VI. Extension to Three-Level NPC Inverter

This section will discuss the applicability of the proposed analytical CMV model to a multilevel inverter, e.g., a three-level active neutral point clamping (3L-ANPC) inverter, as shown in Fig. 30. Compared to a conventional two-level inverter, its phase output voltage has three voltage levels (0, $+V_{dc}/2$, $-V_{dc}/2$).

Fig. 31 shows the SVPWM modulation in a 3L-ANPC. In the positive half cycle, the top switches S_{a1H} and S_{a3H} will be controlled by the top switch carrier, while S_{a2H} stays ON. All bottom switches (S_{a1L}, S_{a2L}, and S_{a3L}) are OFF. In the negative half cycle, the bottom switch S_{a1L} and S_{a3L} will be controlled by bottom switch carrier while S_{a2L} remains ON. The top switches (S_{a1H}, S_{a2H}, and S_{a3H}) then remain off. According to the switching profile of SVPWM in 3L-ANPC and following the general procedure of DFI analysis for CMV shown in Fig. 12, the corresponding DFI integral bounds can be derived, as shown in Fig. 32. There are eight sections for each fundamental cycle. Specially, in sections 1, 2, 5, and 6, there are three integration areas. In sections 3, 4, 7, and 8, there is only one integration area (ignore the area where the pole voltage is 0). For instance, in section 1, the integration segments should be $(-\pi, 1-)$, $(1-, 1+)$, and $(1+, \pi)$. In section 3, the integration segments should be $(3-, 3+)$.

The DFI model for SVPWM in a 3L-ANPC is then generated from (10). Using (6)–(7) and substituting different values for m and n, the carrier harmonics and sideband components of the CMV can be calculated and compared to the simulation at $f_0 = 100$ Hz, $f_s = 10$ kHz, 200-V DC bus voltage, and 0.8 modulation index. As shown in Fig. 33, the calculated carrier harmonics and the sideband component of both phase voltage and CMV are very close to the simulation. Here, only the $f_s \pm 15f_0$ sideband harmonics around f_s are plotted. Therefore,

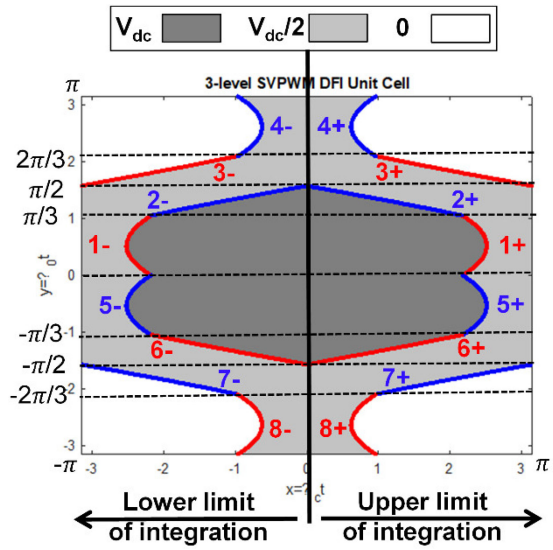

Fig. 32. DFI integral bounds for SVPWM in a 3L-ANPC inverter.

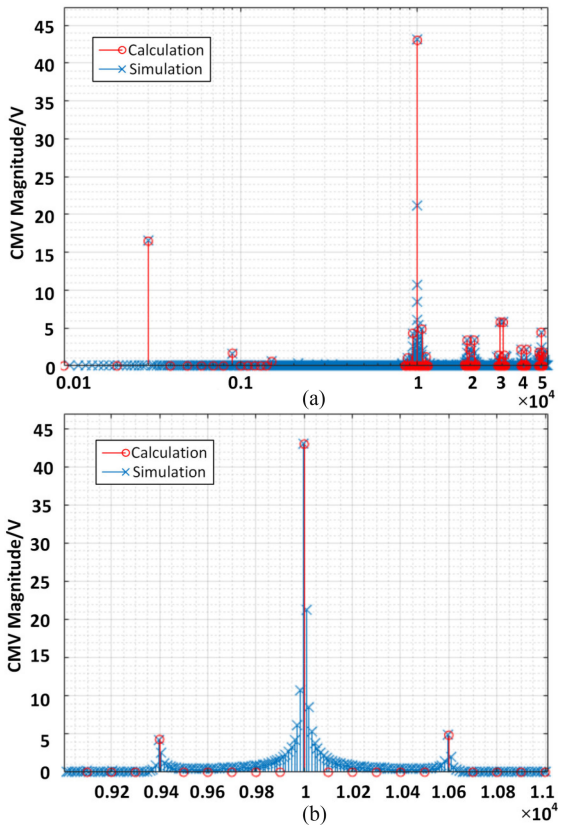

Fig. 33. Comparison of DFI result and simulation for 3L-ANPC inverter. (a) Wide frequency range. (b) Zoomed-in view @f_s.

the proposed analytical approach for CMV can be extended to multilevel scenarios

$$A_{mn} + jB_{mn} = \frac{1}{2\pi 2}\int_{-\pi}^{\pi}\int_{\substack{lower\\ limit\ in\\ sector\ i}}^{\substack{upper\\ limit\ in\\ sector\ i}} Ue^{j(mx+ny)}dxdy$$

$$
\begin{aligned}
&= \int_{-\pi}^{-\frac{2\pi}{3}} \int_{8-}^{8+} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{2\pi}{3}}^{-\frac{\pi}{2}} \int_{7-}^{7+} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{-\pi}^{6-} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{6-}^{6+} V_{dc} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{6+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{-\pi}^{5-} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi/2}^{-\pi/3} \int_{5-}^{5+} V_{dc} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi/2}^{-\pi/3} \int_{5+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi/2}^{-\pi/3} \int_{-\pi}^{1-} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi/2}^{-\pi/3} \int_{1-}^{1+} V_{dc} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi/2}^{-\pi/3} \int_{1+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{-\pi}^{2-} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{2-}^{2+} V_{dc} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi/2}^{-\pi/3} \int_{2+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-\pi}^{-2\pi/3} \int_{3-}^{3+} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy \\
&+ \int_{-2\pi/3}^{-\pi/2} \int_{4-}^{4+} \frac{V_{dc}}{2} e^{j(mx+ny)} dxdy. \quad (10)
\end{aligned}
$$

VII. Conclusion

This article has given a comprehensive consideration of the three-phase motor drive system by building analytical models of CMV and DMI for various PWM controls, which have been validated by simulation and experiments. The DFI model quantifies existing sideband harmonics in AZSPWM CMV and shows excellent extendibility to a multilevel inverter. Together with the DMI model predicting current ripple and THD, some conclusions have been drawn that are different from previous literature.

1) Due to such sideband harmonics, the CM performance of AZSPWM is not necessarily better than DPWMs, especially at a low modulation index.
2) AZSPWM causes higher phase current ripple than other PWM.

How to apply the best PWM at different operation scenarios still remains unknown, but such analytical model provides us with a powerful tool, allowing a comprehensive vision for further evaluations. Compared to the traditional solution, e.g., simulation model in Simulink, the proposed analytical model could help designers to summarize the principle of CMV effectively. By using DFI, the analytical result of CMV could be coupled with the CM impedance, thereby conducting the CMI. The impact of all other variables, such as motor and controller parameters, could be actively evaluated through analytical equations instead of repeating the simulation. However, for some novel and complex modulation method with irregular modulation waveform, the DFI bounds might be difficult to derive, which will increase the difficulty of applying the proposed model.

According to the performance evaluation, each PWM has its merits and drawbacks. Applying single method in full modulation range is not an optimal solution. Combining several PWMs with respect to specific operation scenarios can be a balanced approach, which is also the future work of this article.

It is also found that FPGA's high control frequency can benefit the DM reduction while having little impact on the CMI. An analytical model considering other non-ideal factors such as the sampling frequency and delay is also subject to future work.

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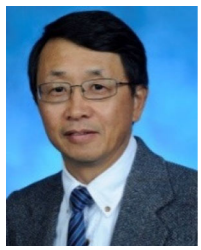

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