An Automated Semi–symbolic State Equation Generation Method for Simulation of Power Electronic Systems

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***Abstract*—Computer-aided analysis is playing an important role in the design and control of power electronic systems. A discrete-state event-driven (DSED) framework with state-space modeling has been proposed recently for accurate and efficient off-line simulation. Nevertheless, automated equation formulation for arbitrary circuits is also required to develop the DSED framework toward general simulation software. However, the traditional state equation generation method is very time-consuming, especially for large-scale systems due to the variable topologies brought by switching events. In this article, an automated semi–symbolic state equation generation method is proposed. Based on the switching function modeling of basic switching legs, an explicit function from switching states to state equation matrices is given, which reduces the computational cost without sacrificing any accuracy. The operating and topological characteristics of power electronics systems are utilized for further optimization. The proposed method greatly increases the simulation efficiency of power electronic systems, especially for large-scale systems. Two cases of the 2 MW 4-port solid-state transformers with different system scales are simulated with the proposed method under the DSED framework. About 700-fold and 1200-fold acceleration is achieved compared with one fast-speed commercial software, where the proposed method contributes 50-fold and 110-fold acceleration in the two cases, respectively.**

***Index Terms*—Large-scale circuits, power electronic system simulation, state equation formulation.**

I. Introduction

COMPUTER-AIDED analysis and simulation of power electronic systems are of great significance in the design and control of power converters for engineers. Unlike other common circuits, power electronic systems are usually combined by several power conversion stages composed of basic switching legs and energy storage elements. Multiple switching events cause the frequent change of the circuit topology and introduce discontinuous points. Therefore, power electronic systems are typically hybrid systems consisting of both continuous states and discrete events [1], [2], which bring great challenges to the simulation tools.

Based on the knowledge of the hybrid nature of power electronic systems, a discrete state event-driven (DSED) framework with a flexible adaptive algorithm has been proposed recently to obtain accurate and efficient simulation [3], [4]. A flexible adaptive (FA) variable-step and variable-order algorithm is utilized for numerical integration of continuous states. An event-driven mechanism is adopted for efficient locating of discrete events. Ten-fold to hundred-fold speed-up has been achieved in several test cases compared with commercial software [4]. However, simulation of arbitrary circuits built by users in the graphical user interface (GUI) like other general software was not realized in the previous work. In order to achieve this goal, automated formulation of network equations must be realized for computer implementation.

Among modern circuit simulation software, the formulation methods of network equations mainly fall into two categories: 1) the nodal analysis method adopted by PSIM [5], and 2) the state-space approach employed by Simulink [6] and PLECS [7]. Compared with the nodal analysis method, the state-space approach is more suitable for power electronic system simulation as the state-space matrices are independent of step-size so that a variable-step solver can be used to obtain faster simulation speed [8], [9]. The DSED framework also adopts the state-space approach since the FA method is a variable-step solver and the event-driven mechanism relies on the discretization of physical states [4]. However, one main disadvantage of the state-space approach is the complexity to automatically generate the state equations according to the circuit topology by computer. Complicated identification of topological information and multiple matrix operations are involved in the process, which is rather time-consuming [8], [9]. It is usually not a problem for common circuits as their topologies are fixed. But for power electronic systems whose topologies are variable due to the discrete switching events, the network equation formulation is no longer a one-time job but is periodically repeated. The complicated equation generation process will dramatically increase the whole simulation time [10]–[12]. Therefore, considering the hybrid nature of power electronic systems, the computer formulation

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method of state equations for such systems should have the following characteristics.

A. Accurate and Stable Modeling of the System

In power electronics systems, the continuous states and discrete events deeply interact with each other because the states of switching devices determine the mathematical forms and properties of the system matrices and further influence the accuracy and efficiency of numerical integration of continuous states. Therefore, accurate and stable modeling of the system must be ensured to precisely reflect the influences brought by switching devices on the system operating modes and avoid introducing stiffness issues for numerical integration [12]–[14].

B. Simple and Efficient Generation and Updating Method of the Network Equations

Generally, the number of possible topologies is up to 2^n when the system contains n switches. In high-power conversion systems with hundreds or thousands of switching devices, both the time and space complexity of the matrix generation can be unacceptable [10]. For such systems, optimizing the generation and updating process of the state-space matrices will greatly reduce the computational cost.

C. Automated and Systematic Methods Without Manual Intervention for Computer Implementation

Power electronic systems are usually composed of several typical converters. Many researchers have proposed simplified physical or mathematical models for specific topologies [15]–[18]. However, when it comes to computer-aided simulation with GUI, the state equation formulation method should be applicable to different topologies and can be automatically done by computer programs. The users only need to build the circuit with elements in the libraries without extra work.

Commercial software usually adopts ideal switched model for state equation formulation due to its stability and accuracy in numerical integration. In the ideal model, switches are modeled as small resistors, shorted circuits, or zero-value voltage sources during ON-state and open circuits or zero-value current sources during OFF-state [19]. Automated state-model generation algorithms with ideal switched model are fully discussed in [8], [12], [20]–[24]. Topology identification based on the incidence matrix is first adopted to pick up all the independent state variables. By solving the equality constraints from KCL, KVL, and *I–V* characteristics of the circuit elements, the state-space equation matrices can be obtained afterward. However, the ideal model is actually a variable-topology model, making it impossible to provide a unified form for the state equations when the switching states change. Even there is only one switch changing its state, the above steps need to be restarted from the very beginning, which greatly influences the simulation efficiency.

Many other methods have been proposed to solve the variable-topology problem. Two-value (small/large) resistor model proposed in [25] and [26] can convert the variable-topology problem into a variable-parameter problem, which avoids the repeated identification of circuit topologies. However, it should be very careful to choose the value of the ON/OFF resistors otherwise the system may become stiff and encounter convergence problems [12], [13]. Pejovic [14] proposed a discrete-time switch model containing a constant conductance in parallel with a current source to obtain a constant system matrix. Similar discrete-time approximation methods can be found in transmission-line models in [13]. However, in all the discrete-time models, the simulation step is fixed and constrained by the circuit parameters to make the matrices constant. In addition, abnormal voltage or current spikes can be observed in the simulated results at the switching point, which cannot match physical waveforms. Another idea is to model the influences of the switching devices as variable inputs while the system matrices remain constant [16]–[18], [27]–[32]. There are two subcategories of this kind of method. One is to use time average models based on the mathematical analysis of state-space equations under different operating modes [16]–[18], [27], [28]. Converters are modeled as variable sources whose values are associated with the duty ratio and are updated each switching cycle. The other one is to update the values of the variable sources each calculation step according to the measurement results of certain elements and switching states [29]–[32]. Discretization methods like first-order or zero-order holder are introduced in the calculation process. Therefore, one-step delay exists in this process and the accuracy highly depends on the step size and the properties of interface elements. Usually, large capacitors (or dc voltage sources) and inductors to be measured are required in this modeling method. Besides, the dimensions of the input and output variables are greatly increased, thus increasing the single-step computational burden of numerical integration, regardless of whether the switching states change or not. To conclude, in both subcategories, the variable sources are determined by the data from previous time steps so extra errors are introduced during the modeling process

$$\frac{\mathrm{d}}{\mathrm{d}t}i_{L_\mathrm{O}} = -\frac{R_\mathrm{O}}{L_\mathrm{O}}i_{L_\mathrm{O}} + \frac{s_1 - s_3}{L_\mathrm{O}}u_E,$$
$$\boldsymbol{A} = \left[-\frac{R_\mathrm{O}}{L_\mathrm{O}}\right], \boldsymbol{B} = \left[\frac{s_1 - s_3}{L_\mathrm{O}}\right]. \tag{1}$$

In fact, in power electronic systems, a switching device does not work alone but cooperates with other switching devices, forming some basic commutation units. Basic switching legs like half-bridge rather than single device act as the smallest units, especially in high-power conversion systems [15], [31], [33]. By fully exploiting this topological characteristic of power electronic systems, it is possible to derive the state equations in a unified form like the symbolic expression. Taking the H-bridge converter as a simple example, the state equation of the system under different switching states can be written as a unified form as illustrated in Fig. 1 and (1) with the expression $s_1 - s_3$. Using this unified function to modify the matrices is obviously more efficient than the traditional variable-topology method.

In this article, a semi–symbolic state equation generation and updating method is proposed for the simulation of power electronic systems. This method is an extension of the previous

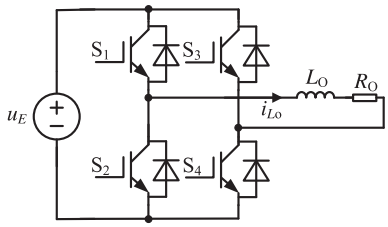

Fig. 1 Topology of an H-bridge converter.

work on the DSED framework in the aspect of computer implementation. As illustrated in Fig. 2(b), the key characteristics of the proposed method are as follows.

1) A unified form of state equation matrices under different switching states is derived. Based on the modeling of basic switching legs, the influences of switching devices on the state equations are modeled by the symbolic switching states vector. Thus, an explicit function from switching states to the state equation matrices can be given, which is exactly the same as the ideal switched model in the aspect of numerical values, so no stability problems are faced and the accuracy is not sacrificed. As the symbols only exist in the switching functions rather than all the physical parameters, the method is referred to as "semi–symbolic."
2) Simple and efficient updating of state equations is realized under the semi–symbolic method. The complicated variable-topology problem is converted to a variable-coefficient problem by the semi–symbolic function, thus reducing the computational cost when modifying the system matrices. Full utilization of the operating and topological characteristics of power electronic systems can further optimize the equation updating process and minimize the calculation time.
3) Automated computer implementation without manual interventions can be realized with this method, which is suitable for simulation software with GUI.

The rest of the article is organized as follows. Section II introduces the modeling method for basic switching legs to derive a semi–symbolic function for the equation formulation. Section III presents the automated state equation generation method based on the switch model. Section IV presents the case studies of two 2 MW four-port solid-state transformers (SSTs) with the proposed method. Finally, the conclusion is drawn in Section V.

II. Modeling of Basic Switching Legs

Unlike some other methods focusing on the modeling of a single switching device, in this article, an *n*-level switching leg is considered to be the smallest unit of the converters to derive the semi–symbolic form of state equations under different switching states.

A. Half-Bridge

Fig. 3 illustrates the equivalent circuit of a half-bridge. The coupling relationship of the dc and ac side is presented by a pair of controlled current source *J* and voltage source *E* with a resistor *R*, where $v_E = k_1 v_J$, $i_J = k_2 i_E$, and $R = R_{\rm on}$ if ON-state resistance is considered. The ON-state resistances of the insulated gate bipolar transistor (IGBTs) and diodes are assumed all the same so that R remains constant. The coefficients of the controlled sources are dependent on the switching states, which are listed in Table I. Therefore, the influences of the switching states on the state equations are modeled by the coefficients with switching functions. The actual states of the switching devices can either be directly determined by the gate signals or by monitoring the switching currents and voltages and toggling the states of devices in violation [7], [10], [34], which is out of the scope of this article.

TABLE I
Coefficients Under Different States for Half-Bridge

Switching states [S_1, S_2]	Coefficients	
	k_1	k_2
[1, 0]	1	-1
[0, 1]	0	0

TABLE II
Coefficients Under Different States for Three-Level Diode-Clamped Leg

Switching states [S_1, S_2, S_3, S_4]	Output Level	Coefficients			
		k_1	k_2	k_3	k_4
[1, 1, 0, 0]	1	1	0	-1	0
[0, 1, 1, 0]	0	0	1	0	-1
[0, 0, 1, 1]	-1	0	0	0	0

In this model, the node injection current of the dc side and the output voltage level of the ac side are totally the same as the original circuit when the half-bridge is operated under continuous conduction mode. Therefore, the KVL and KCL equations under this modeling method are equivalent to the ideal switched model as long as the two switching devices are complementary.

All the topologies with the half-bridge as the smallest unit can be represented by the combinations of this model. Fig. 4 is an example of the equivalent circuit of the modular multilevel converter based on the model of half-bridge.

B. Three-Level Diode-Clamped Leg

Fig. 5 shows the equivalent circuit of the three-level diode-clamped leg. Similar to the modeling of half-bridge, two pairs of the controlled current sources and voltage sources along with a resistor are utilized to replace the original circuit. In an *n*-level diode-clamped leg, only some combinations of the gate signals are permitted. Relationships between the switching states, the output level and the coefficients are listed in Table II.

C. General Modeling Method of Typical Topologies

For other typical topologies like flying capacitor leg, the controlled source modeling method is still applicable. Fig. 6 is an example of the model for the three-level flying capacitor leg. Generally, the switching leg can be modeled as several pairs

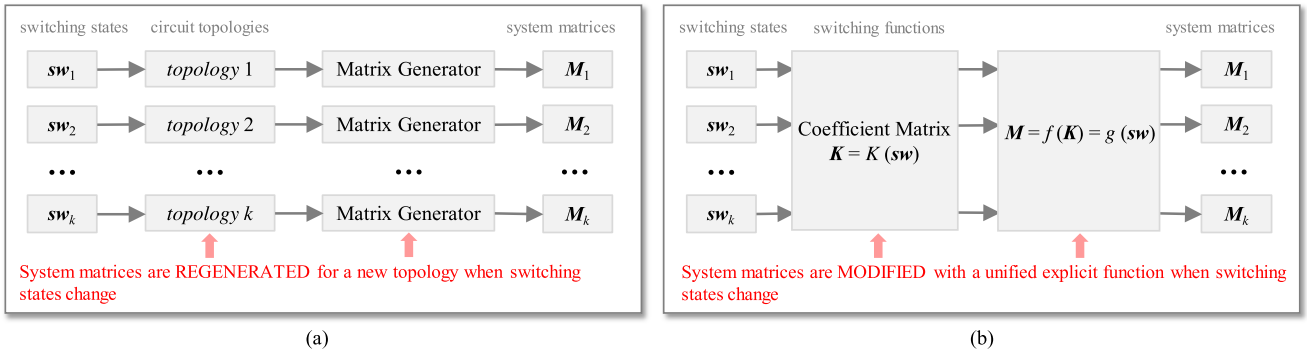

Fig. 2 (a) State equation generation and updating process with traditional method. (b) State equation generation and updating process with the proposed method.

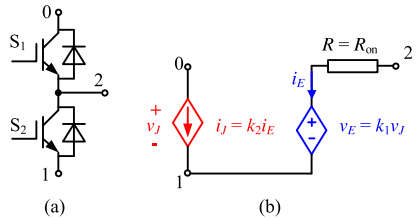

Fig. 3 Equivalent circuit of the half-bridge.

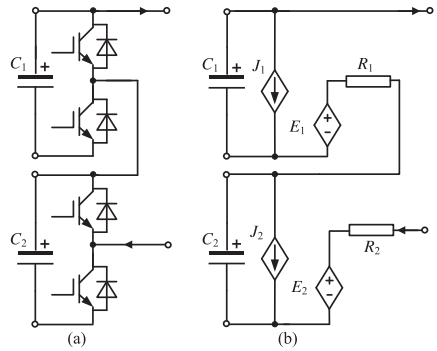

Fig. 4 Equivalent circuit of the modular multilevel converter.

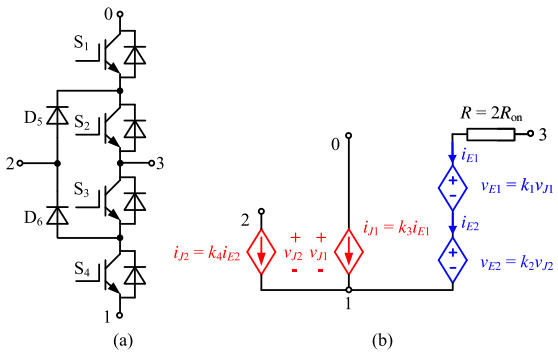

Fig. 5 Equivalent circuit of the three-level diode-clamped leg.

of controlled current sources and voltage sources along with an equivalent resistor if ON-state resistance is taken into account. Choosing the negative bus terminal as the reference, the voltage sources are in serial connection to model the output voltage level from the view of the ac side. Correspondingly, the current

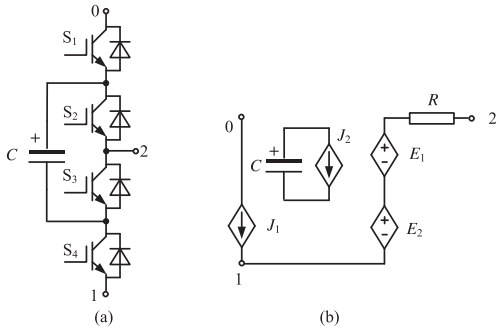

Fig. 6 Equivalent circuit of the three-level flying capacitor leg.

sources are injected into the nodes in the dc side or in parallel with the flying capacitors to model the influence of the loads. The coefficients of each controlled source can be looked up from the switching states table. Therefore, this modeling method is referred to as the "switching function model" in this article since the value of the controlled sources are written as the symbolic functions of switching states.

It should be noted that the controlled sources are only used for derivation of symbolic switching functions and do not act as real input variables in the simulation process, which will be further explained in Section III.

III. Automated State Equation Generation Method

In this section, the proposed automated state equation generation method is introduced. Section III-A illustrates the automated equation generation process based on the switching function models presented in Section II. Section III-B discusses the optimizing method for equation updating. And finally the analysis is given in Section III-C.

A. Automated Equation Generation Method Based on Switching Functions and Controlled Source Elimination

Power electronic systems can be modeled by a set of piecewise linear state-space equations

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{A}_k \boldsymbol{x} + \boldsymbol{B}_k \boldsymbol{u} \\ \boldsymbol{y} &= \boldsymbol{C}_k \boldsymbol{x} + \boldsymbol{D}_k \boldsymbol{u}. \end{aligned} \tag{2}$$

In above equations, $\boldsymbol{x}$ is an $n \times 1$ vector consisting of the independent state variables such as capacitor voltage and inductor current, $\boldsymbol{u}$ is an $m \times 1$ vector consisting of the system inputs such as power sources, $\boldsymbol{y}$ is an $l \times 1$vector consisting of the output variables, and the matrices $\boldsymbol{A}_k$, $\boldsymbol{B}_k$, $\boldsymbol{C}_k$, and $\boldsymbol{D}_k$ correspond to the kth permutation of switches and piecewise linear device segments.

Automated computer-aided construction of the system matrices of a given topology has been presented in [8]. This article will not illustrate the method in detail again but try to provide a systematic method of reconstructing the system matrices when the switching states change. To achieve this goal, all the converters consisting of the basic units are first replaced by the switching function model presented in Section III-A. Thus, the state equations can be rewritten as follows:

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{A}_0\boldsymbol{x} + \boldsymbol{B}_0\boldsymbol{u} + \boldsymbol{B}_s\boldsymbol{u}_s \\ \boldsymbol{y} &= \boldsymbol{C}_0\boldsymbol{x} + \boldsymbol{D}_0\boldsymbol{u} + \boldsymbol{D}_s\boldsymbol{u}_s \end{aligned} \tag{3}$$

where $\boldsymbol{u}_s$ is a $p \times 1$ vector composed of two parts: the equivalent controlled voltage source, and the current source

$$\boldsymbol{u}_s = \begin{bmatrix} \boldsymbol{v}_{E_s} \\ \boldsymbol{i}_{J_s} \end{bmatrix}. \tag{4}$$

On the other hand, $\boldsymbol{u}_s$ can be represented by multiples of the controlling variables according to the modeling method in Section II

$$\boldsymbol{u}_s = \begin{bmatrix} \boldsymbol{v}_{E_s} \\ \boldsymbol{i}_{J_s} \end{bmatrix} = \begin{bmatrix} \boldsymbol{K}_{E_k} & \\ & \boldsymbol{K}_{J_k} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{J_s} \\ \boldsymbol{i}_{E_s} \end{bmatrix} = \boldsymbol{K}_k\boldsymbol{y}_s \tag{5}$$

where $\boldsymbol{K}_{E_k}$, $\boldsymbol{K}_{J_k}$, and $\boldsymbol{K}_k$ are all diagonal matrices. The values in $\boldsymbol{K}_k$ can be looked up from the switching states table, thus the matrix is the function of the switching states vector $\boldsymbol{sw}_k$

$$\boldsymbol{K}_k = \boldsymbol{K}\left(\boldsymbol{sw}_k\right). \tag{6}$$

Representing the controlling variables $\boldsymbol{y}_s$ by the output equation, we have

$$\boldsymbol{y}_s = \boldsymbol{E}\boldsymbol{x} + \boldsymbol{F}\boldsymbol{u} + \boldsymbol{F}_s\boldsymbol{u}_s. \tag{7}$$

Substituting (7) to (5), we have

$$\boldsymbol{u}_s = \left(\boldsymbol{I} - \boldsymbol{K}_k\boldsymbol{F}_s\right)^{-1}\boldsymbol{K}_k\left(\boldsymbol{E}\boldsymbol{x} + \boldsymbol{F}\boldsymbol{u}\right). \tag{8}$$

Therefore, the state equations only containing the original input variables can be written as follows:

$$\begin{aligned} \dot{\boldsymbol{x}} = &\left[\boldsymbol{A}_0 + \boldsymbol{B}_s(\boldsymbol{I} - \boldsymbol{K}_k\boldsymbol{F}_s)^{-1}\boldsymbol{K}_k\boldsymbol{E}\right]\boldsymbol{x} \\ &+ \left[\boldsymbol{B}_0 + \boldsymbol{B}_s(\boldsymbol{I} - \boldsymbol{K}_k\boldsymbol{F}_s)^{-1}\boldsymbol{K}_k\boldsymbol{F}\right]\boldsymbol{u} \\ \boldsymbol{y} = &\left[\boldsymbol{C}_0 + \boldsymbol{D}_s(\boldsymbol{I} - \boldsymbol{K}_k\boldsymbol{F}_s)^{-1}\boldsymbol{K}_k\boldsymbol{E}\right]\boldsymbol{x} \\ &+ \left[\boldsymbol{D}_0 + \boldsymbol{D}_s(\boldsymbol{I} - \boldsymbol{K}_k\boldsymbol{F}_s)^{-1}\boldsymbol{K}_k\boldsymbol{F}\right]\boldsymbol{u}. \end{aligned} \tag{9}$$

In (9), only the diagonal matrix $\boldsymbol{K}_k$ contains symbols, which is dependent on the switching states, while all the other matrices are constant. Therefore, this method is referred to as "semi–symbolic" since the influences of the other element parameters are not given in the symbolic form. With this method, the system matrices can be written as an explicit function of switching states

$$\boldsymbol{M}_k = f_{\boldsymbol{M}}\left(\boldsymbol{K}_k\right) = g_{\boldsymbol{M}}\left(\boldsymbol{sw}_k\right) \tag{10}$$

where $\boldsymbol{M}$ can refer to the system matrices $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, or $\boldsymbol{D}$.

Since no estimation or one-step delay is involved and the KVL and KCL equations have the same forms with the original circuit under this method, the final results are exactly the same as the ideal switched model while there is no need to restart the topology identification process to get the system matrices when the switching states change. Therefore, the proposed method is more efficient than the traditional way without introducing extra errors during the modeling process.

B. Optimized Equation Updating Method Based on the Operating Characteristics and Topological Information

Equation (9) provides a general way to update the system matrices when the switching states and the corresponding coefficient matrix $\boldsymbol{K}_k$ change. However, in most cases, at each step just a few switching devices change their states in power electronic systems. Therefore, only a small part of the elements in the coefficient matrix are different from the previous one and it is not the best way to recalculate the whole system matrices. The most efficient method is to accurately locate the influences of each switching device on the matrix elements like the symbolic expression. Although pure symbolic operation is not realistic, the semi–symbolic function given in this article has the potential for the simplification of calculation. By observing (9), it is easy to find that the coefficient matrix $\boldsymbol{K}_k$ is a diagonal matrix and the highest computational cost lies in the calculation of $(\boldsymbol{I} - \boldsymbol{K}_k\boldsymbol{F}_s)^{-1}$. If the matrix $\boldsymbol{F}_s$ has some special properties which can simplify the matrix conversion operation, the equation updating process can be further optimized.

Actually, in power electronic systems, the dc side of the switching leg is typically in parallel with a capacitor or an independent voltage source and the output terminal is typically in serial connection with an inductor. With such topological characteristics, the output variables can be represented by the linear combination of a few state variables and input variables exclusively. Therefore, the condition that $\boldsymbol{F}_s = \boldsymbol{0}$ holds in most cases. Taking the matrix $\boldsymbol{A}_k$ as an example, the expression of $\boldsymbol{A}_k$ can be simplified to

$$\boldsymbol{A}_k = \boldsymbol{A}_0 + \boldsymbol{B}_s\boldsymbol{K}_k\boldsymbol{E}. \tag{11}$$

Then, we consider the situation when only parts of $\boldsymbol{K}_k$ are different after the switching events happen. Assuming that the first element of $\boldsymbol{K}_k$ changes from k_{11} to $k_{11} + \Delta k_{11}$ without the loss of generality, the changes of A_k can be expressed by the following:

$$\Delta\boldsymbol{A}_k = \boldsymbol{B}_s\begin{bmatrix} \Delta k_{11} & \\ & \boldsymbol{0}_{(p-1)\times(p-1)} \end{bmatrix}\boldsymbol{E} = \Delta k_{11}\boldsymbol{b}_{s1}{\boldsymbol{e}_1}^{\mathrm{T}} \tag{12}$$

where $\boldsymbol{b}_{s1}$ is the first column vector of matrix $\boldsymbol{B}_s$ and ${\boldsymbol{e}_1}^{\mathrm{T}}$ is the first row vector of matrix $\boldsymbol{E}$. The computational cost can be further reduced if considering the sparsity of ${\boldsymbol{e}_1}^{\mathrm{T}}$, which can

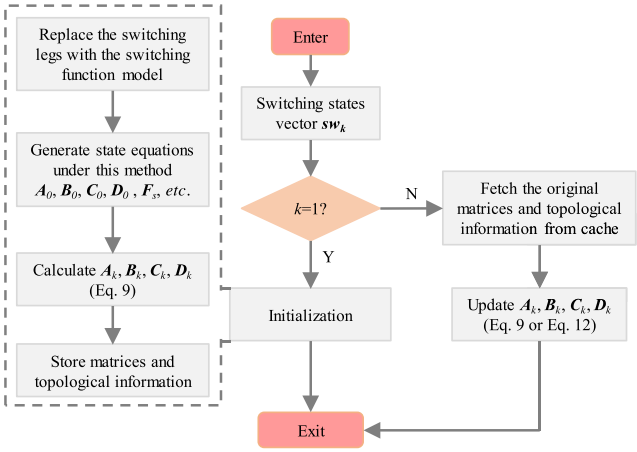

Fig. 7 Flowchart of the proposed method.

also be known from the topological information of the original systems.

C. Discussions

The proposed method provides a systematic method to generate and update the state equation matrices. Switching function modeling of basic switching legs and controlled source elimination are the core highlights in this method. Besides, topological characteristics are fully utilized to minimize the computational cost. It can be easily implemented in simulation software and is also suitable for theoretical analysis as this method provides an explicit function from the switching states to the system matrices in a unified form.

The flowchart of the proposed method is presented in Fig. 7. Compared with the traditional method using the ideal model, the proposed method only needs to identify the topology and generate the system matrices with the equivalent controlled source as input variables once during initialization. The updating of the matrices can be completed by (9) or (12) with a unified semi–symbolic form, while the traditional method needs to repeat the whole generation process from the very beginning since the topology has been changed. In addition, the proposed method exploits the operating and topological characteristics of the power electronic systems to further simplify the calculation. In most cases where the optimization conditions of (12) are satisfied, the influences of the state of a single switching device on the state equation matrices can be accurately limited to several specific elements in the matrices, as can been seen from (12). The updating of the matrices only involves a few steps of multiplications and additions and no other complicated matrix operations are needed. As the single-step computational cost is not very high, in some cases where the space complexity is taken into account, it is even possible to update the matrices each time according to the switching states instead of storing all the existing matrices.

However, there are still some limitations in this method. When implemented in the software, since the n-level switching legs are defined as the smallest units, they should be prebuilt in the library browser as basic elements. Otherwise, if the converters are built by discrete switching devices, they cannot be modeled automatically by the semi–symbolic function for acceleration. But the modeling idea remains applicable to some unusual topologies. For other user-defined converters, if the switching function modeling method is still valid, users can provide the relationships between switching states and coefficient matrices themselves. Then, the proposed equation formulation method can be utilized as well to simplify the generation and updating of system matrices.

Another limitation is that the switching function modeling is only valid for normal operating conditions. For half-bridges, the switching states must be 10 or 01. For three-level diode-clamped switching legs, the switching states must be 1100, 0110, or 0011 as listed in Tables I and II. However, in some cases, like the discontinuous conduction mode in the buck converter where both switching devices are OFF, the switching function model is not applicable. Therefore, during simulation, for a given n-level switching leg, we will first check whether the switching function model can be used with the current switching states. If not, the traditional ideal switched model is used instead, and then a new series of the matrices under this topology is generated. In addition, the above method is concentrated on the modeling of voltage source converters. Under this modeling method, circuit elements with current source behavior cannot be in serial connection with the equivalent current sources and elements with voltage source behavior cannot be in parallel connection with the equivalent voltage sources. However, there are no extra requirements for the properties of the dc capacitor or the loads. Capacitors with ESR or resistive loads are also valid with this model and will not introduce any error due to the previous analysis.

IV. Case Study and Result Analysis

In this section, the proposed state equation generation method is applied to simulate two operating modes of 2 MW four-port SSTs upon the DSED framework. The SST cases with complicated structures and numerous switching devices are typical examples of high-power applications. When simulating such systems, it is not practical and efficient to store all the possible matrices like what is done in small-scale systems. Therefore, the two cases are chosen to verify the accuracy and efficiency of the proposed method in simulating large-scale power electronic systems.

This section is organized as follows. Section IV-A introduces the topologies and operating modes of the two cases. Section IV-B verifies the accuracy of the proposed method by comparisons with the commercial software. Section IV-C analyzes the efficiency of the proposed method in simulating large-scale systems.

A. Test Cases

The SST has been regarded by many researchers as one of the key components in the future smart grid for the integration of distributed generation and storage [35]–[37]. In this article, the studied cases contain a 2 MW SST with four ports: a 10 kV high-voltage ac (HVAC) port, a 10 kV high-voltage dc (HVDC) port, a 380 V three-phase low-voltage ac (LVAC) port and a $\pm$375 V low-voltage dc (LVDC) port. With isolation among

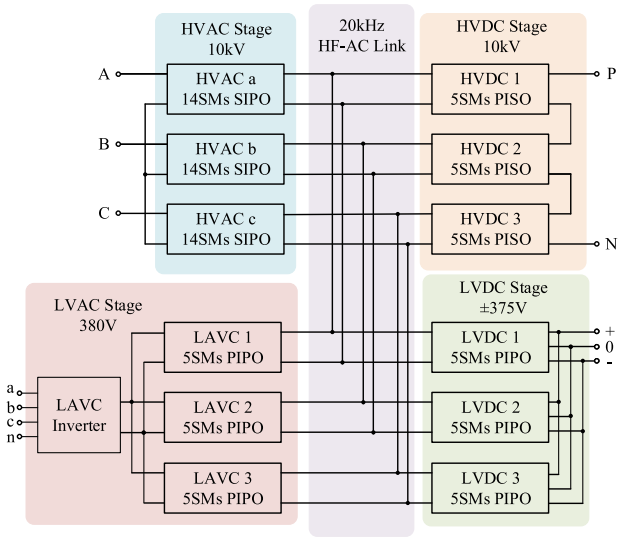

Fig. 8 Topology of a single 2MW 4-Port SST. SIPO denotes series input parallel output, PISO denotes parallel input series output and PIPO denotes parallel input parallel output.

TABLE III
SYSTEM INFORMATION OF THE SOLID-STATE TRANSFORMER

Components and parameters of a single SST		
Number of switching devices	IGBT	32
	SiC MOSFET	544
	Total	576
Number of sub-modules (SMs)	HVAC stage	42
	HVDC stage	15
	LVAC stage	15
	LVDC stage	15
	Total	87
Number of high-frequency transformers (HFTs)	72	
Highest modulation frequency	20kHz	

all ports and support for bidirectional power flow, the SST can act as a powerful interface device to integrate various sources and loads, especially renewable generation in the future energy internet.

The topology of the SST is illustrated in Fig. 8. Each stage is composed of several submodules. Numerous cascaded H-bridges, high-frequency transformers (HFTs), and a 20 kHz HFAC link proposed in [38] are utilized in this case. Detailed information of the components in the SST is listed in Table III. With 576 switching devices and 87 submodules in a single SST, the scale of the whole system is extremely large, which brings great challenges to the simulation.

Two operating modes are simulated to verify the accuracy and efficiency of the proposed method.

1) *Load changes of a single SST:* In this case, a 0.15 s dynamic process is simulated. All the dc bus capacitors are precharged to the reference value (rated voltage) before the simulation starts. When $t = 0$ s, the SST is started with 1/6 MW LVAC load. 200 kW LVDC load and 250 kW HVDC load are added when $t = 0.05$ s and $t = 0.1$ s, respectively.
2) *Two SSTs operating in the master/slave mode:* In this case, two SSTs are operating in the master/slave mode. The master SST controls the port voltage while the slave SST controls the port current. As illustrated in Fig. 9, 1 MW power flows from the grid side to the HVAC port of SST1. The LVDC, HVDC, and LVAC ports of the two SSTs are connected together, with 500, 250, and 250 kW power flowing from SST1 to SST2, respectively. And finally 1 MW power flows out of the HVAC port of SST2 back to the grid side. All the dc bus capacitors are precharged to the reference value before $t = 0$ and a 0.1 s dynamic process is simulated.

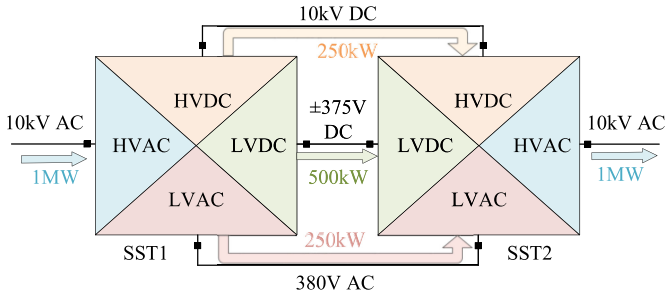

Fig. 9 Structures of two SSTs operating in the master/slave mode.

B. Comparisons of the Simulated Results

The two cases are simulated under the DSED framework with the traditional ideal switched model (switches are modeled as small resistors during ON-state and open circuits during OFF-state) and with the proposed method, respectively. Simulated results with the ideal switched model in one of the fastest commercial software for power electronic system simulation, are chosen as the reference. The maximum step size is 1e–3 s and the relative tolerance is 1e–4 in both DSED framework and the commercial software.

Waveforms of the two test cases are presented in Figs. 10 and 11. It can be observed that, in both cases, the simulated results under the DSED framework with the proposed method are exactly the same with the waveforms simulated with the traditional method, since the final system matrices of the two methods are equivalent according to the analysis in Section III. When compared with the reference waveforms given by commercial software, it can be seen that the simulated results of the three methods are in great agreement, both for the millisecond-order waveforms such as the voltage of HVDC port in Fig. 10(b) and the microsecond-order switching ripples such as the current of the HFT in Fig. 11(c).

Quantitative analysis of the relative error is listed in Table IV. The error calculation equation is given by the following equation:

$$\mathrm{Error}_{\mathrm{rel}} = \frac{\|\boldsymbol{y}_{\mathrm{sim}} - \boldsymbol{y}_{\mathrm{ref}}\|_2}{\|\boldsymbol{y}_{\mathrm{ref}}\|_2} \tag{13}$$

where $\mathrm{Error}_{\mathrm{rel}}$ is the relative error, $\boldsymbol{y}_{\mathrm{sim}}$ is the simulated waveform vector, $\boldsymbol{y}_{\mathrm{ref}}$ is the reference vector, and $\|\cdot\|_2$ is the operator of the Euclidean norm.

It can be seen from Table IV that even for the HFT current, which has the highest frequency (20 kHz) in the system and is the most difficult to accurately simulate, the relative error of the

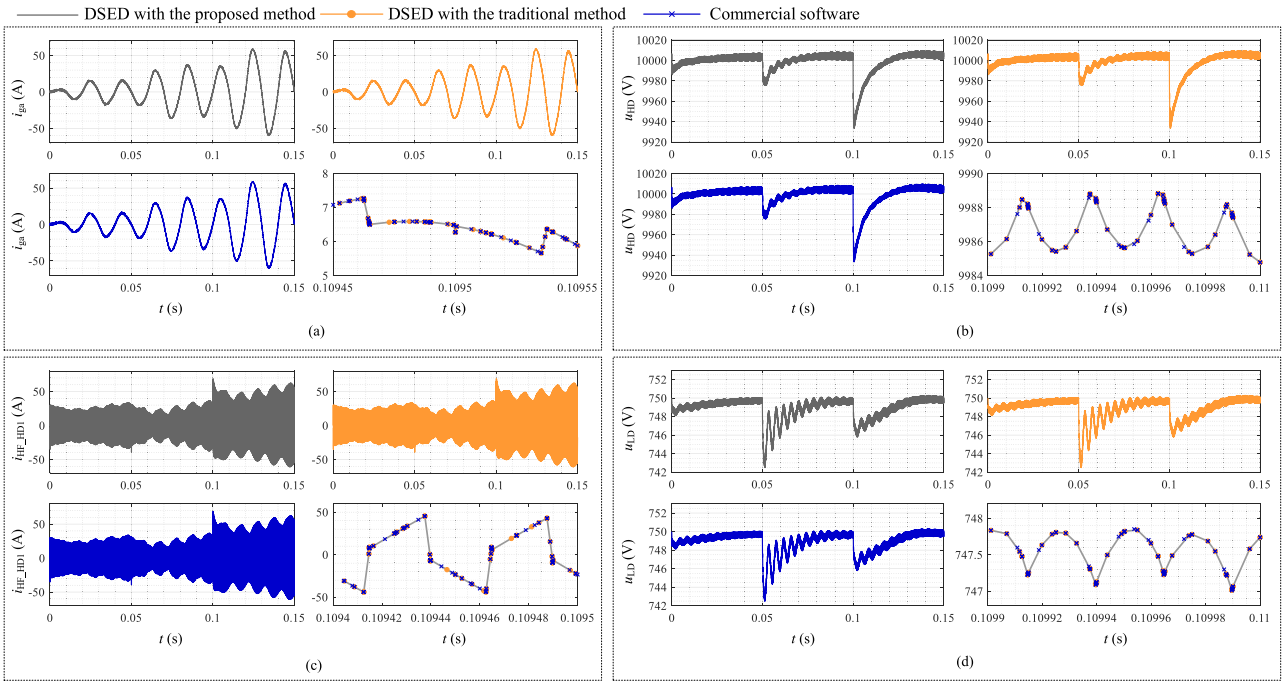

Fig. 10 Comparisons of the simulated results of a single SST by different methods. Zoomed-in view is placed in the lower right corner of each subfigure. (a) Grid-side phase current iga of HVAC port. (b) Output voltage uHD of HVDC port. (c) HFT current of SM1 in HVDC stage. (d) Output voltage uLD of LVDC port.

TABLE IV
RELATIVE ERRORS OF SIMULATED RESULTS UPON DSED FRAMEWORK COMPARED WITH COMMERCIAL SOFTWARE

Test case	Measured waveform	Relative error
Single SST, 0.15s dynamic process	HVAC grid-side phase current	3.87e-5
	HVDC output voltage	6.85e-4
	HVDC HFT current	1.34e-5
	LVDC output voltage	2.18e-5
Double SSTs, 0.1s dynamic process	SST1 HVDC output current	5.89e-4
	SST1 LVDC output voltage	5.96e-5
	SST2 HVAC HFT current	5.65e-4
	SST2 LVAC output current	2.60e-4

TABLE V
SYSTEM SCALES AND PROPERTIES OF THE TWO CASES

	Test case 1	Test case 2
Number of switching devices	576	1152
Number of basic switching legs	288	576
Number of power sources	3	6
Number of capacitors	105	210
Number of inductors	166	331
Number of resistors	79	150
Number of independent state variables	183	365
Number of output variables (measured by sensors or probes)	134	256

proposed method with DSED framework is only 6.85e–4, which confirms the accuracy of the proposed method.

C. Comparisons of the Simulation Efficiency

When evaluating the simulation efficiency of the proposed method with the DSED framework, same level of accuracy must be ensured when compared with commercial software for fairness. When decreasing the relative error tolerance of commercial software from 1e–4 to 1e–6, the simulated results are almost the same while the CPU time increases. The same applies to the results with the DSED framework. Therefore, in the efficiency test, both simulation tools utilize the setting of 1e–3 s maximum step size and 1e–4 relative error tolerance.

The DSED framework with two different state equation generation methods is programmed in C++. All the parts are totally the same except for the generation and updating of system matrices to evaluate the contribution of the proposed method independently. Similar to what has been done in the commercial software, with the traditional way, when a switching event occurs, the calculation of a new set of state equation matrices is initiated or the simulator fetches the previously calculated results from cache. With the proposed method, the matrices are updated each time without storage.

Detailed descriptions of the two studied cases are given in Table V in order to provide more information about the system scales and mathematical properties since the speed of state equation generation is greatly influenced by the size of the matrices. Table VI lists the results of efficiency tests with different simulation methods in the two cases. All the simulations are performed in the same computer environment with a 3.00 GHz Intel Xeno Gold 6316 CPU core and 512G memory.

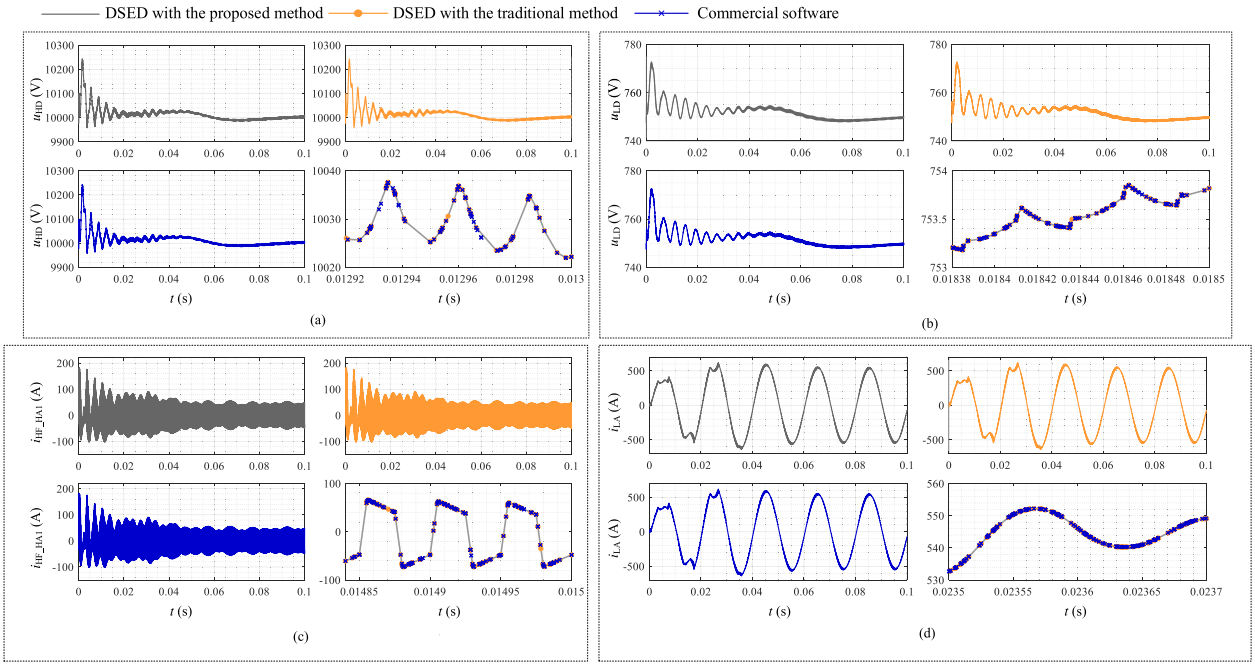

Fig. 11 Comparisons of the simulated results of double SSTs by different methods. Zoomed-in view is placed in the lower right corner of each subfigure. (a) Output voltage uHD of SST1 HVDC port. (b) Output voltage uLD of SST1 LVDC port. (c) HFT current of SM1 in SST2 HVAC stage. (d) Output current iLA of SST2 LVAC port.

TABLE VI
EFFICIENCY TEST RESULTS OF THE TWO CASES

		DSED with the proposed method	DSED with the traditional method	Commercial software
Simulation settings	Maximum step-size	1e-3s	1e-3s	1e-3s
	Relative error tolerance	1e-4	1e-4	1e-4
Test case 1	Simulation end time	0.15s	0.15s	0.15s
	CPU time	**28s**	**23min**	**5h24min**
	Normalized CPU time	**1**	**49.2**	**694.3**
	Number of calculated points	119254	119254	181453
	Time per step	2.35e-4s	1.15e-2s	1.07e-1s
Test case 2	Simulation end time	0.1s	0.1s	0.1s
	CPU time	**1min50s**	**3h28min**	**38h22min**
	Normalized CPU time	**1**	**113.5**	**1255.6**
	Number of calculated points	126592	126592	211225
	Time per step	8.69e-4s	9.86e-2s	6.54e-1s

It can be observed from Table VI that in the first case, about 700-fold acceleration is achieved in total compared with commercial software and the proposed method contributes 50-fold acceleration. In the second case with a larger scale and more switching devices, the acceleration of the DSED framework with the proposed method reaches up to about 1200-fold and the improvement brought by the proposed method is increased to about 110-fold. The above results confirm the efficiency of the proposed method in simulating power electronic systems, especially in large-scale systems.

IV. CONCLUSION

An automated semi–symbolic state equation generation and updating method is proposed in this article for simulation and analysis of power electronic systems. Based on the perspectives of module combination, basic switching legs in power electronic systems are treated as the smallest units to derive the symbolic switching functions. A unified semi–symbolic form of state equation matrices is given, providing an explicit function from switching states to system matrices. The final numerical results are totally the same with the matrices generated by traditional way with the ideal switched model, while the computational cost for updating matrices when the switching states change is greatly reduced. Full utilization of the operating and topological characteristics of power electronic systems can further optimize the equation updating process and minimize the calculation time.

This method is an extension of the recently proposed DSED framework in the aspect of computer implementation to develop

it toward practical simulation software. In this article, two cases of the megawatts SSTs are simulated with the proposed method upon the DSED framework. About 700-fold and 1200-fold acceleration is achieved in total compared with commercial software under the same level of accuracy, where the proposed method contributes 50-fold and 110-fold acceleration in the two cases, respectively. In conclusion, the proposed method provides an efficient and systematic way to generate and update the state equation matrices, thus benefiting the analysis and simulation of power electronic systems, especially for large-scale systems.

REFERENCES

[1] M. Senesky, G. Eirea, and T. J. Koo, "Hybrid modelling and control of power electronics," in *Hybrid Systems: Computation and Control*. Berlin, Germany: Springer, 2003, pp. 450–465.

[2] A. J. Van Der Schaft and J. M. Schumacher, *An Introduction to Hybrid Dynamical Systems*, vol. 251. London, U.K.: Springer, 2000.

[3] B. Li, Z. Zhao, Y. Yang, Y. Zhu, and Z. Yu, "A novel simulation method for power electronics: Discrete state event driven method," *CES Trans. Elect. Mach. Syst.*, vol. 1, no. 3, pp. 273–282, Sep. 2017.

[4] Y. Zhu, Z. Zhao, B. Shi, and Z. Yu, "Discrete state event-driven framework with a flexible adaptive algorithm for simulation of power electronic systems," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11692–11705, Dec. 2019.

[5] Powersim Inc., PSIM User Manual, Version 12.0, 2020. [Online]. Available: https://powersimtech.com/support/resources/tutorials/psim-user-manual/

[6] MathWorks Inc., Simulink user's guide R2020a, 2020. [Online]. Available: https://www.mathworks.com/help/pdf_doc/simulink

[7] Plexim GmbH., PLECS User Manual, Version 4.3.6, 2020. [Online]. Available: https://www.plexim.com/download/documentation

[8] L. O. Chua, *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1975.

[9] C. Dufour, J. Mahseredjian, and J. Bélanger, "A combined state-space nodal method for the simulation of power system transients," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 928–935, Apr. 2011.

[10] A. Massarini, U. Reggiani, and M. K. Kazimierczuk, "Analysis of networks with ideal switches by state equations," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 44, no. 8, pp. 692–697, Aug. 1997.

[11] A. Massarini and U. Reggiani, "An efficient algorithm for the formulation of state equations and output equations for networks with ideal switches," in *Proc. IEEE Int. Symp. Circuits Syst.*, May. 2001, vol. 3, pp. 521–524.

[12] J. Jatskevich and T. Aboul-Seoud, "Automated state-variable formulation for power electronic circuits and systems," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, pp. V-952–V-955.

[13] S. Y. R. Hui and C. Christopoulos, "A discrete approach to the modeling of power electronic switching networks," *IEEE Trans. Power Electron.*, vol. 5, no. 4, pp. 398–403, Oct. 1990.

[14] P. Pejovic and D. Maksimovic, "A method for fast time-domain simulation of networks with switches," *IEEE Trans. Power Electron.*, vol. 9, no. 4, pp. 449–456, Jul. 1994.

[15] E. Van Dijk, J. N. Spruijt, D. M. O'Sullivan, and J. B. Klaassens, "PWM-switch modeling of DC-DC converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 659–665, Nov. 1995.

[16] J. Chen and K. D. T. Ngo, "Simplified analysis of PWM converters operating in discontinuous conduction mode using alternate forms of the PWM switch models," in *Proc. IEEE SoutheastCon 2000. "Preparing for The New Millennium,"* Apr. 2000, pp. 505–509.

[17] D. Maksimovic, A. M. Stankovic, V. J. Thottuvelil, and G. C. Verghese, "Modeling and simulation of power electronic converters," *Proc. IEEE*, vol. 89, no. 6, pp. 898–912, Jun. 2001.

[18] N. Ahmed *et al.*, "Efficient modeling of an MMC-based multiterminal DC system employing hybrid HVDC breakers," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 1792–1801, Aug. 2015.

[19] Y. M. Lai, C. K. Tse, and Y. S. Lee, "A systematic method for computer-aided modelling of switching DC/DC converters," in *Proc. IEEE Region 10 Int. Conf. Comput., Commun. Automat.*, Oct. 1993, vol. 5, pp. 518–521.

[20] O. Wasynczuk and S. D. Sudhoff, "Automated state model generation algorithm for power circuits and systems," *IEEE Trans. Power Syst.*, vol. 11, no. 4, pp. 1951–1956, Nov. 1996.

[21] K. Altun, B. E. Platin, and T. Balkan, "Systematic state equation derivation for linear systems using the normal tree method," in *Proc. Int. Mech. Eng. Congr. Expo.*, 2003, pp. 869–877.

[22] R. J. Dirkman, "The simulation of general circuits containing ideal switches," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1987, pp. 185–194.

[23] G. Reißig, "Extension of the normal tree method," *Int. J. Circuit Theory Appl.*, vol. 27, no. 2, pp. 241–265, Mar. 1999.

[24] A. Lekić, "Automated DC-DC converters symbolic state-space model generation by the use of free software," in *Proc. 22nd Telecommun. Forum Telfor (^{TEL}FOR)*, Nov. 2014, pp. 995–998.

[25] S. R. Bowes and J. C. Clare, "Computer-aided design of PWM power-electronic variable-speed drives," *IEE Proc. B, Elect. Power Appl.*, vol. 135, no. 5, pp. 240–260, Sep. 1988.

[26] H. Takano, T. Domoto, T. Hatakeyama, and M. Nakaoka, "A generic computer-aided simulation approach for digitally-controlled switching mode power converter circuits and systems," in *Proc. 6th Int. Conf. Power Electron. Variable Speed Drives*, Sep. 1996, pp. 483–489.

[27] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1976, pp. 18–34.

[28] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 251–259, Apr. 1991.

[29] L. Salazar and G. Joos, "PSPICE simulation of three-phase inverters by means of switching functions," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 35–42, Jan. 1994.

[30] H. Le-Huy, G. Sybille, R. Gagnon, and V. Q. Do, "Real-time simulation of PWM power converters in a doubly-fed induction generator using switching-function-based models," in *Proc. 32nd Annu. Conf. IEEE Ind. Electron.*, Nov. 2006, pp. 1878–1883.

[31] H. Jin, "Behavior-mode simulation of power electronic circuits," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 443–452, May 1997.

[32] J. Allmeling and N. Felderer, "Sub-cycle average models with integrated diodes for real-time simulation of power converters," in *Proc. IEEE Southern Power Electron. Conf.*, Dec. 2017, pp. 1–6.

[33] B. Shi, Z. Zhao, and Y. Zhu, "Piecewise analytical transient model for power switching device commutation unit," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5720–5736, Jun. 2019.

[34] D. Bedrosian and J. Vlach, "Time-domain analysis of networks with internally controlled switches," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 39, no. 3, pp. 199–212, Mar. 1992.

[35] A. Q. Huang and J. Baliga, "FREEDM System: Role of power electronics and power semiconductors in developing an energy internet," in *Proc. 21st Int. Symp. Power Semicond. Devices IC's*, Jun. 2009, pp. 9–12.

[36] S. Falcones, R. Ayyanar, and X. Mao, "A DC–DC multiport-converter-based solid-state transformer integrating distributed generation and storage," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2192–2203, May 2013.

[37] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.

[38] K. Li, Z. Zhao, L. Yuan, C. Zhang, W. Wen, and J. Sun, "Synergetic control of high-frequency-link based multi-port solid state transformer," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2018, pp. 5630–5635.

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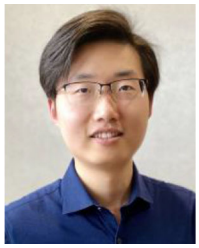

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