A Variable-Frequency Current-Dependent Switching Strategy to Improve Tradeoff Between Efficiency and SiC MOSFET Overcurrent Stress in Si/SiC-Hybrid-Switch-Based Inverters

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***Abstract*—Reliability remains an issue for the Si/SiC hybrid switch adopting the conventional switching strategy of the internal SiC MOSFET that turns ON earlier, and OFF later. Such issue is attributable to the overcurrent stress under the heavy load operating condition, which adversely affects the SiC MOSFET during the gate delay time. To solve this problem without increasing the extra power loss, a novel variable-frequency current-dependent switching strategy combining the variable switching pattern strategy, and the variable pulsewidth modulation (PWM) frequency strategy is proposed. Variable switching pattern strategy can avoid the overcurrent stress of the SiC MOSFET at the heavy load operating condition, and the designed optimal delay time in different switching patterns can achieve the compromise between the excellent reliability, and the power loss of Si/SiC hybrid switch. Variable PWM frequency strategy can effectively reduce the switching loss of the Si/SiC hybrid switch by decreasing the switching frequency around the peak current region. An Si/SiC-hybrid-switch-based single-phase inverter platform is constructed and tested. Test results show that the power loss of the single-phase inverter adopting such switching strategy outperforms the current-dependent switching strategy with 9.4% reduction of power loss, and overcurrent stress of SiC MOSFET is avoided.**

***Index Terms*—Inverters, losses, power semiconductor switches, reliability.**

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I. Introduction

Si/SiC hybrid switch comprising a large current rating Si IGBT and a small current rating SiC MOSFET in parallel offers excellent advantages in the tradeoff between performance and cost, which makes it attractive for high-performance and low-cost power converters [1]–[7]. Generally, the internal SiC MOSFET should be turned ON earlier and turned OFF later than the internal Si IGBT in order to minimize the switching loss of the Si/SiC hybrid switch [8]–[11]. During the gate delay time, the load current will flow through the SiC MOSFET, which is larger than the current rating of the SiC MOSFET under the heavy load operating condition. When the overcurrent exceeds the safe operating area (SOA) current of the SiC MOSFET, the reliability of the Si/SiC hybrid switch adopting this conventional switching strategy will be greatly reduced [12], [13].

Most previous research works mainly focused on reducing the power loss of the Si/SiC hybrid switch to achieve its reliability improvement [14]–[17]. In [14] and [15], the power loss models of the Si/SiC hybrid switch are derived as a function of the gate delay time, and several gate delay time switching strategies are proposed to reduce power loss of the Si/SiC hybrid switch, including the gate control optimization strategy with the thermal balance control mode [14] and the active gate delay time control strategy with the electrothermal coupling loss model [15]. In [16] and [17], the new gate drive patterns are proposed to reduce the power loss by means of multiple commutating the currents between two internal devices of the Si/SiC hybrid switch during each switching cycle. Therefore, the junction temperature reduction and the junction temperature balance of each device inside the Si/SiC hybrid switch can be achieved by these methods. However, these switching strategies cannot prevent the reliability issue of the internal small current SiC MOSFET caused by the overcurrent stress. Some restrictions on the adoption of the small current rating SiC MOSFET and size ratio selection of two internal switches inside the Si/SiC hybrid switch are induced by them, which greatly sacrifices the cost-effectiveness of the Si/SiC hybrid switch.

In order to effectively eliminate the adverse influence of the overcurrent stress on the SiC MOSFET under the heavy load

operating condition, a current-dependent switching strategy for the Si/SiC-hybrid-switch-based single-phase inverter is proposed [12], [13]. Three kinds of different switching patterns are adopted for the Si/SiC hybrid switch under various current levels. The power loss of the Si/SiC hybrid switch is minimized by means of two switching patterns at the light and medium load operating condition. In the third switching pattern, the large current rating Si IGBT is turned ON earlier and turned OFF later to effectively eliminate the overcurrent of SiC MOSFET at the heavy load operating condition. However, the efficiency of the inverter adopting this current-dependent switching strategy is greatly reduced because the switching loss of the Si/SiC hybrid switch at the heavy load operating condition is almost as large as that of pure IGBT solution. Meanwhile, the influence of the gate delay time in different switching patterns on the tradeoff performance between the overcurrent stress of the SiC MOSFET and power loss of the Si/SiC hybrid switch has not been extensively studied.

In order to solve these problems, a novel variable-frequency current-dependent switching strategy comprising the variable switching pattern strategy and the variable pulsewidth modulation (PWM) frequency strategy is proposed. Variable switching pattern strategy is implemented to avoid the overcurrent stress of the SiC MOSFET at the heavy load operating condition, and the optimal delay time in different switching patterns is designed to achieve the tradeoff performance between the excellent reliability of the SiC MOSFET and power loss of the Si/SiC hybrid switch. Variable PWM frequency strategy is implemented to effectively reduce the switching loss of the Si/SiC hybrid switch without significantly increasing the current harmonics by means of the drop of the switching frequency value around the peak current region. Therefore, both the optimal efficiency of the Si/SiC-hybrid-switch-based inverter and reliability improvement of the SiC MOSFET can be achieved. The rest of this article is organized as follows. In the Section II, the structure of the Si/SiC-hybrid-switch-based single-phase inverter is presented at first. Then, the overcurrent stress of the SiC MOSFET is analyzed. In the Section III, a novel variable-frequency current-dependent switching strategy is proposed. Meanwhile, the influence of the delay time on the power loss of the Si/SiC hybrid switch is analyzed. Experiment results are presented to validate the variable-frequency current-dependent switching strategy in the Section IV. Finally, Section V concludes this article.

II. SiC MOSFET Overcurrent Stress Concerns

In this section, the structure of the Si/SiC-hybrid-switch-based single-phase inverter is presented, and the overcurrent stress of the SiC MOSFET adopting the conventional switching strategy is discussed. The details are shown as follows.

A. Structure of the Si/SiC-Hybrid-Switch-Based Single-Phase Inverter

The topology of the Si/SiC-hybrid-switch-based single-phase inverter is shown in Fig. 1. I_o, I_{SOA}, L_n $(n = 1, 2)$, C, R, U_{dc}, U_o, and S_n $(n = 1, 2, 3, 4)$ represent the output current (load current), amplitude of the SiC MOSFET's SOA current, filter inductance, filter capacitor, load, dc voltage, output voltage, and

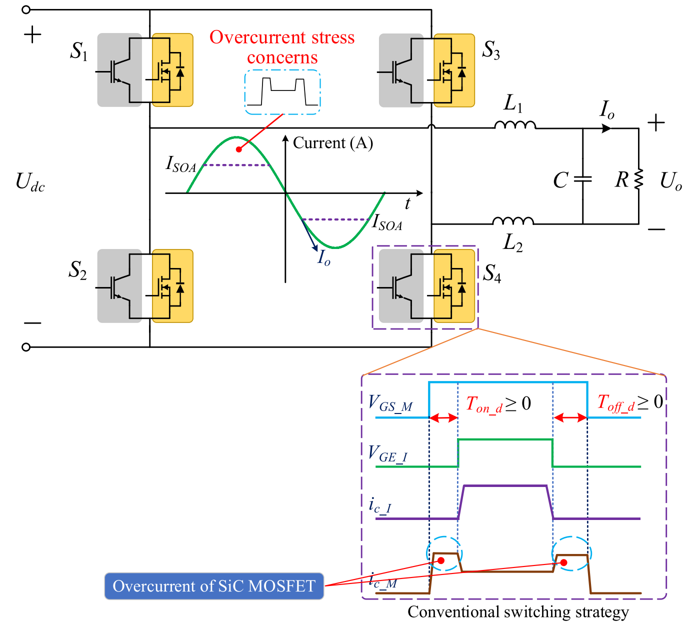


Fig. 1. Topology of the Si/SiC-hybrid-switch-based single-phase inverter: When the overcurrent of the SiC MOSFET is larger than I_{SOA}, the reliability of the Si/SiC hybrid switch will be greatly reduced by the overcurrent stress.

Si/SiC hybrid switches, respectively. The Si/SiC hybrid switch is configured by a Si IGBT (IGW25N120H3, 1200 V/25A [18]) and a SiC MOSFET (C2M0160120D, 1200 V/12.5A [19]), which means that the current-carrying capacity of the SiC MOSFET is smaller than that of the Si IGBT. In generally, the SiC MOSFET should be turned ON earlier and turned OFF later, which is called the conventional switching strategy [8]–[11]. Turn-ON delay time and turn-OFF delay time between the SiC MOSFET and Si IGBT are defined as T_{on_d} and T_{off_d}, respectively. And, V_{GS_M} and V_{GE_I} represent the gate drive signals of the SiC MOSFET and Si IGBT, respectively.

B. Overcurrent Stress Concerns of SiC MOSFET

As shown in Fig. 1, and S_4 is taken as example, when the conventional switching strategy is adopted, the load current will flow through the SiC MOSFET during the delay time. When the load current is larger than the rated current of the SiC MOSFET, which is called as the overcurrent. And, if the overcurrent is larger than I_{SOA}, the adverse effect of the overcurrent on the SiC MOSFET will cause the reliability issue of the Si/SiC hybrid switch [12], [13].

III. Variable-Frequency Current-Dependent Switching Strategy

To solve the reliability issue of the Si/SiC hybrid switch under the heavy load operating condition and avoid the large increase of the power loss, a novel variable-frequency current-dependent switching strategy is proposed. The variable switching pattern strategy and the variable PWM frequency strategy in the proposed switching strategy are presented in this section. Meanwhile, the relationship between the delay time and the power loss

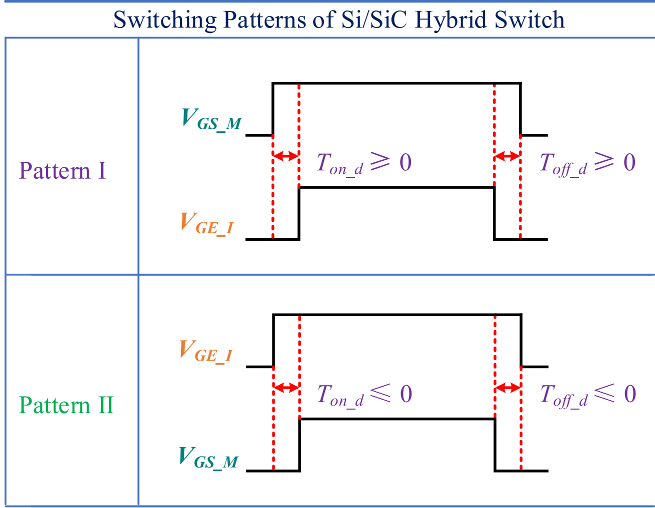


Fig. 2. Different switching patterns in the variable switching pattern strategy.

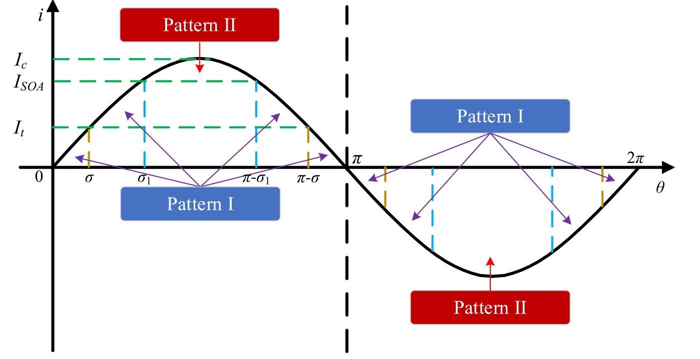


Fig. 3. Positions of different switching patterns during a fundamental cycle: When the load current is smaller than $I_{\rm SOA}$, Pattern I is adopted. When the load current is larger than $I_{\rm SOA}$, Pattern II is adopted.

at various switching patterns is analyzed. Details are presented as follows.

A. Variable Switching Pattern Strategy

The variable switching pattern strategy is adopted to improve the reliability of the Si/SiC hybrid switch under the heavy load operating condition. Based on [12] and [13], there are two different switching patterns adopted, which are shown in the Fig. 2. As can be seen from Fig. 2, "$T_{{\rm on}_d} \geq 0$" means that the SiC MOSFET is turned ON earlier than the Si IGBT, and "$T_{{\rm on}_d} \leq 0$" is the reverse switching order. Meanwhile, "$T_{{\rm off}_d} \geq 0$" means that the SiC MOSFET is turned OFF later than the Si IGBT, and "$T_{{\rm off}_d} \leq 0$" is the reverse switching order.

1) Pattern I. SiC MOSFET is Turned ON Earlier and Turned OFF Later: When the load current is smaller than $I_{\rm SOA}$, the SiC MOSFET with faster switching speed can be used to achieve the low switching loss of the Si/SiC hybrid switch, so the conventional switching strategy is adopted in this switching pattern.

2) Pattern II. Si IGBT is Turned ON Earlier and Turned OFF Later: When the load current is larger than $I_{\rm SOA}$, the Si IGBT with large current-carrying capacity can be turned ON earlier and turned OFF later to withstand the load current during the delay time, which is aim at effectively reducing the adverse effect of the overcurrent on the SiC MOSFET. However, the Si IGBT with lower switching speed will greatly increase the switching loss of the Si/SiC-hybrid-switch-based single-phase inverter.

B. Power Loss Analysis of Different Switching Patterns

The delay time in different switching patterns is the key to affecting the power loss of the Si/SiC hybrid switch. When the unipolar SPWM strategy is adopted [20]–[22], the position of different switching patterns during a fundamental cycle is shown in Fig. 3, and detailed analysis about the relationship between the delay time and the power loss is shown in the following.

1) Switching Loss of Si/SiC Hybrid Switch: According to [23]–[26], when the Pattern I is adopted, the influence of $T_{{\rm on}_d}$ on the switching loss of the Si/SiC hybrid switch is very small, so only $T_{{\rm off}_d}$ in the Pattern I should be considered, and there are $T_{{\rm on}_d} = 0$ and $T_{{\rm off}_d} > 0$. When the Pattern II is adopted, because the turn-OFF speed of the SiC MOSFET is faster than that of the Si IGBT [27]–[29], the influence of $T_{{\rm off}_d}$ on the turn-OFF loss of the Si/SiC hybrid switch is very small, which means that $T_{{\rm off}_d}$ in the Pattern II is not considered. In fact, $T_{{\rm on}_d}$ in the Pattern II must be larger than the turn-ON time of the Si IGBT to prevent the adverse effect of the overcurrent on the SiC MOSFET, so there is zero-voltage switching (ZVS) for the SiC MOSFET. It also means that the influence of $T_{{\rm on}_d}$ on the turn-ON loss of the Si/SiC hybrid switch can also be neglected, and there are $T_{{\rm on}_d} < 0$ and $T_{{\rm off}_d} = 0$.

According to the aforementioned analysis and Fig. 3, the total switching loss of the Si/SiC hybrid switch is calculated as [30]–[33]

$$\begin{aligned} P_s(T_{{\rm off}_d}) &= P_{s1}(T_{{\rm off}_d}) + P_{s2} \\ &= [P_{s1_{\rm MOSFET}} + P_{s1_{\rm IGBT}}(T_{{\rm off}_d})] \\ &\quad + [0 + P_{s2_{\rm IGBT}}] \\ &= [(E_{{\rm son1_MOSFET}} + E_{{\rm soff1_MOSFET}}) \\ &\quad + E_{{\rm soff1_IGBT}}(T_{{\rm off}_d})] + [E_{{\rm son2_IGBT}} \\ &\quad + E_{{\rm soff2_IGBT}}] \end{aligned} \tag{1}$$

where

$$\begin{cases} E_{{\rm son1_MOSFET}} + E_{{\rm soff1_MOSFET}} = f_s\left(AI_c^2 + BI_c + \dfrac{c_{pm}}{2}\right) \\ E_{{\rm soff1_IGBT}}(T_{{\rm off}_d}) = f_s\left[e^{-\tau\times T_{{\rm off}_d}}\left(A_1I_c^2 + B_1I_c + \dfrac{c_{pi1}}{2}\right.\right. \\ \qquad \left.\left. - \dfrac{e_{sr}}{2}\right) + \dfrac{e_{sr}}{2}\right] \\ E_{{\rm son2_IGBT}} + E_{{\rm soff2_IGBT}} = f_s\left(A_2I_c^2 + B_2I_c + \dfrac{c_{pi2}}{2}\right). \end{cases} \tag{2}$$

In (1) and (2), P_{s1} and P_{s2} represent the switching losses of the Pattern I and Pattern II, respectively. In the Pattern I, $P_{s1_{\rm MOSFET}}$, $E_{{\rm son1_MOSFET}}$, and $E_{{\rm soff1_MOSFET}}$ represent the switching loss, turn-ON loss, and turn-OFF loss of the SiC MOSFET, respectively. And, $P_{s1_{\rm IGBT}}$ and $E_{{\rm soff1_IGBT}}$ represent the switching loss and turn-OFF loss of the Si IGBT, respectively. In the Pattern II,

P_{s2_IGBT}, $E_{\mathrm{son2_IGBT}}$, and $E_{\mathrm{soff2_IGBT}}$ represent the switching loss, turn-ON loss, and turn-OFF loss of the Si IGBT, respectively. And, f_s, τ, I_c, and e_{sr} represent the switching frequency, exponent related to the turn-OFF delay time, ON-state current amplitude of the Si/SiC hybrid switch, and residual switching loss of the Si IGBT, respectively. In (2), there are

$$\begin{cases} A = \dfrac{a_{pm}(2\sigma_1 - \sin(2\sigma_1))}{4} \\ B = \dfrac{b_{pm}(1-\cos(\sigma_1))}{\pi} \\ A_1 = \dfrac{a_{pi1}(2\sigma_1 - \sin(2\sigma_1))}{4} \\ B_1 = \dfrac{b_{pi1}(1-\cos(\sigma_1))}{\pi} \\ A_2 = \dfrac{a_{pi2}(\pi - 2\sigma_1 + \sin(2\sigma_1))}{4} \\ B_2 = \dfrac{b_{pi2}\cos(\sigma_1)}{\pi} \\ \sigma_1 = \arcsin\left(\dfrac{I_{\mathrm{SOA}}}{I_c}\right). \end{cases} \tag{3}$$

In (2) and (3), a_{pm}, b_{pm}, c_{pm}, a_{pin}, b_{pin}, and c_{pin} $(n = 1, 2)$ are the fitting parameters, which can be obtained by the DPT experiments [30]–[33]. Meanwhile, the condition of the DPT experiments must be the same as that of the application of the single-phase inverter. According to (1)–(3), as the increase of T_{off_d}, the switching loss of the Si/SiC hybrid switch will be decreased.

2) Conduction Loss of Si/SiC Hybrid Switch in Pattern I: When the Pattern I is adopted, and according to Fig. 3, the conduction loss of the Si/SiC hybrid switch is calculated as [30], [34]–[36]

$$\begin{aligned} P_{c1} &= P_{c1_\mathrm{MOSFET}}(T_{\mathrm{off}_d}) + P_{c1_\mathrm{IGBT}}(T_{\mathrm{off}_d}) \\ &= \frac{1}{\pi}\int_{\sigma}^{\sigma_1} (R_{c_M} i_{c_M}^2 D_{c_I} + R_c i_c^2 D_{c_\mathrm{off}d}) d\theta \\ &\quad + \frac{1}{\pi}\int_{0}^{\sigma} R_c i_c^2 D_c d\theta + \frac{1}{\pi}\int_{\sigma}^{\sigma_1} R_{c_I} i_{c_I}^2 D_{c_I} d\theta \\ &= (C + E(T_{\mathrm{off}_d}))\Big[\frac{2\sigma_1 + \sin(2\sigma)}{4\pi} \\ &\quad - \frac{2\sigma + \sin(2\sigma_1)}{4\pi}\Big] + R_c D_c I_c^2 \frac{(2\sigma + \sin(2\sigma))}{4\pi} \end{aligned} \tag{4}$$

where

$$\begin{cases} C = R_{c_M} D_c I_{c_M}^2 + R_{c_I} D_c I_{c_I}^2 \\ E(T_{\mathrm{off}_d}) = \dfrac{T_{\mathrm{off}_d}}{T_s}[R_c I_c^2 - (R_{c_M} I_{c_M}^2 + R_{c_I} I_{c_I}^2)] \\ D_c = D_{c_M} = D_{c_\mathrm{off}d} + D_{c_I} \\ R_c = \dfrac{R_{c_M} R_{c_I}}{R_{c_M} + R_{c_I}} \\ i_c = I_c \sin\theta = I_{c_M}\sin\theta + I_{c_I}\sin\theta \\ \sigma = \arcsin\left(\dfrac{U_t}{R_{c_M} I_c}\right). \end{cases} \tag{5}$$

In (4) and (5), P_{c1_MOSFET}, R_{c_M}, i_{c_M}, and D_{c_M} represent the conduction loss, ON-state equivalent resistor, ON-state current, and duty cycle of the SiC MOSFET, respectively. P_{c1_IGBT}, R_{c_I}, i_{c_I}, and D_{c_I} represent the conduction loss, ON-state equivalent resistor, ON-state current, and duty cycle of the Si IGBT, respectively. i_c, D_c, T_s, and U_t represent the ON-state current of the Si/SiC hybrid switch, duty cycle of the Si/SiC hybrid switch, switching cycle of the Si/SiC hybrid switch, and threshold voltage amplitude of the Si IGBT, respectively. And, $D_{c_\mathrm{off}d}$ represents the duty cycle of T_{off_d} in the Pattern I. According to (4) and (5), as the increase of T_{off_d}, the conduction loss of the SiC MOSFET will be increased, and the conduction loss of the Si IGBT will be reduced.

3) Conduction Loss of Si/SiC Hybrid Switch in Pattern II: When the Pattern II is adopted, and according to Fig. 3, the conduction loss of the Si/SiC hybrid switch is calculated as

$$\begin{aligned} P_{c2} &= P_{c2_\mathrm{MOSFET}}(T_{\mathrm{on}_d}) + P_{c2_\mathrm{IGBT}}(T_{\mathrm{on}_d}) \\ &= \frac{1}{\pi}\int_{\sigma_1}^{\frac{\pi}{2}} R_{c_M} i_{c_M}^2 D_{c_M} d\theta \\ &\quad + \frac{1}{\pi}\int_{\sigma_1}^{\frac{\pi}{2}} (R_{c_I} i_{c_I}^2 D_{c_M} + R_c i_c^2 D_{c_\mathrm{ond}}) d\theta \\ &= (F + G(T_{\mathrm{on}_d}))\frac{[\pi - 2\sigma_1 + \sin(2\sigma_1)]}{4\pi} \end{aligned} \tag{6}$$

where

$$\begin{cases} F = R_{c_M} D_c I_{c_M}^2 + R_{c_I} D_c I_{c_I}^2 \\ G(T_{\mathrm{on}_d}) = \dfrac{T_{\mathrm{on}_d}}{T_s}[R_c I_c^2 - (R_{c_M} I_{c_M}^2 + R_{c_I} I_{c_I}^2)] \\ D_c = D_{c_I} = D_{c_\mathrm{ond}} + D_{c_M}. \end{cases} \tag{7}$$

In (6) and (7), P_{c2_MOSFET}, P_{c2_IGBT}, and $D_{c_\mathrm{on}d}$ represent the conduction loss of the SiC MOSFET, conduction loss of the Si IGBT, and duty cycle of T_{on_d} in the Pattern II, respectively. As the increase of T_{on_d}, the conduction loss of the SiC MOSFET will be slightly decreased, and the conduction loss of the Si IGBT will be greatly increased.

Combining with (1), (4), and (6), the total power loss of the Si/SiC hybrid switch is calculated as

$$P_{tl}(T_{\mathrm{off}_d}, T_{\mathrm{on}_d}) = P_s(T_{\mathrm{off}_d}) + P_{c1}(T_{\mathrm{off}_d}) + P_{c2}(T_{\mathrm{on}_d}). \tag{8}$$

According to (1), (4), (6), and (8), as the increase of T_{off_d} in the Pattern I, the total power loss of the Si/SiC hybrid switch will be gradually decreased at first. Then, it will be gradually increased. It means that the value of T_{off_d} in the Pattern I should be neither too small nor too large. And as the increase of T_{on_d} in the Pattern II, the total power loss of the Si/SiC hybrid switch will be gradually increased. Therefore, the design of the T_{on_d} in the Pattern II requires a tradeoff between the excellent reliability of the SiC MOSFET and the power loss of Si/SiC hybrid switch.

C. Variable PWM Frequency Strategy

Even if the optimal delay time is adopted, the increased power loss caused by the variable switching pattern strategy cannot be effectively restrained. In order to solve this problem, an optimal switching frequency curve $(f_s = 1/T_s)$ is adopted, which is

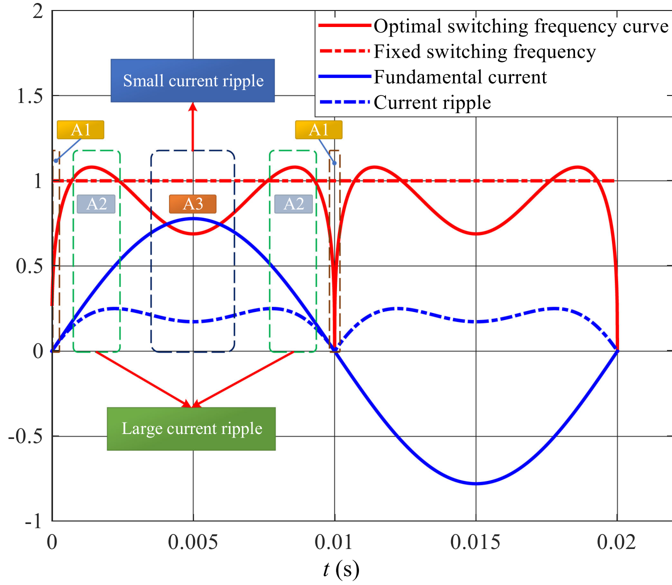


Fig. 4. Normalized optimal switching frequency curve, fixed switching frequency, fundamental current, and current ripple.

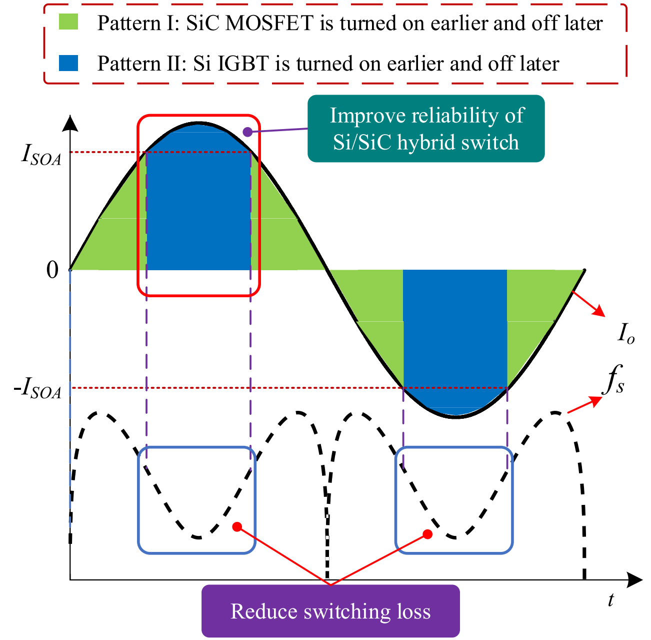


Fig. 5. Principle of the variable-frequency current-dependent switching strategy.

written as [37]

$$T_s(\omega_c t) = C' \left[\frac{|\sin(\omega_c t)|}{M_1^2 \sin^2(\omega_c t)} \right]^{\frac{1}{3}} \tag{9}$$

where

$$\begin{cases} C' = \dfrac{2\sqrt{3}\Delta I_{\text{rms,req}} L}{\sqrt{\frac{1}{\pi}\int_0^\pi \left[\sin^4(\omega_c t) M_2^2\right]^{\frac{1}{3}} d\omega_c t}} \\ \Delta I_{\text{rms,req}} = \dfrac{1.177}{f_{fs} L} \sqrt{\displaystyle\int_0^\pi \sin^2(\omega_c t) M_3 d\omega_c t} \\ M_1 = 1 - m\,|\sin(\omega_c t)| \\ M_2 = 1 - m \sin(\omega_c t) \\ M_3 = [1 - m \sin(\omega_c t)(1 + M_2)]. \end{cases} \tag{10}$$

In (9) and (10), m is the modulation ratio, $\triangle I_{\text{rms,req}}$ is the required root mean square (rms) value of the current ripple, f_{fs} is the fixed switching frequency, and ω_c is the angular frequency of the fundamental current. Based on (9) and (10), the normalized optimal switching frequency curve, fixed switching frequency, fundamental current, and current ripple are shown in Fig. 4. When the fundamental current is close to the zero (A1 region), the current ripple is negligible, which means that the increase of the current harmonics in this area can be neglected even if a very low switching frequency in the optimal switching frequency curve is adopted. As the increase of the fundamental current, there is large current ripple around the zero-crossing point region (A2 region), and the higher switching frequency in the optimal switching frequency curve is adopted to effectively reduce the current harmonics in this area. And there is small current ripple around the peak current region (A3 region), where the increase of current harmonics will not be obvious even if the switching frequency in the optimal switching frequency curve is lower than the fixed switching frequency. Therefore, the optimal switching frequency curve can effectively improve the efficiency of the Si/SiC-hybrid-switch-based single-phase inverter without significantly increasing the current harmonics.

D. Variable-Frequency Current-Dependent Switching Strategy

Combing with the variable switching pattern strategy and the variable PWM frequency strategy, the principle of the variable-frequency current-dependent switching strategy is proposed, which is shown in Fig. 5. When the load current is smaller than I_{SOA}, the Pattern I is adopted. In this condition, the switching frequency is gradually increased at first, and then, it is gradually reduced. When the load current is larger than I_{SOA}, the Pattern II is adopted. In this condition, the switching frequency is gradually reduced.

IV. Experimental Investigation

In order to demonstrate the superiority of the variable-frequency current-dependent switching strategy, comparison experiments of different switching strategies are presented, and the experimental platform is shown in Fig. 6. It comprises the DSP control board, dc power source, power analyzer, oscilloscope, single-phase inverter, and load. Experimental parameters are described in Table I. In Table I, I_{SOA} is equal to 20 A (rms) [13].

A. Optimal Delay Time at Different Switching Patterns

Determination of the optimal delay time under different switching patterns is the premise of the comparison experiments. In order to facilitate experimental research, only the variable switching pattern strategy is adopted, and the switching frequency is set as 40 kHz. Corresponding experiments are shown in the following.

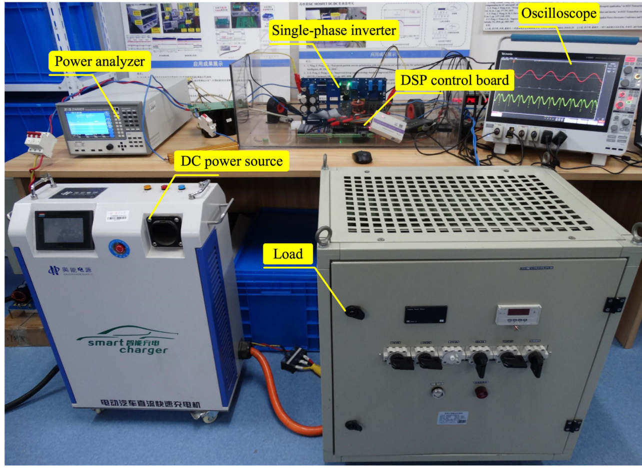


Fig. 6. Experimental platform.

TABLE I
EXPERIMENTAL PARAMETERS

Parameters	Values
DC voltage (U_{dc})	400V
Filter inductance (L_1 and L_2)	0.308mH
Filter capacitor (C)	24μF
Modulation ratio (m)	0.778
Fundamental frequency	50Hz
I_{SOA}	20A

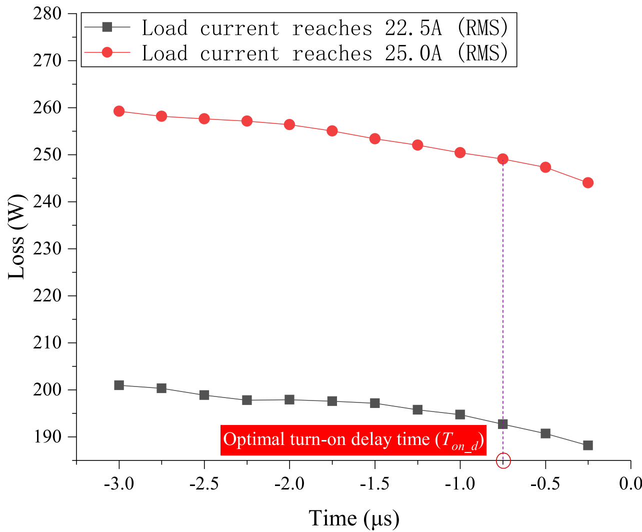


Fig. 7. Power loss curves of a single-phase inverter at different T_{on_d} (Pattern II).

According to the comparison experiments of different T_{off_d} in the Pattern I, the optimal T_{off_d} in the Pattern I can be set as 1.25 μs. When the Pattern II is adopted, the power loss curves of the single-phase inverter at different T_{on_d} are shown in Fig. 7. When the load current reaches 22.5 A, as the increase of T_{on_d}, the power loss of the single-phase inverter will be gradually increased. And when the load current reaches 25 A, as the increase of T_{on_d}, the power loss of the single-phase inverter will also be gradually increased. Because T_{on_d} must be larger than the turn-ON speed of the Si IGBT, and considering the actual interaction between the drivers of the Si IGBT and the SiC MOSFET, the optimal T_{on_d} in the Pattern II can be set as $-0.75\,\mu$s. Finally, this optimal delay time is adopted in the following experiments.

TABLE II
EXPERIMENTAL RESULTS OF DIFFERENT SWITCHING FREQUENCY CURVES (MINIMUM SWITCHING FREQUENCY IS CHANGED)

f_s (kHz)	THD	Total power loss (W)
10~41	1.34%	91.0
15~41	1.34%	91.1
20~41	1.33%	91.3
25~41	1.32%	91.7

B. Design of Optimal Switching Frequency Curve

The maximum switching frequency in the optimal switching frequency curve can be calculated by (9) and (10), and it is set as 41 kHz. The value of the minimum switching frequency in the optimal switching frequency curve should be obtained by the corresponding comparison experiments.

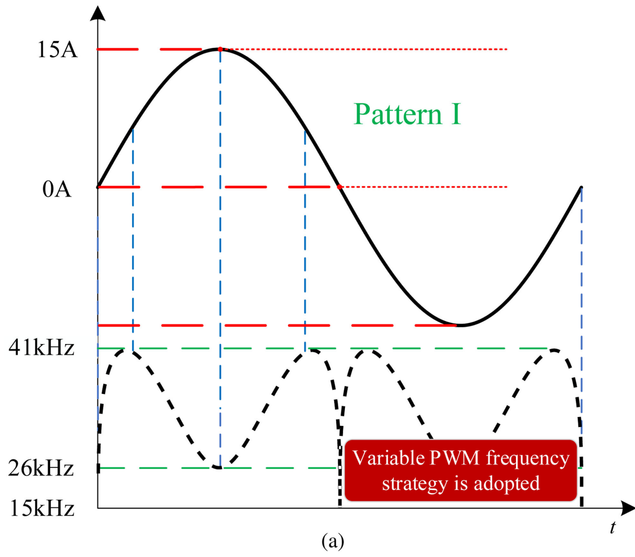
When the load current is set as 15 A and the minimum switching frequency is changed, the experimental results of different switching frequency curves are shown in Table II. When different switching frequency curves are adopted, the difference of the total harmonic distortion (THD) is smaller than 0.03%, and the difference of the power loss is smaller than 0.9 W. It means that the minimum switching frequency has little influence on the performance of a single-phase inverter. In this article, the minimum switching frequency is set as 15 kHz.

C. Comparison Experiments

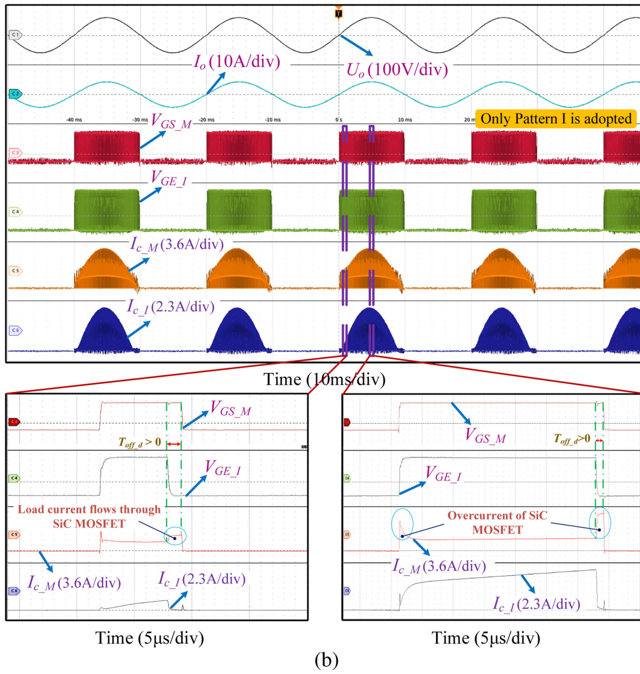
Comparison experiments of the conventional switching strategy, current-dependent switching strategy [13], and variable-frequency current-dependent switching strategy are presented in following.

Case 1: 60% of nominal load (at a load current of 15 A).

Taking the positive half period of the load current as an example, the principle of the variable-frequency current-dependent switching strategy is shown in Fig. 8(a), and its experimental waveforms are shown in Fig. 8(b). As can be seen from Fig. 8, I_{c_M} and I_{c_I} represent the ON-state current of the SiC MOSFET and ON-state current of the Si IGBT, respectively. Because the load current is smaller than 20 A (I_{SOA}), only Pattern I in the variable switching pattern strategy is adopted to achieve the low switching loss of the Si/SiC hybrid switches. Therefore, the load current always flows through the SiC MOSFET during the delay time. Furthermore, when the switching frequency is changed from 15 ~41 kHz, the power loss of the single-phase inverter can be further reduced.

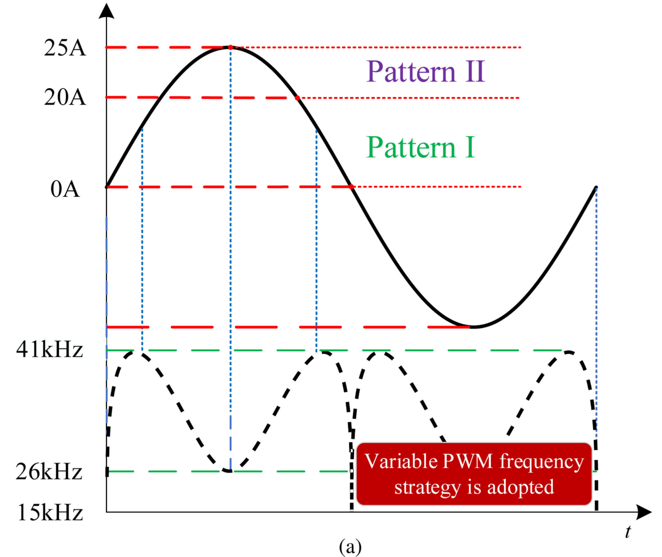


(a)

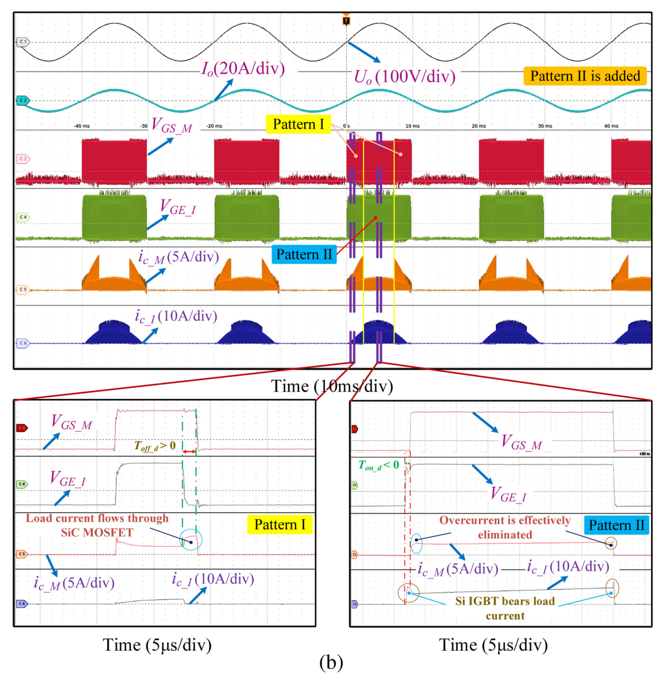


(b)

Fig. 8. Variable-frequency current-dependent switching strategy at a load current of 15 A (rms): The load current always flows through the SiC MOSFET during the delay time, and the switching frequency is changed from 15∼41 kHz to further reduce the power loss of the single-phase inverter. (a) Control principle. (b) Experimental waveforms.



(a)



(b)

Fig. 9. Variable-frequency current-dependent switching strategy at a load current of 25 A (rms): When the load current is smaller than 20 A, the load current in this region will flow through the SiC MOSFET during the delay time. When the load current is larger than 20 A, the Si IGBT in this region will bear the load current during the delay time. Meanwhile, the switching frequency is changed from 15∼41 kHz to prevent the power loss of the single-phase inverter from significantly increasing. (a) Control principle. (b) Experimental waveforms.

Experimental results of different switching strategies at a load current of 15 A are shown in Table III. $D_{d_\max}$ represents the overcurrent time duration of each fundamental cycle when the load current is larger than 20 A, and $I_{p_\max}$ represents the peak overcurrent value of the SiC MOSFET when the load current is larger than 20 A. When the variable-frequency current-dependent switching strategy is adopted, the THD of the load current is 1.34%, which is slightly larger than that of the conventional switching strategy and current-dependent switching strategy (1.20% and 1.20%). And the power loss of the single-phase inverter adopting the variable-frequency current-dependent switching strategy is 91.1 W, which is smaller than that of the conventional switching strategy and current-dependent switching strategy (97.4 and 97.3 W). Because the load current is smaller than 20 A, the overcurrent stress concerns are not considered in this condition.

Case 2: 100% of nominal load (at a load current of 25 A).

In this condition, the principle of the variable-frequency current-dependent switching strategy is shown in Fig. 9(a), and its experimental waveforms are shown in Fig. 9(b). As can be seen from Fig. 9. When the load current is smaller than 20 A,

TABLE III
COMPARISON OF DIFFERENT SWITCHING STRATEGIES AT A LOAD CURRENT OF 15 A (rms)

	f_s (kHz)	THD	Total power loss (W)	Overcurrent Time Duration (% of each fundamental cycle) D_{d_cysle}	Peak overcurrent value I_{p_max}
Conventional switching strategy	40	1.20%	97.4	×	×
Current-dependent switching strategy [13]	40	1.20%	97.3	×	×
Variable-frequency current-dependent switching strategy (This work)	15 ~ 41	1.34%	91.1	×	×

TABLE IV
COMPARISON OF DIFFERENT SWITCHING STRATEGIES AT A LOAD CURRENT OF 25 A (rms)

	f_s (kHz)	THD	Total power loss (W)	Overcurrent Time Duration (% of each fundamental cycle) D_{d_cysle}	Peak overcurrent value I_{p_max}
Conventional switching strategy	40	1.36%	225.2	$D_{d_cysle} > 1\%$	20A ≤ I_{p_max} ≤ 25A
Current-dependent switching strategy [13]	40	1.39%	249.1	0%	I_{p_max} ≤ 12A
Variable-frequency current-dependent switching strategy (This work)	15 ~ 41	1.56%	225.6	0%	I_{p_max} ≤ 12A

Pattern I can be adopted to achieve the low switching loss of the Si/SiC hybrid switch, so the load current will flow through the SiC MOSFET during the delay time. When the load current is larger than 20 A, Pattern II must be adopted in order to effectively eliminated the adverse influence of the overcurrent stress on the SiC MOSFET, so this switching pattern makes it possible for Si IGBT to bear the load current during the delay time when operating under a heavy load condition. Furthermore, when the switching frequency is changed from 15∼41 kHz, the significant increase of power loss on single-phase inverters caused by Pattern II can be prevented effectively.

Experimental results of different switching strategies at 100% of nominal load are shown in Table IV. When the conventional switching strategy is adopted, and the load current is larger than 20 A, there are $D_{d_\text{cycle}} > 1\%$ and 20A $\leq I_{p_\text{max}} \leq 25$ A. It means that there is severe overcurrent stress on the SiC MOSFET under the heavy load operating condition. When the current-dependent switching strategy is adopted, there are $D_{d_\text{cycle}} = 0\%$ and $I_{p_\text{max}} \leq 12A$. It means that the adverse influence of the overcurrent stress on the SiC MOSFET can be effectively eliminated. However, the power loss of the single-phase inverter adopting the current-dependent switching strategy is 249.1 W, which is 23.9 W larger than that of the conventional switching strategy.

When the proposed switching strategy is adopted, the power loss of the single-phase inverter is 225.6 W, which is close to that of the conventional switching strategy, and 23.5 W smaller than that of the current-dependent switching strategy. When the load current is larger than 20 A, there are $D_{d_\text{cycle}} = 0\%$ and $I_{p_\text{max}} \leq 12$ A. It also means that the adverse influence of the overcurrent stress on the SiC MOSFET can be effectively eliminated. Meanwhile, the THD of the load current is 1.56%, which is slightly larger than that of the conventional switching strategy and current-dependent switching strategy (1.36% and 1.39%).

V. CONCLUSION

In this article, a novel variable-frequency current-dependent switching strategy is proposed to solve the reliability issue of the Si/SiC hybrid switch without reducing the efficiency of the inverter. The proposed switching strategy comprises the variable switching pattern strategy and the variable PWM frequency strategy. The variable switching pattern strategy is implemented by adopting two different switching patterns, and the optimal delay time in different switching patterns is designed by the power loss model and comparison experiment. The designed variable switching pattern strategy can adjust the switching frequency based on the current ripple.

An experimental platform of the Si/SiC-hybrid-switch-based single-phase inverter is set up and tested, and the experimental results prove that the proposed switching strategy can avoid the overcurrent stress of the SiC MOSFET under the heavy load operating condition compared with the conventional switching strategy. And it also can achieve the lower power loss than that of the current-dependent switching strategy. Therefore, the Si/SiC-hybrid-switch-based single-phase inverter adopting the proposed switching strategy can be further improved toward the high current-carrying capacity, efficiency, and power density. In fact, the concept of this switching strategy can be applied to different kinds of inverters, which will be studied in a more comprehensive way in the future.

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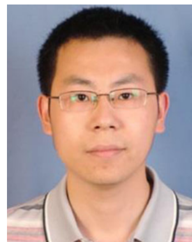

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