A Reconfigurable Totem-Pole PFC Rectifier With Light Load Optimization Control Strategy and Soft-Switching Capability

Young-Dal Lee, *Student Member, IEEE*, Gun-Woo Moon, *Member, IEEE*, Jaeil Baek, *Member, IEEE*, and Chong-Eun Kim, *Member, IEEE*

***Abstract*—This article presents a reconfigurable totem-pole bridgeless power factor correction converter employing an auxiliary circuit and a simple control scheme to achieve high efficiency. Under light load condition, instead of delivering the energy through the main switch, the proposed converter utilizes only the auxiliary switches by using a different control scheme. Since the auxiliary switches have much smaller parasitic capacitances than the main switches, the proposed converter can obtain high efficiency under light load condition. Over middle-to-heavy load condition, the proposed converter can acquire both zero-voltage switching operation and relieved reverse-recovery problem thanks to the auxiliary circuit, which leads to high efficiency even with Si-MOSFET in the continuous conduction mode control. As a result, the proposed converter can achieve high efficiency over the entire load condition. The effectiveness of the proposed converter is verified by a prototype with ac 230$V_{\rm rms}$ input and 750 W output.**

***Index Terms*—Light load efficiency, server power supply, soft-switching operation, totem-pole bridgeless power factor correction (PFC) rectifier, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

RECENTLY, moving to the Big Data era, the capability to process tremendous data quickly has been required in server computers [1]. Accordingly, higher and higher power level has been required in the server power system. But at the same time, higher efficiency has been gradually expected for energy conservation [2]. In general, since most power consumption occurs at daytime when most information technology (IT) equipment operate, the server power system requires high efficiency under the heavy load conditions. Moreover, the server power system even operates under light load condition at night and dawn consistently.

Thus, manufacturers of the server power system have made an effort to minimize power loss under light load condition as well as heavy load condition. This tendency is specified by the 80 PLUS incentive program and Climate Saver Computing Initiative requiring high efficiency from 10% to 100% load conditions. Furthermore, most manufacturers of the server power supply tend to require high efficiency even below 5% load condition, which clarifies the latest Energy Star specifications [3], [4].

Generally, server power system typically consists of a front-end boost power factor correction (PFC) converter and a main dc–dc converter. Among them, a boost PFC converter is used to fulfill the high power factor and low current distortion for meeting IEC 61000-3-2 standards and Energy Star specifications. The importance of these international standards continues to be emphasized to minimize power loss, noise, and line current distortion caused by reactive power. To mitigate these problems, a continuous conduction mode (CCM) mode is preferred in middle-to-heavy power applications in order to benefit from its small conduction losses and high power density [5]. Furthermore, for obtaining high efficiency, many leading power supply companies are currently working on the development of bridgeless PFC converters to reduce relative large conduction loss of bridge diode, which is a definite disadvantage of conventional boost PFC converters [6]–[15].

A representative candidate for bridgeless PFC converters is totem-pole bridgeless PFC converter, as shown in Fig. 1. It has the merit of a simple structure due to low component counts on conduction paths compared to the conventional boost PFC converter with bridge diodes. Thus, this structure can reduce conduction losses compared to the conventional one.

However, it is hard for the totem-pole structure to use Si-MOSFET in CCM control because the totem-pole structure still suffers from the hard-switching operation and reverse-recovery problems. Therefore, majority of conventional research usually considered wide-band-gap (WBG) devices such as GaN-FET

Manuscript received November 30, 2019; revised March 28, 2020, May 23, 2020, and July 18, 2020; accepted August 16, 2020. Date of publication August 24, 2020; date of current version November 20, 2020. This work was supported by the Ministry of Science and ICT, Government of South Korea, through the National Research Foundation of Korea (NRF) under Energy Cloud R&D Program 2019M3F2A1072469. This article was presented in part at the Eighth International Power Electronics Conference-Energy Conversion Congress and Exposition Asia, May 2018, entitled "A Zero-Voltage-Switching Totem-Pole Bridgeless Boost Power Factor Correction Rectifier Having Minimized Conduction Losses." Recommended for publication by Associate Editor F. J. Azcondo. *(Corresponding author: Chong-Eun Kim.)*

Young-Dal Lee and Gun-Woo Moon are with the Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea (e-mail: youngdal.lee@kaist.ac.kr; gwmoon@kaist.ac.kr).

Jaeil Baek is with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08540 USA (e-mail: jaeil.baek@princeton.edu).

Chong-Eun Kim is with the Department of Control and Instrumentation Engineering, Gyeongsang National University, Jinju 52828, South Korea (e-mail: cekim@gnu.ac.kr).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3019085

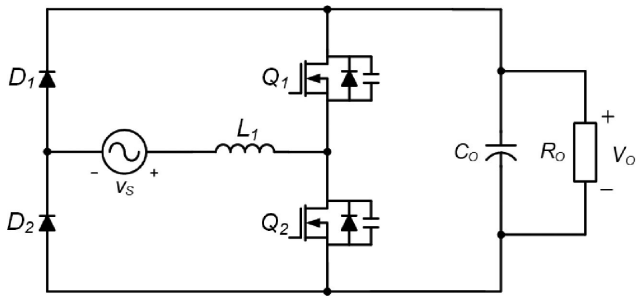


Fig. 1. Circuit diagram of conventional totem-pole bridgeless rectifier.

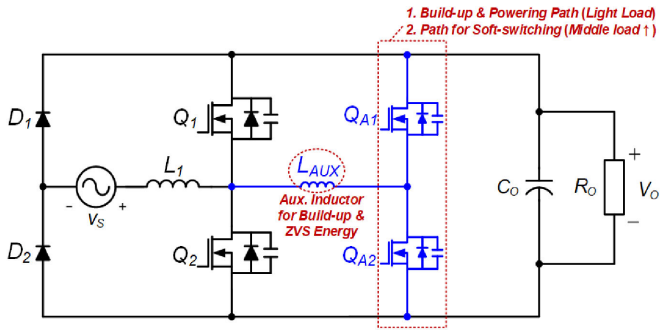


Fig. 2. Derivation process of the proposed reconfigurable totem-pole bridgeless PFC converter.

and SiC-MOSFET in CCM totem-pole structure. However, despite using high-cost WBG devices, totem-pole bridgeless PFC converter still has a limitation in achieving high efficiency due to the significant switching loss and reverse-recovery problem in CCM.

Therefore, in order to relieve this limitation, it is most likely to operate the critical conduction mode (CRM) operation reliably in the totem-pole structure [6], [7]. However, when operating with CRM operation, it is not easy to apply in the high power applications on account of high conduction loss. So as to overcome this problem, many types of research have been conducted on soft-switching techniques, enabling the totem-pole bridgeless PFC converter to achieve high efficiency even in CCM operation [8]–[13], [18].

In [12], soft-switching operation by employing a coupled inductor was proposed. Although it can achieve the relieved reverse-recovery and zero current switching (ZCS) turn-OFF operation by utilizing a coupled inductor, conduction loss increases in the auxiliary circuit, which decreases the light load efficiency. In [13], additional passive LC network provided the ZCS turn-OFF operation. However, relatively large circulating current occurs due to the auxiliary circuit, which also degrades light load efficiency. Also, the voltage stress across the LC network is double the output voltage because of using resonance. Therefore, there is a limit to utilizing low-voltage rating devices with high performance. In [14], both ZCS turn-OFF and zero voltage switching (ZVS) turn-ON could be achieved by using the auxiliary circuit. Thus, it improved its efficiency by reducing switching losses. However, since large conduction loss is caused by the large number of components in the auxiliary circuit, it is still difficult for the totem-pole bridgeless PFC converter to achieve high efficiency.

This article proposes a reconfigurable totem-pole bridgeless converter adopting not only light load control strategy but also soft-switching capability. In the light load condition, the proposed converter utilizes auxiliary switches instead of the main switches for build-up and powering operation. Therefore, it can achieve high efficiency in light load conditions by reducing the switching loss because the auxiliary switches have low current rating and small parasitic capacitance compared to that of the main switches. Under middle-to-heavy load condition, the proposed converter can secure the soft-switching operation of the main switch through the auxiliary circuit. Thus, the proposed converter can reduce the switching loss and reverse-recovery loss, which results in high efficiency. For this reason, the proposed converter can have high efficiency over the entire load condition even with general Si-MOSFET in spite of CCM operations.

II. Concept of the Proposed Converter

Based on the conventional totem-pole bridgeless PFC rectifier shown in Fig. 1, the proposed converter is configured with an auxiliary circuit as described in Fig. 2. In order to obtain reconfigurable operation, such as light load control strategy and soft-switching operation, the additional current path is required by adopting auxiliary inductor $L_{\rm AUX}$ as a current source. $L_{\rm AUX}$ is connected between two main switches and two auxiliary switches. Here, Q_1 and Q_2 are the main switches responsible for general build-up and powering operation of the proposed converter. Also, Q_{A1} and Q_{A2} are auxiliary switches which perform the build-up and powering operation instead of the main switches with small switching loss in the light conditions. Under the middle-to-heavy load conditions, Q_{A1} and Q_{A2} play the role of the main switches Q_1 and Q_2 in ZVS operations as well.

A. Operational Principles With Light Load Control Strategy

In this section, the operational principles of the proposed converter are described in detail under the light load conditions. If the proposed converter keeps ZVS operation under light load condition, the conduction losses caused by the auxiliary circuit become relatively larger than reduced switching losses, which degrades the light load efficiency as in the conventional research [12]. Therefore, the proposed converter needs to adopt an additional control scheme under the light load condition. When the proposed converter is in the light load condition, the proposed converter transfers the energy stored in the inductor to the output side not by using the two main switches Q_1 and Q_2 but by utilizing the two auxiliary switches Q_{A1} and Q_{A2} as shown in Fig. 3(b) and (c).

For the sake of convenience in analysis, only the positive half-cycle of ac input voltage is considered. To simplify the analysis, it is assumed that the proposed converter operates in the steady state and the following suppositions are premised during a few switching cycles.

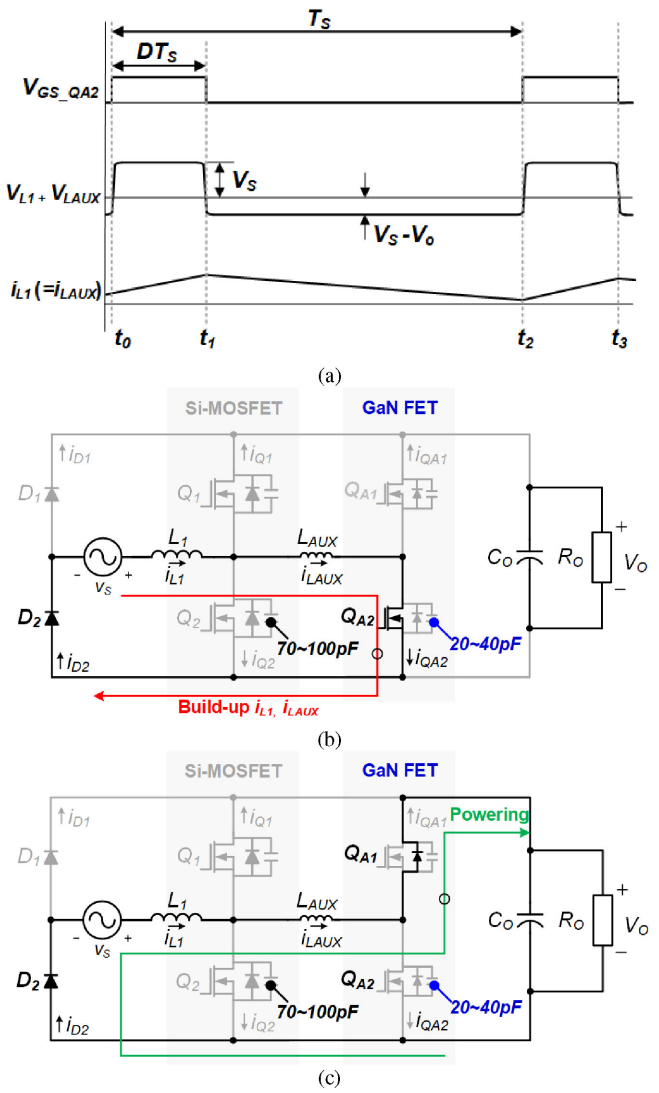


Fig. 3. Operational modes of the proposed reconfigurable totem-pole bridgeless PFC rectifier under light load conditions. (a) Key waveforms of the proposed control strategy. (b) Proposed build-up operation. (c) Proposed powering operation.

1) All the components and devices are ideal.
2) The output capacitor C_O is large enough to assume that output voltage V_O is constant.
3) All the semiconductors, i.e., two main switches and two auxiliary switches, are ideal states having parallel body diode and parasitic capacitance $C_{\rm OSS}$.

Mode 1 [t_0–t_1]: In the light load conditions, Mode 1 begins not by turning ON Q_2 but by turning ON Q_{A2}. Therefore, since the input voltage V_S is applied to L_1 and $L_{\rm AUX}$ simultaneously, the inductor current $i_{\rm LAUX}$ is built up as shown in Fig. 3(b). The peak value of $i_{\rm LAUX\_peak}$ can be expressed as follows:

$$i_{L1}(t) = i_{\rm LAUX}(t) = i_{L1}(t_0) + \frac{V_S}{L_1 + L_{\rm AUX}}\ (t - t_0). \quad (1)$$

Mode 2 [t_1–t_2]: Mode 2 starts when the switch Q_{A2} is turned OFF. In this interval, the energy stored in both L_1 and $L_{\rm AUX}$ transfer to the output side through the body diode of Q_{A1} shown in Fig. 3(c).

The two auxiliary switches Q_{A1} and Q_{A2} used in this article have smaller current rating specifications compared to the main switches Q_1 and Q_2, hence the two auxiliary switches Q_{A1} and Q_{A2} have smaller output capacitance $C_{\rm OSS}$ than that of the main switches Q_1 and Q_2. It means that the proposed converter can reduce the switching loss more dramatically than the conventional operation using the main switches Q_1 and Q_2. Therefore, the proposed control strategy can improve the system efficiency by utilizing auxiliary switches Q_{A1} and Q_{A2} under the light load conditions.

B. Operational Principles Under the Middle-to-Heavy Load Condition With Soft-Switching Capability

In this section, the operational principles of the proposed converter are going to be analyzed in detail under the middle-to-heavy load conditions. In order to describe the operational principles of the proposed converter, Fig. 4 shows the key waveforms and operational modes of the proposed converter under middle-to-heavy load conditions.

Mode 1 [t_1–t_2]: After the build-up operation of the inductor L_1 is finished, the unique operation of the proposed converter starts at Mode 1 with powering operation. First, let us define two nodes between the two sides of auxiliary inductor $L_{\rm AUX}$. One is a_{node} in the left side and the other is b_{node} in the right side of auxiliary inductor $L_{\rm AUX}$. At the start of powering operation, a_{node} is clamped to the output voltage and b_{node} is induced to zero voltage due to preoperation. Therefore, the output voltage V_O is applied to $L_{\rm AUX}$. When the energy stored in $L_{\rm AUX}$ is large enough to charge and discharge the parasitic capacitance $C_{\rm OSS\_QA1}$ and $C_{\rm OSS\_QA2}$, the commutation operation is performed by resonating with $L_{\rm AUX}$ and $C_{\rm OSS\_QA1}$ and $C_{\rm OSS\_QA2}$. In this interval t_1–t_2, the peak value of $i_{\rm LAUX\ peak}$ can be expressed as follows:

$$i_{\rm LAUX\_peak} = \sqrt{\frac{C_{\rm OSS\_QA1} + C_{\rm OSS\_QA2}}{L_{\rm AUX}}} \cdot V_O. \quad (2)$$

Mode 2 [t_2–t_3]: Mode 2 starts when the junction capacitor $C_{\rm OSS\_QA2}$ is fully charged up to V_O. As both a_{node} and b_{node} are induced with the same output voltage V_O, $i_{\rm LAUX}$ is circulating through the body diode of Q_{A1}. Assuming the body diodes of Q_1 and Q_{A1} have different forward voltage drop like $V_{F\_Q1\ body} < V_{F\_QA1\ body}$, $i_{\rm LAUX}$ decreases with reduced conduction loss in this interval as follows:

$$\Delta i_{\rm LAUX} = \frac{V_{F\_Q1\_body} - V_{F\_QA1\_body}}{L_{\rm AUX}}. \quad (3)$$

Mode 3 [t_3–t_4]: At the end of powering operation, Mode 3 starts to begin turning ON Q_{A2} with ZCS turn-ON due to reduced circulating current $i_{\rm LAUX}$. Also, $i_{\rm LAUX}$ is built up as follows:

$$i_{\rm LAUX}(t) = i_{\rm LAUX}(t_3) + \frac{V_O}{L_{\rm AUX}}\ (t - t_3). \quad (4)$$

Since the output voltage V_O is applied to $L_{\rm AUX}$, the current i_{Q1} flowing through the main switch decreases to zero value

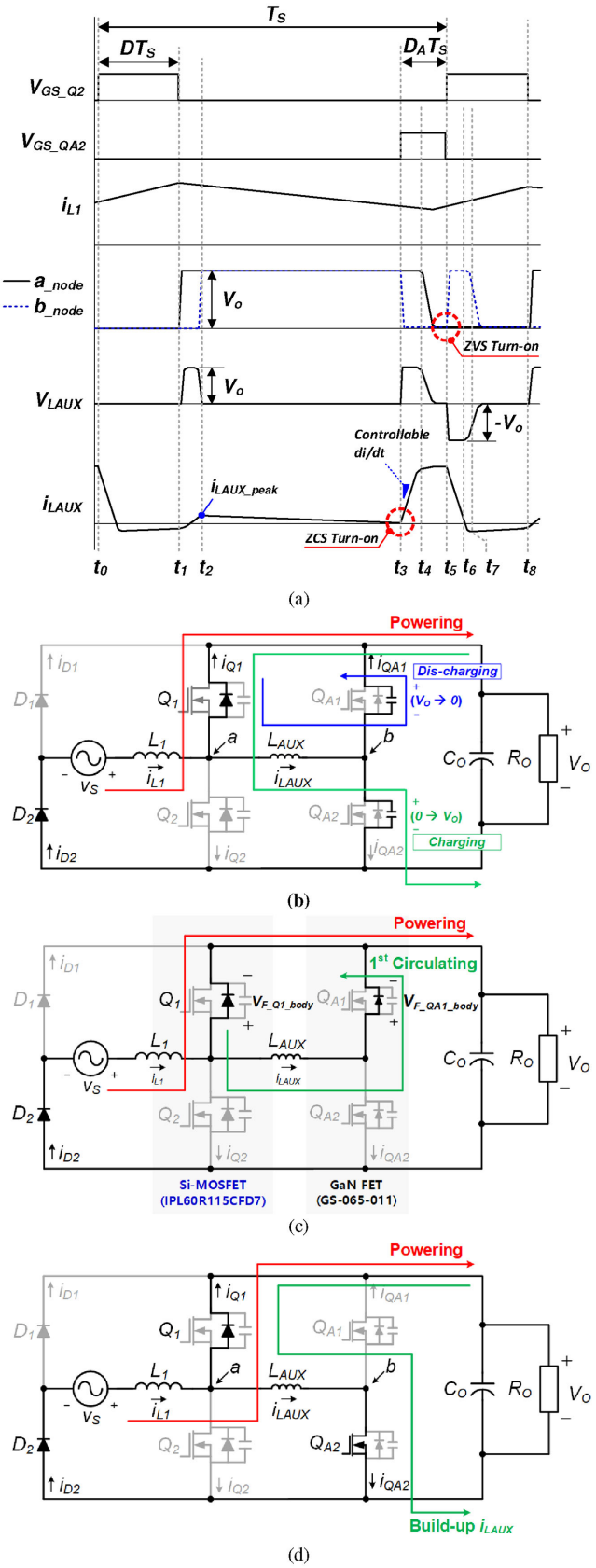


Fig. 4. Operational modes of the proposed reconfigurable converter under middle-to-heavy load. (a) Key waveforms of the proposed soft-switching capability. (b) Mode 1 (t_1–t_2). (c) Mode 2 (t_2–t_3). (d) Mode 3 (t_3–t_4). (e) Mode 4 (t_4–t_5). (f) Mode 5 (t_5–t_6). (g) Mode 6 (t_6–t_7). (h) Mode 7 (t_7–t_8).

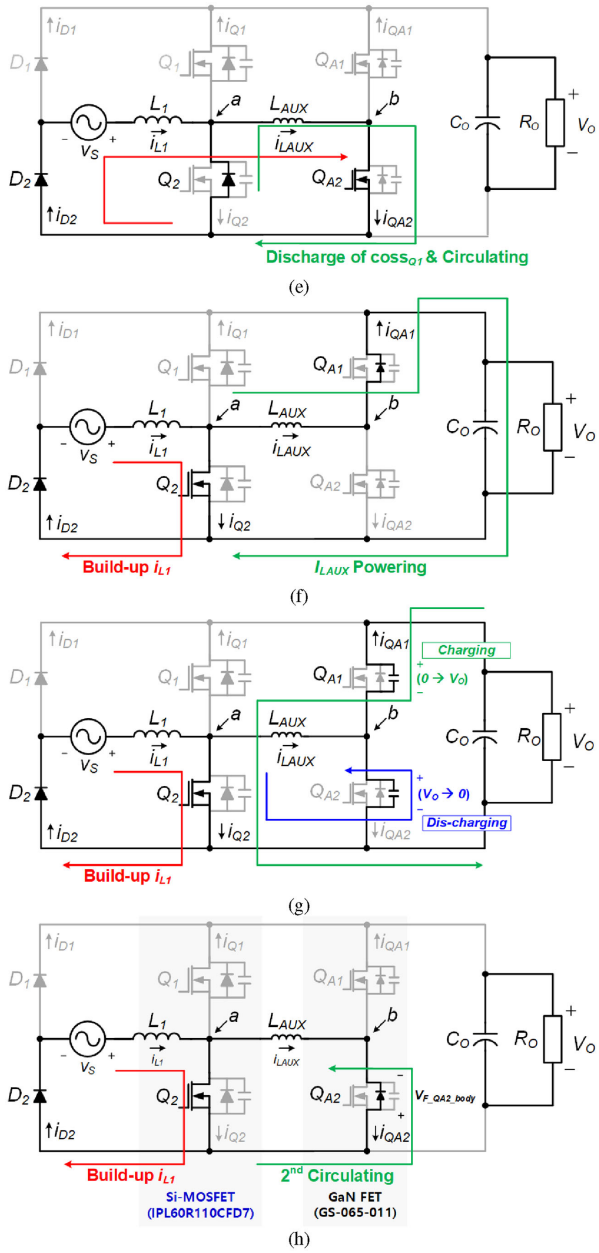


Fig. 4. (Continued) Operational modes of the proposed reconfigurable converter under middle-to-heavy load. (a) Key waveforms of the proposed soft-switching capability. (b) Mode 1 (t_1–t_2). (c) Mode 2 (t_2–t_3). (d) Mode 3 (t_3–t_4). (e) Mode 4 (t_4–t_5). (f) Mode 5 (t_5–t_6). (g) Mode 6 (t_6–t_7). (h) Mode 7 (t_7–t_8).

with the same slope of i_{LAUX}. It means that the slope of i_{Q1} is controllable by the current flowing through L_{AUX}. Therefore, the reverse-recovery concern can be relieved in the proposed converter. These characteristics can facilitate the utilization of Si-MOSFET for main switches even in the CCM operations.

Mode 4 [t_4–t_5]: In Mode 4, when i_{Q1} reaches zero, the auxiliary inductor current i_{LAUX} keeps on increasing since the voltage across L_{AUX} remains in a positive state.

Therefore, the difference between i_{LAUX} and i_{L1} contributes to the commutation, which means charging and discharging

junction capacitor for Q_1 and Q_2. After finishing the commutation between the junction capacitor for Q_1 and Q_2, i_{LAUX} keeps flowing through the body diode of Q_2, L_{AUX}, and Q_{A2} because the voltage across L_{AUX} is zero. If this circulating interval would be longer, system efficiency becomes lower. In order to minimize conduction loss by this circulating current, the proper adaptive turn-ON time for Q_{A2} should be carefully designed.

Mode 5 [t_5–t_6]: Mode 5 begins with turning ON Q_2 with ZVS operation due to preoperation. This soft-switching operation can reduce the switching loss significantly. In the auxiliary circuit, the build-up current i_{LAUX}, i.e., the energy stored in L_{AUX}, transfers to the output side through the body diode of Q_{A1}.

Mode 6 [t_6–t_7]: Mode 6 starts when i_{LAUX} reaches zero. At this time, if the energy stored in L_{AUX} is large enough to charge and discharge the parasitic capacitance C_{OSS_QA1} and C_{OSS_QA2}, the commutation operation is obtained by resonating with L_{AUX} and C_{OSS_QA1} and C_{OSS_QA2}. Therefore, in this interval t_6–t_7, the peak value of i_{LAUX_peak} can be expressed as in (2).

Mode 7 [t_7–t_8]: When C_{OSS_QA1} is fully charged up to output voltage V_O, this mode starts. The voltage across a_node is zero with Q_2 turn-ON state. Also, the voltage across b_node is zero because the junction capacitor C_{OSS_QA2} is fully discharged. Therefore, i_{LAUX} is circulating through Q_2, the body diode of Q_{A2}, and L_{AUX}. Hence, i_{LAUX} has a declined slope as follows:

$$\Delta i_{LAUX} = -\frac{V_{F\_QA2\_body}}{L_{AUX}}. \tag{5}$$

Therefore, as shown in the above mode analysis under middle-to-heavy load conditions, the proposed converter can achieve both soft-switching operation and relieved reverse-recovery concern utilizing the auxiliary circuit. As a result, the proposed reconfigurable totem-pole bridgeless PFC converter can improve the middle-to-heavy load efficiency even when utilizing Si-MOSFET having low cost and higher reliability, which is proved sufficiently by not using GaN-FET or SiC-MOSFET despite the CCM control method.

III. Design Guideline of the Proposed Converter

Since the proposed converter has similar characteristics with conventional totem-pole bridgeless PFC rectifier for main components such as main inductor L_1 and main switches Q_1 and Q_2, this section only emphasizes the design for an auxiliary circuit including L_{AUX} and auxiliary switches Q_{A1} and Q_{A2}.

A. Selection for Auxiliary Switches Q_{A1} and Q_{A2}

In the proposed converter, the voltage stress on the auxiliary switches Q_{A1} and Q_{A2} is clamped to output voltage V_O. It means the maximum voltage stress across auxiliary switches Q_{A1} and Q_{A2} is the output voltage from 390 to 400 V. Therefore, when selecting the auxiliary switch, the voltage stress can be obtained by having the same rating as the main switches Q_1 and Q_2. Under the $230V_{rms}$ input and full load conditions, the i_{LAUX_rms} value is less than 2 A. Considering current stress, the auxiliary switches can be selected with much lower current specification than the main switches. Therefore, it can allow choosing auxiliary switches that have smaller current rating and smaller parasitic capacitance value, resulting in high efficiency.

B. Reduction of Circulating Current i_{LAUX}

In this section, the reduction method of the circulating current value for i_{LAUX} is introduced in detail.

Under the middle-to-heavy load conditions, the circulating current occurs during Mode 2 and Mode 7 shown in Fig. 4(c) and (h). In these cases, its peak value i_{LAUX_peak} can be expressed by (2). In order to minimize the circulating current, the i_{LAUX_peak} value needs a way to optimize the inductance value L_{AUX} and capacitance $C_{OSS,Q2}$, considering the additional conduction losses.

However, even if L_{AUX} and $C_{OSS,Q2}$ are optimized, the circulating current still maintains a constant value over those periods, causing high conduction loss. Therefore, in the proposed converter, high efficiency can only be obtained by reducing the constant circulating current value. In order to alleviate the constant circulating current intentionally, the additional voltage source C_{AUX} can be considered, as shown in Fig. 5(a). However, the proposed converter cannot operate in the normal build-up and powering operation due to the additional voltage source by C_{AUX}.

Considering a different approach, if the main switches and auxiliary switches use different FETs which have different forward voltage drop values V_F of the body diodes, the circulating current can be declined dramatically, as shown in Fig. 5(b) and (c). Thus, different body diode's forward voltage V_F is utilized as a voltage source. Consequently, the circulating current i_{LAUX} can be decreased without additional components or circuits, as demonstrated in Fig. 5(d). Therefore, in this article, high efficiency can be obtained by reducing the constant circulating current without additional components or circuits.

C. Adaptive Duty Control for Auxiliary Switches

In the proposed converter, so as to ensure ZVS operation of main switches Q_1 and Q_2, the total turn-ON time t_A, as shown in Fig. 6(b), should be determined in the above-calculated boundary region, written in the soft-switching area according to the following:

$$t_A = t_{A1} + t_{A2} = \frac{i_{Q1}(t_3) \cdot L_{AUX}}{V_O} + \frac{1}{2} \cdot \pi \cdot \sqrt{2C_{OSS,Q2} \cdot L_{AUX}}. \tag{6}$$

In addition, if the total turn-ON time t_A is very long, the circulating current could be increased with high conduction loss. Accordingly, total turn-ON time t_A should be close to the boundary region as much as possible. As aforementioned, t_{A1} is depended on i_{Q1}. Whereas, t_{A2} is not a variable but a constant value regarding L_{AUX} and $C_{OSS,Q2}$. To retain proper adaptive duty control for turn-ON time t_A, the optimized turn-ON time t_A should be determined by sensing the inductor current i_{L1}, which is a variable. The value of the inductor current can be used to

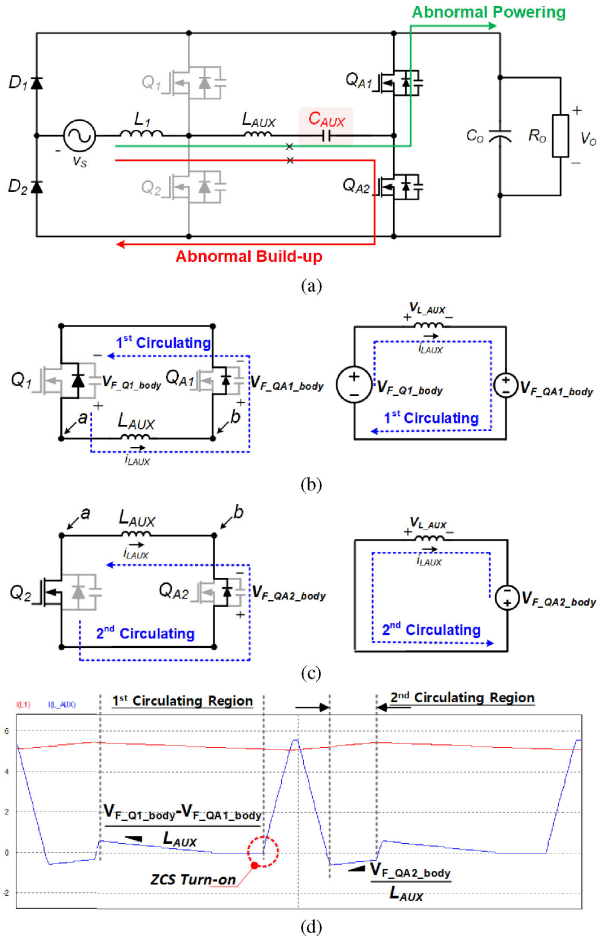


Fig. 5. Reduction method of circulating current, i_{LAUX}. (a) Method 1: Adding voltage source C_{AUX} on conduction path. (b) Method 2: Utilizing different forward voltage drop V_F characteristics in Mode 2. (c) Method 2: Utilizing different forward voltage drop V_F characteristics in Mode 7. (d) Verification for the effect of different Bode diode V_F characteristics.

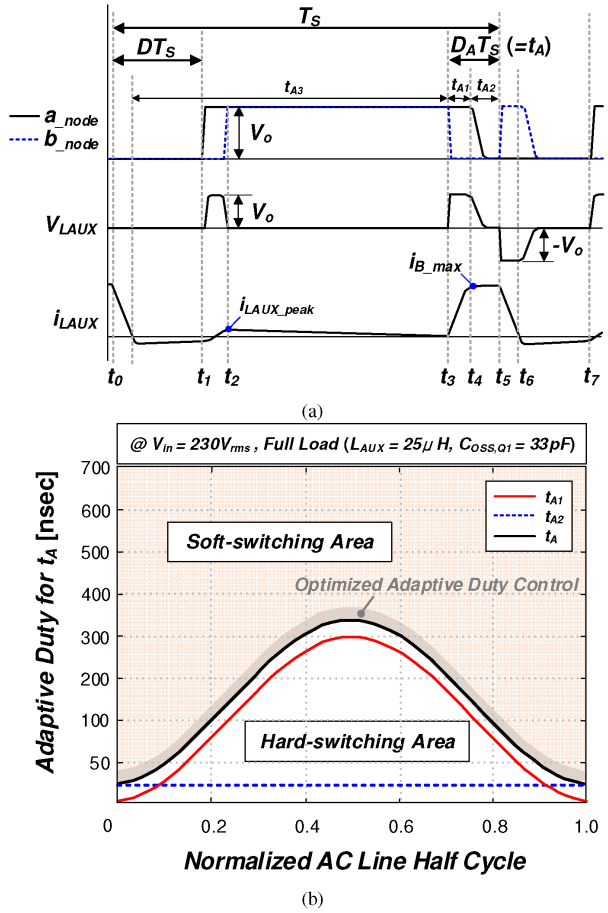


Fig. 6. Analysis for proper adaptive turn-ON time t_A for auxiliary switches. (a) Key waveforms for additional turn-ON time t_A. (b) Design example for adaptive turn-ON time t_A under $230V_{\mathrm{rms}}$ and full load conditions.

sense the existing inductor current i_{L1} of the PFC converter rather than an additional sensing method. As a result, the total turn-ON time t_A can be expressed as follows:

$$t_A \geq \frac{L_{\mathrm{AUX}}}{V_O} \cdot i_{L\_\mathrm{AVG}} + \frac{1}{2} \cdot \pi \cdot \sqrt{2C_{\mathrm{OSS},Q2} \cdot L_{\mathrm{AUX}}}. \quad (7)$$

In addition, it is significant to design a proper inductance value for the auxiliary inductor L_{AUX}. Therefore, the additional losses, such as conduction loss and switching loss, should be carefully considered in the proposed converter. At first, the current i_{LAUX}, as shown in Fig. 6(a), can be modeled by using a geometric average method as follows:

$$i_{\mathrm{LAUX\_rms}} = \sqrt{\sum_{n=1}^{n_{\max}} \left(\frac{V_O \cdot {t_{A1}}^2[n] \cdot \left({}^2\!/_3 \cdot t_{A1}[n] + t_{A2} \right)}{{L_{\mathrm{AUX}}}^2 \cdot T_S} + \left(\tfrac{1}{2} \cdot i_{\mathrm{LAUX\_peak}}[n] \right)^2 \cdot \left(\frac{t_{A3}}{T_S} \right) \right)^2} \cdot \quad (8)$$

Based on the above $i_{\mathrm{LAUX\_rms}}$ value (8), the additional losses regarding conduction loss can be calculated as follows:

$$P_{\mathrm{LOSS\_COND\_SW}} = R_{ds(\mathrm{on})} \times {i_{\mathrm{LAUX\_rms}}}^2$$

$$= R_{ds(\mathrm{on})} \times \sqrt{\sum_{n=1}^{n_{\max}} \left(\frac{V_O \cdot {t_{A1}}^2[n] \cdot \left({}^2\!/_3 \cdot t_{A1}[n] + t_{A2} \right)}{{L_{\mathrm{AUX}}}^2 \cdot T_S} + \left(\tfrac{1}{2} \cdot i_{\mathrm{LAUX\_peak}}[n] \right)^2 \cdot \left(\frac{t_{A3}}{T_S} \right) \right)^2} \quad (9)$$

$$P_{\mathrm{LOSS\_COND\_DIODE}} = V_{F\_\mathrm{TOTAL}} \times i_{\mathrm{LAUX\_AVG}}$$

$$= V_{F\_\mathrm{TOTAL}} \times \left(\sum_{n=1}^{\max} \sqrt{2} \sqrt{\frac{C_{\mathrm{OSS}}}{L_{\mathrm{AUX}}}} V_O[n] \right). \quad (10)$$

where $R_{ds(\mathrm{on})}$ is the channel resistance of the auxiliary switches, V_{F_TOTAL} is forward voltage, and the variable $[n]$ represents to the total number of each switching state transitions during the half-line cycle. By using (9) and (10), the minimum value for the sum of switching loss and conduction loss can be calculated in the auxiliary circuit. Considering additional losses in the auxiliary circuit, the inductance value L_{AUX} is designed as

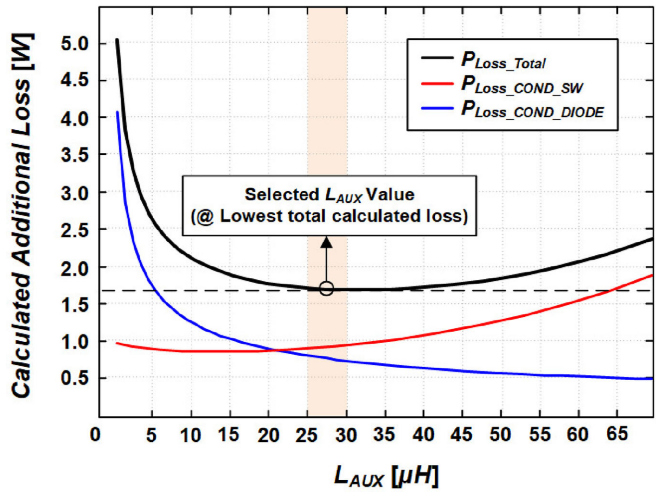


Fig. 7. Design example for proper inductance value L_{AUX} under $230V_{\mathrm{rms}}$ and full load conditions.

25–30 μH for high efficiency under $230V_{\mathrm{rms}}$ input and full load conditions, as shown in Fig. 7.

D. Control Circuit

Fig. 8 describes the control method utilizing a digital controller (TMS320F28069). The control block for the proposed converter is configured with three control blocks.

At first, the main control block is the same with the conventional bridgeless PFC converter. Next, the control block for d_A, which is the adaptive duty control block of auxiliary switches, is associated with adaptive turn-ON time for t_A in (7). As aforementioned, in the case of the proposed converter, the main inductor current i_{L1} is used as a variable without additional sensing method of the inductor current for the proper turn-ON time t_A. The switch selection block decides the proper gate signals according to the half-cycle detector that recognizes where the proposed converter is in the positive or negative status.

E. Control for Switch Transition

In Fig. 8(b), "Aux. Switch Enable" block with blue color is related to activating the auxiliary switches Q_{A1} and Q_{A2}. This control block is a factor directly involved in the transition and enabling of the auxiliary switches Q_{A1} and Q_{A2}. Fig. 8(b) shows the transition sequence of the "Aux. Switch Enable" control block. First, the criteria for dividing the transition between the light load and the heavy load are selected in advance based on the converter efficiency. The average value "$i_{L1\_AVG\_CAL}$" per half-cycle of the main inductor current is calculated inside the digital controller (TMS320F28069). Since the calculated "$i_{L1\_AVG\_CAL}$" reflects the load information proportionally, load information can be acquired without additional sensing circuit.

Based on the load information considering converter efficiency, when the load becomes larger than the reference level, the "auxiliary switch enable signal" is generated. When this signal is generated, the auxiliary switches are activated by starting the duty as small as possible for the stable operation of the system.

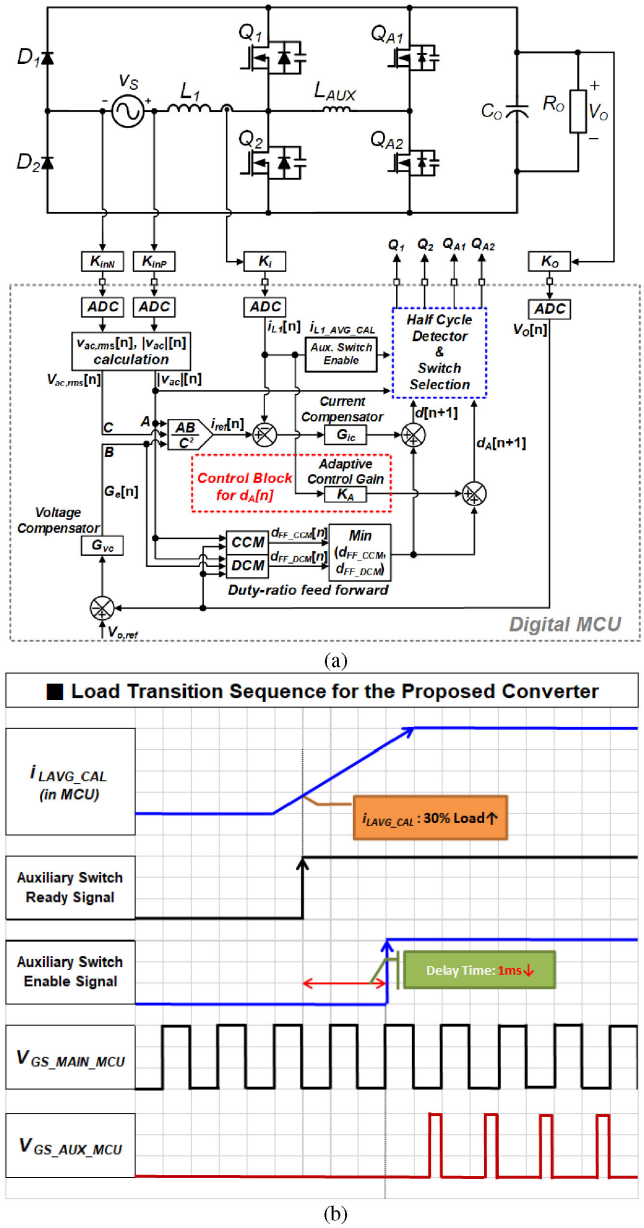


Fig. 8. Control block diagram of the proposed bridgeless PFC converter. (a) Inner control block. (b) Sequence for the switch transition.

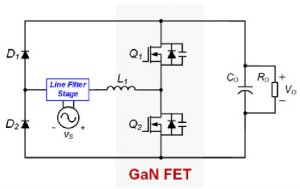
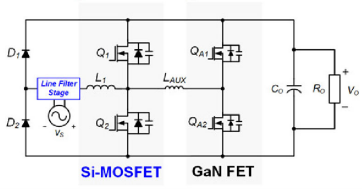
Fig. 9 is an experimental verification waveform related to the switch transition from light load to heavy load. As you can see in Fig. 9, as the load increases, the "$i_{L1\_AVG\_CAL}$" value increases inside digital micro controller unit (MCU). When this value reaches the reference level, the "Aux. Switch Enable" block is activated and the auxiliary switches are turned ON.

IV. Experimental Result

Based on the former analysis, the feasibility of the proposed structure has been verified by experimental results with a 750-W prototype with ac $230V_{\mathrm{rms}}$ input, 750 W/400 V output, and 65 kHz switching frequency as commonly used.

We also implemented a conventional totem-pole bridgeless PFC converter as a comparison with a similar optimization procedure. Table I summarizes the details of the two circuits.

TABLE I
DETAILED DESIGN PARAMETERS OF CONVENTIONAL AND PROPOSED CONVERTER

Components	Conventional Totem-pole Converter	Proposed Totem-pole Converter
		
Input	High Line ($230V_{RMS}$)	
Output	$400V/1.875A(750W)$	
f_{sw}	$65kHz$	
Main Switches (Q_1, Q_2)	**GaN FET** (2EA x \$10.12) GS66504B ($650V, 15A, 100m\Omega$)	**Si-MOSFET** (2EA x \$2.69) IPL60R115CFD7($650V, 22A, 115m\Omega$)
Auxiliary Switches (Q_{A1}, Q_{A2})	-	GaN FET (2EA x \$3.48) GS-065-011 ($650V, 11A, 150m\Omega$)
Driver IC	Si8238AB-D (Q_1, Q_2) (\$1.99 x 1)	Si8237AB-D (Q_{A1}, Q_{A2}) (\$1.48 x 1) UCC27714 (Q_1, Q_2) (\$1.21 x 1)
Inductors	1 Main Inductor, L_1 ($CH270043, 1.0\Phi, 82Turns, 820\mu H$)	1 Main Inductor, L_1 ($CH270043, 1.0\Phi, 82Turns, 820\mu H$) 1 Auxiliary Inductor, L_{AUX} (\$0.4) ($CH170060, 0.2\Phi, 19Turns, 20\mu H$)
Cost	High cost (\$22.23)	Low cost (\$15.43, 30%↓)

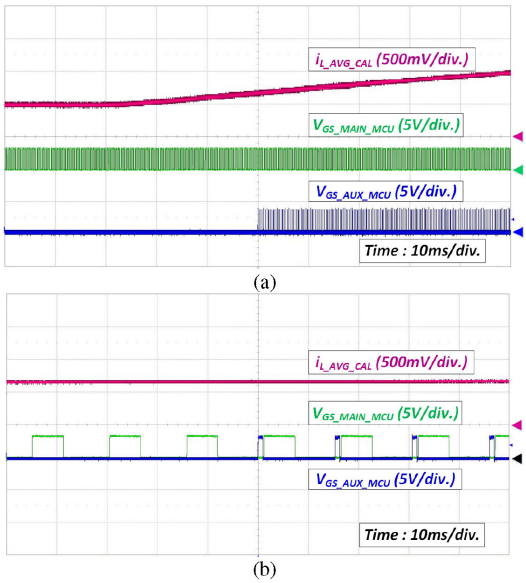


Fig. 9. Experimental verification for switch transition. (a) Switch transition. (b) Zoom-in waveform.

The conventional structure is general totem-pole bridgeless PFC rectifier. In the conventional structure, GaN-FET is used for main switches Q_1 and Q_2 considering CCM operations due to reverse-recovery problem. Whereas, the proposed structure in the right side of Table I can adopt Si-MOSFET as main switches Q_1 and Q_2. In addition, the auxiliary switches Q_{A1} and Q_{A2} are selected as GaN-FET having a relatively lower current rating with smaller parasitic capacitance than that of the main switches.

Fig. 10 shows the input and output characteristics regarding input voltage V_S, main inductor current i_L, auxiliary inductor current $i_{L\mathrm{AUX}}$, and output voltage V_O at the $230V_{\mathrm{rms}}$ input, 50% load, and full load conditions.

The additional current $i_{L\mathrm{AUX}}$ facilitates soft-switching operation in the proposed converter. As seen from the auxiliary inductor current $i_{L\mathrm{AUX}}$ waveform, it can be seen that the circulating current decreases gradually with a declining slope, securing ZCS turn-ON, as shown in Section III-B.

This is because the proposed converter utilizes different body diode's forward voltage V_F characteristics of main and auxiliary switches as a voltage source. Moreover, as seen in Fig. 9, it can be shown that the peak value of the auxiliary inductor current $i_{L\mathrm{AUX}}$ is slightly larger than the main inductor current i_L. This is because ZVS energy can be used as the difference between the auxiliary inductor current $i_{L\mathrm{AUX}}$ and the main inductor current i_L. This allows the proposed converter to achieve a soft-switching operation.

Fig. 11 shows steady-state waveforms including the input voltage and current and output voltage from light load to full load conditions. In the light load conditions, as shown in Fig. 11(a) and (b), the proposed converter can reduce the switching loss by utilizing the auxiliary switches for build-up and powering operations, as shown in Fig. 3(b) and (c). Over middle load conditions, as shown in Fig. 11(c) and (d), the proposed converter can improve efficiency by soft-switching operation.

Fig. 12 describes soft-switching operation for main switch Q_2 and adaptive duty control of auxiliary switches Q_{A2}. As seen in Fig. 12, the proposed converter can achieve ZVS turn-ON operation for main switch Q_2 and retain ZCS turn-ON operation

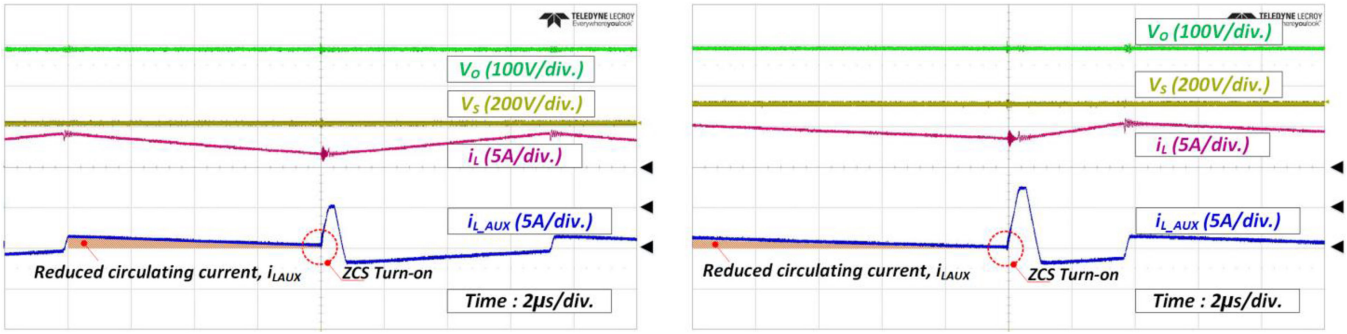


Fig. 10. Experimental waveforms of the proposed converter. (a) Under $230V_{\rm rms}$ 50% load conditions. (b) Under $230V_{\rm rms}$ full load conditions.

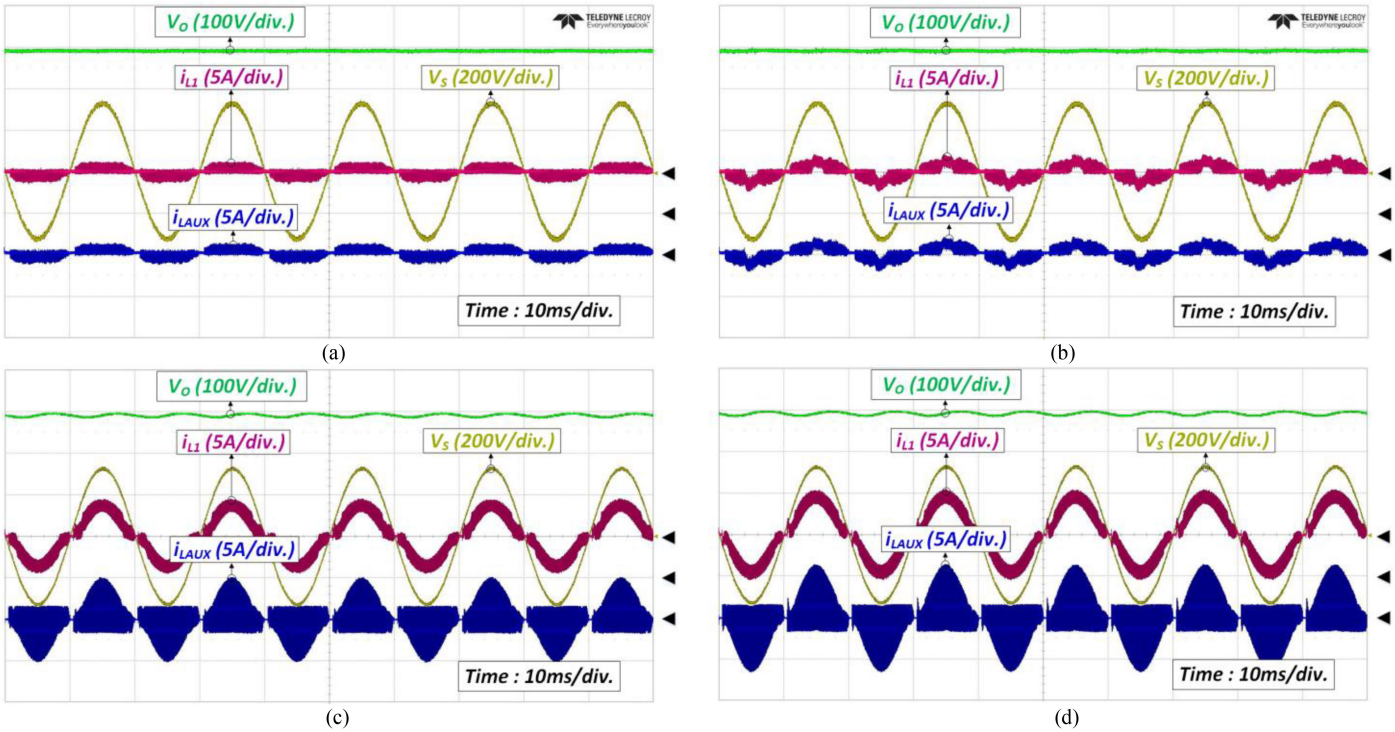


Fig. 11. Experimental waveforms of the proposed converter for $230V_{\rm rms}$ input and output characteristics. (a) Under 10% load conditions. (b) Under 20% load conditions. (c) Under 80% load conditions. (d) Under 100% load conditions.

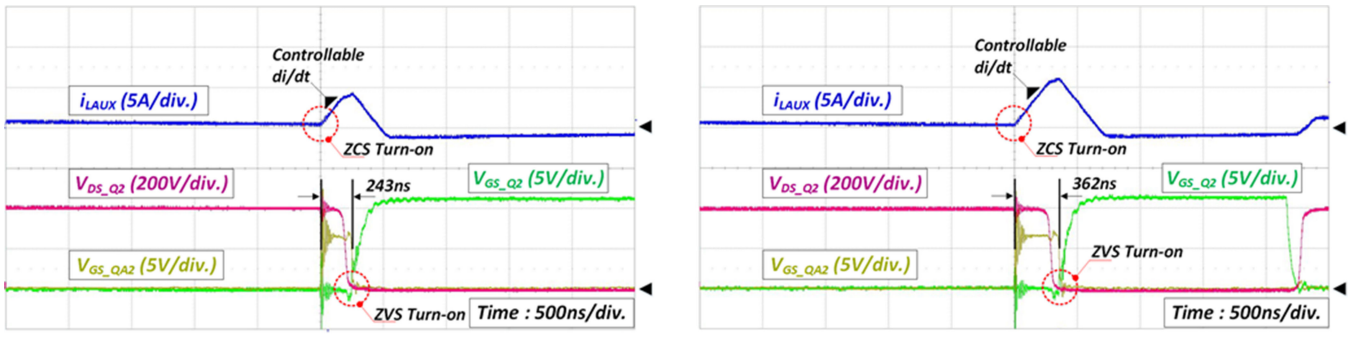


Fig. 12. Adaptive duty control waveforms for auxiliary switch turn-ON time t_A under $230V_{\rm rms}$ full load conditions. (a) $i_{LAUX} = 4$ A. (b) $i_{LAUX} = 7$ A.

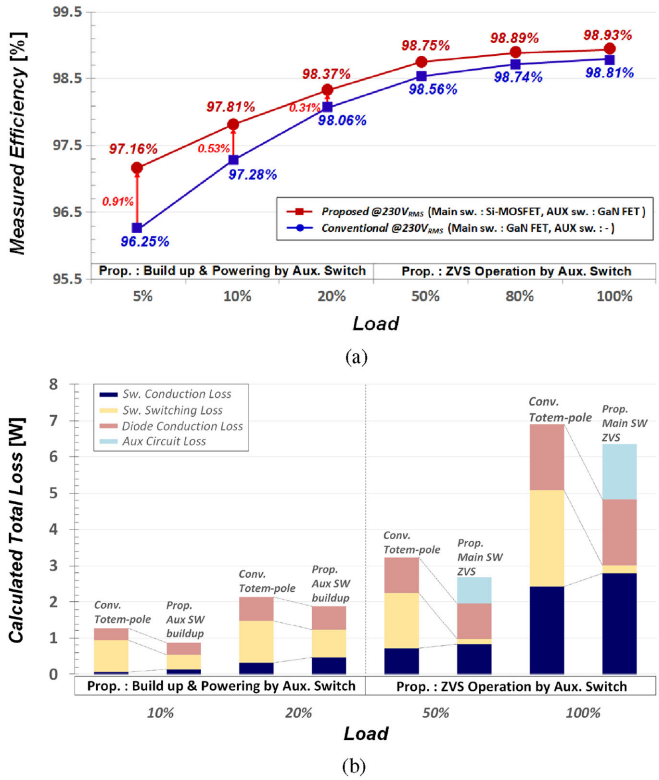


Fig. 13. Measured efficiency and calculated loss distribution chart according to the load variation under high-line 230$V_{\rm rms}$ conditions. (a) Measured efficiency. (b) Loss distribution chart.

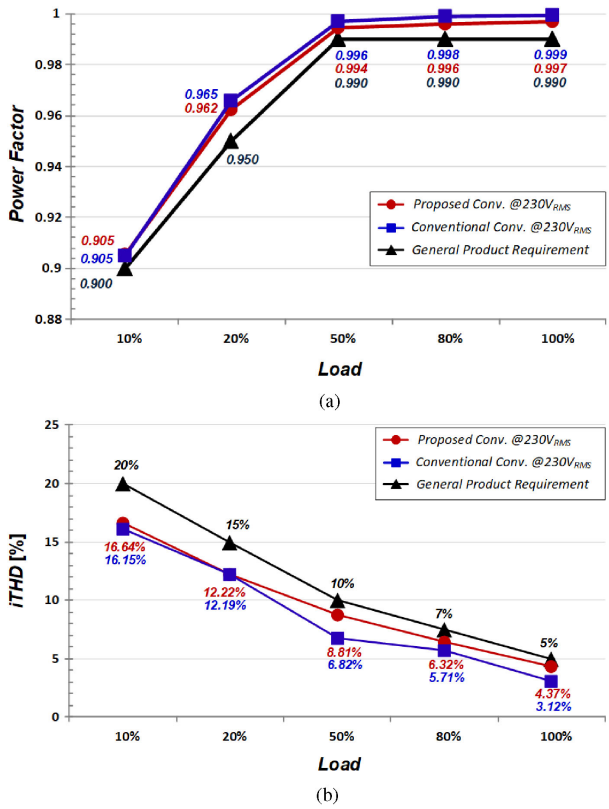


Fig. 14. Measured power quality according to the load variation under the high-line 230$V_{\rm rms}$ conditions. (a) Power factor. (b) iTHD.

for auxiliary switch Q_{A2}. Through these waveforms, the current in the additional circuit flows with controllable *di/dt* slope, resulting in relieved reverse-recovery concern.

Fig. 12 also presents adaptive turn-ON time t_A for auxiliary switches. By controlling adaptive turn-ON time for t_A, the proposed converter can obtain stable soft-switching operation and minimized conduction losses.

In Fig. 13, the measured efficiency and loss distribution chart are presented to compare with conventional totem-pole converter and the proposed reconfigurable totem-pole converter at the rated conditions. Overall, the proposed structure shows higher efficiency, especially at the light load conditions. Fig. 13(b) presents loss distribution regarding both the conventional and proposed converter. For light load conditions of less than 20%, the auxiliary switches that have smaller output capacitance are utilized as the main circuit for build-up and powering operation. This contributes to have lower switching losses of the proposed converter. In the case of 20% or heavier load, i.e., middle-to-heavy load conditions, the proposed converter can achieve soft-switching operation, such as ZVS turn-ON for the main switch and ZCS turn-ON for auxiliary switch, and the proposed converter can reduce reverse-recovery loss with controllable *di/dt*. This is why the proposed reconfigurable converter can acquire higher efficiency than a conventional totem-pole bridgeless converter.

Also, the power quality of the conventional and proposed converter is measured by using YOKOGAWA WT-1600 power analyzer. As shown in Fig. 14, the proposed converter has slightly lower PF and total harmonic distortion (THD) characteristics, but both the conventional and the proposed converter satisfy the general product requirements for the server power application. Therefore, it can be seen that, unlike the expected power quality concerns, the proposed converter can meet the power quality required by the general product requirement.

Finally, a comprehensive comparison is shown in Table II with various soft-switching bridgeless PFC topologies in terms of efficiency, the number of components, volume, circuit implementation, cost, and power quality (PF, iTHD).

As can be seen from Table II, in the case of "dual-boost ZVS bridgeless PFC rectifier structure [15]," low cost and easy implementation can be acquired. However, it is difficult to have high efficiency and high power density because of two large main inductors and a large number of components.

Next, "interleaved totem-pole ZVS bridgeless PFC rectifier [16]" can have a small input filter due to the interleaved operation. Thus, it is possible to secure a high power density. In addition, it is very easy to implement a driver circuit for driving all the switches. However, since a large circulating current should flow for ZVS operation, it causes a high conduction loss and is not advantageous in terms of efficiency. In addition, despite the ZVS operation, all the four switches utilize a high-cost GaN-FET, so there is no cost advantage.

Third, "totem-pole bridgeless PFC converter with bidirectional switch ZVS cell [17]" can meet high efficiency with no large circulating current for ZVS operation. However, in this article, the authors mention that both the main switches and the auxiliary switches use high-cost SiC-FETs. In addition,

TABLE II
COMPREHENSIVE COMPARISON WITH VARIOUS SOFT-SWITCHING BRIDGELESS PFC CONVERTERS

Topologies	[15]	[16]	[17]	Proposed
Efficiency	△ (Many number of components)	△ (Large circulating current for ZVS)	○	◎
Active Components	Switches : 4ea Diodes : 6ea	Switches : 4ea (All the sw. : GaN-FET) Diodes : 2ea	Switches : 6ea (Main sw. : SiC-FET, Aux sw. : SiC-FET) Diodes : 4ea (Anti-parallel SiC-diodes for main sw.)	Switches : 4ea (Main sw. : Si-FET, Aux sw. : GaN-FET) Diodes : 2ea
Passive Components	Main Inductor : 2ea (Dual-boost structure) Auxiliary Inductor : 1ea	Main Inductor : 2ea (Interleaved structure) Auxiliary Inductor : 1ea	Main Inductor : 1ea Auxiliary Inductor : 1ea	Main Inductor : 1ea Auxiliary Inductor : 1ea
Volume	△ (Large volume of 2-main inductors)	○	△ (Many number of components)	○
Driving Circuit Implementation	○	○	△ (Floating or isolated gate driver)	○
Cost	○	△ (High cost GaN-FETs for all the sw.)	△ (High cost SiC-FETs for all the sw.)	○
PF, THD	○	◎	○	○

◎: Very good, ○: Good, △: Poor.

four antiparallel SiC-diodes are used to reduce reverse-recovery characteristics for the main switches.

As a result, the topologies in [17] could not have high power density and low-cost advantage. Furthermore, in order to drive the auxiliary switches, a floating or isolated driver circuit should be required, which has a disadvantage in terms of driving circuit implementation.

Meanwhile, the proposed converter in Table II can have higher efficiency with reduced circulating current without additional circuit. Moreover, it is easy to drive the proposed converter with simple bootstrap circuit due to leg structure such as high-side and low-side switches. In addition, the proposed converter can use low-cost Si-FET for the main switches even in totem-pole structure by utilizing simple ZVS circuit. As a result, compared to other topologies in terms of cost, the proposed converter can have an advantage in terms of low cost.

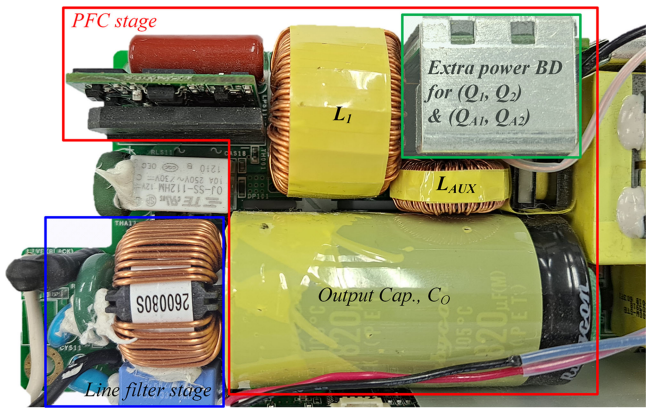


Fig. 15. Prototype of the Proposed Structure.

V. CONCLUSION

A reconfigurable totem-pole bridgeless PFC rectifier for high efficiency is proposed in this article. The proposed converter adopts the auxiliary circuit to reduce the switching loss in the conventional totem-pole bridgeless PFC rectifier. By utilizing an auxiliary circuit, the proposed converter can acquire high efficiency over the entire load condition. In the light load conditions, the auxiliary circuit is utilized as a main circuit for build-up and powering operation. This allows the proposed converter to reduce the switching loss, resulting in high light load efficiency. Moreover, in the case of middle-to-heavy load conditions, the proposed converter can obtain ZVS turn-ON, relieved reverse-recovery concerns of main switches, and ZCS turn-ON of auxiliary switches. In addition, the conduction loss in the auxiliary circuit can be minimized by adopting adaptive duty control for auxiliary switches. Moreover, the additional conduction loss regarding circulating current can be reduced by utilizing different body diode's forward voltage V_F characteristics of both main switches and auxiliary switches without additional voltage sources.

The feasibility of proposed converter has been verified with 230*VRMS* input and 750W (400V/1.875A) output conditions with prototype as shown in Fig. 15. Based on the experimental results with rated input and output conditions, the proposed converter can achieve stable CCM operation with Si-MOSFET, resulting in low cost and high efficiency over the entire load condition.

REFERENCES

[1] S. P. Vanka, A. F. Shinn, and K. C. Sahu, "Computational fluid dynamics on graphics processing units: Challenges and opportunities," in *Proc. ASME Int. Mech. Eng. Congr. Expo.*, 2011, pp. 429–437.

[2] Grattan analysis of ABS, "Retail electricity prices rose sharply from the late 2000s," 2017.

[3] *80 Plus Incentive Program*. [Online]. Available: http://www.80plus.org

[4] *Energy Savers Program*. [Online]. Available: http://www.energystar.gov

[5] H. S. Youn, J. S. Park, K. B. Park, J. I. Baek, and G. W. Moon, "A digital predictive peak current control for power factor correction with low-input current distortion," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 900–912, Jan. 2016.

[6] J. W. Kim and G. W. Moon, "Minimizing effect of input filter capacitor in a digital boundary conduction mode power factor corrector based on time-domain analysis," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3827–3836, May 2016.

[7] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 799–807, May 2016.

[8] F. C. Lee, Q. Li, Z. Liu, Y. Yuchen, C. Fei, and M. Mu, "Application of GaN devices for 1 kW server power supply with integrated magnetics," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 3–12, 2016.

[9] M. M. U. Alam, W. Eberle, and F. Musavi, "A semi-bridgeless boost power factor corrected converter with an auxiliary zero voltage switching circuit for electric vehicle battery chargers," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 1820–1825.

[10] J. Zhang, Z. Lu, and B. Su, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electron.*, vol. 5, no. 3, pp. 358–365, 2012.

[11] T. Shimada, A. Kanouda, and S. Tshkamoto, "A novel bridgeless PFC boost rectifier with a simple ZVS circuit," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–7.

[12] W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, "Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction," *IET Power Electron.*, vol. 1, no. 2, pp. 194–202, Jun. 2008.

[13] K. S. B. Muhammad and D. D. C. Lu, "ZCS bridgeless boost PFC rectifier using only two active switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2795–2806, May 2015.

[14] M. Alam, W. Eberle, D. S. Gautam, and C. Botting, "A soft-switching bridgeless AC–DC power factor correction converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7716–7726, Oct. 2017.

[15] Y. Jeong, J. K. Kim, and G.-W. Moon, "A bridgeless dual boost rectifier with soft-switching capability and minimized additional conduction loss," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2226–2233, Mar. 2018.

[16] M. H. Park, J. I. Baek, Y. Jeong, and G.-W. Moon, "An interleaved totem-pole bridgeless boost PFC converter with soft-switching capability adopting phase-shifting control," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10610–10618, Nov. 2019.

[17] Z. Yu, Y. Xia, and R. Ayyanar, "A simple ZVT auxiliary circuit for totem-pole bridgeless PFC rectifier," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2868–2878, May/Jun. 2019.

[18] J. W.-T. Fan, R. S.-C. Yeung, and H. S.-H. Chung, "Optimized hybrid PWM scheme for mitigating zero-crossing distortion in totem-pole bridgeless PFC," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 928–942, Jan. 2019.

Young-Dal Lee (Student Member, IEEE) received the B.S. degree in control and instrumentation engineering from Hanbat National University, Daejeon, South Korea, in 2011, and the M.S. degree in electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2013. He is currently working toward the Ph.D. degree with the Korea Advanced Institute of Science and Technology, Daejeon, South Korea.

From 2013 to 2017, he was a Senior Engineer with the Power R&D Team, Samsung Electro-Mechanics, Suwon, South Korea, developing high efficiency server power supply. His research interests include ac/dc and dc/dc converters, bridgeless PFC boost converter, and wireless power transfer systems.

Gun-Woo Moon (Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1992 and 1996, respectively.

He is currently a Professor with the Department of Electrical Engineering, KAIST. His research interests include modeling, design and control of power converters, soft-switching power converters, resonant inverters, distributed power systems, power-factor correction, electric drive systems, driver circuits of plasma display panels, and flexible ac transmission systems.

Dr. Moon is a member of the Korean Institute of Power Electronics (KIPE), Korean Institute of Electrical Engineers (KIEE), Korea Institute of Telematics and Electronics (KITE), Korea Institute of Illumination Electronics and Industrial Equipment (KIIEIE), and Society for Information Display (SID).

Jaeil Baek (Member, IEEE) received the B.S. degree in electronics and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2007, and the M.S. and Ph.D. degrees in the electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2018, respectively.

He is currently a Postdoctoral Research Associate with the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA. His current research interests include point-of-load power converter, grid-interface power electronics, digital control approach of converters, and advanced power electronics architectures.

Dr. Baek was the recipient of the Research Outstanding Award from the KAIST, and the Global Ph.D. Fellowship and Postdoctoral Fellowship from the National Research Foundation of Korea.

Chong-Eun Kim (Member, IEEE) received B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 2001, and the M.S. and Ph.D. degrees in power electronics from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2003 and 2008, respectively.

In 2105, he was a Senior Engineer developing high efficiency server power supply with the Power R&D Team, Samsung Electro-Mechanics, Suwon, South Korea, where he became a Principal Engineer in 2019. He is currently an Assistant Professor with the Department of Control and Instrumentation Engineering, Gyeongsang National University, Jinju, South Korea. His research interests inlcude ac/dc and dc/dc converters, including bridgeless PFC boost converters, high-frequency *LLC* resonant converters, and high-efficiency PSFB converters.