A New Gate Drive Power Supply Configuration for Common Mode Conducted EMI Reduction in Phase-Shifted Full-Bridge Converter

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***Abstract*—This article presents a cascaded gate drive power supply configuration to reduce the common mode (CM) current in phase-shifted full-bridge (PSFB) converters. In such converters, there are at least two dV/dt sources generated at different floating points associated to the parasitic capacitances of the isolated barriers of the gate drivers (power supplies, and control signal isolation units), which can increase the conducted electromagnetic interference perturbations. This article is focused on the analysis of a new gate drive power supply configuration, which reduces the CM currents that circulate in the control part of the switching cells. This improvement is achieved by modifying the impedance network of CM current pathways. Experimental results are provided to prove the effectiveness of the new gate drive power supply configuration on a PSFB converter based on SiC-MOSFET devices.**

***Index Terms*—Electromagnetic interference (EMI), full-bridge, gate driver, parasitic capacitance, SiC-MOSFET.**

I. Introduction

THE use of wide-band gap (WBG) transistors such as GaN-HEMT and SiC-MOSFET allows the power electronics designers to increase the power density and the efficiency of power converters [1]–[4]. Compared to silicon devices, the switching speed of WBG devices is increased to reach few 100 V/ns for the drain-to-source dV/dt for instance [5]. Unfortunately, the main drawback is the increase of common mode (CM) current due to dV/dt and parasitic capacitances between the power part and the control part.

SiC-MOSFET-based phase-shifted full-bridge (PSFB) converters have been proposed for medium to high power applications because of simple topology and easy switching control. Theoretically, a full-bridge converter under bipolar pulsewidth modulation (PWM) should produce very little CM noise because the two phase-legs can compensate for each other. However, in the PSFB converters, the electric potential variation of the two phase-leg midpoints happens at different times, and the displacement current generated by two midpoints through associated parasitic capacitances cannot be cancelled by each other [6]. Various methods to reduce CM noises in the power side have been proposed for isolated power converters [7], [8]. Gate driver configurations have been proposed in the literature [9]–[11] to mitigate these CM currents in the control side for a simple inverter leg. In these proposed solutions, the drive circuitries (gate drive power supplies and transfer signals) are completely cascaded. In this case, delay between the gate signals are introduced. This is unacceptable for fast switching times, especially for PSFB converters where minimal mismatching delay between high side and low side control signals is required in order to reduce leakage inductance value and to minimize dead-time duration while zero voltage switching (ZVS) operation [12], [13]. Therefore, this article proposes a new gate drive power supply configuration to reduce the CM currents that circulate from the power part to the control part in PSFB converters without introducing gate signal delays. The proposed gate driver configuration can be applied in many topologies that have at least one inverter leg configuration like three-phase and multilevel inverters, series-connected devices, etc. Nevertheless, this article is focused in the full-bridge topology under phase-shift modulation.

The CM currents that circulate in PSFB converters can be divided in two categories: 1) the CM currents that circulate in the power part through the power devices and the ground (through the dielectric barrier of the package) [14], [15], and 2) the CM currents that circulate in the control part through the isolation barriers of the dc–dc power supplies and signal transmission functions of gate drivers [16], [17]. This article is focused on the second category, i.e., on the CM currents that circulate through the parasitic capacitances introduced by dc–dc power supplies and signal transmission functions of gate drivers. Fig. 1 shows these parasitic capacitances: 1) the parasitic capacitance introduced by the primary to secondary gate drive power supply (C_{ps}), and 2) the parasitic capacitance of the signal isolation (C_{iso}). The parasitic capacitances C_{ps} and C_{iso} have the same dynamic influence on the system. However, in this article, it is considered that the capacitance C_{iso} is negligible in relation to C_{ps} since in the experiments, insulation signals are implemented by optical fibers.

The parasitic elements of the gate drive power supply and its connections are shown in Fig. 2. As can be seen, two reference

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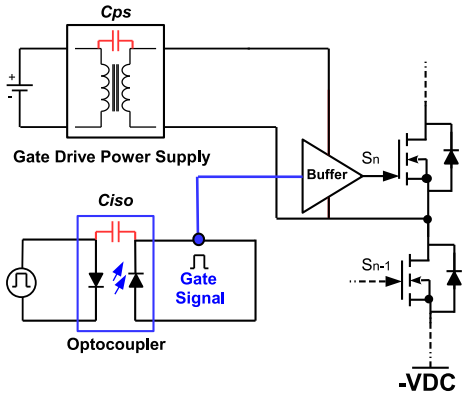

Fig. 1. Gate drive power supply and signal isolation unit parasitic capacitances.

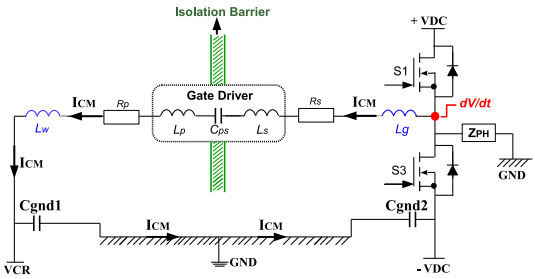

Fig. 2. Parasitic elements of the gate drive power supply and its connections.

TABLE I
GATE DRIVE CIRCUITRY ELEMENTS PRESENTED IN Fig. 2

Element	Description
C_{ps}	Parasitic capacitance of the isolated DC/DC converter.
C_{gnd1}	Parasitic capacitance between the control reference (VCR) and the ground (GND).
C_{gnd2}	Parasitic capacitance between power reference (-VDC) and the ground (GND).
L_p	Parasitic terminal inductance on the primary side of the gate drive power supply.
L_s	Parasitic terminal inductance on the secondary side of the gate drive power supply.
L_w	Parasitic inductance of the power supply on the primary side.
L_g	Parasitic inductance of the power supply on the secondary side.
R_p	Parasitic resistance of the power supply on the primary side.
R_s	Parasitic resistance of the power supply on the secondary side.
Z_{PH}	Parasitic impedance between the middle point of each power leg and the heatsink connected to the ground.

potentials are presented in classical switching cells [18], [19], i.e., the ground or reference potential of the remote control circuit (VCR) and the reference potential of the power circuit (−VDC). Both VCR and −VDC are isolated from each other. Therefore, isolated supply converters are implemented in order to enable the isolation dedicated to the power supply parts. Optocouplers or optical fibers are used to isolate the paths for the control signals. Table I describes the main elements presented in Fig. 2.

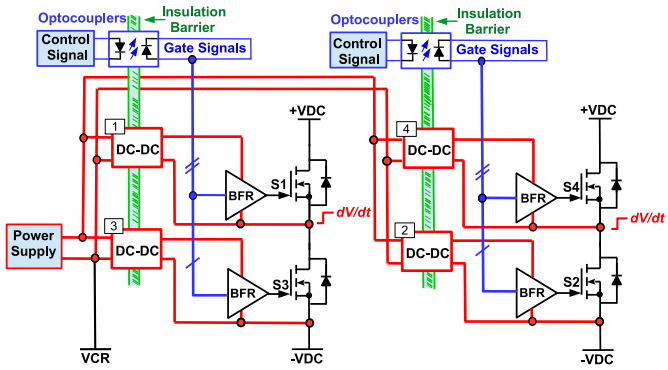

Fig. 3. Traditional gate drive power supply configuration (TGD).

To clarify the purpose of this article, the CM parasitic impedance (ZPH) between the middle point of each power leg and the heatsink connected to the ground of the primary side of the control circuit is presented in Fig. 2 [20], [21]. However, this article focuses on the perturbations of the power circuit on the control side, i.e., the CM currents that circulate through the parasitic capacitances C_{gnd1} and C_{gnd2}. The noise currents that circulate through ZPH will not be analyzed in this article.

In PSFB converters there are two middle points which correspond to two dV/dt sources. Then, if isolated power supplies in the drive circuitry are used, they introduce primary to secondary parasitic capacitances (C_{ps}), and therefore several CM conducted EMI pathways. As shown in Fig. 2, where the gate drive circuitry elements are presented, each dV/dt source produces its own conducted current disturbance that propagates to the control parts and then through the ground. The CM current that flows through the parasitic capacitance of the gate driver and circulates in the control side is described by (1). As can be seen, the CM current is directly proportional to the switching speed of the devices. Therefore, to avoid damages caused by a large amount of noise currents in the control side, this article proposes a new gate drive power supply configuration

$$I_{CM} = C_{ps}\frac{dV}{dt}. \tag{1}$$

The rest of this article is organized as follows. In Section II, the traditional and the new gate drive power supply configurations for PSFB converters are presented. In Section III, impedance network circuits are used to achieve transfer functions that predict the behavior of CM currents that circulate in the control side. The traditional and new gate drive power supply configurations are analyzed by using a step response in time domain. The validation of the proposed gate driver configuration by electrical measurements are presented in the Section IV.

II. TRADITIONAL AND CASCADED GATE DRIVER CONFIGURATIONS

In this section, the traditional and the proposed gate drive power supply configurations are introduced in the PSFB converter. Two inverter legs are also modeled with their associated gate drive power supplies. In Figs. 3 and 4, the dc–dc and

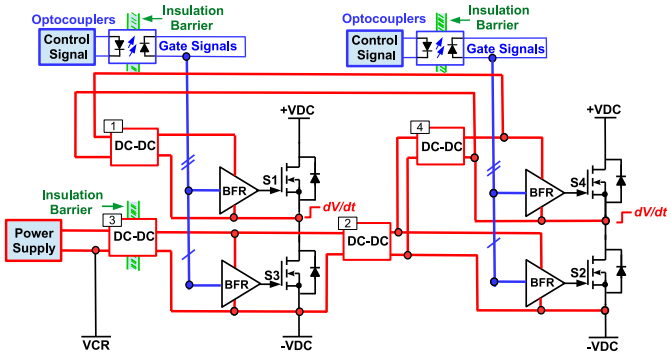

Fig. 4. Cascaded gate drive power supply configuration (CGD).

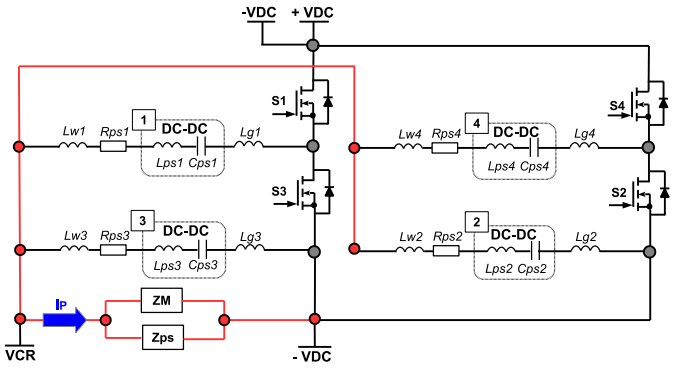

Fig. 5. TGD: Equivalent impedance network circuit.

buffer (BFR) blocks represent, respectively, the gate drive power supplies and the buffers used to turn-ON and turn-OFF the power devices.

A. Traditional Gate Driver Configuration (TGD)

The traditional gate driver configuration is shown in Fig. 3, which each isolated power supply of each gate driver is supplied independently by an external power supply. In this configuration, there are two sources of perturbation produced by two floating points. As can be seen, each floating point that has a high dV/dt is directly connected to a gate drive power supply (dc–dc block) that introduces a parasitic capacitance (C_{ps}). In the TGD configuration, the CM currents, produced by the dV/dt sources, have to cross one isolation barrier that is modeled by C_{ps} to circulate into the control side. According to (1), the CM currents in the control side, maintaining the same switching speed, can be mitigated by reducing the C_{ps} value. However, the lower the capacitance C_{ps}, the more expensive is the power supply. Furthermore, most of commercial isolated gate drivers are often rated for a CM transient of < 100 kV/μs [22]. Nevertheless, some WBG power devices, such as GaN transistors require more than 100 kV/μs for the CM transition [23]. In other words, the complexity to develop isolated gate drivers (with ultralow parasitic capacitance) that respects the WBG requirements becomes each time more difficult (and more expensive). Therefore, a smart solution to decrease the CM currents in the control side, is to change the CM current pathway by cascading the gate drive power supplies as shown in the next sections. Furthermore, advanced gate drive power supplies with ultralow parasitic capacitances can also be cascaded to further improve the CM transient immunity.

B. Cascaded Gate Driver Configuration

The proposed gate driver configuration is shown in Fig. 4, where the gate drive power supplies are fully cascaded: the gate driver 3 (corresponding to the switch S3) is directly powered by an external power supply connected to the control reference (VCR), the gate driver 2 is powered by the gate driver 3, the gate driver 4 is powered by the gate driver 2, and the gate driver 1 is powered by the gate driver 4. The control signal configuration does not change. Therefore, the gate signals are not affected by changing the gate drive power supply configuration.

In the CGD, the CM currents, produced by the dV/dt sources, have to cross more than one isolation barrier to circulate into the control side. As will be explained in the next sections, when the CGD configuration is used, the CM currents in the control side are drastically reduced when compared to the conventional gate driver configuration.

III. Traditional and Cascaded Gate Driver Configurations: Analytical Analysis

In this section, an analytical approach is proposed to estimate the CM current that circulates into the control part. The behavior of CM currents can be achieved by deriving a transfer function or a step response in time domain for determining a relationship between the cause and effect of disturbances [24]. To this end, impedance network circuits are used to achieve transfer functions that relate the CM current that circulates in the control side (I_P) to the total CM current generated by each leg inverter (I_{CM}). A step response in time domain is used to estimate I_P for TGD and CGD configurations. The total CM noise generated at the middle point of each power leg (I_{CM}) is used to estimate the CM current that circulates in the control side (I_P). Therefore, it is supposed that both gate driver configurations produce, at the middle points of the power legs, the same amount of noise current. The current levels are estimated related to the one produced by TGD configuration since it remains difficult to estimate the absolute level of disturbance without exact calculations. In other words, the models and equations proposed in this article are used to compare the control side CM current levels produced by both gate driver configurations. Therefore, the classical and cascaded gate driver configurations can be compared toward criteria on the CM current.

A. Traditional Gate Driver Configuration

The analytical approach is based on an equivalent circuit of the PSFB considering the parasitic elements of the gate drivers as shown in Fig. 5. The equivalent impedance network circuit is achieved by short circuiting the electrodes of large capacitors/voltage supplies such as power side dc bus (+VDC) and the ground of power circuit ($-$VDC) [5], [10]. To facilitate the analysis and simplify the equations, the gate driver parasitic

TABLE II
SUMMARIZED SWITCHING STATES IN PSFB CONVERTERS

State	I	II	III	IV
S1	OFF	Switching	ON	Switching
S2	Switching	ON	Switching	OFF
S3	ON	Switching	OFF	Switching
S4	Switching	OFF	Switching	ON

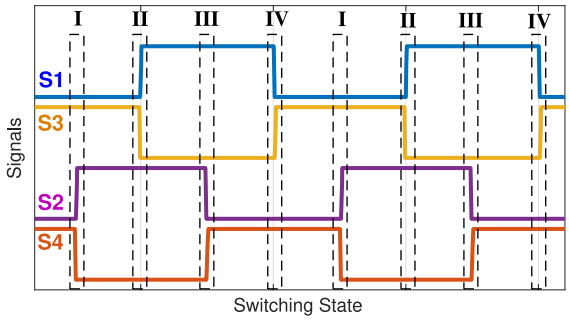

Fig. 6. Gate signals and switching states in PSFB converters.

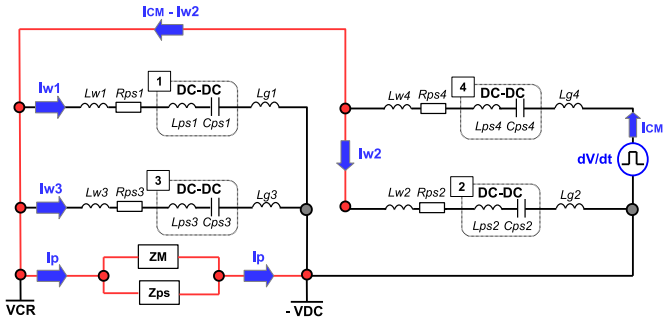

Fig. 7. TGD: Equivalent impedance network circuit in states I and III.

inductances L_p and L_s, and the resistances R_p and R_s shown in Fig. 2 are replaced by L_{ps} and R_{ps}, which represents $L_p + L_s = L_{ps}$ and $R_p + R_s = R_{ps}$, respectively. The impedance Z_{PS} represents the parasitic impedance between VCR and $-$VDC. In the experimental part, an additional impedance ZM (characterized by a large capacitor $>> Cgnd1 + Cgnd2$) is connected between VCR and $-$VDC to concentrate and measure the noise current that circulates in the drive circuit. In other words, to facilitate the conducted EMI measurements, ZM is added to short Z_{PS}. Therefore, the total amount of the CM current in the control side circulates through ZM.

The electrical scheme shown in Fig. 5 is a generic impedance network circuit used to clarify the TGD configuration. However, in the PSFB converter, as shown in Table II and in Fig. 6, the middle point potential variations occur during four main switching states. In this case, the impedance and the pathway seen by the CM current can be different for each switching state.

To investigate the CM current that circulates in the control side as a function of each switching state, Figs. 7 and 8 show the total CM current (I_{CM}) distribution generated by middle points

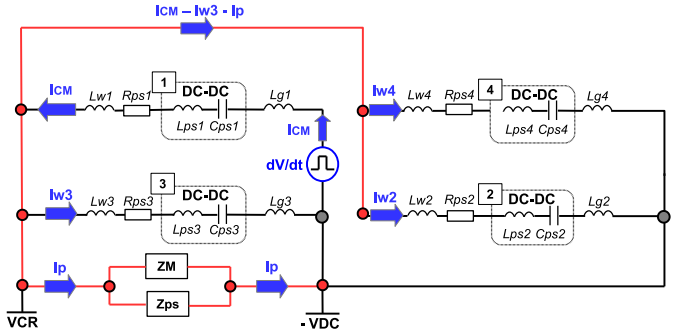

Fig. 8. TGD: Equivalent impedance network circuit in states II and IV.

of the two legs of the PSFB. Note that, the state I is similar to the state III, and the state II is similar to the state IV, i.e., two devices are in static mode while the two others are switching. In this case, only two equivalent impedance network circuits are necessary to analyze the four switching events.

The first model, shown in Fig. 7, represents the equivalent impedance network circuit for the states I and III, where the switches S1 and S3 are in the static state, and S2 and S4 are in transition.

To simplify the equations and facilitate the analysis, the gate drive power supplies are considered identical

$$L_{ps1} = L_{ps2} = L_{ps3} = L_{ps4} = L_{ps} \tag{2}$$

$$L_{w1} = L_{w2} = L_{w3} = L_{w4} = L_w \tag{3}$$

$$L_{g1} = L_{g2} = L_{g3} = L_{g4} = L_g \tag{4}$$

$$R_{ps1} = R_{ps2} = R_{ps3} = R_{ps4} = R_{ps} \tag{5}$$

$$C_{ps1} = C_{ps2} = C_{ps3} = C_{ps4} = C_{ps}. \tag{6}$$

In this case, according to the distribution conductive I_{CM} current in Fig. 7, it is easy to note that, the impedances formed by the circuits $L_w - R_{ps} - C_{ps} - L_g$ of the gate drivers 1, 2, and 3 are connected in parallel. Therefore, the following current relation can be written in the Laplace domain:

$$\frac{I_P(s)}{I_{CM}(s)} = \frac{\frac{X_{ps}(s)+X_{Lw}(s)+X_{Lg}(s)}{3}}{\frac{X_{ps}(s)+X_{Lw}(s)+X_{Lg}(s)}{3} + Z_M(s)} \tag{7}$$

where

1) $I_{CM}(s)$ is the total CM current;
2) $I_P(s)$ is CM current that circulates in the control side;
3) $X_{ps}(s)$, $X_{Lw}(s)$, $X_{Lg}(s)$, are the equivalent impedances expressed by (8), (9), and (10), respectively

$$X_{ps}(s) = \frac{1}{sC_{ps}} + sL_{ps} + R_{ps} \tag{8}$$

$$X_{Lw}(s) = sL_w \tag{9}$$

$$X_{Lg}(s) = sL_g. \tag{10}$$

The impedance network shown in Fig. 8, where the switches $S2$ and $S4$ are in static state, and $S1$ and $S3$ are in transition, represents the switching states II and IV. Similar to the model

TABLE III
ELEMENT VALUES OF THE EQUIVALENT IMPEDANCE NETWORK CIRCUITS

Element	Value	Description
C_{ps}	15 pF	Estimated primary-secondary parasitic capacitance for the gate drive power supplies used in this work [25].
Z_M	1 nF // 100 MΩ	Impedance used to concentrate and measure the noisy current in the control side.
L_w	20 nH	Estimated parasitic inductance of connections of the power supply on the primary side.
L_{ps}	40 nH	Estimated primary-to-secondary parasitic terminal inductance of the gate drive power supplies.
L_g	25 nH	Estimated parasitic inductance of connections of the power supply on the secondary side.
R_{ps}	100 mΩ	Estimated resistance of connections.

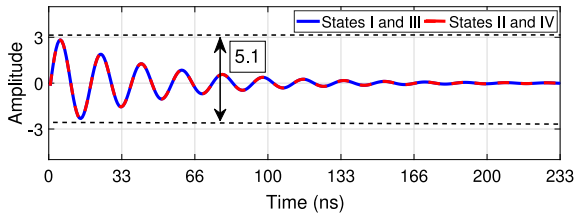

Fig. 9. TGD: Time-domain characteristics in step response in states I, II, III, and IV.

presented in Fig. 7, in Fig. 8 the impedances formed by $L_w - R_{ps} - C_{ps} - L_s$ of the gate drivers 2, 3, and 4 are connected in parallel. In other words, the TGD configuration is symmetrical. Therefore, considering the (2)–(6), the current relation $I_P(s)/I_{CM}(s)$, for the states II and IV is also expressed by (7).

Using (7) and the estimated values in Table III [10], the time-domain characteristics in step response of the CM current that circulates in the control side in the TGD configuration can be achieved as shown in Fig. 9. As can be seen, the same CM current is presented for the four switching states. However, it is important to note that, in practice, the parasitic elements are not perfectly identical. The same can be said about the SiC-MOSFET devices. In this case, different impedances and different dV/dt are present, and consequently the CM current is a function of the switching states.

B. New Cascaded Gate Driver Configuration

The impedance network circuit of the cascaded gate driver configuration is shown in Fig. 10. In this configuration, the pathway of perturbations is modified. As can be seen in Figs. 11 and 12, the CM currents are returned locally to the power parts (through the parasitic inductances L_{g1}, L_{g2}, L_{g3}, and L_{g4}) each time the dV/dt events are applied across the parasitic capacitances of the power supplies.

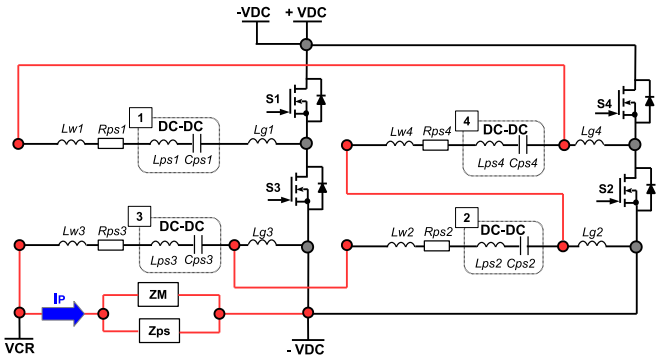

Fig. 10. CGD: Equivalent impedance network circuit.

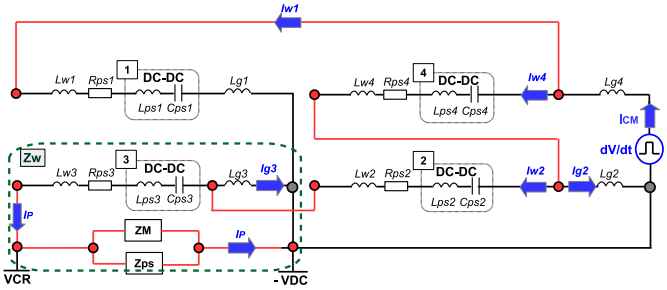

Fig. 11. CGD: Equivalent impedance network circuit in states I and III.

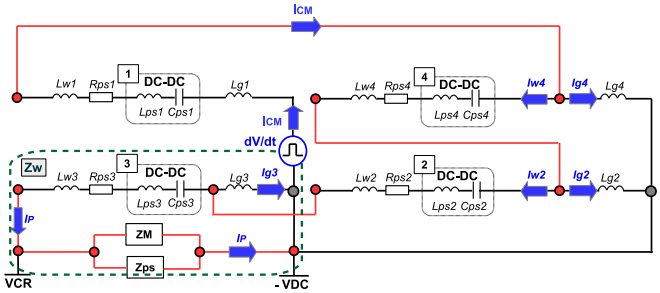

Fig. 12. CGD: Equivalent impedance network circuit in states II and IV.

To investigate the CM current behavior in the CGD configuration as a function of the switching states, Fig. 11 shows the equivalent circuit for the states I and III, where the switch $S1$ and $S3$ are in the static state, and $S2$ and $S4$ are in transition.

According to the conductive EMI noise current distribution in Fig. 11, the following current relations can be written:

$$I_{CM} = I_{w1} + I_{w4} \tag{11}$$

$$I_{w4} = I_{g2} + I_{w2} \tag{12}$$

$$I_{w2} = I_P + I_{g3} \tag{13}$$

$$\frac{I_{g2}}{I_{w2}} = \frac{Z_w + X_{ps} + X_{Lw}}{X_{Lg}} \tag{14}$$

$$\frac{I_{w1}}{I_{w4}} = \frac{\frac{(Z_w + X_{ps} + X_{Lw})X_{Lg}}{X_{Lg} + Z_w + X_{ps} + X_{Lw}} + X_{ps} + X_{Lw}}{X_{ps} + X_{Lw} + X_{Lg}} \tag{15}$$

$$\frac{I_{g3}}{I_P} = \frac{Z_M + X_{ps} + X_{Lw}}{X_{Lg}} \tag{16}$$

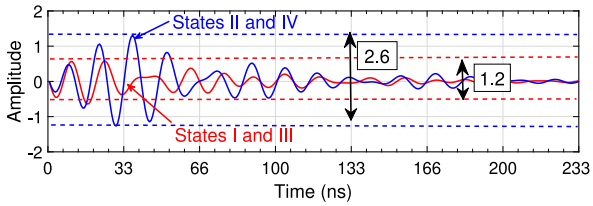

Fig. 13. CGD: Time-domain characteristics in step response, comparison between the states I–III and states II–IV.

where Z_w is expressed by

$$Z_w = \frac{Z_M + X_{ps} + X_{Lw}}{Z_M + X_{Lg} + X_{ps} + X_{Lw}}. \tag{17}$$

Using (14)–(16) in (11)–(13), the current I_P that circulates in the control part, during the switching states I and III, can be expressed in the Laplace domain by

$$\left(\frac{I_P(s)}{I_{CM}(s)}\right)_{I,III} = \frac{1}{(\frac{I_{g2}(s)}{I_{w2}(s)}+1)(\frac{I_{w1}(s)}{I_{w4}(s)}+1)(\frac{I_{g3}(s)}{I_P(s)}+1)}. \tag{18}$$

The behavior of the CM current that circulates in the control side during the switching states II and IV can be investigated according to the noise current distribution shown in Fig. 12. Therefore, the following current relations can be written:

$$I_{CM} = I_{g4} + I_{w4} \tag{19}$$

$$I_{w4} = I_{g2} + I_{w2} \tag{20}$$

$$I_{w2} = I_P + I_{g3} \tag{21}$$

$$\frac{I_{g2}}{I_{w2}} = \frac{Z_w + X_{ps} + X_{Lw}}{X_{Lg}} \tag{22}$$

$$\frac{I_{g4}}{I_{w4}} = \frac{\frac{(Z_w+X_{ps}+X_{Lw})X_{Lg}}{X_{Lg}+Z_w+X_{ps}+X_{Lw}} + X_{ps} + X_{Lw}}{X_{Lg}} \tag{23}$$

$$\frac{I_{g3}}{I_P} = \frac{Z_M + X_{ps} + X_{Lw}}{X_{Lg}}. \tag{24}$$

Using the (22)–(24) in (19)–(21), the portion CM current that circulates in the control part, during the switching states II and IV, can be expressed in the Laplace domain by

$$\left(\frac{I_P(s)}{I_{CM}(s)}\right)_{II,IV} = \frac{1}{(\frac{I_{g2}(s)}{I_{w2}(s)}+1)(\frac{I_{g4}(s)}{I_{w4}(s)}+1)(\frac{I_{g3}(s)}{I_P(s)}+1)}. \tag{25}$$

Using the (18) and (25), and the estimated values in Table III, the time-domain characteristics in step response of the CM current that circulates in the control side in the CGD configuration can be achieved, as shown in Fig. 13. Note that, unlike the TGD, the CGD configuration is not symmetrical, i.e., depending of the switching states, the ratio $I_P(s)/I_{CM}(s)$ presents different values since the (18) and (25) are not identical.

The comparison between TGD and CGD configurations is shown in Fig. 14. As can be seen, when the CGD is used, during the switching states I and III, the CM current in the control side can be reduced by 75% in relation to the TGD configuration.

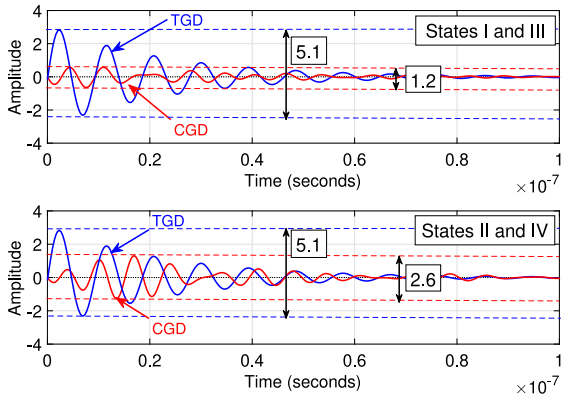

Fig. 14. Time domain simulation results, comparison between TGD and CGD.

TABLE IV
SUMMARIZED SIMULATION RESULTS SHOWN IN Fig. 14

Switching State	I	II	III	IV
$I_P(TGD)$	5.1 A	5.1 A	5.1 A	5.1 A
$I_P(CGD)$	1.2 A	2.6 A	1.2 A	2.6
I_P reduction	75%	49%	75%	49%

During the switching states II and IV the reduction is around 49%. These results are summarized in Table IV.

The analytical approach proposed in this section is based on the following considerations: 1) all gate drivers and all SiC-MOSFETs are considered identical; 2) the parasitic element considerations done in (2)–(6); 3) the dV/dts in the middle point of both power legs are equal, 4) a unit step represents the source of perturbation. However, in practice, the parasitic elements are not perfectly identical, e.g., the not perfectly symmetrical PCB layout. The same can be said about the SiC-MOSFET devices. In this case, different impedances and different dV/dts will be presented. Nevertheless, the theoretical analysis is useful to investigate the impact of gate drive power supply configurations on the CM conducted EMI and to confirm that the CGD configuration is an effective gate drive power supply technique to reduce the noise current in the control side. Therefore, as shown in the next section, the analytical approach is validated by experimental results.

IV. EXPERIMENTAL VALIDATIONS

To validate the theoretical analysis, a SiC-MOSFET-based full-bridge converter prototype with four Cree^{TM} C2M SiC-MOSFETs (C2M0160120) is developed as shown in Fig. 15. The dc–dc converter implemented for each gate driver is a Murata^{TM} MGJ6D242005SC with an isolation voltage and a parasitic capacitance of 5.7 kVDC and 15 pF, respectively. Optical fibers are used to achieve the signal isolation. A bus voltage of 800 V and gate-to-source voltages of -5 and 20 V are used in this experiment. A fixed duty cycle of 50%, and a phase shift of 45° are used for the phase shift modulation. The CM current between VCR and $-$VDC is measured by adding an artificial impedance Z_M (100 MΩ//1 nF). The experiments are performed using a

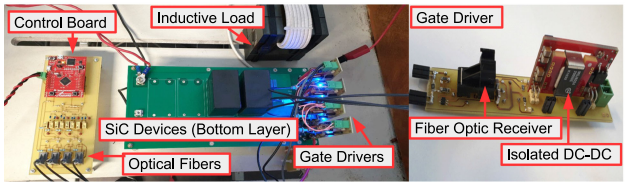

Fig. 15. PSFB switching cell and gate driver prototypes.

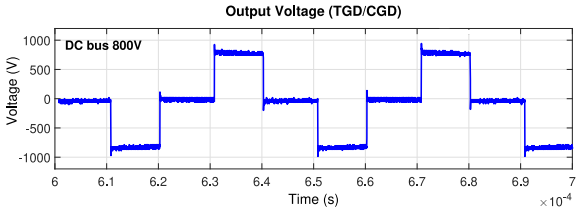

Fig. 16. Experimental results: PSFB output voltage.

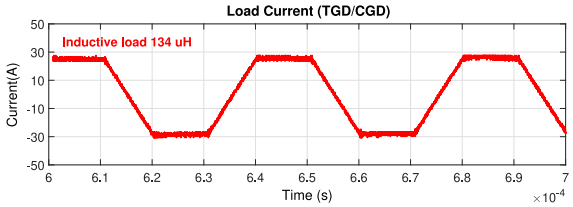

Fig. 17. Experimental results: PSFB load current.

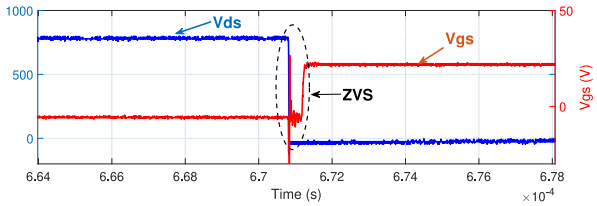

Fig. 18. Experimental results: PSFB ZVS behavior.

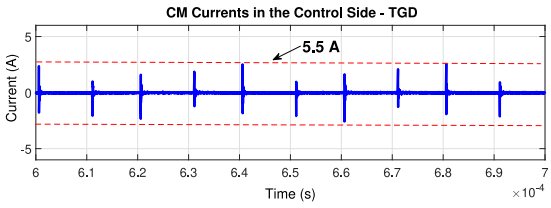

Fig. 19. Experimental results: TGD I_P CM currents.

train of pulses in order to switch the devices under specific load currents. The analyses are done in this case, i.e., in pulsed mode, because no heatsink is attached to the prototype.

A. Time-Domain Experimental Results

The experimental results depicted in Figs. 16–20 validate the proposed gate driver configuration. Note that, the main advantage of the phase-shift modulation, i.e., the ZVS is ensured for both gate drive power supply configurations. Although this

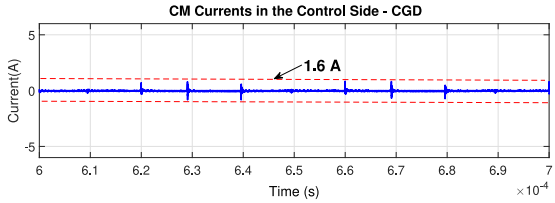

Fig. 20. Experimental results: CGD I_P CM currents.

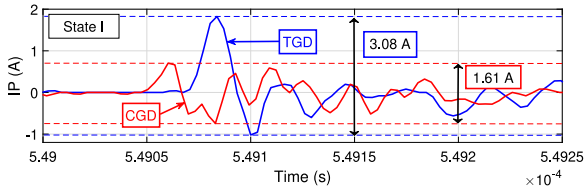

Fig. 21. Experimental results: CM currents in the control side during the state I.

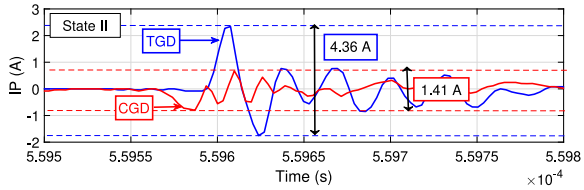

Fig. 22. Experimental results: CM currents in the control side during the state II.

is not the focus of this article, these results are presented in this section to show that the modification of gate drive power supply configuration has no impact on the output voltage, load current, V_{ds}, V_{gs}, or on the ZVS behavior.

However, focusing in the CM currents in the control side (Figs. 19 and 20), in the TGD configuration, a CM current of around 5.5 A (peak-to-peak) is presented. On the other hand, this noise current has been significantly reduced in the proposed gate drive power supply configuration, which presents a CM current of around 1.6 A (peak-to-peak), i.e., the proposed gate driver architecture has reduced the CM current by 71% in relation to the conventional gate driver configuration. Reducing the CM currents in the control side is critical for any converter. Isolated gate drivers are required to have good immunity toward CM currents to ensure data integrity. A CM current of 5.5 A circulating in the control side could drastically affect the data system. The problem can be aggravated in high-frequency applications, where the average CM current (in the control side) will be increased.

In Figs. 19 and 20 is presented the total peak-to-peak CM current in the control side. However, the CM current presents different values at different switching times. In Figs. 21–24, the CM current that circulates in the control side is analyzed for each switching event.

As shown in Fig. 21, even in the worst case (state I), the proposed gate driver configuration has been considerably reduced the CM current by 47% in relation to the traditional one, i.e., the current I_P decreases from 3.08 to 1.61 A. In the state II,

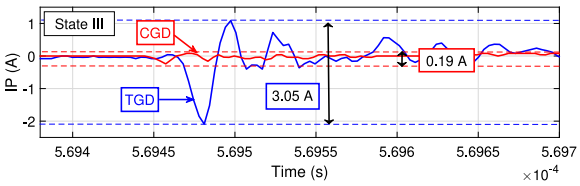

Fig. 23. Experimental results: CM currents in the control side during the state III.

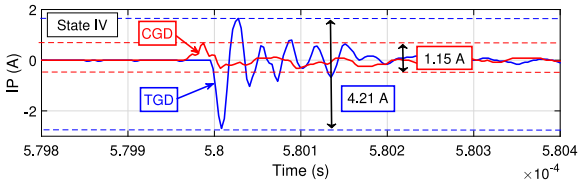

Fig. 24. Experimental results: CM currents in the control side during the state IV.

TABLE V
SUMMARIZED EXPERIMENTAL RESULTS SHOWN IN Figs. 21–24

Switching State	I	II	III	IV
$I_P(TGD)$	3.08 A	4.36 A	3.05 A	4.21 A
$I_P(CGD)$	1.61 A	1.41 A	0.19 A	1.15
I_P reduction	47%	68%	93%	73%

Fig. 17, the CM current has been reduced from 4.36 to 1.41 A, it represents a reduction of around 68%.

The best result, shown in Fig. 23, is achieved during the switching state III, where the CGD configuration has reduced the CM current by 93% in relation to the TGD configuration, the current I_P decreases from 3.05 to 0.19 A.

In the state IV, shown in Fig. 19, the CM current has been reduced from 4.21 to 1.15 A, which represents a reduction of around 73%. Table V summarizes the experimental results for the four switching states.

In TGD configuration, similar CM current values are presented in switching states I and III (3.08 and 3.05 A), and in states II and IV (4.36 and 4.21 A). On the other hand, the CGD configuration is not symmetrical. Therefore, different I_P current values are presented in switching states. In the CGD configuration, the largest difference is observed in the switching state III, where CM current I_P has a small value of around 0.19 A. Comparing these results with the simulation results shown in Table IV, some discrepancies can be seen in the values. It is due to the fact that in the theoretical analyses, it was considered a perfect symmetry of the power legs, i.e., it was supposed that the gate drivers (dc/dc, buffers, optical isolation, etc.) and their elements (parasitic capacitance, layout inductances, etc.) are perfectly identical. It was also supposed that the power devices are identical, and the middle points of the power legs have the same dV/dt. However, in experimental set-up, even under optimized layout, it can not be ensured. For example, the mismatch between the intrinsic parasitic capacitances of the devices can generate different switching speeds (dV/dt). Furthermore, as explained in [26], PSFB can have different dV/dt between leading and lagging legs. In the experiments performed

TABLE VI
PEAK-TO-PEAK CM CURRENTS FOR DIFFERENT LOAD CURRENTS

Load Current	8 A	18 A	28 A
$I_P(TGD)$	2.1 A	3.1 A	5.5 A
$I_P(CGD)$	1.2 A	1.4 A	1.6 A
I_P reduction	42%	55%	71%

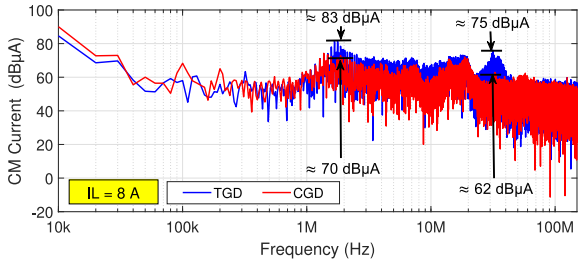

Fig. 25. Measured CM noises of the PSFB converter for TGD and CGD configurations (IL = 8 A).

in this article, the maximum dV/dt at the switching cell middle points for the leading and lagging legs are approximately 63 and 73 V/ns, respectively. This explains why different CM currents are observed as a function of the states for TGD and CGD configurations. Note that, even under ZVS operation, which can slow down the dV/dt during the turn-ON transitions, the C2M0160120 SiC-MOSFET devices switch very fast compared to traditional Si-IGBTs/Si-MOSFETs, which leads to serious CM noise.

The proposed gate drive power supply is also validated under different load currents as shown in Table VI. For a load current (IL) equal to 8 A, the CM current was reduced from 2.1 to 1.2 A (43 % of reduction). For IL = 18 A, the CM current was reduced from 3.1 to 1.4 A (55% of reduction). For IL = 28 A, the CM current was reduced from 5.5 to 1.6 A (71% of reduction). As can be seen in Table VI, the proposed gate drive power supply configuration is more suitable for applications with fast dV/dt since the switching speed of the devices are proportional to the load current, and in this case, more conducted EMI noise is generated.

B. Frequency-Domain Experimental Results

To investigate the conducted CM current reduction in the frequency domain, spectral analyses are done. The data of the CM currents were obtained by the DSOX3024 T Keysight Oscilloscope in the experiments and the spectrum was obtained with MATLAB software after the data were processed. The conducted EMI spectra in the range of 10 to 100 MHz is shown in Figs. 25–27 for three different load currents.

In Fig. 25 is shown the EMI spectra for a load current equal to 8 A. As can be seen, the proposed CGD configuration reduces the conducted CM noise, practically, in all 1.5–40 MHz range. The most notable improvements are ≈13 dB in 1.6–1.8 MHz range, ≈10 dB in 8–10 MHz range, and ≈13 dB at 30 MHz.

In Fig. 26, the EMI spectra for a load current equal to 18 A is shown . The proposed CGD configuration reduces the conducted

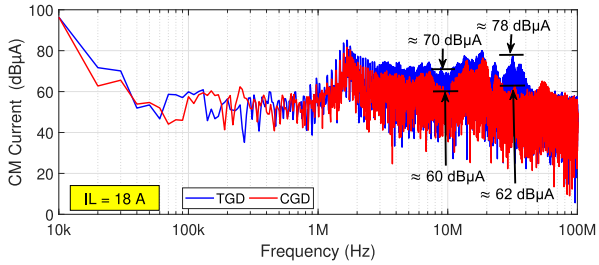

Fig. 26. Measured CM noises of the PSFB converter for TGD and CGD configurations (IL = 18 A).

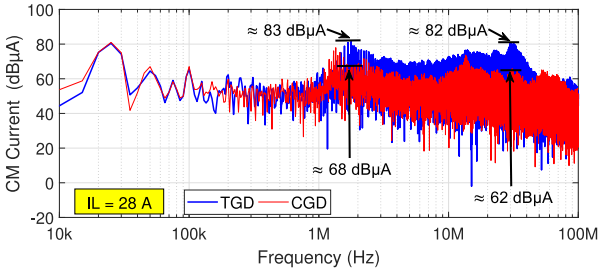

Fig. 27. Measured CM noises of the PSFB converter for TGD and CGD configurations (IL = 28 A).

CM noise, practically, in all 1.5–40 MHz range. The most notable improvements are ≈10 dB in 8–10 MHz range, and ≈16 dB at 30 MHz.

In Fig. 27, the EMI spectra for a load current equal to 28 A is shown . In the same way, the proposed CGD configuration reduces the conducted CM noise, practically, in all 1.5–40 MHz range. An improvement of ≈15 dB is achieved between 1.6 and 2 MHz. An improvement of ≈10 dB is achieved, practically, in all 2–10 MHz range. The most notable reduction is ≈20 dB at 30 MHz.

In the three cases, from 30 to 40 MHz, the amount of noise reduction decreases as a function of the frequency. Furthermore, for frequencies <1.5 and >40 MHz, the noise reduction is not so effective. In the 0–1.5 MHz range, both gate driver configurations have similar performances. Maybe this is due to the impedance provided by each configuration, which is not so different from each other in the 0–1.5 MHz range. Therefore, the CM currents have similar behaviors in both gate drive power supply configurations. From 1.5 MHz, the difference between the gate driver configuration impedances starts to be significant. The TGD impedance starts to be smaller than the impedance provided by the CGD configurations. In the 30–40 MHz range, the TGD impedance reaches its minimum absolute value, and at this point, the CGD impedance is much greater than the TGD one. From 40 MHz, both gate driver configurations have similar performances. This is due to the impedance of the gate drive power supply, which drastically decreases in both gate driver configurations [9], allowing that the CM currents circulate in the control side.

It is clear that the control system could be damaged by a large amount of the noise current that may flow through the control parts if the gate drive power supplies are not taken into account in the system implantation. Efforts must be engaged not only toward the design and implementation of gate drivers but also toward the gate drive power supplies. The analytical analysis and experimental results validate the proposition of this article. The CGD configuration is an effective technique to reduce the current noise in the control part and to increase the reliability of the control system.

However, for optimal design the power rating of the dc/dc converters has to be taken into account. The advantages offered by the cascaded gate drive supply configuration must be mitigated by the increased complexity and the additional power consumption due to the cascaded power supplies. The cascaded gate drive power supplies must be designed carefully since their power ratings are changing from one to another, specially for the gate drive power supply 3, which must be designed to supply all other drive circuits. Optimal design in terms of power rating, volume, efficiency, and parasitic currents has been addressed in [27].

V. Conclusion

This article presents a new gate driver configuration to decrease the CM currents in full-bridge topologies under phase-shift modulation. In a first step, basics and concepts are explained: The new gate driver configuration modifies the pathways of the parasitic currents generated by high dV/dt in the middle points of the inverter legs. To further investigate the concept of the new gate driver configuration applied to PSFB converters, an analytical analysis is proposed to predict the behavior of the CM current in the control side. This first step validates the interest of the proposed cascaded configuration according to the peak-to-peak value of the CM current. Thereafter, experimental results are provided in the same switching conditions: Bus voltage of 800 V and a load current of 28 A. The experimental results are in accordance with the analytical model used to predict the behavior of the CM current in the control side. The performance of the proposed gate driver configurations under different switching frequencies remains as an expectation of future works since some EMI characteristics are dependent on the switching frequencies f_{sw} such as the magnitude of first peak of the spectrum that is located on the f_{sw}, which should be more or less attenuated depending on the EMI standard. In the MHz range, the noise will be larger with the increased switching frequency. Furthermore, the effectiveness of the proposed gate driver configuration should be verified with total amount of CM currents (power and control stages).

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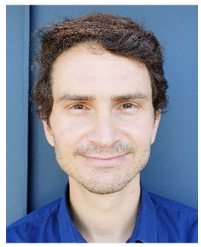

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