A Hybrid, Fully-Integrated, Dual-Output DC–DC Converter for Portable Electronics

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***Abstract*—This article describes a hybrid, dual-output dc–dc converter suitable for low-power application. It consists of inductor based subconverter providing one output, which is cascaded with a switched-capacitor based subconverter providing the second output. The converter uses bondwire inductance, and on-chip metal-oxide-semiconductor (MOS) capacitance to realize the passive components making it a fully-integrated solution. For target specification of output voltage levels, and input voltage range, the stepped-up output is generated by the inductor-based, high-frequency, voltage-mode boost converter. And, a switched capacitor based, frequency-controlled step-down converter generates the second output. The hybrid converter uses a π-filter to attenuate the switching ripple to an acceptable value. The filter also helps to isolate the internal ground from the noisy power ground connected to boost converter power stage. By the virtue of time-interleaved switching pattern, switching noise induced in its supply rails by the S-C stage is significantly less, which makes the S-C stage an equivalent quiescent load to the boost stage. A prototype of the proposed hybrid converter has been designed, and implemented in 0.18-μm CMOS process. It consumes 0.82 mm^2 area, and provides -1.45 V, and 3.2 V from an input voltage varying from 1.2 V to 2.7 V at an efficiency $> 52\%$ (maximum 77%) for all load conditions.**

***Index Terms*—Cross regulation, dc–dc, inductor, ripple, switched-capacitor.**

I. Introduction

THE unprecedented development of semiconductor technology in last two decades has seen a proliferation of portable solutions in the consumer and wireless electronics markets. Continuous shrink of device dimensions into the subhundred nanometer regimes has enabled integration of various subsystems on a single chip resulting in compact system-on-chips (SoC). However, this closely packed mixed-signal integration on a single silicon real estate ensues several design requirements and associated challenges. One of these challenges is the requirement of multiple, on-chip power supply domains [1].

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These portable devices are predominantly powered by rechargeable batteries. Output voltage of a fully-charged battery decreases slowly with time. This imposes specific requirements from the dc–dc converters for portable, battery-operated systems such as a good line regulation against an input voltage having wide range of variation. For example, a typical Ni-MH battery voltage varies from 1.5 V to 1.0 V and a typical Li-ion battery exhibits maximum voltage of 4.1 V and minimum voltage of 3.0 V [2]. Similarly, a Li-Titanate or LTO battery (a modified version of Li-ion battery) has voltage variation, typically from 2.7 V to 1.5 V [2]. So, the converter must have the capability to regulate its output voltage against a widely varying input supply voltage. On the other hand, in a mixed-mode and mixed-voltage SoC, more than one on-chip supply voltages are essential. Power efficiency of the converter should also be as high as possible to support extended run-time of the system. Another important design consideration is the converter's geometry, which is primarily dominated by the sizes of the passive components. For a compact design solution, it is preferable to integrate the passive components so that it is feasible to implement the complete converter unit along with its application circuits within the same die. Moreover, integrating the converter with the application circuits eliminates the problem of load transient spikes caused by inductance from package and global power grid [3]. In summary, a compact, on-chip dc–dc converter providing multiple supply voltages from a widely varying input voltage is essential for a low-power, battery-operated, portable device.

Generation of multiple regulated supply voltage levels from a single input supply may be accomplished by dedicated point-of-load regulators for each of the loads. However, it proportionately increases the number of required off-chip components resulting in more printed circuit board (PCB) area. An area-saving alternative could be the use of a single inductor that can store and deliver energy (on a time-sharing basis) for multiple loads [4], [5]. It is more popularly referred to as single inductor multiple output (SIMO) converter. In the SIMO converters, while the number of inductor reduces to one and the number of power switches gets reduced, the number of filter capacitor, however, remains the same, because each of the outputs needs dedicated capacitor. Even if the single inductor is kept off the chip, it still needs big (enough to filter the switching ripple) capacitors to be integrated [6], this is a hindrance to design a fully-integrated SIMO converter. So, most of the integrated SIMO converters found in literature used off-chip inductor and capacitors and then integrated the rest of the circuit [7], [8].

In recent times, switched-capacitor (also known as charge-pump) based topologies have emerged as popular alternative to achieve fully-integrated dc–dc converter solution particularly for low-power applications [9]–[15]. The reason is feasibility of complete integration of S-C-based converters with the load circuitry on the same die using on-chip MOS capacitor exhibiting very good quality factor and capacitance density. It enables the designers to avoid external inductor, which eliminates the detrimental effect caused by the package parasitic especially, ground bounce produced by large current peak. Moreover, it is easier to implement time-interleaved versions [16]–[19] of S-C-based topologies on the chip. It may be noted that the cost overhead due to increase in capacitor and switch count in the time-interleaved topologies is negligible for on-chip components. Time-interleaving technique essentially reduces the required value of output capacitance used to filter the switching ripple. Some recent works [20] have even developed functional prototypes of output capacitor-less S-C-based converter using time-interleaving technique. However, there are few practical limitations of the S-C-based converters. An S-C-based converter provides best power efficiency only for a fixed conversion ratio and deviating from the optimal conversion ratio leads to high loss of power efficiency. Also, regulation of S-C-based converter is different than that of an inductor-based converter. Typically, frequency of the switching clock is varied to modulate the equivalent output impedance of the converter to achieve the regulation [18], [19]. However, converter output impedance is practically limited by "ON" resistance of power switches resulting in loss of regulation beyond a limit. So, to regulate the converter for a large line/load variation, a series linear regulator [21], [22] is used at the cost of power efficiency.

Therefore, the S-C-based converter, although edges ahead in terms of on-chip integration. On the other hand, an inductor-based converter provides power-efficient regulation against a widely varying line voltage and load current. So, hybridization of the two classes of converter can help to blend their merits and overcome the respective shortcomings to good extent. In this article, we demonstrate an in-package-integrated, inductor, and switched-capacitor based hybrid dc–dc converter, which can provide two regulated output voltages from a widely varying, single input supply. It uses on-chip capacitance and bondwire inductance resulting a compact power management unit. The contribution of this article is a design solution to the integration issues of a fully-integrated, hybrid dc–dc converter architecture. This article also analyses the cross-regulation effect between the two converters.

The rest of this article is organized as follows. The state-of-the-art hybrid architectures are discussed in Section II followed by the system requirement and design consideration of our prototype being explained in Section III. In Section IV, design details of the proposed hybrid converter are presented. Experimental results and performance comparison are discussed in Section V. Finally, the conclusion is drawn in Section VI.

II. State-of-the-Art Hybrid Architectures

Most of the existing hybrid converters [23]–[25] consist of switched-capacitor-based front-end power stage (may or may not be regulated) followed by regulated, inductor-based conversion stage, as shown in Fig. 1(a). Benefits of these architectures are mainly threefold. First, the S-C stage steps the input voltage down by a large fraction. Thus, the inductor-based stage faces a scaled-down range of input voltage and, hence, can work without running into the problem of duty-cycle saturation. Second, voltage stress on the power switches of the inductor-based stage reduces making it possible to use lower-voltage devices, which take lesser chip area. Third, a higher pulse width modulation (PWM) frequency can be used for the inductor-based stage because of the low-voltage switching devices. This makes it possible to reduce the required inductance value and, hence, size of the off-chip inductor. It may be noted that all these hybrid converters are designed using discrete components to provide high power output at very high efficiency. However, a hybrid solution for integrated power management unit is a nascent design concept till date. Kudva *et al.* [26] presented a fully-integrated hybrid converter to enhance power efficiency of an inductive buck converter for high conversion ratio by mode switching to a parallel capacitive step-down unit. In this article, we demonstrate an integrated hybrid architecture targeting low-power applications.

III. System Requirement and Design Considerations

Primary design consideration of the hybrid converter presented in this article is to integrate all the passive components on chip or inside the IC package. The hybrid converter must also satisfy the system requirement of generating two well-regulated, fixed output voltages from a variable input voltage. This mandates that the S-C converter stage also provides a regulated output. However, it suffers from poor line regulation for a wide input range and exhibits good power efficiency only around the output voltage level defined by its fixed conversion ratio. So, it is inevitable that the inductor-based converter is placed at the front-end of the system so that it can provide a regulated output voltage level from an unregulated supply. Then, the subsequent S-C stage can process the output of the inductor-based stage to provide another regulated output voltage level with maximum possible efficiency. An architecture with the inductor-based converter as front-end stage is illustrated in Fig. 1(b).

The next step is to consider circuit level implementation/integration issues, which influence the design of each of the converter stages. The first one of these issues is ground bounce. As shown in Fig. 1(b), the internal (on-chip) ground is separated from the external, clean ground by package bondwire inductance, L_{par}. Pulsed current flowing through the power switch connected to the power ground produces a ringing (due to significant parasitic inductance L_{par}) in the power ground. This ringing is referred to as the ground bounce and amplitude (ΔV_{bounce}) of the ringing can be quantified by

$$\Delta V_{\text{bounce}} = L_{\text{par}} \frac{di}{dt} \tag{1}$$

where *di/dt* represents the rate of change of current through L_{par}. Now, as illustrated in Fig. 1(c), using a small power inductance, L_1 induces a large inductor current peak resulting in a very high "*di/dt*", which essentially creates a large ground bounce

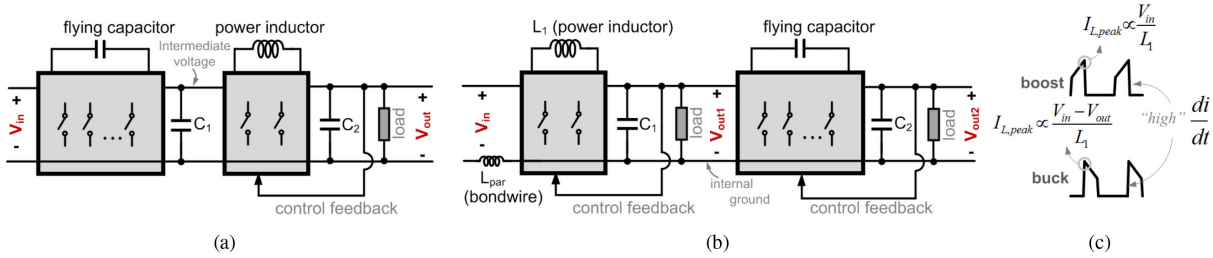


Fig. 1. (a) Hybrid converter having S-C converter as the first stage and single output voltage. (b) Hybrid converter having inductor-based converter as the first stage and two output voltages. (c) Pulsed current waveform in buck and boost converters.

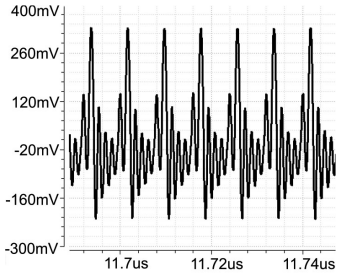


Fig. 2. Simulated ground bounce.

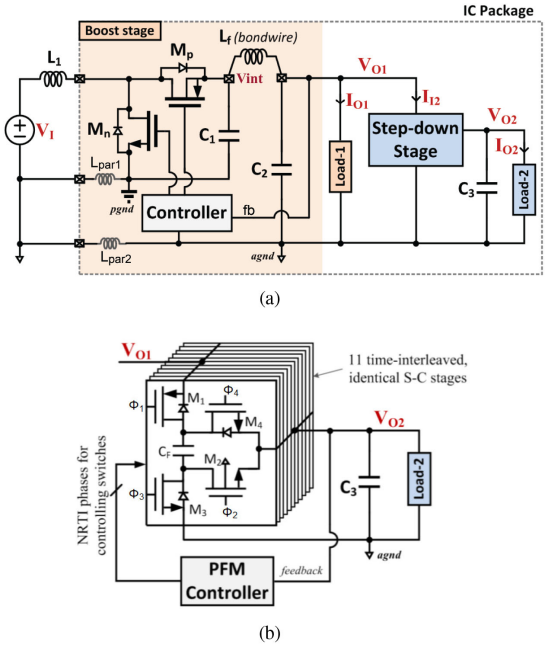


Fig. 3. (a) Proposed hybrid, dual-output converter. (b) S-C-based step-down stage.

amplitude. Moreover, a smaller inductance inevitably imposes that a higher switching frequency be used and hence the switching period becomes smaller compared to the time required for the power ground ringing to decay. A typical simulation result of the bounce in the power ground of a boost converter with $L_1 = 20$ nH and $L_{\text{par}} = 1$ nH is shown in Fig. 2. The simulated peak-to-peak amplitude of the noise in the power ground is close to 0.55 V, which is quite high for an analog block working with a 1.5 V supply. The situation may become very critical design bottleneck for the cascaded architecture shown in Fig. 1(b) as it is not possible to use a separate and clean ground line (instead of the common power ground) for the S-C stage. So, it becomes an inevitable design requirement to maintain the ground bounce within tolerable limit either by using high L_1 (to reduce *di/dt*) or by decreasing L_{par}.

The next implementation issue is the switching noise injected to the output of the first stage [see Fig. 1(b)] by the cascaded S-C-based stage. In general, input current of the S-C-based converter contains high spikes due to periodic charging of flying capacitor/s. These high current spikes tend to destabilize the first-stage output unless a very high filter-capacitor (C_1) is used to suppress the switching noise as mentioned in [24]. This requirement imposes a limitation to integrate the intermediate capacitor unless suitable measure is taken to reduce input noise of the S-C stage.

IV. Proposed On-Chip Hybrid Converter

The proposed hybrid converter is presented in Fig. 3(a). It is a cascade connection of an inductor-based boost stage and an S-C-based step-down stage.

It may be noted that the boost converter supplies the load current, I_{O1} to the boost port as well as supports the input current, I_{I1} of the step-down converter. So, its load regulation is designed by taking both I_{O2} and I_{I1} into account. The boost stage also maintains a steady output voltage level, which is higher than the input (V_I). The step-down converter, on the other hand, generates the second voltage level, which is half of the boost output. In this architecture, the input of the step-down converter is regulated by the boost stage and, hence, is not affected by the variation of the primary input supply line. So, the step-down stage always works with a fixed input voltage, which helps to design it optimally for delivering power with high efficiency. Design specification of the hybrid converter is shown in Table I. Input voltage is from 1.5 to 2.7 V. Target output of the boost converter is 3.3 V while it supplies a quiescent load having relatively less fluctuations. On the other hand, target output of the step-down converter is 1.5 V. It may be noted that the boost converter, along with its specified maximum load current of 50 mA, must deliver the input current drawn by the step-down converter. The input current drawn by the step-down converter is nearly half of its load current. So, effectively, the boost converter needs to support maximum load of 62.5 mA.

TABLE I
HYBRID CONVERTER SPECIFICATION

Parameter	Value
Input voltage (V_I)	1.5-2.7 V
V_{O1}	3.3 V $\pm$ 5%
I_{O1}	50 mA
V_{O2}	1.5 V $\pm$ 5%
I_{O2}	25 mA
Ripple	$\leq$ 1%

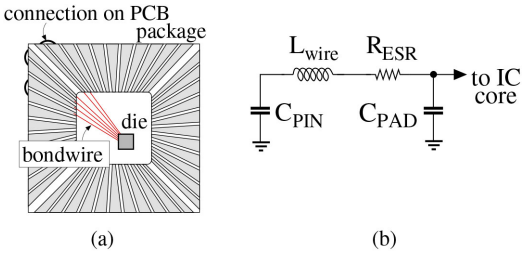


Fig. 4. (a) Bondwire connection. (b) Bondwire model.

TABLE II
BONDWIRE PARAMETERS

Parameter	Value
Material	Gold (Au)
Diameter	1.2 mil (30.48 μm)
Self-inductance	0.95 nH/mm
K_{11}^{*}	0.56
Series resistance (ESR)	35 mΩ/mm

*Coupling coefficient between two adjacent bondwires.

A. Boost Stage

The boost stage of the hybrid converter is a conventional boost converter followed by a π-filter formed by C_1, L_f, and C_2 [27]. The filter capacitors C_1 and C_2 have been implemented on chip using high density MOS capacitance. The filter inductor, L_f has been realized using bondwires. Design value of the primary inductor, L_1 (although it is connected as an external component in the prototype) has been chosen in such a way that it can also be implemented by standard package bondwires. The prototype has been packaged in a 44 pin CLCC package. As shown in Fig. 4(a), six bondwires are connected in series to realize L_f. The zig–zag arrangement of the wires and alternate directions of current through adjacent bondwires give rise to a magnetic coupling effect. It effectively increases the overall inductance.

For each of the bondwires, the equivalent electrical model shown in Fig. 4(b) has been used for simulation. The values of L_{wire} and R_{ESR} have been calculated based on the data provided by the manufacturer, which are enlisted in Table II. Total nominal inductance of 30 nH has been used in the simulation. The reader is encouraged to study [27] for a detailed design description of the boost stage.

The π-filter helps to attenuate the output ripple significantly, even using on-chip capacitance much smaller compared to that used by the existing integrated converters. The amount of ripple suppression provided by the π-filter in the prototype design is shown in Fig. 5 by the simulated waveforms of voltages Vint and V_{O1}. In this design, the switching frequency ($\approx$120 MHz) is

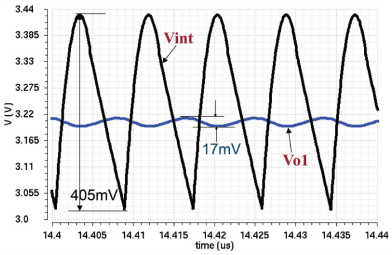


Fig. 5. Simulated ripple suppression by the π-filter.

chosen to be significantly higher than the two complex-conjugate pole pairs arising due to the π-filter structure. As a result, the filter provides a good attenuation at the switching frequency. The obtained attenuation is more than that provided by a traditional filter comprising of one output capacitor (equal to the total capacitance used in the π-filter) manifesting one complex-conjugate pole pair. In other words, to attain same amount of suppression, the value of one output capacitance in traditional filter would be much higher than the sum of two capacitance used in the π-filter. It is important to note that apart from ripple-suppression, the π-filter also isolates the analog ground (agnd) from the noisy power ground (pgnd), which is discussed in Section IV-D.

The boost converter is regulated by a voltage-mode PWM scheme. The duty-to-output transfer function is shown in (2). Detailed derivation of the transfer function can be found in [27]

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{a_2 s + a_1}{b_4 s^4 + b_3 s^4 + b_2 s^2 + b_1 s + 1}. \quad (2)$$

The coefficients of the abovementioned transfer function are

$$a_2 = \frac{V_I L_1 \lambda^2}{D'^4 R_L}$$

$$a_1 = \frac{V_I \lambda}{D'^2}\left[1 + \frac{D'^2 r_{Lf} - r_{L1}}{D'^2 R_L} + \frac{D'\left(2r_{\text{ON2}} - r_{\text{ON1}}\right) + D r_{\text{ON1}}}{D'}\right]$$

$$b_4 = \frac{L_1 L_f C_1 C_2 \lambda}{D'^2}, b_3 = b_4\left[\frac{1}{R_L C_2} + \frac{r_{\text{par}}}{L_1} + \frac{r_{Lf}}{L_f}\right]$$

$$b_2 = b_4\left[\frac{1}{L_f C_1} + \frac{1}{L_f C_2} + \frac{D'^2}{L_1 C_1} + \frac{r_{\text{par}} r_{Lf}}{L_1 L_f} + \frac{r_{\text{par}}}{R_L L_1 C_2} + \frac{r_{Lf}}{R_L L_f C_2}\right]$$

$$b_1 = b_4\left[\frac{\left(L_1 + D'^2 L_f\right)}{R_L L_1 L_f C_1 C_2} + \frac{r_{\text{par}}\left(C_1 + C_2\right)}{L_1 L_f C_1 C_2} + \frac{r_{\text{par}} r_{Lf}}{R_L L_f C_2} + \frac{D'^2 r_{Lf}}{L_1 L_f C_1}\right]$$

where $\lambda = \frac{D'^2 R_L}{r_{\text{par}} + D'^2\left(r_{Lf} + R_L\right)}$, $r_{\text{par}} = \left(D r_{\text{ON1}} + D' r_{\text{ON2}} + r_{L1}\right)$, D is the duty ratio, R_L is load resistance, r_{Lf} and r_{L1} are DCRs of L_f and L_1, respectively, and r_{ON1} and r_{ON2} are on-resistance of the NMOS and PMOS switches, respectively. It may be noted that the power-stage of the converter consists of two resonating poles ($\omega_1 = D'/\sqrt{L_1(C_1+C_2)}$ and $\omega_2 = \sqrt{C_1+C_2}/\sqrt{L_f C_1 C_2}$) [27] as opposed to one resonating pole in the conventional boost converter. Traditionally, type-III technique is used to compensate

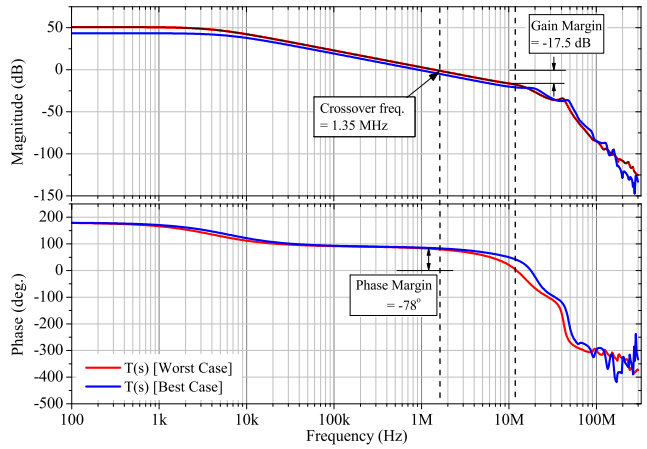


Fig. 6. Frequency response of the compensated control loop of the boost stage; worst-case: $V_I = 1.8$ V, load current = 60 mA, best-case: $V_I = 2.7$ V, and load current = 10 mA.

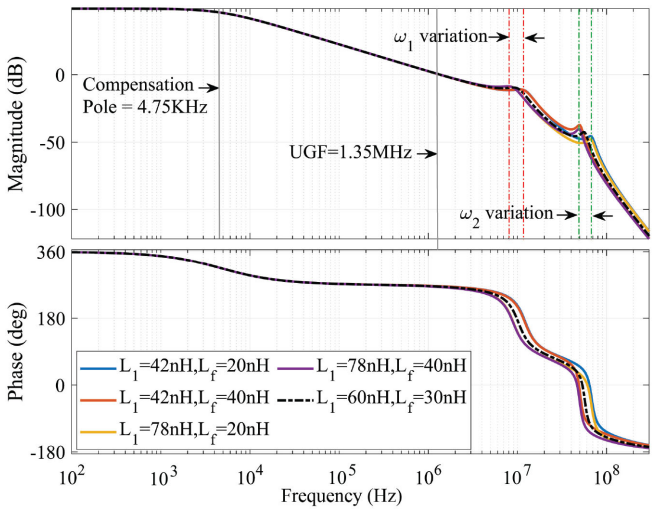


Fig. 7. MATLAB simulated bode plot with ±30% L variation at $I_{O1} = 60$ mA.

the effect of the single resonant frequency appearing before the gain-crossover frequency (f_{gc}) in a conventional boost converter topology. But, in case of the proposed converter, if f_{gc} is placed beyond ω_1 and ω_2, then compensating their combined effects is difficult. In this prototype, we have used a simpler dominant-pole compensation technique, which limits the loop-bandwidth (f_{gc}) though. Frequency response of the compensated loop-gain (obtained by periodic steady-state analysis of the actual design) is shown in Fig. 6.

B. Effect of Component Variation

It was anticipated that the actual value of inductance may significantly vary from what is used as in typical in simulation. Hence, sufficient design margin should preferably be kept by placing f_{gc} approximately at one tenth of the typical value of ω_1 so that, even if L_1 increases significantly, ω_1 remains far from f_{gc}. On the other hand, if L_1 decreases then the stability of the feedback loop does not degrade, however, the inductor current ripple increases yielding higher rms power loss. In addition, the output voltage ripple is affected by the variation of the filter inductance. If L_f decreases, the output ripple increases. In the present design, assuming ±30% variation over the nominal design values of both L_1 and L_f, a frequency domain analysis of compensated loop gain $T(s)$ [27] at the maximum load (worst-affected case) has been carried out in MATLAB. The corresponding bode plot of $T(s)$ shown in Fig. 7. As expected, it is evident from the figure that ω_1 remains satisfactorily higher than f_{gc} even with $L_1 = 78$ nH and, hence, the loop stability is hardly affected. The fact is also corroborated by the simulated transient response of the transistor-level design for a load step of 0 to 60 mA and vice versa, as shown in Fig. 8. It has been observed from simulation that the power-stage efficiency (excluding the control circuit loss) varies from 74% to 87% for ±30% variation of L_1 and L_f with respect to their nominal values. And, the corresponding output voltage ripple varies from 9 mV to 37 mV.

Similar to the bondwire inductance, C_1 and C_2 may also change due to process variation. If the capacitance decreases,

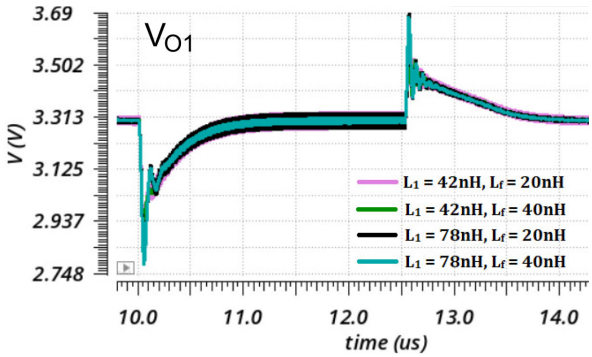


Fig. 8. 0→60 mA load-step response with ±30% L variation.

there is no impact on the stability but output ripple increases. On the other hand, if capacitance increases, both ω_1 and ω_2 move closer towards f_{gc} but the said design margin is sufficient able to tolerate that variations. In the prototype design, 30% increase in L_1, C_1, and C_2 decreases ω_1 from 10.3 MHz to 7.9 MHz, which is a 23.4% reduction over the nominal value and it barely affects the loop stability.

C. Step-Down Stage

The step-down stage, as illustrated in Fig. 3(b), is realized by a switched-capacitor (SC) converter architecture developed using time-interleaved, series-parallel topological units. The four switches of each unit are realized using low-V_T, 1.8-V transistors available in the process to have lower $R_{ON} \times C_G$ compared to that of high-V_T, 3.3 V transistors. Flying capacitance of 60 pF in each of the units are implemented by normal 1.8 V device as it provides maximum on-chip gate-capacitance density resulting in maximum possible power density of the converter stage.

Switching pattern of the eleven converter units are governed by the nonoverlapped rotational time interleaved (NRTI) switching scheme [18], [19]. It is a regularized switching pattern, which helps to improve both ripple performance and power

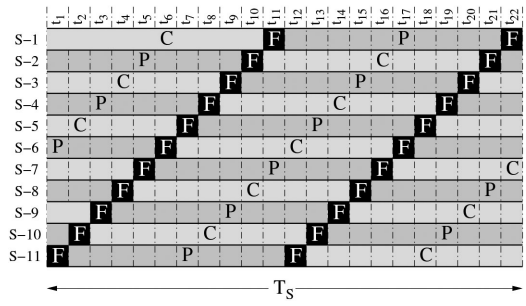


Fig. 9. NRTI switching pattern of the SC converter units.

efficiency of the SC converter. For an N-stage NRTI, the duty ratio of each clock phase is equal to $[(N-1)/2N] \times 100\%$ and the nonoverlapping duration between the charging and pumping phases is equal to $1/2NF_S$. In N converter units, there are N number of identical flying capacitors each one of which has the capacitance of C_F/N where C_F is the total flying capacitance. At any given time instance, $(N-1)$ capacitors are active, half of which is in charging (C) state, half is in discharging or pumping (P) state, and the remaining capacitor is in floating (F) state. So, the flying capacitance utilization factor is $N-1/N$. Hence, the number of stages should be more to increase the utilization factor. Fig. 9 shows states of the flying capacitors in eleven units (S-1 to S-11) in one cyclic period (T_S).

Internal schematic of the pulse frequency modulating (PFM) controller is shown in detail in Fig. 10(a). It comprises of a clock signal generation block and an error amplifier. The clock signal generator consists of two stacked voltage-controlled oscillator (VCO) [28] followed by two stacked NRTI signal generators and then the gate drivers. It may be noted that the stacked VCOs, stacked signal generators, and stacked gate-drivers used to generate synchronous switch signals for the upper and the lower voltage domains, namely, $V_{O1} \rightarrow V_{O1}/2$ and $V_{O1}/2 \rightarrow 0$. The stacked architecture works on the principle of current sharing between the stacked stages. Symmetrical switching activities in the stacked blocks powered in the two voltage domains set the intermediate supply line close to $V_{O1}/2$ without any regulation. The stacked VCO generates 22 clock phases (Φ_U<1:22> and Φ_L<1:22>) in each of the voltage domains and corresponding phases in two voltage domains are synchronized with each other. Frequency of the clock phases are modulated by the input control voltage (V_{ctrl}) of the VCO bias generator, which produces the bias voltages (V_{BU} and V_{BL}) for VCO-1 and VCO-2, respectively. Further details of this block are not discussed in this article and readers are encouraged to refer to [28] for more details about this block. The VCO phases are logically combined to derive the required NRTI phases (Φ_C<1:11> and Φ_P<1:11>) for the eleven-unit converters. Switches M_1 and M_4 [see Fig. 3(b)] are driven by NRTI gate signals (Φ_1<1:11> and Φ_4<1:11>) from the upper voltage domain, whereas, switch M_3 is driven by gate signal (Φ_3<1:11>) from the lower voltage domain. Corresponding NRTI gate signals from the two voltage domains are combined to create the NRTI signal (Φ_2<1:11>) having full rail-to-rail ($0 \Rightarrow V_{O1}$) voltage swing for the switch M_2. This strategy ensures that gate-oxide of none of the switches is overstressed.

Load regulation of the converter is achieved through controlling the VCO frequency by the output voltage of a compensator. The compensator is an error-amplifier having dominant pole at its output. The loop gain transfer function is given by the following equation:

$$T(s) = -K_{\text{VCO}} \times A_V(s) \times \frac{R_{\text{out}}(s)}{\hat{f}(s)} \tag{3}$$

where K_{VCO} is the voltage-to-frequency conversion gain of the VCO, $A_V(s)$ is the compensator transfer function, and $\frac{R_{\text{out}}(s)}{\hat{f}(s)}$ is the frequency-to-converter output resistance transfer function. The loop-stability has been analyzed by simulating a macromodel. The macromodel is explained in Section IV-E. Frequency response of the compensated loop-gain is shown in Fig. 11.

D. Merits of the Proposed Architecture

1) Isolation of Analog and Power Grounds: Ground rail of the S-C-based step-down stage is less contaminated by its switching noise because of the NRTI-defined time-interleaved switching of multiple smaller power-stage units. Hence, it can be regarded as an analog (quiet) ground and shared by all other analog subcircuits of the hybrid converter. However, it is necessary that this analog ground is same as the ground of the output of the preceding boost stage. Advantage of the proposed hybrid converter, as shown in Fig. 3(a), is that the topological isolation provided by the π-filter section between the power ground (which is noisy) and output ground helps to connect the later to the chip analog ground. As shown in Fig. 12, peak-to-peak amplitude of the simulated switching noise [for $L_1 = 20$ nH, $L_{\text{par1}} = 1$ nH, and $L_{\text{par2}} = 5$ nH] in the analog and power grounds are 96 mV p-p and 0.55 V, respectively.

2) Minimized Coupling of Switching Noise: The S-C step-down stage appears as an additional load to the boost stage. In general, the input current profile of a S-C converter contains high in-rush spikes, which may disrupt the load regulation of the boost converter, unless sufficiently large output filter capacitance (C_2) is used. However, by the virtue of NRTI switching scheme, in-rush current spike contained in the transient profile of I_{I2} is quite low. So, the S-C stage appears as an equivalent quiescent load to the boost stage. As shown in Fig. 13, simulated switching ripple of I_{I2} is 10 mA, which ensures that a small on-chip filter capacitance (0.54 nF) at the boost output stage is sufficient to satisfactorily filter out the in-rush current noise of the S-C stage.

E. Cross Regulations

Cross-regulation characteristic of the proposed hybrid converter has been analyzed using a macromodel illustrated in Fig. 14, which consists of two parts—macromodel of the boost stage and that of the step-down stage. The former consists of ideal switches and ideal error-amplifier, ideal comparator model, and passive components. Values of the passive components are as follows: $C_1 = C_2 = 0.54$ nF, $L_1 = 20$ nH, $L_f = 30$ nH, PWM

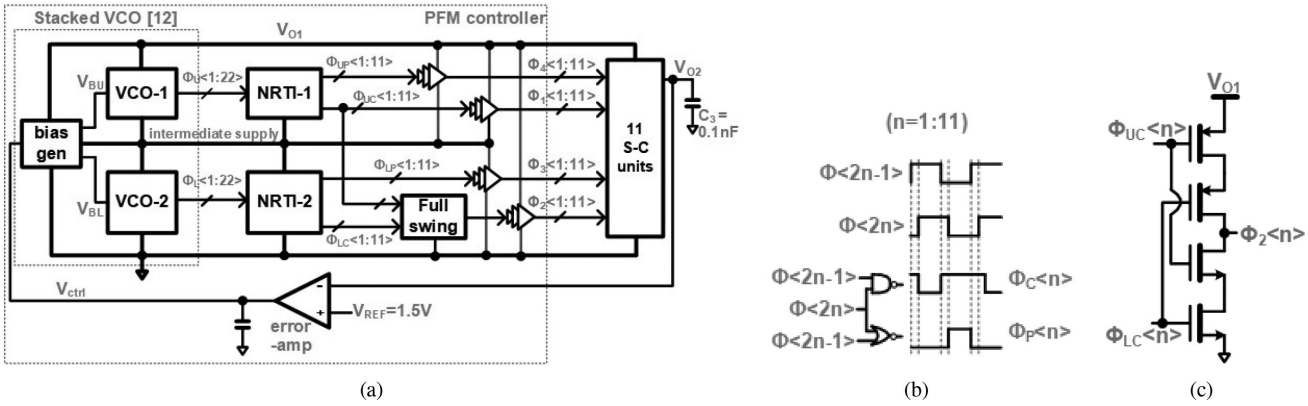


Fig. 10. (a) Schematic diagram of the PFM controller. (b) NRTI logic. (c) Full-swing generation.

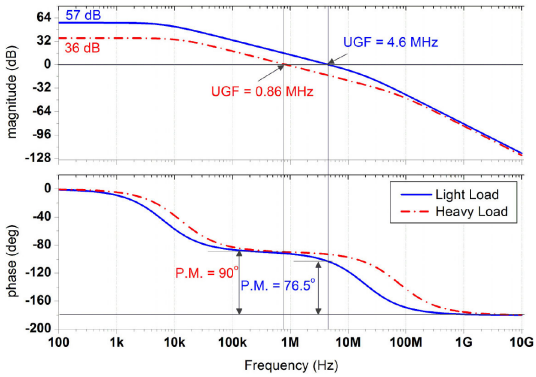


Fig. 11. Frequency response of the compensated control loop of the step-down stage: light-load = 5 mA; heavy-load = 40 mA.

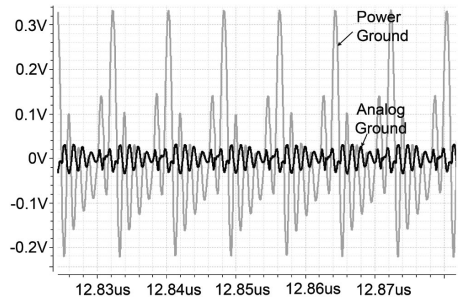


Fig. 12. Simulated analog ground bounce in the proposed hybrid converter.

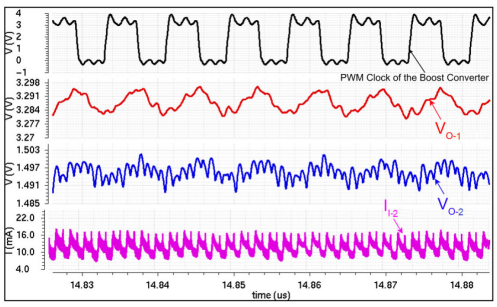


Fig. 13. Simulated effects of the switching noise.

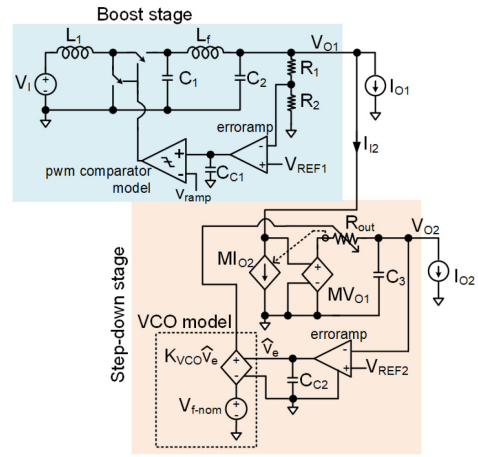


Fig. 14. Hybrid converter macromodel.

frequency=120 MHz, loop compensation capacitance (C_{C1}) = 75 pF, feedback resistance, $R_1 = 35\ K\Omega$ and $R_2 = 20\ K\Omega$.

Macromodel of the step-down stage consists of an ideal dc transformer [29], [30], an output resistance (R_{out}), which takes series power loss components into account, an ideal error amplifier and a VCO model. Output of the dc transformer represents no-load output voltage determined by the ideal conversion ratio (M) of the S-C converter stage. For the step-down stage in consideration, M=0.5. Previous studies [29] have shown that for a given value of flying capacitance, R_{out} is a function of switching frequency. In this setup, frequency-dependent R_{out} has been realized using a Verilog-A-based simulatable model where the controlling input is a voltage, equivalent to the frequency information. The VCO model generates the frequency-equivalent control voltage, which consists of a small-signal component, $K_{VCO}\hat{v}_e$ (represents adjustment of switching frequency by the control loop) and a quiescent component, V_{f-nom} (represents a nominal frequency). Here, K_{VCO} represents the voltage-to-frequency or transfer gain of the VCO and $\hat{v}_e$ represents small-signal error voltage generated by the error amplifier. Net output capacitance, C_3 takes actual output capacitance (100 pF) and total flying capacitance (660 pF) connected at the output node

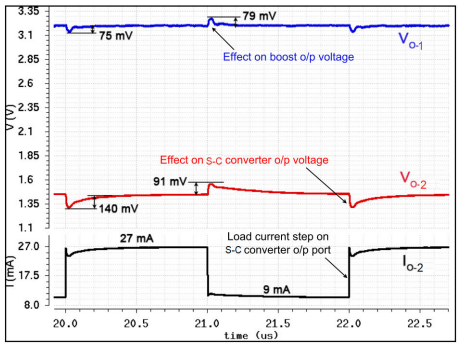
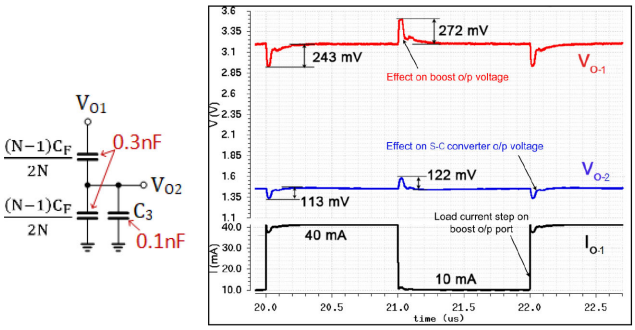


Fig. 15. Cross regulation from V_{O2} to V_{O1}.



(a) (b)

Fig. 16. (a) Equivalent circuit. (b) Cross regulation from V_{O1} to V_{O2}.

into account. It may be noted that, as discussed in Section IV-C, stability analysis of the step-down stage has been performed using this macromodel of the S-C stage.

In this section, the cross-regulation characteristic as analyzed using the abovementioned macromodel of the hybrid converter is presented for two following test cases.

1) Load-Step on V_{O2}: A load step of ΔI_{O2} at the output of the step-down stage (with ideal conversion ratio $= M$) is translated to the output of the boost stage as an equivalent load step of $M \times \Delta I_{O2}$. The boost stage responds to this transient current requirement according to its own control loop's capacity. As an example, a load-step of 9 to 27 mA (and vice versa) has been applied at the output of the step-down stage with $V_I = 1.8$ V and $I_{O1} = 10$ mA. Exactly half of the applied ΔI_{O2} propagates back to the boost output port. The transient undershoot and overshoot observed on V_{O1}, as shown in Fig. 15, are due to an equivalent load step of 9 mA at V_{O1} port. The transient cross regulation from V_{O2} to V_{O1} can be further improved by reducing the ac output impedance of the boost stage directly by increasing the value of capacitance C_2 of the boost stage, however, without affecting the loop stability. It may be noted that dc load regulation is unaffected assuming that the boost converter is able to supply the additional $M \times \Delta I_{O2}$.

2) Load-Step on V_{O1}: In case of an instantaneous change in voltage V_{O1} prompted by a load step at the boost output port, the step-down stage appears as an equivalent capacitive divider, as shown in Fig. 16(a). So, the transient over/undershoot experienced by V_{O1} is translated down to V_{O2} through this capacitive divider. Due to the NRTI switching scheme, $^{(N-1)}/_{2N}$ portion of

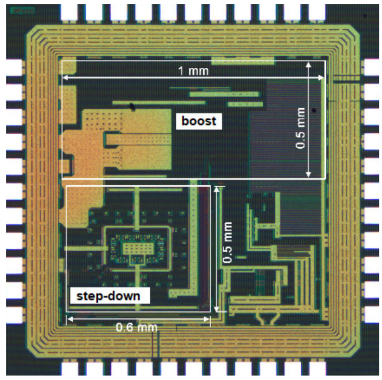


Fig. 17. Die micrograph of the full chip.

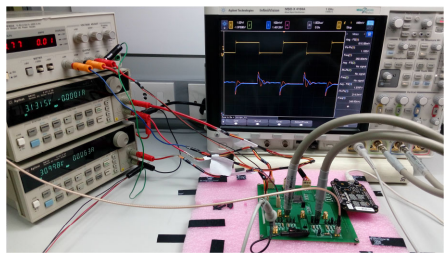


Fig. 18. Experimental setup.

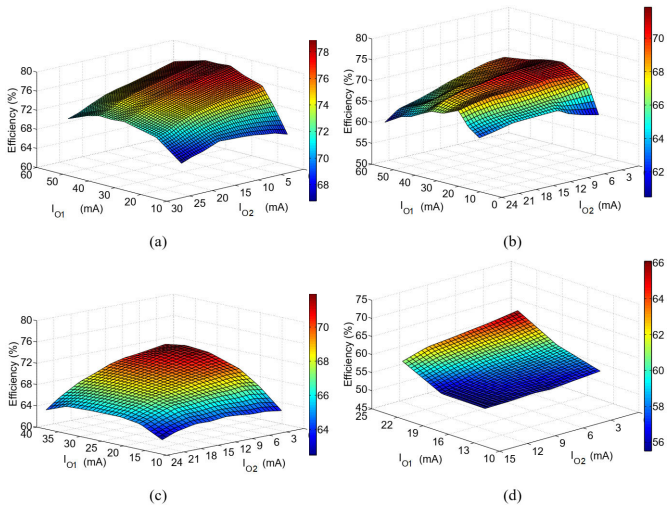


Fig. 19. Combined efficiency of the hybrid converter for different input voltages. (a) $V_I = 2.7$ V. (b) $V_I = 2.2$ V. (c) $V_I = 1.8$ V. (d) $V_I = 1.2$ V.

total C_F is effectively connected from V_{O1} to V_{O2} and an equal portion of C_F is effectively connected from V_{O2} to ground. In the prototype design, the ratio $^{V_{O2}}/_{V_{O1}}$ of the capacitive divider is $^3/_7$. So, approximately 43% of the over/undershoot in V_{O1} is expected to get coupled to V_{O2}, as shown in Fig. 16(b). This transient cross coupling can be reduced further by increasing C_3 without affecting the loop stability. There is no impact on the dc load regulation of V_{O2} as there is no change in I_{O2}. Likewise, the dc line regulation of the step-down stage also remains unaffected. If there is a drop in V_{O1} due to overloaded

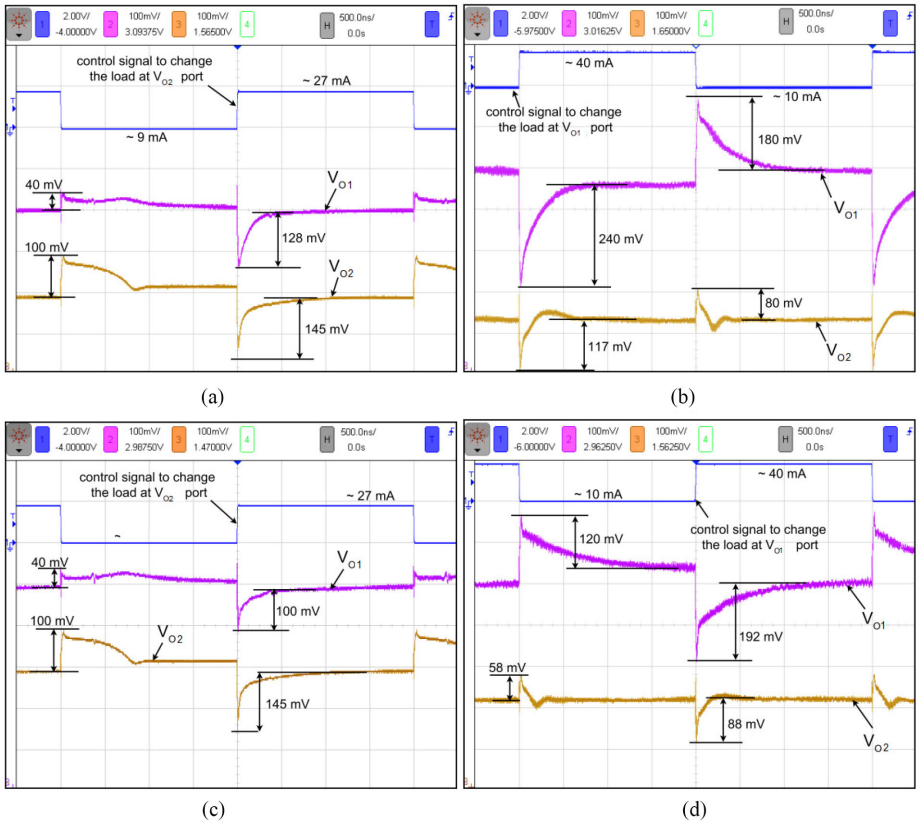


Fig. 20. Cross regulation. (a) Load-step on V_{O2} ($V_I = 1.8$ V). (b) Load-step on V_{O1} ($V_I = 1.8$ V). (c) Load-step on V_{O2} ($V_I = 2.5$ V). (d) Load-step on V_{O1} ($V_I = 2.5$ V).

condition of the boost stage, the step-down stage may be able to regulate V_{O2} provided, R_{out} has not reached its upper limit determined by switch resistance and, hence, the frequency control loop can decrease the dropout voltage (MV_{O1}-V_{O2}) by required margin.

V. Experimental Results

The test chip has been fabricated within a 1.5 mm × 1.5 mm die area in 0.18 μm CMOS process. Die micrograph of the fabricated die is shown in Fig. 17. It may be noted that the prototype shares space of the test chip with some other IPs. The total chip area occupied by the proposed converter is 0.82 mm^2. of which the boost stage consumes 0.52 mm^2 and the step-down stage consumes 0.29 mm^2. It may be noted that a major portion (84%) of the area occupied by the boost converter is effectively consumed by its two capacitors.

Lab setup for silicon validation of the prototype is shown in Fig. 18. Measured circuit performance of the prototype converter is discussed the following sections.

A. Measured Efficiency

The hybrid converter has been characterized for different input voltage and load current (at both the output ports) combinations. The combined efficiency of the hybrid converter is calculated based on the following relationship:

$$\eta_{\text{comb}} = 100 \times \frac{(V_{O1}I_{O1}) + (V_{O2}I_{O2})}{P_{\text{IN}}} \tag{4}$$

where P_{IN} is the total input power. η_{comb}, for four different input voltages (namely, 2.7, 2.2, 1.8, and 1.2 V), is plotted in Fig. 19 for combinations of load currents subject to the constraint that the output voltages, and V_{O1} and V_{O2} remain regulated within 2% tolerance of their respective steady-state levels. The steady-state levels ($V_{O1} = 3.2$ V, $V_{O2} = 1.45$ V) are slightly lower than the typical targets because of variation of the on-chip, bandgap reference voltage.

It may be observed that for higher input voltage ($V_I = 2.2$ V), the boost converter can support up to 56 mA load in addition to the input current drawn by the step-down converter. Maximum load capability reduces with decreasing input voltage as it delivers maximum 21 mA at $V_I = 1.2$ V.

From the measured data, it is evident that the overall efficiency drops with increase of I_{O1}. Efficiency of the step-down stage is ideally 90% [$= (2\times1.45)/3.2$] and practically, near about 82%. So, it is understood that efficiency of the boost stage drops with higher load. The tradeoff performance of conduction loss versus frequency-dependent drive loss of an on-chip switch is inferior to that of an external MOSFET/IGBT switch commonly used in on-board realization. Moreover, Q-factor of the bond wire inductor

TABLE III
SUMMARY OF HYBRID ARCHITECTURES

Parameter	**[24]**	**[26]**	**This Article**
Architecture	Reconfigurable SC front-end stage followed by inductive buck stage	SC step-down stage parallel to inductive buck stage	Inductive boost stage followed by time-interleaved SC step-down stage
Application	Wide input range, LED driver	Supply to DVS load	Analog and digital supply for SoC
Process	Discrete	32nm SOI	180nm CMOS
L / C (inductive stage)	0.84μH / 10μF	2nH / 2nF	20nH, 30nH / 2×0.54nF
C_F / C_O (capacitive stage)	2×1μF / 20nF	Not available	0.66nF / 0.1nF
Input	25-200V	1.2V	1.2-2.7V
Output	Single → 35V	Single → 0.4V-0.9V	Dual → 1.45V, 3.2V
Load	30W	2-140 mA	25mA, 50mA
Efficiency	88-96%	74.5% (peak)	52-77%

is better than that of metal inductor but not as good as that of an external inductor.

B. Measured Cross Regulations

Measurements of cross regulations of the hybrid converter have been performed for two input voltages, namely, 1.8 and 2.5 V. The plots from the measurements are shown in Fig. 20. For $V_I = 1.8$ V, the applied load current step at the step-down converter output port results in 4% of undershoot and 1.25% of overshoot in V_{O1}. On the other hand, the applied load current step at the boost converter output port, results in 8.06% of undershoot and 5.52% of overshoot in V_{O2}. For $V_I = 2.5$ V, the load step at the step-down converter output port results in 3.12% of undershoot and 1.25% of overshoot in V_{O1}. On the other hand, the load step at the boost converter output port, results in 6.07% of undershoot and 4% of overshoot in V_{O2}.

C. Comparison With State-of-the-Arts

As already mentioned, most of the existing hybrid architectures are discrete component based and there is one fully-integrated hybrid converter design found in literature. A direct comparison among these architectures is not appropriate. So, a summary of topological configuration, application, and performance of those state-of-the-art hybrid architectures and the work presented in this article is provided in Table III. As described, motivation of hybridization in these architectures are different as they target different applications. The discrete component based architecture [24] naturally provides very high efficiency compared to the other two that is [26] and this work. The prototype presented in [26] is a fully-integrated architecture but, it uses the two converters in parallel where the switched-capacitor-based converter is selected over the inductor based buck converter in light-load condition to improve light-load efficiency. Whereas, in this article, the two converters are used in series and its efficiency is a function of efficiency of two individual converters across all load conditions. The measured peak efficiency of the converter of [26], for 1.2 to 0.9 V conversion, in inductive mode is 74.5%, which is slightly less than the efficiency of a linear regulator. Whereas, the combined efficiency of the hybrid converter presented in this work exhibits 77% peak efficiency for 2.7 to 3.2 V boost conversion. Although the light-load efficiency of the proposed converter prototype is not as good as that of the prototype of [26], the former provides one boosted and one stepped-down output voltages simultaneously, with higher efficiency at higher loads and it also covers a much wider range of input voltage.

VI. CONCLUSION

Here, we have demonstrated a prototype of a hybrid, dual-output converter comprising of an inductor-based boost stage cascaded with a switched-capacitor-based step-down stage. The proposed hybrid architecture helps to combine merits of the individual converters in an integrated unit. The on-chip integration issues due to ground noise generated in the boost stage and switching noise generated by in-rush current in the step-down stage are discussed followed by the design, analysis, and silicon results of the proposed hybrid converter that show how the aforementioned hurdles are overcome. The use of π-filter at boost converter output helps to isolate the noisy power ground of the boost converter from rest of the circuit. Then, the NRTI-scheme-based design of the step-down converter helps to significantly reduce its in-rush current. Because of this, the step-down converter appears as a quiescent load to the preceding boost converter, which helps to reduce required value of output capacitance of the π-filter and, hence, making it possible to realize the capacitance on-chip. Moreover, integrating all the passive filter components with rest of the design along with the load on same chip helps to eliminate load transient spikes caused by package pin parasitic inductance. The prototype converter provides two regulated output voltages, namely, 1.45 and 3.2 V from an input voltage, varying over a wide range of 1.2 to 2.7 V. Both the output voltages contain very small switching ripple. Peak efficiency of the converter is 77% and the efficiency remains more than 52% for all line and load conditions. In the present prototype, output overshoot/undershoot due to cross-loading effect is within 10%, which is on the higher side. It may be worth exploring to improve the transient cross regulation as part of a potential future work.

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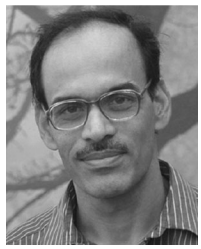

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