A Fully Integrated FVF LDO With Enhanced Full-Spectrum Power Supply Rejection

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***Abstract*—This article presents a fully integrated flipped voltage follower (FVF) based low-dropout (LDO) regulator with enhanced full-spectrum power supply rejection (PSR) and unity-gain bandwidth over 400MHz for noise-sensitive circuits. Following the study of three types of FVF LDO's PSR performances, we propose a novel FVF LDO with a low-gain fast loop-1 and a high-gain slow loop-2. In prior FVF LDOs, their PSRs are either full-spectrum, or not, but with low PSR at low frequency. In this article, we fully utilize both dc gains of loop-1 and loop-2 for the low-frequency PSR, while the high-frequency PSR remains unchanged. In addition, we use dynamic compensation to push the loop-2's UGB to higher frequency for a better PSR bandwidth. This work, fabricated in 65 nm complementary metal oxide semiconductor (CMOS), with 1.2-V input and 1-V output, exhibits a measured quiescent current (I_Q) varying from 27 to 82 μA for a load current I_{LOAD} between 5 μA and 20 mA. The circuit achieves a low frequency PSR of –58 dB with the worst full-spectrum PSR of –9 dB in 20 mA I_{LOAD} with a 300 pF on-chip output capacitor. Further, with an UGB over 400 MHz, the proposed FVF LDO reaches 0.9 ns response time when I_{LOAD} changes between 100 μA and 20 mA with edge times less than 0.8 ns.**

***Index Terms*—Flipped voltage follower (FVF), full-spectrum power supply rejection (PSR), fully-integrated low-dropout (LDO), low-dropout regulator (LDO), PSR.**

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I. Introduction

POWER management integrated circuits (PMICs) are playing an increasingly important role in system-on-a-chip (SoC), especially nowadays when the circuit volume keeps shrinking down while the performance demand keeps increasing [1]–[6]. Among the PMICs, switch mode power converters feature high efficiency and can supply digital circuits. Since low-dropout (LDO) regulators can provide clean supply voltages with fast transient responses they are usually used to drive noise-sensitive circuits, such as transimpedance amplifiers, or low-noise amplifiers in wireline or wireless communication front-end systems [7], [8].

We can categorize LDOs into two types: LDOs with external capacitor, or fully-integrated LDOs (capacitor-less). LDOs with external capacitor show small undershoot and overshoot in load transient response with excellent power supply rejection (PSR) in low frequency. However, the off-chip capacitor occupies a relatively large printed circuit board area even considering the miniaturization of modern circuits. In addition, the off-chip capacitor cannot filter out the high frequency noise due to the parasitic inductance and resistance of the bond wire. Thus, fully integrated LDOs are highly preferable for point-of-load power delivery in area-efficient applications. However, in a fully integrated LDO, the transient response and PSR will degrade significantly due to the absence of the off-chip capacitor, thus becoming the major design challenges.

Many methods emerged to tackle these issues. For example, in [9], an LDO with 0.54 ns response time composed by a fast load tracking feedback loop inside unity-gain buffers. However, it consumes a large quiescent current (6% of the total), leading to a current efficiency of 94%. An adaptively biased LDO with subthreshold undershoot reduction, in [10], shows improvement in the transient response and the PSR, but the undershoot is still 105 mV under a relatively slow current change (100 mA/ μs) with the PSR reaching 0 at 10 MHz. Other techniques like voltage spike detection and push-pull composite power transistor do enhance the load transient response to some extent [11], [12], but they do not improve the PSR. Then, to enhance it, a popular approach is the feed-forward supply ripple (noise) cancellation [13]–[18], that leads to -60 dB PSR up to 1MHz achieved in [13] and [15] and even up to 10 MHz in [16], but they still need an off-chip capacitor in μF range. Park *et al.* [14] and Lavalle-Aviles *et al.* [18] show obvious PSR improvement up to 10 MHz, but they cannot deal with higher frequency noise. On the other hand,

[17] proposed an adaptive supply-ripple cancellation technique to cancel the PSR hump of the LDO with an internal dominant pole. It obtained over −36 dB PSR from 10 kHz to 1 GHz at the cost of consuming nearly 300 μA of quiescent current for a 25 mA load current, not to mention its' complicated implementation. In addition, it sacrificed the transient response speed by locating the dominant pole at the gate of the power transistor. A cascode of three power transistors led to over −38 dB PSR up to 50 MHz in [19], but a 0.6 V dropout voltage drastically degrades the power efficiency. Further, pushing the unit-gain bandwidth (UGB) up to 100 MHz in [20] and [21] caused an ultrafast transient response and relatively good PSR, simultaneously. Though [20] exhibited a full-spectrum PSR, the low frequency PSR is only −22 dB due to the limited gain of the fast loop. In the case of [21], it reached over −55 dB PSR up to 1 MHz, but it degraded close to −10 dB at 40 MHz. In addition, it requires a minimum load current of 120 μA to maintain stability.

From the literature review above, we can conclude that although there are many approaches to increase the transient response or to improve the PSR, there is still no effective solution to obtain a high PSR and an ultrafast transient response, simultaneously. In this article, we present a dual-loop fully integrated flipped-voltage-follower (FVF) [22] based LDO that obtains a 0.9-ns transient response time and a full-spectrum PSR with enhanced low frequency PSR. We revisited the tri-loop LDO from [20], and found that by removing the second loop and isolating the supply ripple in the slow loop, the low frequency PSR can be dramatically improved. Meanwhile, pushing the slow loop UGB to higher frequency with an increase in the load current, further improves the high frequency PSR. On the other hand, the fast FVF loop with a dominant pole at the output guarantees an ultra-fast transient response and a full-spectrum PSR.

The rest of this article is organized as follows. Section II analyses the PSR performance of traditional FVF LDOs. Section III presents the circuit implementation of the proposed FVF LDO together with its stability and PSR analyses. Section IV shows the measurement results. Finally, Section V draws the conclusion.

II. PSR Analysis of Traditional FVF LDOs

First, we categorized FVF LDOs into three types:

1) Fig. 1(a) with only the mirror voltage $V_{\rm MIR}$ feeds back to the error amplifier (EA) [23]–[26];
2) Fig. 1(b) with both $V_{\rm MIR}$ and output voltage $V_{\rm OUT}$ feedback to the EA [20], [27]; and
3) Fig. 1(c) with only $V_{\rm OUT}$ feeds back to the EA [28]–[30].

In example-1, there are mainly two feedback loops. Loop-1 is an FVF loop, which is a fast local loop. Loop-2 is a slow loop that ensures $V_{\rm MIR}$ is equal to the reference voltage $V_{\rm REF}$. Since $V_{\rm OUT}$ does not feedback to EA, its dc voltage accuracy highly depends on the dc gain of loop-1. To analyze the low frequency PSR performance, we investigate the small-signal model from Fig. 2. Here, we are only analyzing the low frequency PSR, thus neglecting the parasitic capacitances. For simplicity, we also ignore the body effect. To calculate the PSR transfer function

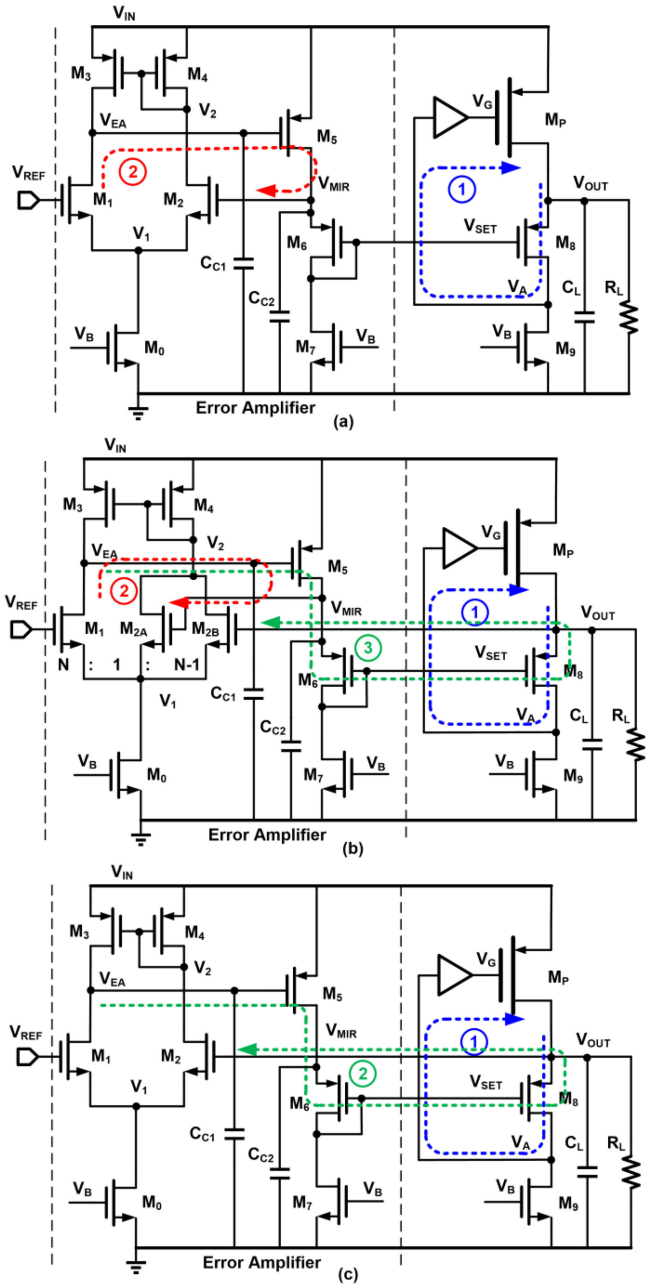

Fig. 1. Three types of FVF LDOs. (a) Example-1. (b) Example-2. (c) Example-3.

we apply a small voltage change v_{in} at the supply, we can get

$$\frac{v_{\rm out}}{v_{\rm in}} = \frac{g_{mp}\left(1+\frac{A_1}{(1+k_1)A_2}\right)+\frac{1}{r_{op}}}{g_{mp}A_1+1/r_{op}+1/R_L} = \frac{A_{mp}\left(1+\frac{A_1}{(1+k_1)A_2}\right)+\frac{R_L}{r_{op}+R_L}}{A_1A_{mp}+1} \approx \frac{A_{mp}+\frac{1}{1+k_2}}{A_1A_{mp}} = \frac{1}{A_1}+\frac{1}{(1+k_2)A_1A_{mp}} \quad (1)$$

where g_{mi} and r_{oi} are the transconductance and output resistance of M_i, respectively, $A_1 = g_{m8}(r_{o8}\|r_{o9})$ is the dc gain of the common gate amplifier consisting of M_8 and M_9, A_2 is the

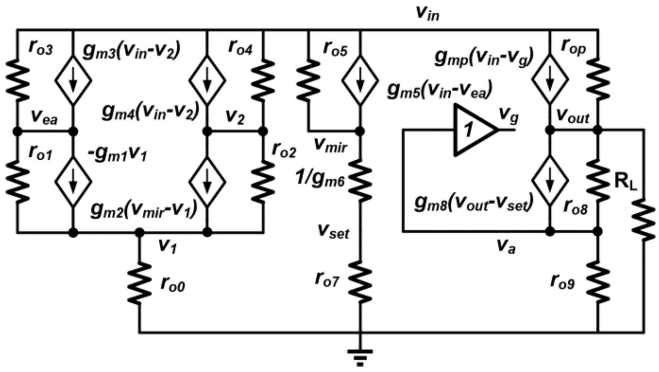

Fig. 2. Simplified small-signal model for low frequency PSR analysis.

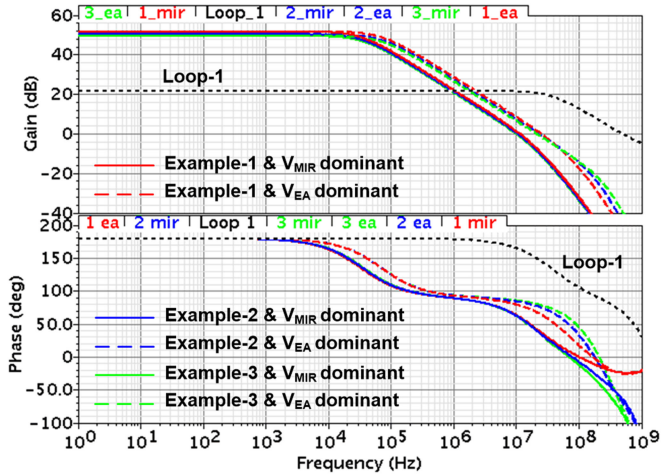

Fig. 3. Simulated Bode plot of fast loop (loop-1) and slow loop (loop-2 and loop-3) with $I_{\rm LOAD} = 20$ mA, $V_{\rm IN} = 1.2$ V, and $V_{\rm OUT} = 1$ V.

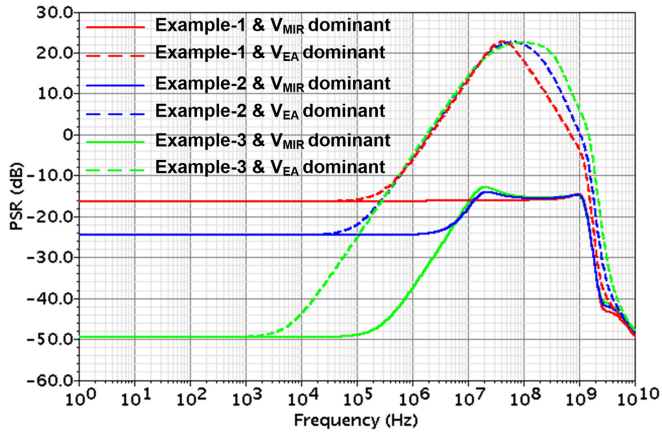

Fig. 4. Simulated PSR performance of the three FVF LDO examples with different dominant poles.

dc gain of the two-stage EA, $A_{mp} = g_{mp}(r_{op}\|R_L)$ is the dc gain of the power stage, $k_1 = r_{o5}/r_{o7}$, and $k_2 = r_{\rm op}/R_L$. In addition, we assume that $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$ and $r_{o1} = r_{o2}$, $r_{o3} = r_{o4}$, $1/g_{m6} \ll r_{o7}$ and the gain of the buffer is 1. Now we observe that, although EA has a high dc gain A_2, it does not dominate the low frequency PSR. In order to get a high PSR as well as a good dc accuracy, we need a large A_1. By using two stages in [25] and three stages in [24], leads to over -50 dB PSR at 1 kHz. Besides, the line regulation and load regulation are better when compared with that FVF LDO using single-transistor-control in [23]. However, the output node $V_{\rm OUT}$ can no longer be the dominant pole for loop-1 without using a large output capacitor $C_{\rm OUT}$, which will deteriorate the high frequency PSR. For example, the PSR drops to 0 at 500 kHz in [24].

In example-2, there are mainly three feedback loops. Compared with example-1, $V_{\rm OUT}$ fed back to a tri-input EA forms the third loop. The *W/L* ratios of the three input transistors M_1, $M_{2\rm A}$, and $M_{2\rm B}$ are $N:1:N-1$. Using similar derivations as in example-1, we obtain

$$\begin{aligned}\frac{v_{\rm out}}{v_{\rm in}} &= \left(A_{mp}\left(1+\frac{NA_1}{(1+k_1)A_2}\right)+\frac{R_L}{r_{op}+R_L}\right)\Big/\left(NA_1A_{mp}+1\right)\\ &\approx \left(A_{mp}+\frac{1}{1+k_2}\right)\Big/NA_1A_{mp} = \frac{1}{NA_1}+\frac{1}{(1+k_2)NA_1A_{mp}}.\end{aligned} \tag{2}$$

We can see that the low frequency PSR increased close to N times when compared with example-1. With a larger N, we can get a higher low frequency PSR. However, a very large N is not practical. In addition, A_2 still does not dominate the low frequency PSR, the same as in example-1.

In example-3, we removed the loop-2 from example-2, thus we can consider this case as example-2 with infinite N. By repeating previous derivations, we have

$$v_{\rm mir} = \frac{1}{(1+k_1)}v_{\rm in} - A_2 v_{\rm out} \tag{3}$$

$$\begin{aligned}\frac{v_{\rm out}}{v_{\rm in}} &= \frac{A_{mp}\left(1+\frac{A_1}{(1+k_1)A_2}\right)+\frac{R_L}{r_{op}+R_L}}{A_1A_{mp}(1+A_2)+1}\\ &\approx \frac{A_1+1+k_1}{A_1A_2(1+k_1)} = \frac{1}{A_2(1+k_1)}+\frac{1}{A_1A_2}.\end{aligned} \tag{4}$$

In this case, A_2 dominates the low frequency PSR. For ultrafast response and full-spectrum PSR, loop-1 is usually set to be a low-gain loop with $V_{\rm OUT}$ being its dominant pole, thus $A_1 \ll A_2$. Therefore, example-3 achieves the best low frequency PSR when compared with example-1and example-2 given the same loop-1.

For the slow loop, we should design $V_{\rm MIR}$ as the dominant pole to offer a clean source to the gate of M_8. Otherwise, a PSR peak will appear (explained next). The EA is a two-stage amplifier with $V_{\rm EA}$ as the internal pole and $V_{\rm MIR}$ the output pole. If the internal pole is dominant, the PSR will begin to degrade at the dominant pole frequency ω_D, and then, forms a PSR hump [17]. To verify the analyses above, Figs. 3 and 4 show the simulation results of these three LDOs, while Table I summarizes transistor sizes and key parameters. In addition, we use two different compensation capacitors C_{C1} (3 pF) and C_{C2} (28 pF) to set the dominant pole at $V_{\rm EA}$ and $V_{\rm MIR}$, respectively. Fig. 3 shows the dc gain of EA and loop-1 that are about 50 and 21 dB, respectively. These three examples have very similar gain

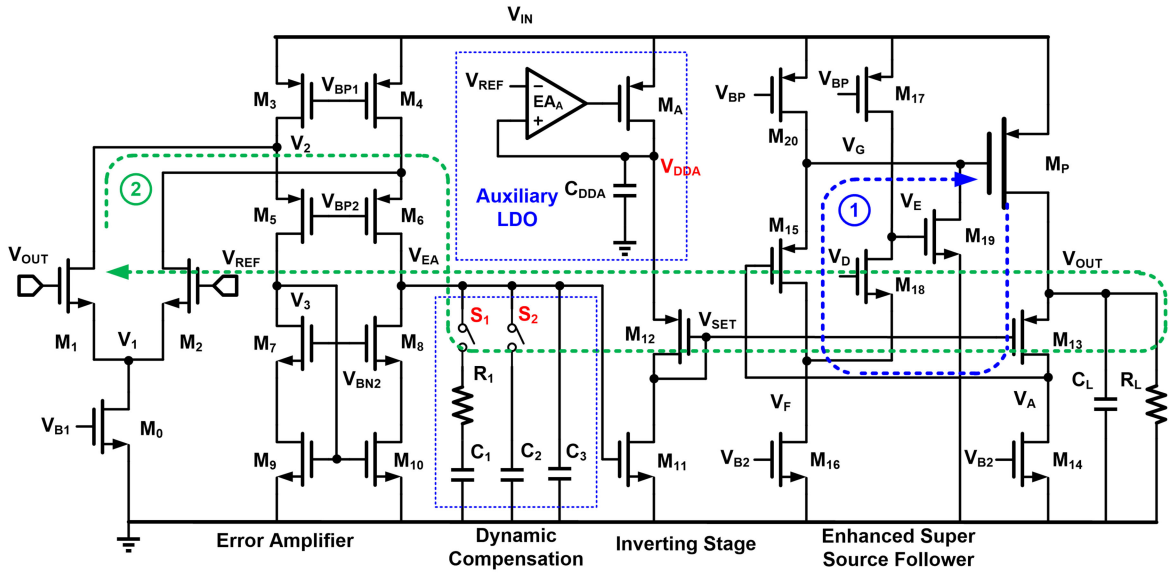

Fig. 5. Schematic of the proposed FVF LDO.

TABLE I
PARAMETERS OF THREE FVF LDO EXAMPLES

M_0	8×0.5/0.5	M_3, M_4	4×0.5/0.5	M_9	3×0.15/0.12
M_1	4×0.5/1	M_5	3×1/0.2	C_L	300 pF
M_2	4×0.5/1	M_6	0.25/0.08	I_0	4 μA
M_{2A}	1×0.5/1	M_7	0.15/0.12	I_7	4 μA
M_{2B}	3×0.5/1	M_8	3×0.25/0.08	I_9	12 μA
C_{C1}	3 pF, V_{EA} dominant		C_{C2}	0 pF, V_{EA} dominant	
	0 pF, V_{MIR} dominant			28 pF, V_{MIR} dominant	

Transistor sizes in μm/μm.

and phase regardless of the dominant pole location. However, the PSR performances are quite different, as shown in Fig. 4. With $V_{\rm MIR}$ as the dominant pole we achieve a full-spectrum PSR while a peak appears with $V_{\rm EA}$ as the dominant pole. As previously discussed, example-3 with $V_{\rm MIR}$ being its dominant pole achieves the best PSR.

However, there are still two main limitations. First, the low frequency PSR is only moderate with the contributions of A_2, A_1. This happens because of the $v_{\rm in}/(1+k_1)$ term in (3). Without this term, (4) becomes

$$\frac{v_{\rm out}}{v_{\rm in}} \approx \frac{1}{A_1 A_2} \tag{5}$$

which improves the low frequency PSR. The power supply of EA determines the $v_{\rm in}/(1+k_1)$ term. To eliminate or minimize this term, a clean source should supply EA, implying an extra effort. Otherwise, we should minimize this term as much as possible. Secondly, because the EA in Fig. 1(c) has two high impedance nodes $V_{\rm EA}$ and $V_{\rm MIR}$, and the pole at $V_{\rm EA}$ is a nondominant pole, it is difficult to expand the UGB of loop-2, thus it will be hard to enhance even further the high frequency PSR. Based on the above discussion, we propose next a novel FVF LDO.

III. PROPOSED FVF LDO

Fig. 5 shows the schematic of the proposed FVF LDO, which consists of a folded-cascode EA, a dynamic compensation network [31], an inverting stage, an auxiliary LDO, an enhanced supersource follower (ESSF) buffer [26], a power transistor M_P and an output capacitor C_L. The EA used here has an output $V_{\rm EA}$ referred to the ground, which will minimize the influence of $v_{\rm in}$. Moreover, because there is only one high impedance node ($V_{\rm EA}$) in the EA, it is easier to push the UGB of loop-2 to higher frequency, thus leading to an improvement in the high frequency PSR. The dynamic compensation network consists of three branches and the capacitance of the three capacitors are $C_1 > C_2 > C_3$. In light load, with all three branches connected to $V_{\rm EA}$, the pole at $V_{\rm EA}$ node $p_{\rm EA}$ remains in low frequency. In medium load, S_1 turns OFF, pushing $p_{\rm EA}$ to higher frequency. In heavy load, both S_1 and S_2 turn OFF, and only C_3 connects to $V_{\rm EA}$, pushing $p_{\rm EA}$ to much higher frequency. The inverting stage consists of M_{11} and M_{12}. The auxiliary LDO, used to provide a clean supply for the inverting stage, consists of a single-stage error amplifier $\rm EA_A$, a power transistor M_A and an output capacitor $C_{\rm DDA}$. Because the current through M_A is less than 10 μA, it is possible to set the dominant pole at $V_{\rm DDA}$ with a 10 pF $C_{\rm DDA}$. Therefore, $V_{\rm DDA}$ is a clean source with full spectrum PSR. As discuss previously, the dominant pole of loop-1 is at $V_{\rm OUT}$, and $p_{\rm OUT}$ can be up to tens of MHz in heavy load, therefore, we used ESSF to push the nondominant pole at M_P's gate p_G to values over the GHz range. To set loop-1's dominant pole at $V_{\rm OUT}$ in 20 mA load current condition we used a 300 pF on-chip capacitor C_L.

A. PSR Analysis

To evaluate the low frequency PSR performance, we need to know how much is $V_{\rm EA}$ being influenced by $v_{\rm in}$. The voltage change in EA's output v_{ea} mainly comes from two sources, one is $v_{\rm in}$, which is a common-mode source; the other one is $v_{\rm out}$, which is a differential source. We use v_{eac} and v_{ead} to denote the changes caused by $v_{\rm in}$ and $v_{\rm out}$, respectively. It is simple to obtain $v_{ead} = A_2 v_{\rm out}$, where A_2 is the dc gain of the EA. Ideally, the bias voltage V_{B1}, $V_{\rm BP1}$, and $V_{\rm BP2}$ remain constant to their reference voltages, where V_{B1} references to ground, and

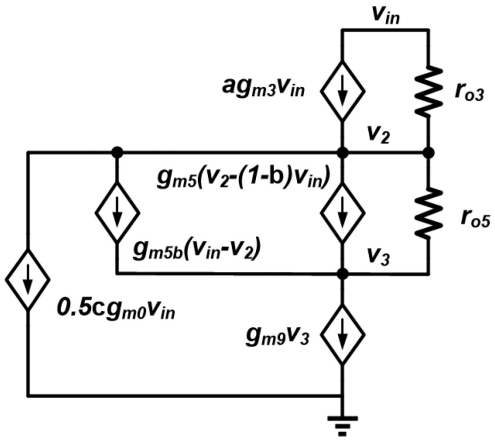

Fig. 6. Small-signal model to calculate v_{eac}.

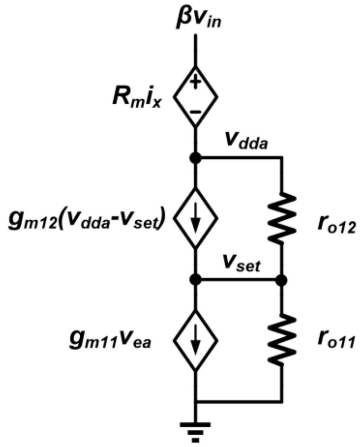

Fig. 7. Small-signal model of inverting stage.

$V_{\rm BP1}$ and $V_{\rm BP2}$ reference to $V_{\rm IN}$. However, in reality, there will be deviations. Let us assume that $v_{\rm bp1} = (1 - a)v_{\rm in}$, $v_{\rm bp2} = (1 - b)v_{\rm in}$, and $v_{b1} = cv_{\rm in}$, where a, b, and c are the deviation factors. Fig. 6 shows the small-signal model used to calculate v_{eac}. Considering that, for $v_{\rm in}$, the two branches are symmetrical, thus we only show one branch here

$$v_{eac} = \left(\frac{ag_{m3} - 0.5cg_{m0}}{g_{m9}} + \frac{1}{g_{m9}(g_{m5} + g_{m5b})r_{o3}r_{o5}}\right) v_{\rm in} = xv_{\rm in}. \tag{6}$$

Then, in the ideal case, $a = 0$ and $c = 0$, and $v_{eac} = v_{\rm in}/g_{m9}(g_{m5} + g_{m5b})r_{o3}r_{o5}$ exactly the voltage value divided by two resistors $(g_{m5} + g_{m5b})r_{o3}r_{o5}$ and $1/g_{m9}$. Now, we have

$$v_{ea} = v_{eac} + v_{ead} = xv_{\rm in} + A_2v_{\rm out}. \tag{7}$$

Assuming that $g_{m11} = g_{m12}$

$$v_{\rm set} = -\frac{g_{m11}}{g_{m12}}v_{ea} = -v_{ea} = -xv_{\rm in} - A_2v_{\rm out}. \tag{8}$$

Finally, we have

$$\frac{v_{\rm out}}{v_{\rm in}} = \frac{A_{mp}(1 - xA_1) + 1}{A_{mp}A_1A_2 + 1 + \frac{r_{op}}{R_L}} \approx \frac{A_{mp}(1 - xA_1) + 1}{A_{mp}A_1A_2} = \frac{1 - xA_1}{A_1A_2} + \frac{1}{A_{mp}A_1A_2}. \tag{9}$$

From (9), we can observe that the low frequency PSR dominated by A_1 A_2. In addition, because usually the bias current of M_3 is larger than that of M_0, then $g_{m3} > g_{m0}$. Usually, a diode-connected transistor in series with a given bias current generates the bias voltage. Assuming that the diode-connected transistor is M_X, and the transconductance is g_{mx}; a current mirror generates the bias current, and the output resistance is r_o, then a or c equals to $1/(1 + g_{mx}r_o)$, then normally a and c are larger than 0 (the actual calculation will be more complicated). If $a > 0.5c$, which can be easily achieved by designing a proper g_m and r_o, then $ag_{m3} - 0.5cg_{m0} > 0$, so $x > 0$, the xv_{in} term at v_{set} no longer deteriorates but benefits the PSR. Here, we conclude that, for the previous example-3, x should be as small as possible; and for the proposed FVF LDO, as long as $x < (A_{mp} + 1)/A_1A_{mp}$, the larger the x, the better the PSR.

B. PSR of the Auxiliary LDO

In the above analyses, we assumed that $V_{\rm DDA}$ is a clean source. However, the auxiliary LDO cannot provide an absolute clean supply. There are two main factors leading to v_{dda} deviations: one is the auxiliary LDO's limited PSR; and the other is the load regulation. As Fig. 7 shows, assuming that the auxiliary LDO has a PSR of β, and the transresistance is R_m. From the small-signal model, we have

$$v_{dda} = \beta v_{in} - R_m i_x \tag{10}$$

$$i_x = g_{m12}(v_{dda} - v_{\rm set}) + \frac{v_{dda} - v_{\rm set}}{r_{o12}} = g_{m11}v_{ea} + \frac{v_{\rm set}}{r_{o11}}. \tag{11}$$

Assuming also that $r_{o11} >> R_m$, $r_{o12} >> R_m$ and $g_{m12}r_{o12} >> 1$, we get

$$v_{\rm set} = (\beta v_{\rm in} - g_{m11}R_mv_{ea}) - v_{ea}. \tag{12}$$

We can see that if $\beta = 0$ and $R_m = 0$, $v_{set} = -v_{ea}$, the inverting stage is an ideal inverting stage. Now, we calculate β's critical value $\beta_{\rm crit}$. Let $\beta_{\rm crit}v_{\rm in} - g_{m11}R_mv_{ea} = 0$, and for simplicity, let $v_{\rm out} = v_{\rm in}/{\rm A_1A_2}$. Substituting (7) into (12)

$$\beta_{\rm crit} = g_{m11}R_m(x + 1/A_1). \tag{13}$$

As a result, as long as $\beta < \beta_{\rm crit}$, $v_{\rm set}$ is not deteriorated, V_{DDA} can be regarded as a clean source. For example, assuming that $g_{m11} = 50$ μs, $R_m = 1$ kΩ (corresponding to a load regulation of 1mV/1 μA), $x = 0.05$, and $A_1 = 10$, then $\beta_{\rm crit} = 0.0075$, corresponding to a PSR of -42 dB. Fig. 8 shows the simulated PSR with $V_{\rm DDA}$ provided by an auxiliary LDO and an ideal source, respectively. Then, the PSR does not deteriorate and even improves slightly with the auxiliary LDO.

C. Stability Analysis

There are two loops in the proposed FVF LDO, we will analyze the stability of loop-1, loop-2, and the entire loop.

Fig. 9 shows the small-signal model for the loop-1 stability analysis, assuming $v_{i2} = 0$ with a clean dc bias voltage and

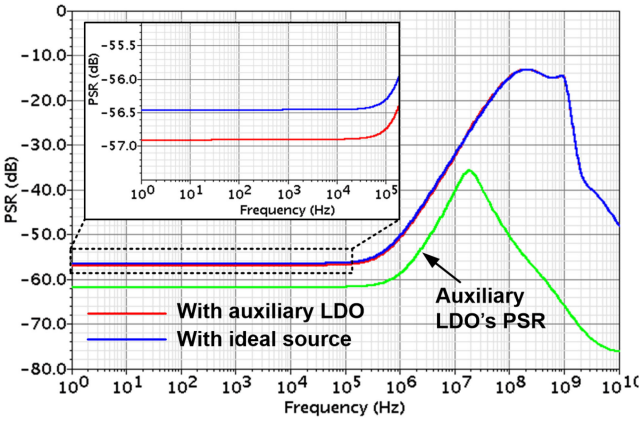

Fig. 8. Simulated PSR with auxiliary LDO and with ideal source.

breaking the signal path between v_a and the input of the ESSF buffer. For ESSF, we have

$$v_g = \frac{(1+\frac{s}{z_1})(1+\frac{s}{z_2})v_{i1}}{(1+\frac{s}{p_G})(1+\frac{s}{p_1})(1+\frac{s}{p_2})} \approx \frac{v_{i1}}{(1+\frac{s}{p_G})} \tag{14}$$

where p_G is the pole at node $\mathrm{V_G}$, p_1, p_2, z_1, and z_2 are the poles and zeros in ESSF. We present a detailed analysis of ESSF in Appendix at the end of this article. c_g is the parasitic capacitances at nodes V_G, and $c_g \approx c_{gsp} + A_{mp}c_{gdp}$, where c_{gsp} and c_{gdp} are the gate-to-source and gate-to-drain parasitic capacitances of M_P, respectively. Finally, we can obtain

$$v_a = \frac{-g_{mp}(r_{op}\|R_L)\cdot g_{m13}(r_{o13}\|r_{o14})\cdot v_g}{(1+sC_L(r_{op}\|R_L))\cdot(1+sc_a(r_{o13}\|r_{o14}))}$$
$$\approx \frac{-A_1A_{mp}v_{i1}}{(1+\frac{s}{p_{\mathrm{OUT}}})(1+\frac{s}{p_G})(1+\frac{s}{p_A})} \tag{15}$$

where $p_{\mathrm{OUT}} = 1/(C_L(r_{o\mathrm{P}}\|R_L))$ and $p_A = 1/(c_a(r_{o13}\|r_{o14}))$. Therefore, the transfer function of loop-1 is

$$T_1(s) = \frac{v_a}{v_{i1}} \approx \frac{-A_1A_{mp}}{(1+\frac{s}{p_{\mathrm{OUT}}})(1+\frac{s}{p_G})(1+\frac{s}{p_A})}. \tag{16}$$

The dominant pole is p_{OUT}, with p_G pushed to near GHz range by ESSF, and p_A locate in a few GHz range due to their small parasitic capacitances. Fig. 10 illustrates the simulated Bode plot of loop-1 with a different load current I_{LOAD}. Since p_{OUT} will change with the load current, the worst case is when $I_{\mathrm{LOAD}} = 20$ mA. We can see that loop-1 has a phase margin (PM) over 62° over the full load range. As a result, loop-1 is stable.

For loop-2, the signal path is broken between v_{ea} and the input of M_{11}. From the signal path, we have

$$v_{\mathrm{out}} = \frac{-A_1A_{mp}}{1+A_1A_{mp}}\cdot\frac{v_{i2}}{(1+\frac{s}{(1+A_1A_{mp})p_{\mathrm{OUT}}})}$$
$$\approx \frac{-v_{i2}}{(1+\frac{s}{A_1A_{mp}p_{\mathrm{OUT}}})}. \tag{17}$$

Then, we get

$$v_{ea} = \frac{g_{m1}r_{ea}v_{\mathrm{out}}}{1+sC_cr_{ea}} \approx \frac{-A_2v_{i2}}{(1+\frac{s}{p_{EA}})(1+\frac{s}{A_1A_{mp}p_{\mathrm{OUT}}})} \tag{18}$$

where c_c is the equivalent capacitance at node V_{EA}, $p_{EA} = 1/(r_{ea}C_c)$ and $r_{ea} = (g_{m6}r_{o4}r_{o6})\|(g_{m8}r_{o8}r_{o10})$. Therefore, the transfer function of loop-2 is

$$T_2(s) = \frac{v_{ea}}{v_{i2}} \approx \frac{-A_2}{(1+\frac{s}{p_{\mathrm{EA}}})(1+\frac{s}{A_1A_{mp}p_{\mathrm{OUT}}})}. \tag{19}$$

The dominant pole is p_{EA} and the non-dominant pole is $A_1A_{mp}p_{\mathrm{OUT}}$. For a PM larger than 45°, the location of the nondominant pole is at a higher frequency than UGB, that is $A_1A_{mp}p_{\mathrm{OUT}} > A_2p_{\mathrm{EA}}$. Finally, we obtain $C_c > (g_{m1}C_L)/(g_{mp}A_1)$. The worst case happens in a light load condition when g_{mp} is very small. With light load, C_1, C_2, and C_3 are connected to V_{EA}, $C_c = C_1 + C_2 + C_3$, such that p_{EA} locates in a low enough frequency. When the load current increases, g_{mp} also increases, which is allowed for a smaller C_c. Therefore, in medium load, switch $\mathrm{S_1}$ turns off, $C_c = C_2 + C_3$. In heavy load, only $\mathrm{C_3}$ connects to V_{EA}, $\mathrm{C_c} = C_3$, with p_{EA} pushing to higher frequency, then leading to a larger UGB. As Fig. 11 shows, the UGB is effectively enhanced from 464 kHz in $I_{\mathrm{LOAD}} = 5\ \mu$A to 70 MHz in $I_{\mathrm{LOAD}} = 20$ mA by dynamic compensation. The capacitances of C_1, C_2, and C_3 are 2.25 pF, 180 fF and 23 fF, respectively, in this design. We used a 200 kΩ resistor R_1 for better PM in light load. Pushing loop-2's UGB to higher frequency, drastically improves the PSR, as presented in Fig. 12.

For the entire loop analysis, we break the signal path between v_a and the input of the ESSF buffer, similarly to the loop-1, but without isolating loop-2. Based on the above derivations, we get the transfer function of the entire loop

$$T(s) = \frac{v_a}{v_{i1}} \approx \frac{-A_1A_2A_{mp}(1+\frac{s}{A_2p_{\mathrm{EA}}})}{(1+\frac{s}{p_{\mathrm{EA}}})(1+\frac{s}{p_{\mathrm{OUT}}})(1+\frac{s}{p_G})}. \tag{20}$$

The left-half-plane zero $z_1 = A_2p_{EA}$, right at the UGB of loop-2, will improve the PM. For a frequency higher than A_2p_{EA}, v_{set} can be considered as 0, and the entire loop is only loop-1. As shown in Fig. 13, the entire loop is also stable at different load conditions. Besides, the maximum UGB reaches 436 MHz, which indicates a good PSR and an ultrafast response.

D. Current Sensor and Comparator

As mentioned earlier, two switches need to be turned ON and OFF according to load current conditions. Fig. 14 shows the schematic circuit of the current sensor and hysteresis comparator. The *W/L* ratio of the sensing transistor M_S and M_P is 1:2600, so $I_5 = I_3 = I_{\mathrm{LOAD}}$ / 2600, $I_6 = \mathrm{I_{LOAD}}$/10400. When $I_{\mathrm{LOAD}} = 0$, $I_5 < I_8 + I_9$, V_1 is high, so S_1 is 0. When I_{LOAD} increases to $I_5 > I_8 + I_9$, that is $I_{\mathrm{LOAD}} > 260\ \mu$A in this design, S_1 turns to 1. When I_{LOAD} decreases to $I_5 < I_8$, or $I_{\mathrm{LOAD}} < 130\ \mu$A, S_1 turns to 0. The hysteresis window is [130 μA, 260 μA]. For S_2, the hysteresis window is [3.6 mA, 5.2 mA].

IV. Measurement Results

We fabricated the proposed FVF LDO in 65 nm complementary metal oxide semiconductor (CMOS) with an active area of 0.053 mm^2, as illustrated in Fig. 15, including a 300 pF output capacitor implemented by stacked metal oxide semiconductor (MOS), metal-oxide-metal (MOM), and metal-insulator-metal (MIM) capacitors. We used an on-chip load and switch for

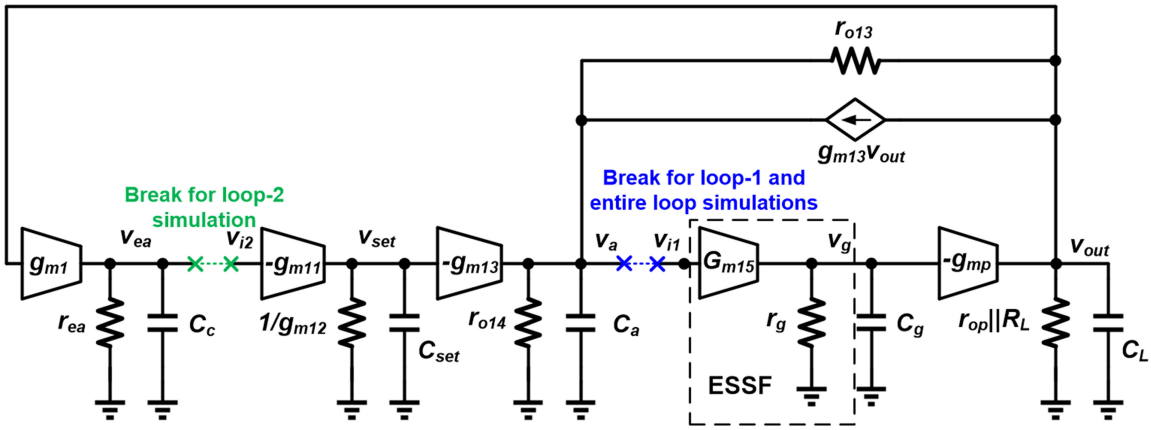

Fig. 9. Small-signal model for stability analysis.

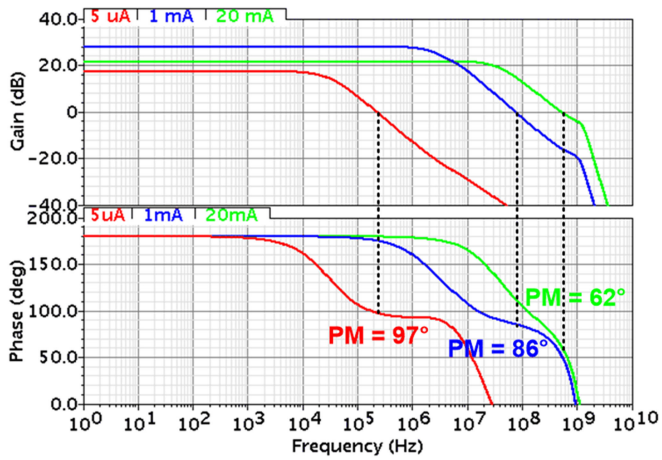

Fig. 10. Simulated Bode plot of loop-1 at different load conditions with $V_{\rm IN}$ = 1.2 V and $V_{\rm OUT}$ = 1 V.

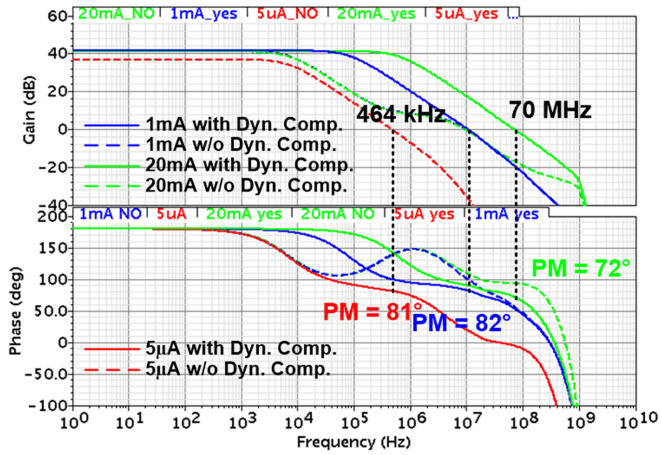

Fig. 11. Simulated Bode plot of loop-2 at different load conditions with $V_{\rm IN}$ = 1.2 V and $V_{\rm OUT}$ = 1 V.

ultrafast load transient response test. The measured quiescent current I_Q is 27 to 82 μA with the load current ranging from 5 μA to 20 mA.

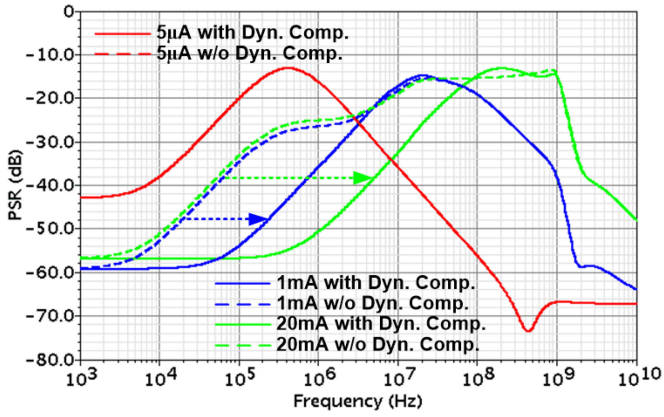

Fig. 12. Simulated PSR with and without dynamic compensation.

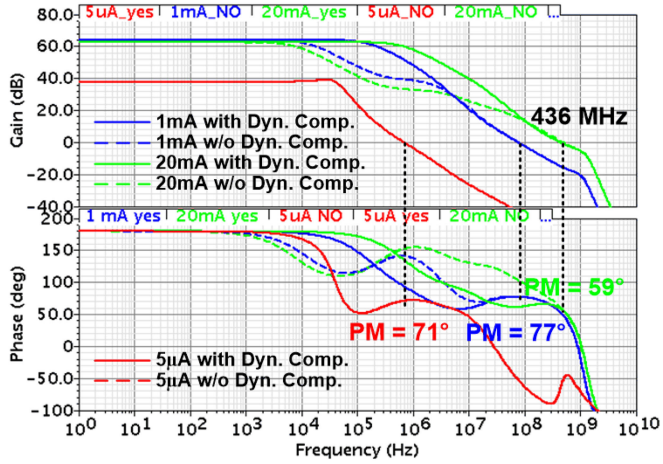

Fig. 13. Simulated Bode plot of entire loop at different load conditions with $V_{\rm IN}$ = 1.2 V and $V_{\rm OUT}$ = 1 V.

Fig. 16 presents the measured PSR from 1 kHz to 1 GHz in different load condition, with $V_{\rm IN}$ = 1.2 V and $V_{\rm OUT}$ = 1 V. The ripples applied to $V_{\rm IN}$ have a peak-to-peak amplitude of 50 mV. We measured the PSR from 1 kHz to 30 MHz with a Keysight E5061B Network Analyzer, and from 30 MHz to 1 GHz with a Keysight 6004 A Mixed Signal Oscilloscope. We can observe

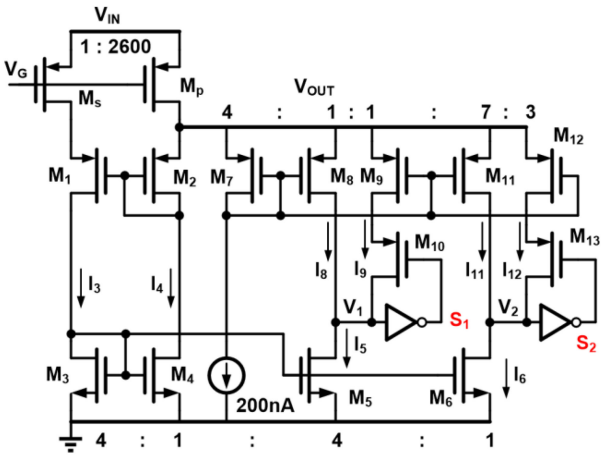

Fig. 14. Schematic circuit of the current sensor and hysteresis comparator.

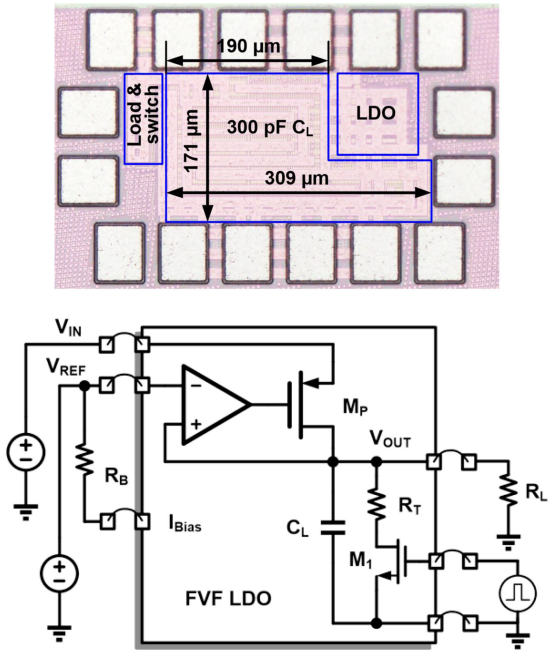

Fig. 15. Micrograph of the fabricated chip and measurement setup.

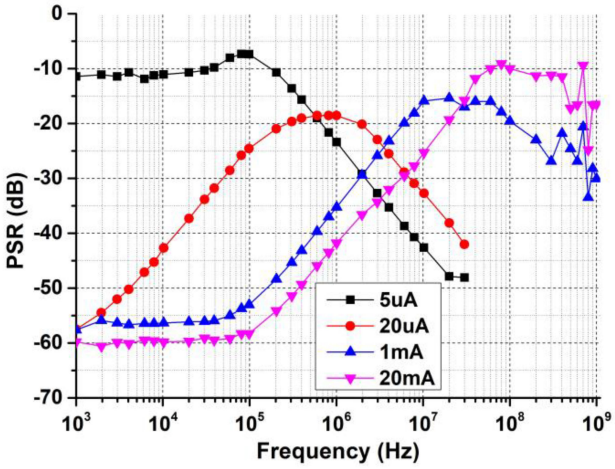

Fig. 16. Measured PSR at 5 μA, 20 μA , 1 mA, and 20 mA I_{LOAD}.

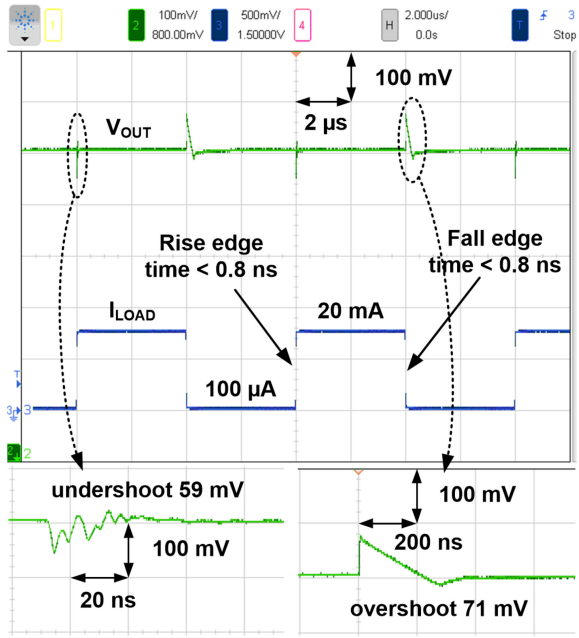

Fig. 17. Measured load transient response with $V_{\mathrm{IN}} = 1.2$ V and $V_{\mathrm{OUT}} = 1$ V.

that the proposed FVF LDO achieves full spectrum PSR in 5 μA, 20 μA, 1 mA, and 20 mA I_{LOAD}. The measured low frequency PSR at $I_{\mathrm{LOAD}} = 5$ μA deviates from the simulated result due to dc operating point shift of the FVF loop. When $I_{\mathrm{LOAD}} = 20$ μA, the PSR performances match well with the simulation results. For frequencies lower than 100 kHz, the PSR is better than -53 dB with $\mathrm{I_{LOAD}} = 1$ mA, and better than -58 dB with $I_{\mathrm{LOAD}} = 20$ mA, which demonstrates a significant enhancement when compared with [20].

Fig. 17 plots the measured load transient response when I_{LOAD} changes between 100 μA and 20 mA with a rise/fall edge time less than 0.8 ns. The measured undershoot and overshoot are 59 and 71 mV, respectively. The calculated response time T_R is 0.9 ns.

Table II summarizes the performance of the proposed FVF LDO and compares it with state-of-the-art works. The proposed work achieves a UGB over 400 MHz, which is three times higher than [21] and consumes less quiescent current. When compared with those LDOs with off-chip capacitors, this article reaches full spectrum PSR. The proposed loop-2, drastically improves the low frequency PSR when compared with [20]. In addition, the high frequency PSR is better than [21] and [24] because of the fast loop-1 with dominant pole located at V_{OUT}. Reference [17] exhibits an excellent PSR in the 1 MHz to 1 GHz range in this table, but has a relatively slow transient response, and it will consume a large quiescent current with its adaptive supply-ripple cancelation technique turned ON. We adopted two figure-of-merits (FOMs) to compare the transient performance. T_{edge} is the edge time of the load current. For fair comparison, we used $I_Q + I_{\mathrm{LOADMIN}}$ to calculate $\mathrm{FOM_1}$. We can conclude that this article achieves an excellent $\mathrm{FOM_1}$ (second only to [33]) and the best $\mathrm{FOM_2}$. In summary, the proposed FVF LDO exhibits an enhanced full-spectrum PSR and an ultrafast transient response simultaneously without large quiescent current and area.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ARTS

parameter		[13] JSSC 2010	[32] JSSC 2017	[16] JSSC 2018	[20] TCAS I 2015	[17] JSSC 2018	[21] TPEL 2018	[18] TPEL 2019	[33] TPEL 2020	This work
C_L		Off-chip				On-chip				
		4 μF	1 μF	4.7 μF	140 pF	240 pF	25 pF	400 pF	0-100 pF	**300 pF**
Technology(nm)		130	130	65	65	65	130	130	65	**65**
V_{OUT} **(V)**		1	1	1	1	1	0.8	1	0.8	**1**
Dropout (mV)		>150	100	200	150	200	200	200	150	**200**
I_Q **(μA)**		50	14-120	40	50-90	8-297.5	112	42-108	14	**27-82**
$I_{LOADMIN}$ **(μA)**		0	0	0	0	0	120	0	0	**5**
$I_{LOADMAX}$ **(mA)**		25	300	100	10	25	25	50	100	**20**
Load regulation (μV/mA)		48	6	10	1100	42	173	10	90	**15**
UGB(MHz)		1.65	0.6**	1**	15**	N/A	130.5	24.7	9.03	**>400**
PSR	**1 MHz**	-67 dB	-12 dB**	-70 dB	-22 dB**	-52 dB	-57 dB	-64 dB	-6 dB**	**-42 dB**
	10 MHz	-56 dB	-33 dB*	-62 dB	-17 dB**	-37 dB	-22 dB	-15 dB	-3 dB**	**-25 dB**
	100 MHz	N/A	-35 dB*	N/A	-24 dB**	-37 dB	-5 dB	N/A	N/A	**-10 dB**
	1 GHz	N/A	N/A	N/A	-15.5 dB**	-36 dB	N/A	N/A	N/A	**-16 dB**
ΔI_{LOAD} **(mA)**		25	300	99.9	10	24	24.88	50	100	**19.9**
ΔV_{OUT} **(mV)/**T_{edge} **(ns)**		15/10	56/1000	20/50	82/0.2	225/100	284/0.3	140/100	230/220	**59/0.8**
T_R **(ns)**		2400	611.1	940.9	1.15	15	0.2	15.0	10	**0.9**
FOM_1 **(ps)**		4800	28.5	376	5.74	4.8	1.86	12.6	1.4	**1.45**
Edge time ratio K		50	5000	250	1	500	1.5	500	1100	**4**
FOM_2 **(mV)**		1.50	13.07	2.00	0.41	37.50	3.97	58.80	35.42	**0.38**
Active area (mm²)		0.049	0.18	0.048	0.018	0.087	0.008	0.0046***	0.0105****	**0.053**

$FOM_1 = T_R \frac{I_Q + I_{LOADMIN}}{\Delta I_{LOAD}}$, $T_R = \sqrt{\frac{2C_L \Delta V_{OUT} T_{\text{edge}}}{\Delta I_{LOAD}}}$ $(T_R < T_{edge})$, $T_R = \frac{\Delta V_{OUT} C_L}{\Delta I_{LOAD}}$ $(T_R \gg T_{edge})$ [21], $FOM_2 = K \cdot \frac{\Delta V_{OUT} \times (I_Q + I_{LOADMIN})}{\Delta I_{LOAD}}$ [24].

*Simulated, ** estimated from figure, ***not include 400 pF C_L, ****not include 100 pF C_L.

V. CONCLUSION

In this article, we comprehensively studied the PSR performance of three types of FVF LDOs. Based on this, we proposed a novel FVF LDO with a fast loop-1 to maintain a full spectrum PSR and a slow loop-2 to enhance the low frequency PSR. The utilization of dynamic compensation pushed the UGB of loop-2 to higher frequency for achieving a better PSR in the range of tens of kHz to tens of MHz. In addition, the proposed FVF LDO reached an UGB over 400-MHz and 0.9-ns response time. As the FOM of this design scales with process, we expect that with a more advanced process, we will obtain a better performance. The proposed FVF LDO is a good candidate for noise-sensitive wideband circuits demanding high PSR and ultrafast transient response.

APPENDIX

Fig. 18 shows the schematics and small signal models of supersource follower (SSF) and ESSF, where C_1, C_2, and C_O are the equivalent capacitances at node V_1, V_2, and V_O; g_{mi} and r_{oi} are the transconductance and output impedance of transistor M_i, respectively; $r_o = r_{o3} \| r_{o4}$ for SSF, and $r_o = r_{o4} \| r_{o5}$ for ESSF.

A. Supersource Follower

For SSF, we have

$$g_{m1}(v_o - v_i) + \frac{v_o - v_1}{r_{o1}} = v_1 \left(\frac{1}{r_{o2}} + sC_1 \right) \tag{21}$$

$$g_{m1}(v_o - v_i) + \frac{v_o - v_1}{r_{o1}} + g_{m3} v_1 = -v_o \left(\frac{1}{r_o} + sC_o \right). \tag{22}$$

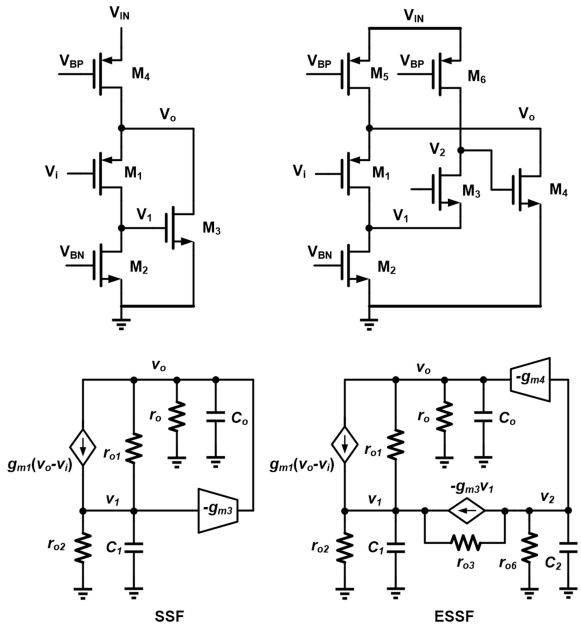

Fig. 18. Schematic circuit and small signal model of SSF and ESSF.

Assuming $g_{m3}(r_{o1} \| r_{o2}) >> 1$ and $g_{m1} r_{o1} >> 1$. By solving (21) and (22), we obtain the transfer function

$$\begin{aligned} T_{\text{SSF}}(s) &= \frac{v_o}{v_i} \\ &\approx \frac{(sC_1(r_{o1} \| r_{o2}) + \frac{r_{o1}}{r_{o1}+r_{o2}} + g_{m3}(r_{o1} \| r_{o2}))}{(1 + \frac{sC_o}{g_{m1}})(1 + sC_1(r_{o1} \| r_{o2})) + g_{m3}(r_{o1} \| r_{o2})} \\ &\approx \frac{(1 + \frac{s}{kp_1})}{(1 + \frac{s}{p_{ok}})(1 + \frac{s}{p_{1k}})} \end{aligned} \tag{23}$$

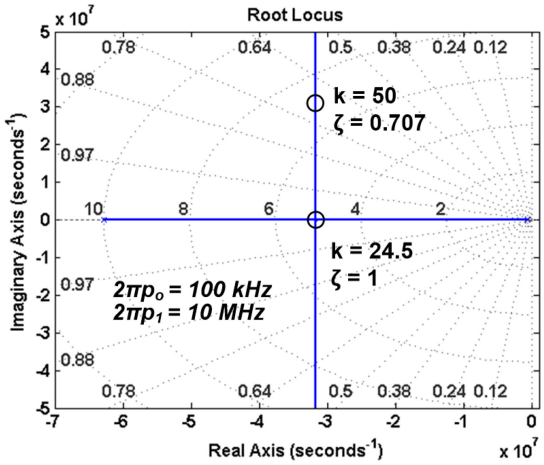

Fig. 19. Root locus of $T_{SSF}(s)$.

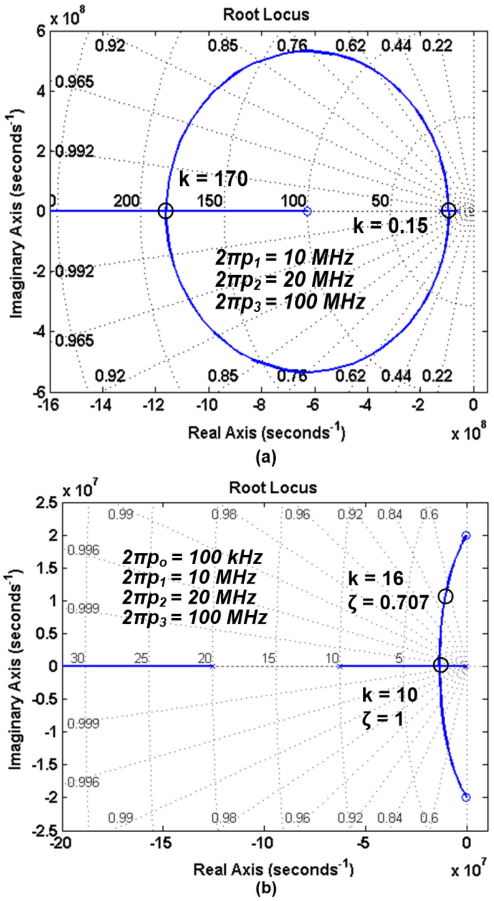

Fig. 20. Root locus of (a) z_{1k} and z_{2k} and (b) p_{ok}, p_{1k} and p_{2k}.

where $p_o = g_{m1}/C_o$, $p_1 = 1/C_1(r_{o1}\|r_{o2})$, $k = g_{m3}(r_{o1}\|r_{o2})$, p_{ok} and p_{1k} are the equivalent poles with respect to k. For a function $f(x) = (1 + x/p_o)(1 + x/p_1)$,we know that

$$f(x)_{\min} = f_1\left(-\frac{p_o + p_1}{2}\right) = -\frac{p_1^2 - 2p_op_1 + p_o^2}{4p_op_1} \approx -\frac{p_1}{4p_o} + \frac{1}{2}. \quad (24)$$

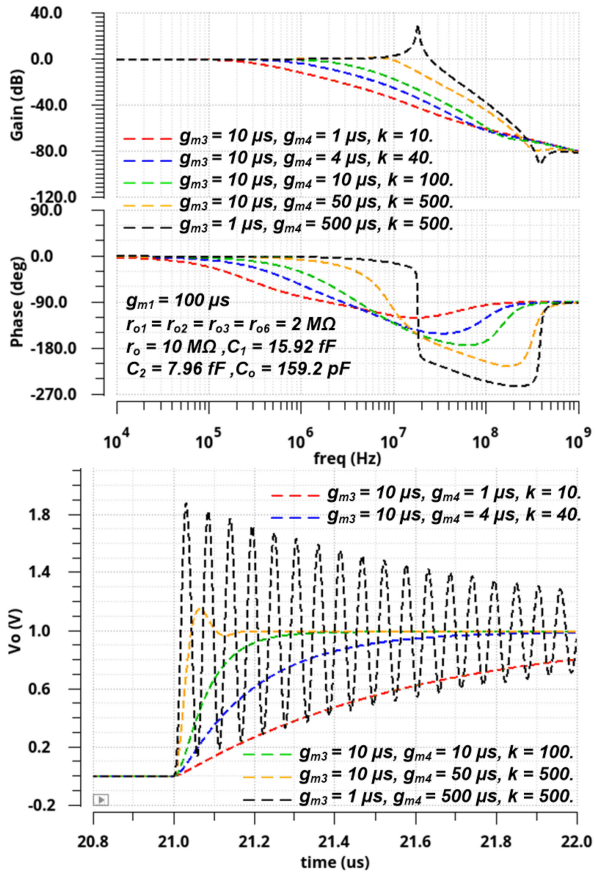

Fig. 21. Simulated Bode plot and transient response of ESSF.

We can see that as long as $k \le p_1/(4p_o) - 1/2$, the function $f(x) + k = 0$ will have two real roots, which mean that there are two real poles in $T_{\rm SSF}(s)$. In addition, the highest frequency p_o can be pushed to $p_{o\_\max} = (p_o + p_1)/2$, without creating complex poles. Fig. 19 shows the root locus of $T_{\rm SSF}(s)$ for given p_o and p_1.

B. Enhanced Supersource Follower

For ESSF, we can get the transfer function

$$T_{\rm ESSF}(s) = \frac{v_o}{v_i} \approx \frac{(1+\frac{s}{p_1})(1+\frac{s}{p_2}) + k(1+\frac{s}{p_3})}{(1+\frac{s}{p_o})(1+\frac{s}{p_1})(1+\frac{s}{p_2}) + k((1+\frac{s}{p_o})(1+\frac{s}{p_3}) - \frac{s}{p_o})} \quad (25)$$

$$\approx \frac{(1+\frac{s}{z_{1k}})(1+\frac{s}{z_{2k}})}{(1+\frac{s}{p_{ok}})(1+\frac{s}{p_{1k}})(1+\frac{s}{p_{2k}})}$$

where $p_o = g_{m1}/C_o$, $p_1 = 1/C_1(r_{o1}\|r_{o2})$, $p_2 = 1/C_2(r_{o3}\|r_{o6})$, $p_3 = g_{m4}/C_2$, $k = g_{m3}g_{m4}(r_{o1}\|r_{o2})(r_{o3}\|r_{o6})$, z_{1k}, z_{2k}, p_{ok}, p_{1k}, and p_{2k} are the equivalent zeros and poles with respect to k. Fig. 20 shows the root locus of these zeros and poles with given p_o, p_1, p_2, and p_3. We can see that in this condition, when $k < 0.15$ (which is not practical) or $k > 170$, z_{1k} and z_{2k} are two real zeros; and for $0.15 < k < 170$, z_{1k} and z_{2k} are a pair of complex zeros. For the poles, when $k < 10$, there are three real poles; otherwise there are a pair of complex poles

and a real pole. Theoretically, the system is stable with infinite k because all poles are in the left-half plane. However, when $g_{m4}(r_{o3}\|r_{o6}) >> g_{m3}(r_{o1}\|r_{o2})$, a few assumptions during the calculation are no longer valid, the complex-pole pair might enter the right-half plane, leading to instability. Therefore, we suggest to keep $g_{m4}(r_{o3}\|r_{o6})/g_{m3}(r_{o1}\|r_{o2})$ within a proper range when designing a large k. Fig. 21 displays the simulated Bode plot and transient response of ESSF based on the small signal model in Fig. 18 with ideal devices. We can see that when $k = 500$, ESSF is still stable with a pair of complex poles. But, if $g_{m4}(r_{o3}\|r_{o6})/g_{m3}(r_{o1}\|r_{o2}) = 500$, it is nearly unstable.

C. Comparison With SSF

For the same p_o and p_1, the $p_{o\_\max}$ in ESSF is lower than that in SSF. However, $p_1 = 1/C_1(r_{o1}\|r_{o2})$ dominates $p_{o\_\max}$, then, a small $r_{o1}\|r_{o2}$ is desirable for a high frequency p_1. As $k = g_{m3}(r_{o1}\|r_{o2})$ in SSF, to achieve to large enough k, we have to increase g_{m3}, which will consume additional power. For ESSF, $k = g_{m3}g_{m4}(r_{o1}\|r_{o2})(r_{o3}\|r_{o6})$, it is easier to get a large k with smaller g_{m3} and g_{m4}, therefore, higher power efficiency.

In conclusion, ESSF can push effectively and efficiently its p_o to a higher frequency.

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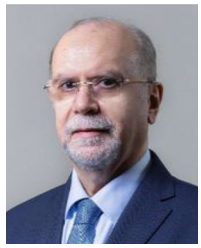

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