Letters

A Digital Control Strategy With Simple Transfer Matrix for Three-Phase Buck Rectifier Under Unbalanced AC Input Conditions

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***Abstract*—In this letter, a digital control strategy with a simple transfer matrix between three-phase ac input voltages and dc-link voltage is proposed for a three-phase buck rectifier (3ph-BR) under unbalanced ac input conditions. The proposed digital control strategy can eliminate both the odd harmonics of the ac input currents and the even harmonics of the output voltage ripple under unbalanced ac input conditions. Compared with the state-of-the-art control strategies, the proposed control strategy does not require the extraction of the positive sequence voltage and the negative sequence voltage, thus a three-phase lock loop and complex calculation are not required. The proposed control strategy is essentially an input voltage feedforward control, which is independent of the loop bandwidth of the feedback system. Therefore, the processing speed of the digital processor is no longer the critical factor for the 3ph-BR under the unbalanced ac input conditions. The proposed control strategy makes it possible to utilize low-cost and small-sized digital processors. An experimental prototype of a 1.5-kW 3ph-BR with the proposed control strategy is built to verify the analysis results.**

***Index Terms*—Digital control, three-phase buck rectifier (3ph-BR), unbalanced ac input conditions.**

I. Introduction

THREE-PHASE rectifiers are widely used in data center and communication center, aviation power supply, and other fields due to their desirable features, such as unity power factor, constant dc bus voltage, and sinusoidal input currents [1]. Compared with three-phase boost rectifier, the three-phase buck rectifier (3ph-BR) not only has wide output voltage range down to low voltage, but also has small start-up current and ability of short-circuit current limiting. Therefore, the 3ph-BR has a wide range of application prospects and is worthy of an in-depth study [2], [3].

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In practical applications, the three-phase input voltages are often under unbalanced conditions, which will deteriorate the performance of three-phase rectifiers due to the odd harmonics of the input currents and the even harmonics of the output voltage ripple [4]–[8]. To improve the performance of three-phase boost rectifiers under unbalanced ac input conditions, various control strategies have been proposed [4], [5]. Most of these control strategies require a three-phase lock loop (PLL) and multiple rotates coordinate transformations. As a result, they require much computation resources, which will affect dynamic response. In addition, whether these control strategies can be applied to the 3ph-BR still needs further study.

Some research works have been reported to improve the performance of the 3ph-BR under unbalanced three-phase ac input conditions [6]–[8]. The transfer matrix between the three-phase ac input voltages and the dc-link voltage was derived in [6], which can eliminate the even harmonics of the output voltage ripples and the odd harmonics of the input currents. Therefore, the 3ph-BR can preserve well-sinusoidal input currents and constant output voltage under unbalanced ac input conditions. However, it requires the computation of the positive and the negative sequence components of the input voltages. Thus, it needs PLL and complex calculations.

A multiloop digital control structure for the 3ph-BR with integrated boost output stage was proposed in [7] and [8]. An outer voltage loop is used to regulate the output voltage and to set the reference for the inner current loop. A complex current-shaping algorithm is designed to ensure sinusoidal mains phase currents and unity power factor under unbalanced ac input conditions. However, the cascaded multiple control loops increase the calculation burden. Besides, the inner current loop needs to be fast to suppress the power fluctuation under unbalanced three-phase ac input conditions, which means the digital processor needs to have fast calculation speed.

In this letter, a simple digital control strategy is proposed to reduce the computing burden for the 3ph-BR under unbalanced three-phase ac input conditions. According to the relationship between the three-phase ac input voltages and the dc-link voltage of the 3ph-BR, a simple transfer matrix is derived directly from the sampled input voltages, which can effectively suppress the even harmonics of the output voltage ripple and the odd harmonics of the input currents. Furthermore, space vector pulsewidth modulation (SVPWM) strategy implantation is discussed in terms of sector identification, switching pattern, and vector selection.

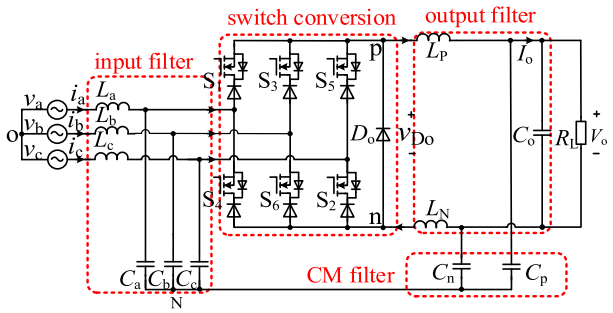

Fig. 1. 3ph-BR with CM filter.

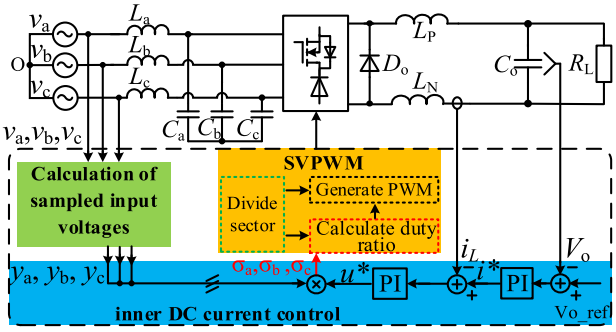

Fig. 2. Proposed control structure for the 3ph-BR under unbalanced ac input conditions.

Different from the state-of-the-art digital control strategies for the 3ph-BR under unbalanced ac input conditions, the proposed control strategy does not require the extraction of the positive sequence voltage and the negative sequence voltage. Thus, it does not need complex calculations. Besides, as the proposed control system does not need a fast response to deal with input unbalance, the processing speed of the digital processor is no longer the critical factor for the 3ph-BR under unbalanced ac input conditions. Therefore, the proposed control strategy significantly simplifies the control scheme and makes it possible to utilize low-cost digital processors. The control strategy proposed in this letter is suitable for the application where there are strict requirements for the cost and volume of a three-phase rectifier.

II. Digital Control Strategy for 3ph-BR Under Unbalanced AC Input Conditions

Fig. 1 shows circuit of the 3ph-BR with common mode (CM) filter [9]. It consists of an input filter unit, switch conversion unit, CM filter unit, and output filter unit. The purpose of the CM filter is to suppress the propagation of high frequency CM noise to the input by providing low impedance paths around the rectifier elements, so that high frequency CM noise is circulated back internally. Therefore, the CM filter can effectively suppress the interference of high frequency noise to the sampling of the input voltage.

A. Proposed Digital Control Structure for 3ph-BR

Fig. 2 shows the proposed control structure for the 3ph-BR under unbalanced ac input conditions. It can be seen from Fig. 2 that the control system is composed of the inner dc current control [10]–[13], the SVPWM strategy [14], [15], and the calculation of sampled voltages.

The inner dc current control consists of an outer voltage loop and an inner control loop. The control strategy only needs to sample input voltages v_a, v_b, and v_c, output voltage V_o, and dc-link current i_L. It does not need to sample input currents, which makes the control system simple.

The inner dc current control does not directly control the three-phase input currents, but restructures the three-phase input currents from the dc-link current i_L by SVPWM strategy. According to the principle of SVPWM strategy, the six bridge legs distribute the dc-link current among the three phases by pulsewidth modulation at a fixed switching frequency. The product of $u*$ and y_a, y_b, and y_c provides three-phase current references σ_a, σ_b, and σ_c for SVPWM strategy, which can realize sinusoidal input currents and ensure the input currents are in phase with the input voltages.

B. Derivation and Implementation of Transfer Matrix

The unbalanced three-phase input voltages can be defined as

$$\boldsymbol{v}_i = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_a\cos(\omega t+\theta_a) \\ V_b\cos(\omega t+\theta_b) \\ V_c\cos(\omega t+\theta_c) \end{bmatrix} \tag{1}$$

where v_a, v_b, and v_c are the three-phase ac input voltages, V_a, V_b, and V_c are their corresponding amplitudes, and θ_a, θ_b, and θ_c are their corresponding phase angles.

For the three-phase three-wire system without neutral line, the unbalanced three-phase input voltages can be decomposed into three-phase symmetrical positive sequence voltages $\boldsymbol{v_p}$ and negative sequence voltages $\boldsymbol{v_n}$ as

$$\boldsymbol{v}_i = \boldsymbol{v}_p + \boldsymbol{v}_n \tag{2}$$

with the positive sequence voltage $\boldsymbol{v_p}$ and the negative sequence voltage $\boldsymbol{v_n}$ are

$$\boldsymbol{v}_p = \frac{1}{3}\begin{bmatrix} V_a\cos(\omega t+\theta_a)+V_b\cos\left(\omega t+\theta_b-\frac{2\pi}{3}\right) \\ +V_c\cos\left(\omega t+\theta_c+\frac{2\pi}{3}\right) \\ V_a\cos\left(\omega t+\theta_a+\frac{2\pi}{3}\right)+V_b\cos(\omega t+\theta_b) \\ +V_c\cos\left(\omega t+\theta_c-\frac{2\pi}{3}\right) \\ V_a\cos\left(\omega t+\theta_a-\frac{2\pi}{3}\right)+V_b\cos\left(\omega t+\theta_b+\frac{2\pi}{3}\right) \\ +V_c\cos(\omega t+\theta_c) \end{bmatrix} \tag{3}$$

$$\boldsymbol{v}_n = \frac{1}{3}\begin{bmatrix} V_a\cos(\omega t+\theta_a)+V_b\cos\left(\omega t+\theta_b+\frac{2\pi}{3}\right) \\ +V_c\cos\left(\omega t+\theta_c-\frac{2\pi}{3}\right) \\ V_a\cos\left(\omega t+\theta_a-\frac{2\pi}{3}\right)+V_b\cos(\omega t+\theta_b) \\ +V_c\cos\left(\omega t+\theta_c+\frac{2\pi}{3}\right) \\ V_a\cos\left(\omega t+\theta_a+\frac{2\pi}{3}\right)+V_b\cos\left(\omega t+\theta_b-\frac{2\pi}{3}\right) \\ +V_c\cos(\omega t+\theta_c) \end{bmatrix}. \tag{4}$$

The transfer matrix between the three-phase ac input voltages and the dc-link voltage of the 3ph-BR is defined as σ; thus, it has

$$v_{Do} = \boldsymbol{\sigma}\boldsymbol{v}_i. \tag{5}$$

The transfer matrix σ can be decomposed into the positive sequence component and the negative sequence component as

$$\boldsymbol{\sigma} = \boldsymbol{\sigma}_{\mathrm{p}} + \boldsymbol{\sigma}_{\mathrm{n}}. \tag{6}$$

By substituting (2) and (6) into (5), it has

$$v_{\mathrm{Do}} = \boldsymbol{\sigma}_{\mathrm{p}}\boldsymbol{v}_{\mathrm{p}} + \boldsymbol{\sigma}_{\mathrm{n}}\boldsymbol{v}_{\mathrm{n}} + \boldsymbol{\sigma}_{\mathrm{p}}\boldsymbol{v}_{\mathrm{n}} + \boldsymbol{\sigma}_{\mathrm{n}}\boldsymbol{v}_{\mathrm{p}}. \tag{7}$$

The first two terms in (7) produce the dc components, and the last two terms in (7) produce the harmonic components.

From (7), it can be known that the harmonic terms can be eliminated when

$$\begin{cases} \boldsymbol{\sigma}_{\mathrm{p}} = k_{\mathrm{m}}\boldsymbol{v}_{\mathrm{p}}^{\mathrm{T}} \\ \boldsymbol{\sigma}_{\mathrm{n}} = -k_{\mathrm{m}}\boldsymbol{v}_{\mathrm{n}}^{\mathrm{T}} \end{cases} \tag{8}$$

where k_{m} is the ratio coefficient.

From (6) and (8), the transfer matrix σ of the 3ph-BR can be expressed as

$$\boldsymbol{\sigma} = k_m\boldsymbol{v}_{\mathrm{p}}^{\mathrm{T}} - k_m\boldsymbol{v}_{\mathrm{n}}^{\mathrm{T}}. \tag{9}$$

By substituting (3) and (4) into (9), the transfer matrix σ is

$$\boldsymbol{\sigma} = \frac{k_m}{3}\begin{bmatrix} -V_{\mathrm{b}}\sin(\omega t+\theta_{\mathrm{b}}) + V_{\mathrm{c}}\sin(\omega t+\theta_{\mathrm{c}}) \\ V_{\mathrm{a}}\sin(\omega t+\theta_{\mathrm{a}}) - V_{\mathrm{c}}\sin(\omega t+\theta_{\mathrm{c}}) \\ -V_{\mathrm{a}}\sin(\omega t+\theta_{\mathrm{a}}) + V_{\mathrm{b}}\sin(\omega t+\theta_{\mathrm{b}}) \end{bmatrix}. \tag{10}$$

By the trigonometric transformation, it can have

$$\boldsymbol{\sigma} = \frac{k_m}{3\omega}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} V_{\mathrm{b}}\cos(\omega t+\theta_{\mathrm{b}}) - V_{\mathrm{c}}\cos(\omega t+\theta_{\mathrm{c}}) \\ -V_{\mathrm{a}}\cos(\omega t+\theta_{\mathrm{a}}) + V_{\mathrm{c}}\cos(\omega t+\theta_{\mathrm{c}}) \\ V_{\mathrm{a}}\cos(\omega t+\theta_{\mathrm{a}}) - V_{\mathrm{b}}\cos(\omega t+\theta_{\mathrm{b}}) \end{bmatrix}. \tag{11}$$

In the digital sampling system, when the sampling frequency is much higher than the ac input frequency, the derivative of the ac input voltage can be defined as

$$\frac{\mathrm{d}v_i(t)}{\mathrm{d}t} = \frac{v_i(n) - v_i(n-1)}{T_c} \tag{12}$$

where $v_{\mathrm{i}}(n)$ and v_{i} $(n-1)$ are the sampled input voltages in two adjacent sampling periods and $i = a$, b, and c. T_{c} is the sampling period.

According to (12), the proposed transfer matrix σ is obtained as

$$\boldsymbol{\sigma} = \frac{k_m}{3T_{\mathrm{c}}\omega}\begin{bmatrix} v_{\mathrm{b}}(n) - v_{\mathrm{b}}(n-1) - (v_{\mathrm{c}}(n) - v_{\mathrm{c}}(n-1)) \\ -(v_{\mathrm{a}}(n) - v_{\mathrm{a}}(n-1)) + (v_{\mathrm{c}}(n) - v_{\mathrm{c}}(n-1)) \\ v_{\mathrm{a}}(n) - v_{\mathrm{a}}(n-1) - (v_{\mathrm{b}}(n) - v_{\mathrm{b}}(n-1)) \end{bmatrix}. \tag{13}$$

For the sake of convenience, define $[y_{\mathrm{a}}, y_{\mathrm{b}}, y_{\mathrm{c}}]^{\mathrm{T}}$ as

$$\begin{bmatrix} y_{\mathrm{a}} \\ y_{\mathrm{b}} \\ y_{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{b}}(n) - v_{\mathrm{b}}(n-1) - (v_{\mathrm{c}}(n) - v_{\mathrm{c}}(n-1)) \\ -(v_{\mathrm{a}}(n) - v_{\mathrm{a}}(n-1)) + (v_{\mathrm{c}}(n) - v_{\mathrm{c}}(n-1)) \\ v_{\mathrm{a}}(n) - v_{\mathrm{a}}(n-1) - (v_{\mathrm{b}}(n) - v_{\mathrm{b}}(n-1)) \end{bmatrix}. \tag{14}$$

Then the transfer matrix σ can be given as

$$\boldsymbol{\sigma} = \begin{bmatrix} \boldsymbol{\sigma}_{\mathrm{a}} \\ \boldsymbol{\sigma}_{\mathrm{b}} \\ \boldsymbol{\sigma}_{\mathrm{c}} \end{bmatrix} = \frac{k_m}{3T_{\mathrm{c}}\omega}\begin{bmatrix} y_{\mathrm{a}} \\ y_{\mathrm{b}} \\ y_{\mathrm{c}} \end{bmatrix}. \tag{15}$$

In (15), $k_{\mathrm{m}}/3T_{\mathrm{c}}\omega$ is determined by the output of the inner current loop $u*$, which is approximately constant when the system parameters are determined. Thus, the transfer matrix is mainly determined by $[y_{\mathrm{a}}, y_{\mathrm{b}}, y_{\mathrm{c}}]^{\mathrm{T}}$.

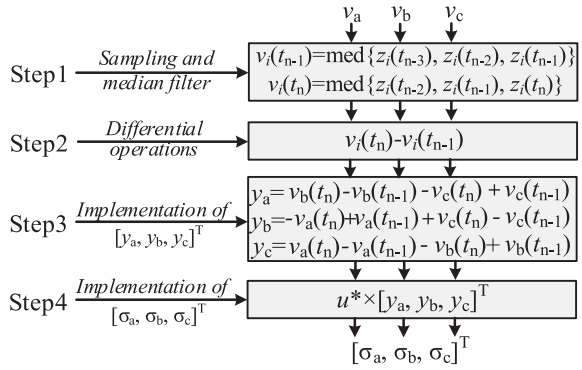

Fig. 3. Practical implementation of transfer matrix σ.

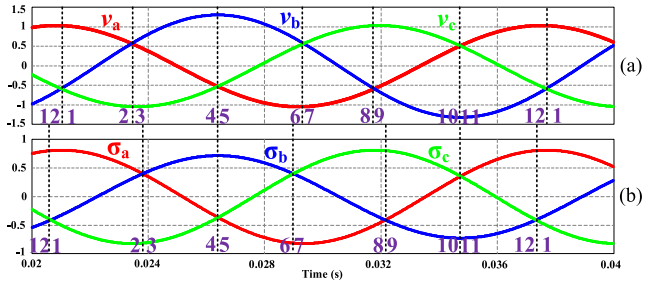

Fig. 4. Simulation result under unbalanced ac input conditions. (a) Three-phase input voltages with 12 sectors. (b) Proposed transfer matrix with 12 sectors.

The calculation process of $[\sigma_{\mathrm{a}}, \sigma_{\mathrm{b}}, \sigma_{\mathrm{c}}]^{\mathrm{T}}$ can be summarized as shown in Fig. 3. In step 1, the input voltages are sampled and stored in an array with three elements, i.e., $[z_i(t_{\mathrm{n-2}}), z_i(t_{\mathrm{n-1}}), z_i(t_{\mathrm{n}})]$, and then the input voltage is processed by median filtering. In each control cycle, three sampled input voltages in each array are compared and the median voltage is obtained as the input voltage in the current control cycle. In step 2, the differential operation is realized by subtracting filtered input voltage in two adjacent control cycles. In step 3 and 4, only (14) and (15) need to be executed, respectively.

C. Implementation of SVPWM Strategy

In this letter, the switching loss optimized (SLO) SVPWM modulation strategy for the 3ph-BR [14], [15] is adopted. In this section, the implantation of the SLO modulation for the proposed control strategy is discussed in terms of switching patterns, sector identification, and vector selection.

Fig. 4 shows the simulation result of three-phase input voltages and the proposed transfer matrix when the three-phase input voltages are unbalanced. When three-phase input voltages are unbalanced, although the waveforms of σ_{a}, σ_{b}, and σ_{c} are well-sinusoidal, they are not balanced. Moreover, the amplitude of σ_{b} is obviously smaller than that of σ_{a} and σ_{c}. Therefore, the input current i_{b} is smaller than input currents i_{a} and i_{c}, which means that smaller currents should be delivered from the phase with higher voltage. In other words, the proposed transfer matrix can suppress the fluctuation of instantaneous input power under unbalanced ac input conditions, so as to obtain the sinusoidal input current and the constant output voltage.

In conventional SLO modulation, one ac input period is divided into 12 sectors according to the magnitude of three-phase

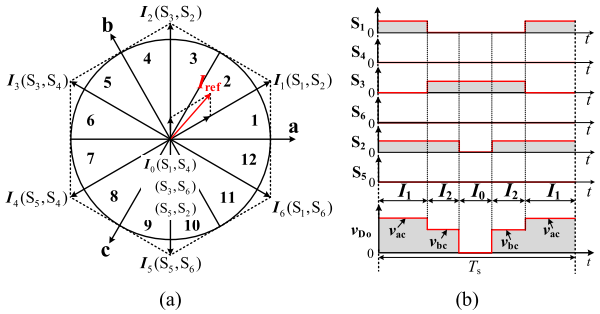

Fig. 5. Current space distribution and switching patterns for SLO modulation. (a) Current space distribution with 12 sectors. (b) Switching patterns and corresponding current vectors in one switching period in sector 2.

TABLE I
DUTY RATIO OF EACH BRIDGE LEG IN ONE SWITCHING PERIOD

Sector	δ_{S1}	δ_{S4}	δ_{S3}	δ_{S6}	δ_{S5}	δ_{S2}
12, 1	σ_a	0	0	$-\sigma_b$	0	$-\sigma_c$
2, 3	σ_a	0	σ_b	0	0	$-\sigma_c$
4, 5	0	$-\sigma_a$	σ_b	0	0	$-\sigma_c$
6, 7	0	$-\sigma_a$	σ_b	0	σ_c	0
8, 9	0	$-\sigma_a$	0	$-\sigma_b$	σ_c	0
10, 11	σ_a	0	0	$-\sigma_b$	σ_c	0

input voltages, as shown in Fig. 4(a). However, in the proposed control strategy, the calculated $[\sigma_a, \sigma_b, \sigma_c]^T$ provides a new three-phase current references for SLO strategy. Therefore, the sectors should be identified based on the magnitude of σ_a, σ_b, and σ_c, as shown in Fig. 4(b). Besides, from Fig. 4(a) and (b), it can be known that the results of these two sector identification methods are obviously different under unbalanced ac input conditions. Furthermore, the sinusoidal input currents can only be ensured by dividing sectors based on the amplitude of σ_a, σ_b, and σ_c.

The implementation of switching patterns and vector selection of conventional SLO modulation can still be used in the proposed control strategy. Fig. 5(a) shows the current vectors and sectors distribution, in which the current vector includes three zero vectors $\boldsymbol{I}_0$ and six active vectors $\boldsymbol{I}_1$–$\boldsymbol{I}_6$. Take active current vector $\boldsymbol{I}_1$ as an example, $\boldsymbol{I}_1$ represents that the bridge legs S_1 and S_2 are turned ON, while the other bridges and the freewheeling diode D_o are turned OFF. Besides, the zero vector $\boldsymbol{I}_0$ is usually realized by the conduction of freewheeling diode D_o to reduce the devices' conduction loss. Normally, two current vectors adjacent to the reference vector $\boldsymbol{I}_{ref}$ are used to obtain the averaged current vector to make it equal to the reference vector.

Fig. 5(b) shows the switching patterns and corresponding current vectors in one switching period in sector 2. For the SLO modulation, there are four current commutations in each sector, and the current vectors are arranged so that the switching devices withstand smaller input line-to-line voltage at the instant of the current commutations [15]. The duty ratio of each bridge leg in one switching period can be calculated, as given in Table I. In Table I, δ_{Si} ($i = 1$–6) is the duty ratio of each bridge leg in one switching period.

In addition, the high frequency noise in the 3ph-BR mainly comes from the switching action of the switch device. In order to avoid the switching noise of the bridge legs interfering with the sampling of input voltage, the input voltage sampling should

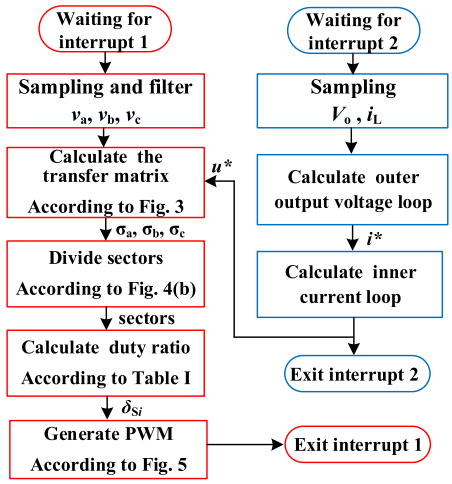

Fig. 6. Flowchart for the proposed digital control strategy.

TABLE II
INSTRUCTION CYCLES FOR THE DIFFERENT OPERATIONS

Operation	Instruction cycle	Operation	Instruction cycle
Addition/Subtraction	4	Square-Root	580
Multiplication	13	Trigonometric calculation	2994
Division	31		

be carried out during the conduction of the freewheeling diode D_o in each switching cycle.

D. Digital Implementation of the Proposed Control Strategy

The conventional control strategies usually require high control loop bandwidth to effectively control the 3ph-BR under the input unbalance conditions. However, the proposed control strategy is essentially an input voltage feedforward control, which is independent of the loop bandwidth of the feedback system. It means that even in the open-loop situation, the impact of three-phase input unbalance can be suppressed effectively. The proposed digital control strategy shown in Fig. 6 is divided into two different control interrupts, i.e., interrupts 1 and 2.

Interrupt 1 includes sampling of input voltage, calculation of transfer matrix and SVPWM strategy, which are placed in an interrupt with the highest priority. As interrupt 1 is simple to calculate, the control frequency of interrupt 1 can be set high. In this letter, the control frequency is set to 100 kHz.

Interrupt 2 realizes the digital PI control of outer voltage loop and inner current loop. As the proposed control system does not need a fast response to deal with input unbalance, interrupt 2 can be placed with lower priority and control frequency of interrupt 2 can be set as 1 kHz. Besides, the detailed design for the inner current loop and the outer voltage loop has been presented based on a simplified small-signal model in [7].

E. Comparison With the State-of-the-Art Digital Control Strategies

In this letter, a low-cost and small-sized digital processor, i.e., dsPIC33EP64GS805 is utilized. The instruction cycles of

TABLE III
PERFORMANCE COMPARISON AMONG DIFFERENT DIGITAL CONTROL STRATEGIES FOR 3ph-BR UNDER UNBALANCED AC INPUT CONDITIONS

	Ref. [6]	Ref. [7] and [8]	This paper
PF	High	High	High
Input current THD	Low	Low	Low
Output voltage ripple	Low	High	Low
Algorithms for unbalance input voltages	Positive / negative sequence component calculation	DC current-shaping control	The proposed transfer matrix
key operations	"Trigonometric calculation", "Multiplication", "Square-Root", "Addition/Subtraction"	one "Square-Root", two "Division", nine "Multiplication", and four "Addition/Subtraction"	three "Multiplication", nine "Addition/Subtraction"
Instruction cycles	Several ten thousand	775	75

various operations are measured and given in Table II. The performance comparison among different digital control strategies for the 3ph-BR under unbalanced ac input conditions is given in Table III.

The SVPWM modulation and the control strategy with outer voltage loop and inner current loop in [6]–[8] is the same as that of the proposed control strategy in this letter. Therefore, the execution times of these algorithms are approximately the same. However, the algorithms for the three-phase input unbalance in different control strategy are different. Table III summarizes the main operations and instruction cycles of the corresponding algorithms.

The control strategy in [6] can achieve lower output voltage ripple and lower input current THD. However, its algorithm for the three-phase input unbalance needs the separation of positive and negative sequence voltage, thus it requires a lot of trigonometric operations and square-root operations, which is difficult to implement by using the simple digital controller adopted in this letter.

The control strategy in [7] and [8] can ensure that the input currents are sinusoidal and proportional to the input voltages. However, due to the time-varying of dc-link current and the relatively small output capacitor, the output voltage is not constant. Besides, it can be obtained from Tables IIandIII and that the algorithm in [7] and [8] needs about 775 instruction cycles, while the proposed control strategy needs only 75 instruction cycles. Compared with [7] and [8], the proposed control strategy in this letter not only has low computational burden but also has small output voltage ripple.

TABLE IV
CIRCUIT PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Quantity	Symbol	Value
Unbalanced input voltage	v_a, v_b, v_c	$115V_{rms}$, $125V_{rms}$, $115V_{rms}$
Unbalanced phase angle	θ_a, θ_b, θ_c	0°, 125°, 240°
Ac input frequency	f_L	60Hz
Output voltage	V_o	200V
Output power	P_o	1.5kW
Switching frequency	f_s	200kHz
Input filter inductor	L_a, L_b, L_c	50μH
Input filter capacitor	C_a, C_b,C_c	2μF
Output inductor	L_P, L_N	300μH
Output capacitor	C_o	100μF
CM capacitor	C_p, C_n	0.47μF
MOSFET	—	STD18N55M5
Diode	—	STPSC8H065BY-TR

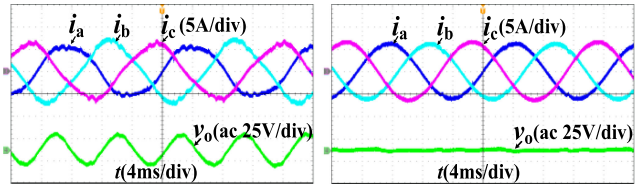

Fig. 7. Experimental results of three-phase ac input currents i_a, i_b, and i_c and output voltage ripple v_o under unbalanced ac input conditions. (a) Without the proposed control strategy. (b) With the proposed control strategy.

III. IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

A. Implementation of the Experimental Prototype

Experimental prototype of a 3ph-BR is developed to verify the analysis results of the proposed digital control strategy. The main circuit parameters of the experimental prototype are given in Table IV.

B. Experimental Results

Fig. 7(a) and (b) shows the experimental results of three-phase ac input currents i_a, i_b, and i_c and output voltage ripple v_o under unbalanced ac input conditions with and without the proposed control strategy. Fig. 7(a) shows the experimental results without the proposed control strategy. It can be seen from Fig. 7(a) that the three-phase input currents have obvious distortion, and the output voltage ripple is about 30 V.

The frequency of the output voltage ripple is twice the frequency of the ac input voltage. Fig. 7(b) shows the experimental results with the proposed control strategy. It can be obtained from Fig. 7(b) that the three-phase input currents are low-distortion sinusoidal currents, and the output voltage has no obvious low frequency ripple.

Fig. 8 shows experimental results of three-phase ac input currents i_a, i_b, and i_c and output voltage ripple v_o under unbalanced ac input conditions with the control strategy in [7] and [8]. It can be seen from Fig. 8 that the three-phase input currents are sinusoidal waveshapes under unbalanced ac input conditions. However, it has obvious double-line frequency output voltage ripple.

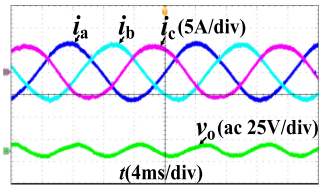

Fig. 8. Experimental results of three-phase ac input currents i_a, i_b, and i_c and output voltage ripple v_o under unbalanced ac input conditions with the control strategy in [7] and [8].

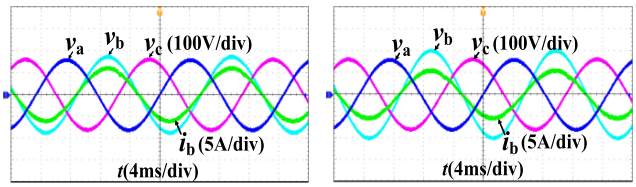

Fig. 9. Experimental results of three-phase ac input voltages i_a, i_b, and i_c and ac input current i_b with the proposed control strategy under different unbalanced ac input voltages when $\theta_a = 0°$, $\theta_b = 125°$, and $\theta_c = 240°$. (a) When $v_a = 115V_{rms}$, $v_b = 125V_{rms}$, and $v_c = 115V_{rms}$. (b) When $v_a = 115V_{rms}$, $v_b = 145V_{rms}$, and $v_c = 115V_{rms}$.

TABLE V
TEST RESULTS OF PF, INPUT CURRENT THD, AND THEIR HARMONIC CONTENTS UNDER UNBALANCED AC INPUT CONDITIONS WITHOUT AND WITH THE PROPOSED CONTROL STRATEGY

	phase	3th	5th	7th	9th	THD	PF
Without proposed control strategy	A	9.215	1.360	1.103	0.888	9.94	0.978
	B	7.839	1.100	1.806	1.498	9.07	0.981
	C	7.976	0.738	0.606	0.527	8.28	0.983
With proposed control strategy	A	0.417	0.770	0.409	0.158	1.77	0.996
	B	0.181	0.551	0.528	0.382	1.51	0.996
	C	0.267	0.186	0.232	0.216	1.03	0.998

Fig. 9 shows experimental results of ac input voltages v_a, v_b, and v_c and ac input current i_b with the proposed control strategy under different unbalanced ac input voltages when $\theta_a = 0°$, $\theta_b = 125°$, and $\theta_c = 240°$. Fig. 9(a) shows experimental results when $v_a = 115V_{rms}$, $v_b = 125V_{rms}$, and $v_c = 115V_{rms}$. Fig. 9(b) shows experimental results when $v_a = 115V_{rms}$, $v_b = 145V_{rms}$, and $v_c = 115V_{rms}$. It can be seen from Fig. 9(a) and (b) that the input current is always sinusoidal and in phase with the corresponding input voltage. Therefore, the 3ph-BR can obtain high power factor under unbalanced ac input conditions.

Table V shows the test results of PF, input current THD, and their harmonic contents with and without the proposed control strategy. It can be known from Table V that the proposed control strategy can effectively suppress the third harmonic of the three-phase input currents, and significantly improve input current THD. Besides, a higher power factor can be obtained by using the proposed control strategy.

VI. CONCLUSION

A digital control strategy for the 3ph-BR under unbalanced ac input conditions is proposed in this letter, which can effectively eliminate the odd harmonics of the input currents and the even harmonics of the output voltage ripple under unbalanced ac input conditions. The proposed control strategy does not need PLL and complex calculations. Therefore, a low-cost digital processor can be used to meet the computing requirement, which effectively reduces the cost and the volume of the digital controller. Furthermore, the processing speed of the digital processor is no longer the critical factor for the 3ph-BR under unbalanced ac input conditions. Experimental results show that the proposed digital control strategy can significantly improve the performance of the 3ph-BR under unbalanced ac input conditions. The control strategy proposed in this letter is suitable for the application where there are strict requirements for the cost and volume of a three-phase rectifier.

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