A 1-A 6-MHz Digitally Assisted Buck–Boost Converter With Seamless Mode Transitions and Fast Dynamic Performance for Mobile Devices

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***Abstract*—A 1-A 6-MHz buck–boost converter with seamless mode transitions and fast dynamic operation is proposed for extending the useable voltage range of Li-ion batteries in mobile devices, and thereby their battery life. The proposed converter employs a proportional-integral peak-current-mode pulsewidth modulation controller with a digital adaptive slew-rate control scheme that minimizes output undershoots, overshoots, and settling time during mode transitions and dynamic events, such as load and output voltage steps. Additionally, hysteretic mode detection is proposed to prevent falsely triggering the converter to transition between the various operation modes (i.e., buck, boost, and buck–boost) and negatively impacting the performance of the circuit loads. The converter is fabricated in 0.13-μm CMOS technology, and supports 2.3–5 V input and 1.5–3.6 V output. The converter achieves 91.7% peak efficiency and over 80% efficiency at 1-mA load across all conditions. The output voltage ripple is less than 10 mV with a 220-nH inductor and a 10-μF output capacitor.**

***Index Terms*—Buck–boost converters, dc–dc power converters, power management ICs, switching power supplies.**

I. Introduction

With the rising demand for extending the running time of battery-operated devices, dc–dc converters that can operate at lower input voltage levels have become a necessity in order to leverage as much energy as possible from the battery. In fact, operating from an input voltage as low as 2.3 V in devices operating from Li-ion batteries can extend the running time of the device by as much as 20% compared to shutting down the device when the battery drops to 2.7 V [1]–[3]. However, since many of these devices require dc power supplies that are higher than 2.3 V, yet lower than the maximum voltage of a Li-ion battery (i.e., 5 V), this introduces the challenge of how to design these power supplies with an input voltage that can sometimes be higher or lower than their output voltage level. One solution is to design two separate dc–dc converters, one is a buck converter and another is a boost converter, and switch between them based on the input voltage level. However, such a solution is quite expensive as it involves two converters, and it introduces the complexity of switching between them, particularly when the input and output voltages are fairly close. Other solutions that involve only a single converter include switch-capacitor (SC) converters [50]–[52], the forward and flyback converters [4]–[7], and the single-ended primary inductance (SEPIC) converter [8]. However, SC converters offer a limited load current range to avoid excessively high switching frequency and degraded efficiency [47]. They also provide optimized efficiency only at fixed conversion ratios, unless dynamically reconfigured [48], which requires a large number of switches and capacitors and results in poor dynamic voltage scaling (DVS) behavior [49], [50]. Moreover, the forward, flyback, and SEPIC converters are still quite costly and bulky due to the need for transformers or multiple inductors. They also expose the power switches to high voltage stresses, which degrades reliability [12]–[16].

An alternative cost-effective solution is the buck–boost converter shown in Fig. 1 [9]–[11], [17]–[25]. In this topology, four power switches are used to configure the converter to operate as a buck converter when the input voltage is higher than the output voltage (i.e., the buck mode), or as a boost converter when the input voltage is lower than the output voltage (i.e., the boost mode). However, when the input and output voltages are fairly close, an intermediate mode (i.e., the buck–boost mode) is typically utilized instead of the pure buck or boost modes to avoid operating the converter at excessively high or low switching duty cycles. Although buck–boost converters suffer from higher conduction losses than a standard buck or boost converters due to the additional power switches, the cost advantage of using a single inductor and the ability to operate from an input that is higher or lower than the output makes this topology an attractive compromise in most cases.

However, there are two key difficulties in the design of the buck–boost converters in Fig. 1. First, the discontinuity in the switching duty cycle, along with inductor current imbalance between various operation modes produces large undershoots and overshoots at the output and slows down its settling time during mode transitions. Second, the susceptibility in noisy operating conditions to being falsely and continuously triggered to change modes when the conversion ratio is fairly close to the boundaries between the various modes. This article addresses these two difficulties. First, a proportional-integral (PI) peak-current-mode pulsewidth modulation (PWM) controller with digital adaptive slew-rate control is proposed to minimize transients and settling

Manuscript received March 11, 2020; revised May 26, 2020 and July 29, 2020; accepted August 21, 2020. Date of publication August 31, 2020; date of current version November 20, 2020. Recommended for publication by Associate Editor W. Huang. *(Corresponding author: Manmeet Singh.)*

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Digital Object Identifier 10.1109/TPEL.2020.3020399

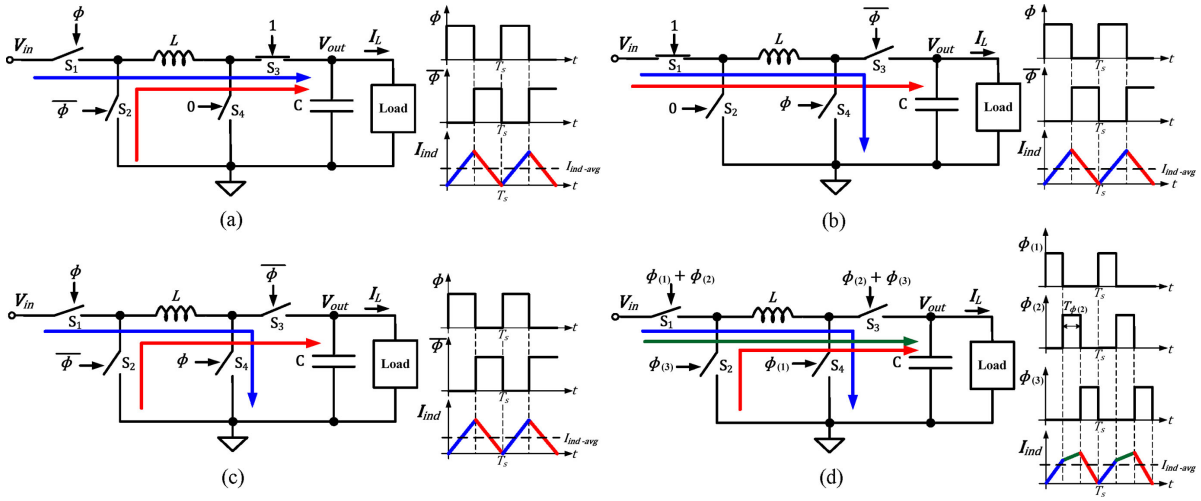

Fig. 1. Various operation modes of the buck–boost converter: (a) buck mode, (b) boost mode, (c) standard buck–boost mode, and (d) modified buck–boost mode. "$I_{\mathrm{ind-avg}}$" is the average inductor current, "I_L" is the load current, and "D" is the switching duty cycle.

time during mode transitions. Second, a hysteretic mode detector is proposed to prevent false mode transitions.

The rest of this article is organized as follows. Section II describes the principles of operation of the buck–boost topology and its key limitations, Sections III and IV present the system- and circuit-level details of the proposed design, while Section V presents the experimental results. Finally, Section VI concludes this article.

II. Operation Principles of the Buck–Boost Topology and Its Limitations

A. Operation Principles

The buck–boost converter shown in Fig. 1 can operate in four different modes. When the input voltage V_{in} is higher than the desired output voltage V_{out}, the converter operates in the buck mode as shown in Fig. 1(a), where the switches S_3 and S_4 are permanently turned ON and OFF, respectively, while the switches S_1 and S_2 are toggled in a complementary fashion. When V_{in} is lower than the desired V_{out}, the converter operates in the boost mode as shown in Fig. 1(b), where the switches S_1 and S_2 are permanently turned ON and OFF, respectively, while the switches S_3 and S_4 are toggled in a complementary fashion. Fig. 2(a) shows the duty cycle of switching D in both the buck and boost modes versus the conversion ratio $(V_{\mathrm{out}}/V_{\mathrm{in}})$, while Fig. 2(b) shows the ratio between the average inductor current $I_{\mathrm{ind-avg}}$ and the load current I_L. In principle, the buck and boost modes alone are sufficient to cover all possible conversion ratio scenarios. However, by examining Fig. 2(a), when the conversion ratio is very close to unity, the converter operates with duty cycle that is very close to 0% and 100% in the boost and buck modes, respectively. To avoid excessively narrow switching pulses, it is common to introduce an intermediate operation mode (i.e., the standard buck–boost mode) for conversion ratios around unity as shown in Fig. 1(c). In this mode, all four switches are toggled in a switching period, where the switches S_1 and S_4 are controlled by one phase of the clock, while S_2 and S_3 are controlled by the complementary phase of the same clock. In this case, the duty cycle of switching and the average inductor current in the standard buck–boost mode can be written as

$$D = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}} + V_{\mathrm{out}}} \tag{1}$$

$$I_{\mathrm{ind-avg}} = \frac{I_L}{1 - D}. \tag{2}$$

By introducing the standard buck–boost mode, the switching duty cycle versus the conversion ratio in this mode becomes as shown in Fig. 2(a), while the ratio between the average inductor current and the load current becomes as shown in Fig. 2(b). The conversion ratios covered by the buck–boost mode depend on the maximum and minimum practical switching duty cycle in the buck and boost modes, respectively. These are determined by the minimum pulsewidth that can be handled by the converter circuits. Typically, the converter circuitry is designed such that the minimum pulsewidth corresponds to a duty cycle of 85% and 15% in the buck and boost modes, respectively. Switching pulses narrower than that require excessively fast gate-drive and controller circuits, which increase power consumption and degrade efficiency.

However, since the standard buck–boost mode involves switching four power switches in one cycle instead of only two, the switching losses are doubled. Additionally, since this mode is only active when the input and output voltages are fairly close to each other, the duty cycle of switching will always be close to 50%, which leads the average inductor current to be always close to twice the load current as predicted by (2) [26]–[39]. As a result, the efficiency in the standard buck–boost mode is degraded due to excessive conduction and switching losses. Nonetheless, to reduce conduction losses, it is common to modify the operation of the standard buck–boost mode by splitting the phase of the clock into three phases rather than only two complementary phases, as shown in Fig. 1(d) [26]–[30]. In this case, the switch S_1 is controlled by the logical OR of the

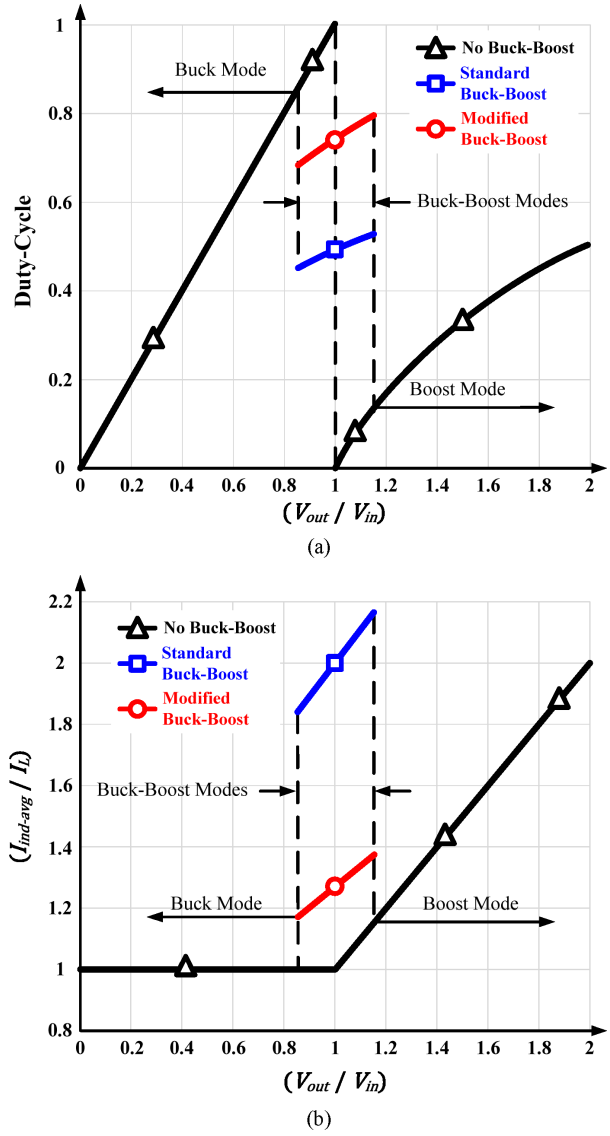

Fig. 2. Behavior of the buck–boost converter in various modes versus the conversion ratio: (a) switching duty cycle; and (b) ratio between the average inductor current and the load current.

first and second phases of the clock, the switch S_2 is controlled by the third phase of the clock, the switch S_4 is controlled by the first phase of the clock, and the switch S_3 is controlled by the logical OR of the second and third phases of the clock. With that modification, the duty cycle of switching and the average inductor current in the modified buck–boost mode can be written as

$$D = \frac{V_{\text{out}}}{V_{\text{in}} + V_{\text{out}}} \left(1 + \frac{T_{\Phi(2)}}{T_s}\right) \tag{3}$$

$$I_{\text{ind-avg}} \approx \frac{I_L}{1 - D + \frac{T_{\Phi(2)}}{T_s}} \tag{4}$$

where $T_{\Phi(2)}$ is the pulsewidth of the second phase of the clock and T_s is the switching period of the converter. The duty cycle versus conversion ratio in the modified buck–boost mode is shown in Fig. 2(a), while the ratio of the average inductor current to the load current is shown in Fig. 2(b). The modified buck–boost mode ensures that the average inductor current is much closer to the load current, which significantly reduces conduction losses and improves efficiency.

B. Limitations

The switching duty cycle and inductor current behavior of the buck–boost converter described in Fig. 2 reveals two serious limitations. The first limitation is the discontinuity in the switching duty cycle and the imbalance in the inductor current at the borders between the various modes of operation. This discontinuity results in poor transient response during mode transitions (i.e., slow output voltage settling and large overshoots and undershoots), which is particularly problematic when the converter is used in DVS applications where mode transitions due to output voltage scaling are quite frequent. In fact, excessively long output voltage settling times reduce the effectiveness of DVS, while large overshoots and undershoots can cause load failures and excessive voltage stresses.

The second limitation is that the addition of the intermediate buck–boost region increases the susceptibility of the converter to being falsely triggered to move between modes, particularly for conversion ratios around unity. This is quite problematic in noisy operating conditions or with loads that have high switching activity since changes in input and output voltages are often only transient rather than permanent, and thus the converter can be repetitively triggered and trapped into a continuous mode transition behavior around these conversion ratios. Although it is common to apply a hysteretic window to the control circuitry that enables and disables mode transitions to circumvent this problem, it is particularly challenging in buck–boost converters to optimize the size of such hysteretic window. In fact, a narrow hysteretic window can be insufficient to prevent false and continuous mode transitions, while a wide hysteretic window can significantly increase the range of conversion ratios where the converter is forced to operate in the relatively low-efficiency buck–boost mode.

III. System-Level Design of the Proposed Current-Mode Digitally Assisted Buck–Boost Converter

A. Top-Level Control

The block diagram of the proposed digitally assisted buck–boost converter is shown in Fig. 3. The converter employs a 6-MHz peak-current-mode PWM controller for heavy loads (i.e., 0.5–1 A), a constant-peak-current pulse frequency modulation (PFM) controller for light loads (i.e., less than 0.5 A), and a hysteretic mode detector for controlling mode transitions. Current-mode operation for both the PWM and PFM controllers is selected because unlike voltage-mode operation, it eliminates the dependency of the control loop transfer function on the power stage configuration (buck, boost, or buck–boost) [32]–[35], which enables using the same control loop for all modes. Moreover, current-mode operation is superior in terms of line regulation performance due to the inherent feedforward path between the input voltage and inductor current [32]–[35]. Nonetheless, slope compensation must be added to prevent

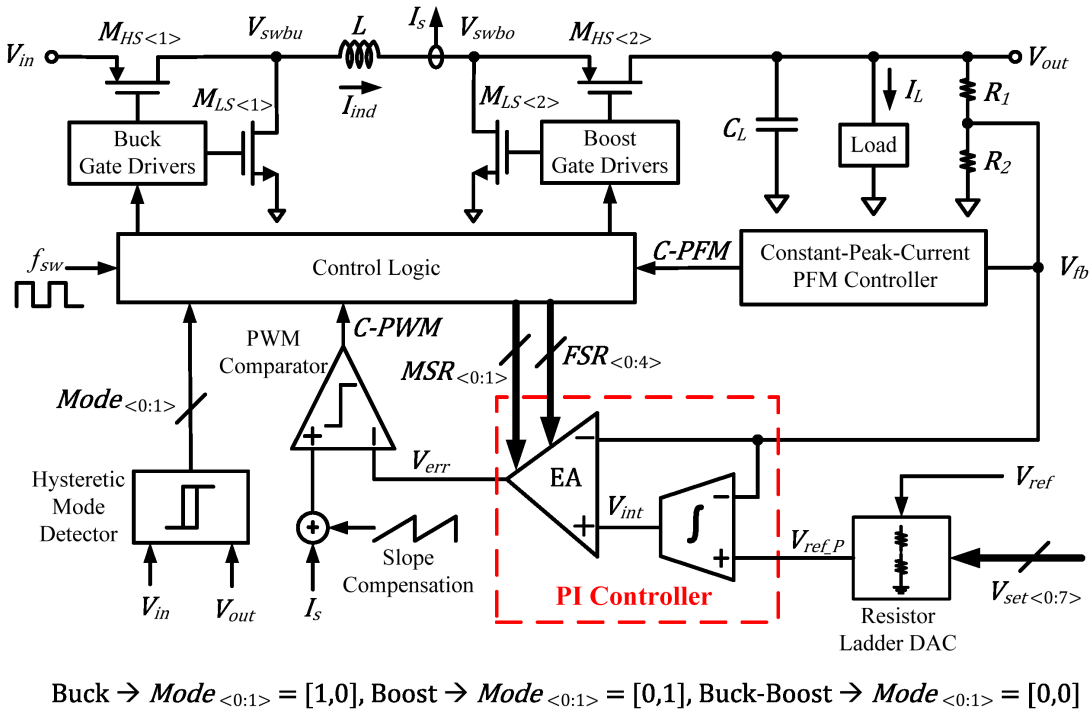

Fig. 3. Block diagram of the proposed digitally assisted buck–boost converter.

subharmonic oscillations when the switching duty cycle is above 50% [40]–[43]. In the proposed converter, the slope of the compensation ramp is designed to be half the maximum expected falling slope of the inductor current under all conditions. This approach eliminates subharmonic oscillations across the full duty-cycle range of the converter [40]–[43], and thus, the slope of the compensation ramp does not have to be changed or adapted to the operating conditions of the converter or its modes. Although the main loop of current-mode PWM controllers can be stable without any active compensation since they are inherently single-pole systems [40], the proposed controller employs an active PI compensation scheme (i.e., type-II compensation) with an error amplifier (EA) and an integrator. This compensation scheme achieves a high dc gain by introducing a dc pole in the control loop while improving the phase margin and load transient response by introducing a zero at frequencies lower than the loop's unity gain frequency [12], [32]–[35], [40]. The operation of the PI controller can be understood with the aid of Fig. 3, where its small-signal transfer function can be written as

$$\frac{\hat{V}_{\rm err}}{\hat{V}_{fb}} = -A_o\left(\frac{\rm s + f_{gbw-int}}{\rm s}\right) \tag{5}$$

where the hat above the symbols indicate the small-signal version of each signal, A_o is the dc gain of the EA, and $f_{\rm gbw-int}$ is the gain-bandwidth product (GBW) of the integrator (also its unity gain frequency). As shown by (5), the transfer function of the PI controller has a pole at dc and a left-half-plane zero. This can be intuitively understood by considering that introducing an integrator in the signal path produces a pole at dc, while introducing a parallel path to the integrator (directly from the input of the controller to the EA) produces a zero. In order to ensure sufficient phase margin, the location of the zero added by the PI compensation network must be designed to be at a significantly lower frequency than the loop's unity gain frequency. In the proposed design with 6-MHz switching frequency, the loop's unity gain frequency is designed to be 100–150 kHz for a load current range between 0.5–1 A, which is the load range the proposed current-mode PWM PI controller is used for. By designing the integrator's GBW to be at 10 kHz (and thus the location of the zero), a phase margin of 61°–65° across the target load range can be ensured. Fig. 4 shows the ac response of the controller, where the dc gain of the loop is 85 dB (30 dB from the EA and 55 dB from the integrator). It is worth noting that although a pole at dc in the transfer function in (5) should ideally result in infinite dc gain, it is limited to 85 dB due to the noninfinite dc gain of the transconductance and amplifier stages used to build the integrator, as described in Section IV-A.

It is worth noting that the dynamic response of the converter is dominated and limited by the PI controller's small-signal and large-signal responses. Thus, one approach to improve the converter's dynamic response is to increase the control loop's small-signal bandwidth beyond 100–150 kHz (possible since 6 MHz switching frequency is sufficiently high). However, this approach increases the quiescent current significantly (which degrades efficiency), and also reduces the dc gain (which degrades accuracy and dc line and load regulation). The increase in quiescent current is not only due to the larger bandwidth needed in all the controller circuits, but more importantly due to having to push all the nondominant poles in these circuits to higher frequencies to ensure stability, which requires even more quiescent current. The proposed design avoids these drawbacks by maintaining a relatively low small-signal bandwidth (100–150 kHz) and relying instead on the proposed adaptive

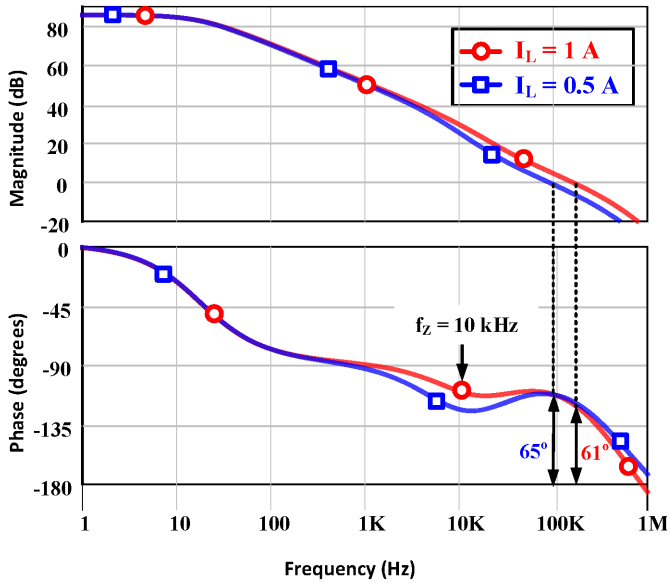

Fig. 4. Control loop gain and phase of the current-mode PWM PI controller.

slew-rate control (described in detail in the next subsection). Since slew-rate control modifies the charging/discharging currents at the output of the EA only temporarily during dynamic large-signal events (such as load, input, and output steps), fast dynamic response to these events can be achieved without permanently increasing the quiescent current and the small-signal bandwidth of the loop.

B. Digital Adaptive Slew-Rate Control

As discussed in Section II-B, one of the challenges associated with the conventional buck–boost topology is its poor transient response during mode transitions, which is attributed to the discontinuity in the switching duty cycle and the inductor current imbalance between the various modes as shown in Fig. 2. Since this is a large-signal effect, it results in saturating the error signal $V_{\rm err}$ at the output of the PI controller during mode transitions, where the response of the converter becomes limited by the slew rate of the EA rather than the small-signal bandwidth of the control loop. Therefore, this article proposes a digital scheme to adapt the rising and falling slew rates of the EA of the PI controller during mode transitions. This is accomplished through the 2-bit digital control bus $\rm MSR_{\langle 0:1\rangle}$ shown in Fig. 3 in the following manner: 1) in the boost mode, the rising slew rate is set to its maximum level while the falling slew rate is set to its minimum level; 2) in the buck–boost mode, both the rising and falling slew rates are set to an intermediate level; and 3) in the buck mode, the rising slew rate is set to its minimum level while the falling slew rate is set to its maximum level. The rationale behind adopting this scheme is that if the converter is in boost mode, the only possible transitions are either to the buck–boost or the buck modes, and in both cases, the falling slew rate needs to increase to improve the transient response. Thus, the falling slew rate is set to a minimum, intermediate, and maximum levels in the boost, buck–boost, and buck modes, respectively. On the other hand, if the converter is in buck mode, the only possible transitions are either to the buck–boost or the boost modes, and in both cases the rising slew rate needs to increase to improve the transient response. Thus, the rising slew rate is set to a minimum, intermediate, and maximum levels in the buck, buck–boost, and boost modes, respectively. However, if the converter is in the buck–boost mode, then transitioning to either the buck or the boost mode is possible. Thus, both the rising and falling slew rates are set to intermediate levels to cover both scenarios. It is important to note that the minimum, intermediate, and maximum rising and falling slew rates of the EA in each operation mode will vary from one application to another since they are determined based on the desired converter response (settling time and undershoots/overshoots) to dynamic events, such as line and load steps and DVS. They will also be a function of the process technology, layout parasitics, and printed circuit board design. Therefore, extensive time-domain simulations of the converter's control loop and power stage at different points in the schematic and layout design process are needed to determine the optimum EA slew rates to achieve a desired performance. In this design, the goal was to reduce undershoots and overshoots by at least 25% and settling time by at least 50%. Fig. 5 shows the converter's transient simulations during mode transitions due to input steps with and without adaptive slew-rate control. As shown, undershoots and overshoots during mode transitions are reduced by 25%–50%, while the settling times are reduced by 75%–83%.

Although the above-mentioned digital adaptive slew-rate concept is proposed primarily for improving transient response during mode transitions, this article also proposes adopting the same concept within each mode of operation by digitally fine-tuning the slew rate of the EA to improve the converter's transient response to dynamic events, such as load and output voltage steps that do not necessarily cause mode transitions. This is accomplished through the 5-bit digital control bus $\rm FSR_{\langle 0:4\rangle}$ shown in Fig. 3, where irrespective of the operation mode (i.e., buck, buck–boost, or boost), the rising slew rate and falling slew rate of the EA are set to higher and lower levels, respectively, as the converter's output voltage setting is increased (through the 8-bit control bus $V_{\rm set\langle 0:7\rangle}$). The rationale behind this fine-tuning slew-rate control scheme is that when the output voltage is increased, only the rising slew rate of the EA needs to increase to improve transient response, while if the output voltage is decreased, only the falling slew rate of the EA needs to increase. Thus, the rising and falling slew rates are changed in a complementary fashion to improve transient response to both rising and falling DVS events.

C. Hysteretic Mode Detection

The proposed hysteretic mode detection is based on the converter's input voltage $V_{\rm in}$, output voltage $V_{\rm out}$, and the minimum pulsewidth $T_{\rm min}$ the converter can handle. $T_{\rm min}$ is determined by the sum of the worst case gate-drivers and PWM comparator propagation delays, which is 25 ns in this proposed design. This corresponds to a maximum and minimum practical switching duty cycle of 85% and 15% in the buck and boost

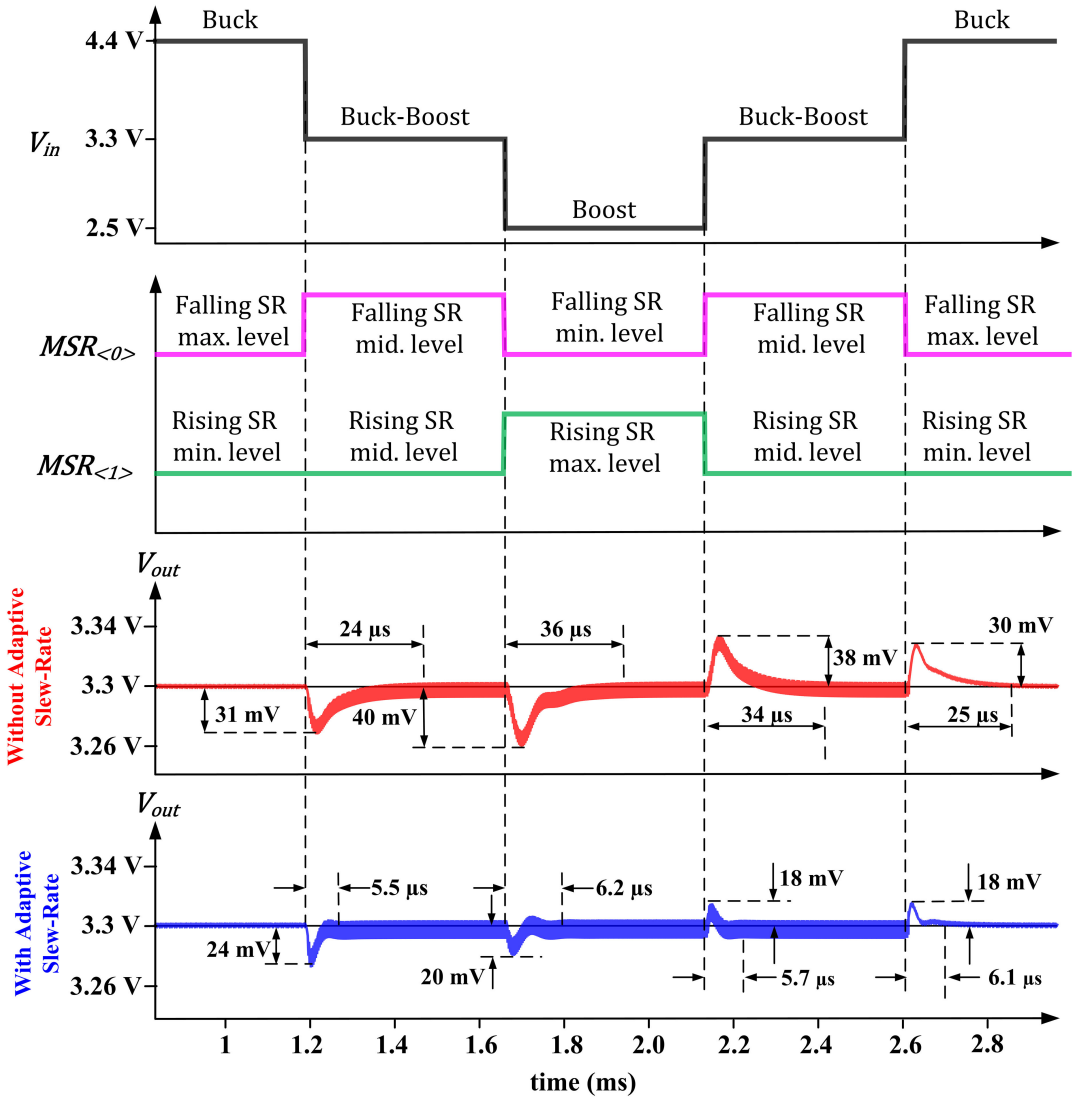

Fig. 5. Converter's simulated response to various input voltage steps with and without adaptive slew-rate control, including the digital bus $\mathrm{MSR}_{\langle 0:1\rangle}$ that sets the rising and falling slew rate of the EA based on the input voltage levels, as described in Section III-B.

modes, respectively. Fig. 6 shows the hysteretic mode detector operation. When V_{in} is much higher than V_{out}, the converter operates in the buck mode. As V_{in} decreases, it transitions to the buck–boost mode once V_{in} drops below V_{THBU}, which should be designed to correspond to the minimum pulsewidth T_{min} in the buck mode. To compute V_{THBU}, the voltage-second equation of a buck converter can be written as

$$V_{\mathrm{out}} \approx DV_{\mathrm{in}} - V_{\mathrm{Loss}} \tag{6}$$

where D is the duty cycle and V_{Loss} is the voltage drop across the power switches and the inductor parasitic resistance due to the load current. Since in the buck mode, T_{min} corresponds to the maximum allowed duty cycle, V_{THBU} can be written as

$$V_{\mathrm{THBU}} = \frac{V_{\mathrm{out}} + V_{\mathrm{Loss-max}}}{\left(\dfrac{T_s - T_{\mathrm{min}}}{T_s}\right)} \tag{7}$$

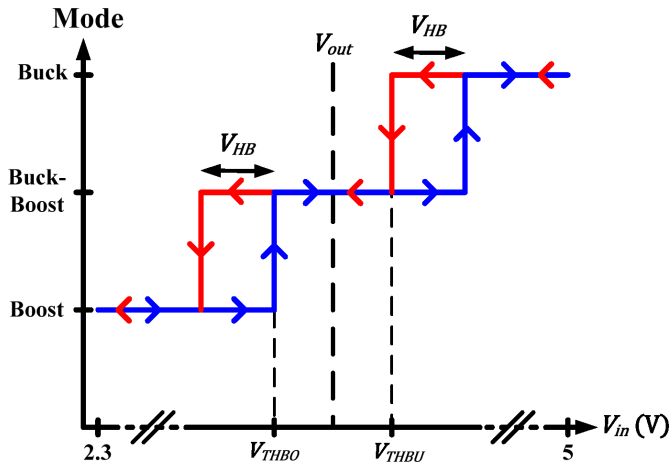

Fig. 6. Operating modes versus input voltage under boundary conditions to justify hysteresis feature during mode change.

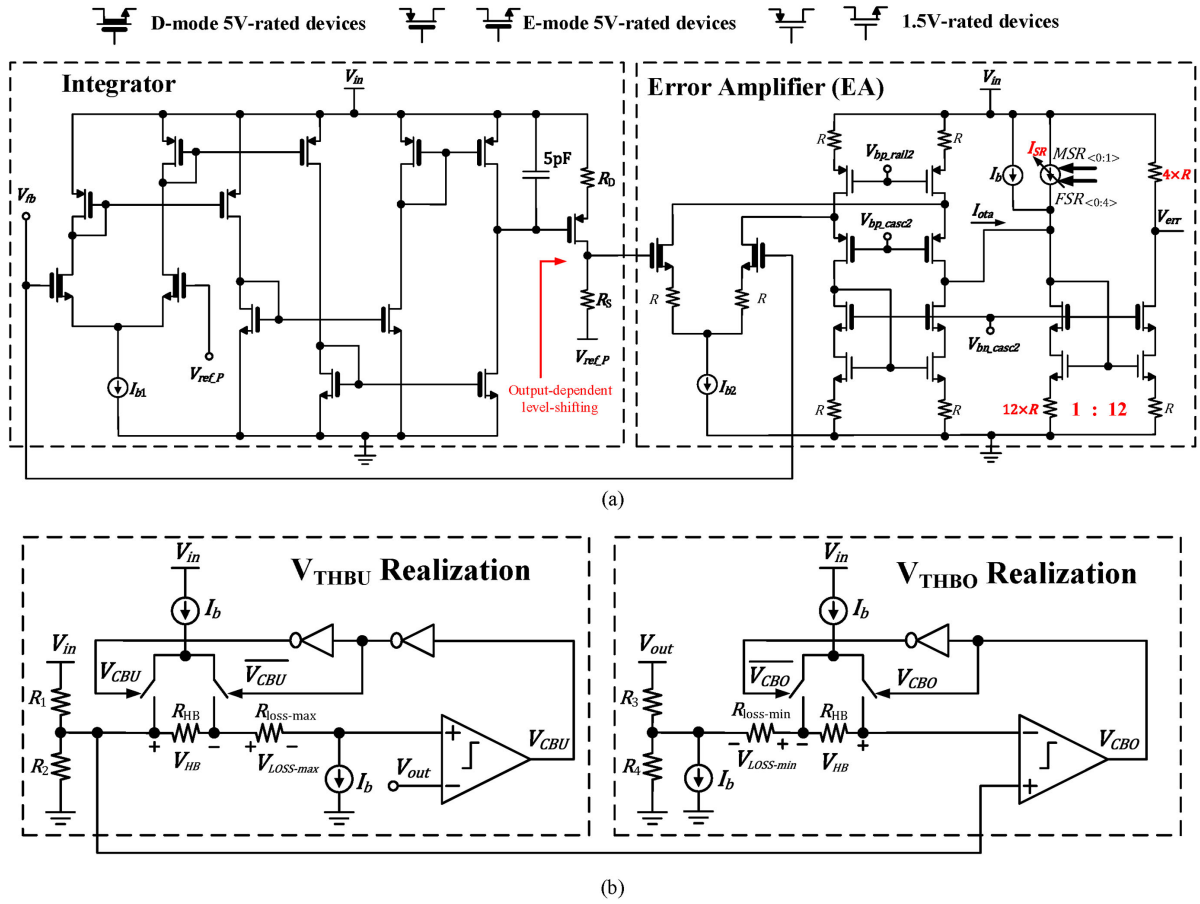

Fig. 7. (a) Circuit-level design of integrator and error amplifier. (b) Threshold voltage realization of buck and boost modes.

where T_s is the switching period and $V_{\mathrm{Loss-max}}$ is the maximum expected voltage drop across the power switches and the inductor parasitic resistance when the load current is set to its maximum. Since V_{out} is known through the output voltage control bus $V_{\mathrm{set}\langle 0:7\rangle}$ setting, V_{THBU} can be set accordingly, as will be discussed in Section IV. Once the converter transitions from the buck mode to the buck–boost mode when V_{in} drops below V_{THBU}, a fixed offset V_{HB} is added to V_{THBU}. By adding this offset, a hysteretic band of V_{HB} is realized, which prevents falsely triggering the converter into moving back to the buck mode. In the proposed design, V_{HB} is set to 50 mV, which was chosen by accounting for all the parasitcs in the power path.

Similarly, when V_{in} is much lower than V_{out}, the converter is in boost mode. As V_{in} increases, it transitions to buck–boost mode once V_{in} exceeds V_{THBO}, which should correspond to the minimum pulsewidth T_{min} in the boost mode. The voltage-second equation of a boost converter is written as

$$V_{\mathrm{out}} \approx \frac{V_{\mathrm{in}}}{(1-D)} - \frac{V_{\mathrm{Loss}}}{(1-D)^2} \tag{8}$$

where D is the duty cycle and V_{Loss} is the voltage drop across the power switches and the inductor parasitic resistance. Since in the boost mode, T_{min} corresponds to the minimum allowed duty cycle, V_{THBO} can be written as

$$V_{\mathrm{THBO}} = V_{\mathrm{out}}\left(\frac{T_s - T_{\mathrm{min}}}{T_s}\right) + \frac{V_{\mathrm{Loss-min}}}{\left(\frac{T_s - T_{\mathrm{min}}}{T_s}\right)} \tag{9}$$

where T_s is the switching period, $V_{\mathrm{Loss-min}}$ is the minimum expected voltage drop across the power switches and the inductor parasitic resistance when the load current is at the minimum to maintain continuous conduction mode (CCM). Once the converter transitions from the boost to the buck–boost mode when V_{in} exceeds V_{THBO}, the fixed offset V_{HB} is added to V_{THBO} to realize a hysteretic band to prevent falsely triggering the converter into moving back to the boost mode.

IV. Circuit-Level Design of the Proposed Current-Mode Digitally Assisted Buck–Boost Converter

The key circuit blocks in the proposed converter are the PI controller with adaptive slew rate and the hysteretic mode detector, which are described in the following subsections.

A. PI Controller With Adaptive Slew Rate

The circuit design of the PI controller is shown in Fig. 7(a). The integrator is comprised of a Gm-C stage followed by a

source-degenerated common-source amplifier stage. The Gm-C stage employs a current-mirror OTA with about 10 μS transconductance loaded by a 5-pF capacitor to realize the integration function with a GBW of $\sim$312 Hz. The output of the Gm-C stage is further amplified by the source-degenerated common-source stage, which also shifts down the quiescent level at the final output of the integrator. This accomplishes two important goals. First, it provides an additional 30 dB of dc gain to shift the GBW of the entire integrator to 10 kHz, which ensures the location of the zero of the PI controller as described in Section III-A. Second, it ensures sufficient operation headroom at the output of the Gm-C stage for the expected range at the final output of the integrator. The total dc voltage gain of the integrator is designed to be about 55 dB.

The error amplifier design is based on a source-degenerated folded-cascode topology, which keeps the dc gain relatively constant with process, voltage, and temperature variations since it is determined by the ratio of similar resistors. The dc gain of the error amplifier is designed to be about 30 dB, which along with the 312-Hz GBW of the integrator ensures that the location of the zero of the PI controller is around 10 kHz, as described in Section III-A. The digital adaptive slew-rate control is incorporated through the digitally programmable current source I_{SR} at the output stage of the error amplifier. By adjusting the value of I_{SR} using the two digital busses MSR and FSR, the rising and falling slew rates can be adjusted in a complementary fashion as described in Section III-B. The operation of the error amplifier with adaptive slew-rate control can be further illustrated with an example. Let us say that the output voltage of the converter is suddenly set to a higher level by increasing the digital word in the bus $V_{\mathrm{set}\langle 0:7\rangle}$. As explained in Section III-B, the digital word in the bus $\mathrm{FSR}_{\langle 0:4\rangle}$ will also increase, which causes I_{SR} to increase, and consequently, V_{err} to drop more rapidly (compared to leaving I_{SR} unchanged). This in turn causes the output voltage to rise faster without being limited by the control loop's small-signal bandwidth. Once the control loop catches up, and due to its high dc gain (85 dBs), it adjusts the steady-state dc operating point at the output of the error amplifier to the proper level needed to precisely regulate the output voltage of the converter to its new level. Thus, I_{SR} only affects the error amplifier's output slew rate during large signal dynamic events, with little impact on its steady-state output operating point.

Both the integrator and the error amplifier operate directly from the unregulated input voltage of the converter (i.e., 2.3–5 V). Thus, enhanced-mode 5 V-rated transistors are used for both blocks, with the exception of the input differential pairs, where depletion-mode 5 V-rated transistors are used instead. This is because the expected range of the feedback voltage V_{fb} is 0.55–1.44 V for the desired output voltage range of the converter (i.e., 1.5–3.6 V). Such a range is too low for the input differential pairs if enhanced-mode transistors are used.

Other important parts of the proposed PI controller are the slope compensation ramp (to prevent subharmonic oscillations) and the inductor current sensors. As described in Section III-A, the slope of the compensation ramp is designed to be constant and equal to half the maximum expected falling slope of the inductor current under all conditions. The standard approach for generating a sawtooth signal (i.e., a constant current source charging a capacitor) is adopted in the proposed converter for realizing the ramp. The inductor current sensors are based on the standard sense FET approach [44]–[46]. In the buck and buck–boost modes, the peak inductor current is indicated by sensing the current in the high-side switch ($M_{HS\langle 1\rangle}$ in Fig. 3), while in the boost mode, it is indicated by sensing the current in the low-side switch ($M_{LS\langle 2\rangle}$ in Fig. 3).

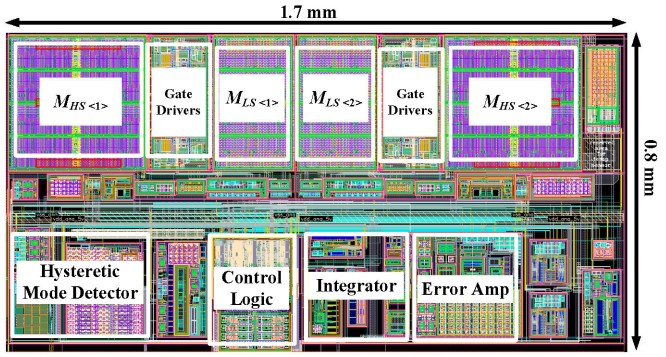

Fig. 8. Layout of the proposed converter highlighting the main building blocks.

B. Hysteretic Mode Detector

The design of the hysteretic mode detector is shown in Fig. 7(b). The realization of V_{THBU} is accomplished by first scaling the input voltage V_{in} of the converter by the ratio $[(T_s - T_{\mathrm{min}})/T_s]$ through the resistor ladder comprised of R_1 and R_2. The scaled version of V_{in} is then reduced by the voltage drop $V_{\mathrm{Loss-max}}$, which is realized through the bias current I_b and the resistor $R_{\mathrm{Loss-max}}$; both are designed to mimic the worst case voltage drop across the power switches and the parasitic resistance of the inductor. The resulting voltage is then compared to the output voltage of the converter using a single-threshold comparator in order to realize (7). To realize the hysteretic band V_{HB}, the output of the comparator controls two switches in a complementary fashion to either add or eliminate an additional voltage drop that is equal to the desired V_{HB}, which is realized through the bias current I_b and the resistor R_{HB}. It is worth noting that using matching source and sink bias currents in the structure in Fig. 7(b) is necessary to eliminate the loading effect of R_{HB} and $R_{\mathrm{Loss-max}}$ on the resistor ladder ratio of R_1 and R_2. The realization of V_{THBO} is accomplished similarly to V_{THBU} as shown in Fig. 7(b). However, to properly realize (9), V_{in} is scaled by $[(T_s - T_{\mathrm{min}})/T_s]$, while V_{out} is scaled by $[(T_s - T_{\mathrm{min}})/T_s]^2$. Since the scaled version of V_{in} is already available from the circuit realizing V_{THBU}, it is simply reused, while the scaled version of V_{out} is generated through the resistor ladder comprised of R_3 and R_4. The outputs of both comparators in Fig. 7(b) are used by the converter's state machine to determine the proper mode of operation of the converter (i.e., buck, boost, or buck–boost).

V. Measurement Results

The proposed 6-MHz current-mode buck–boost converter with adaptive slew-rate control is designed and fabricated in

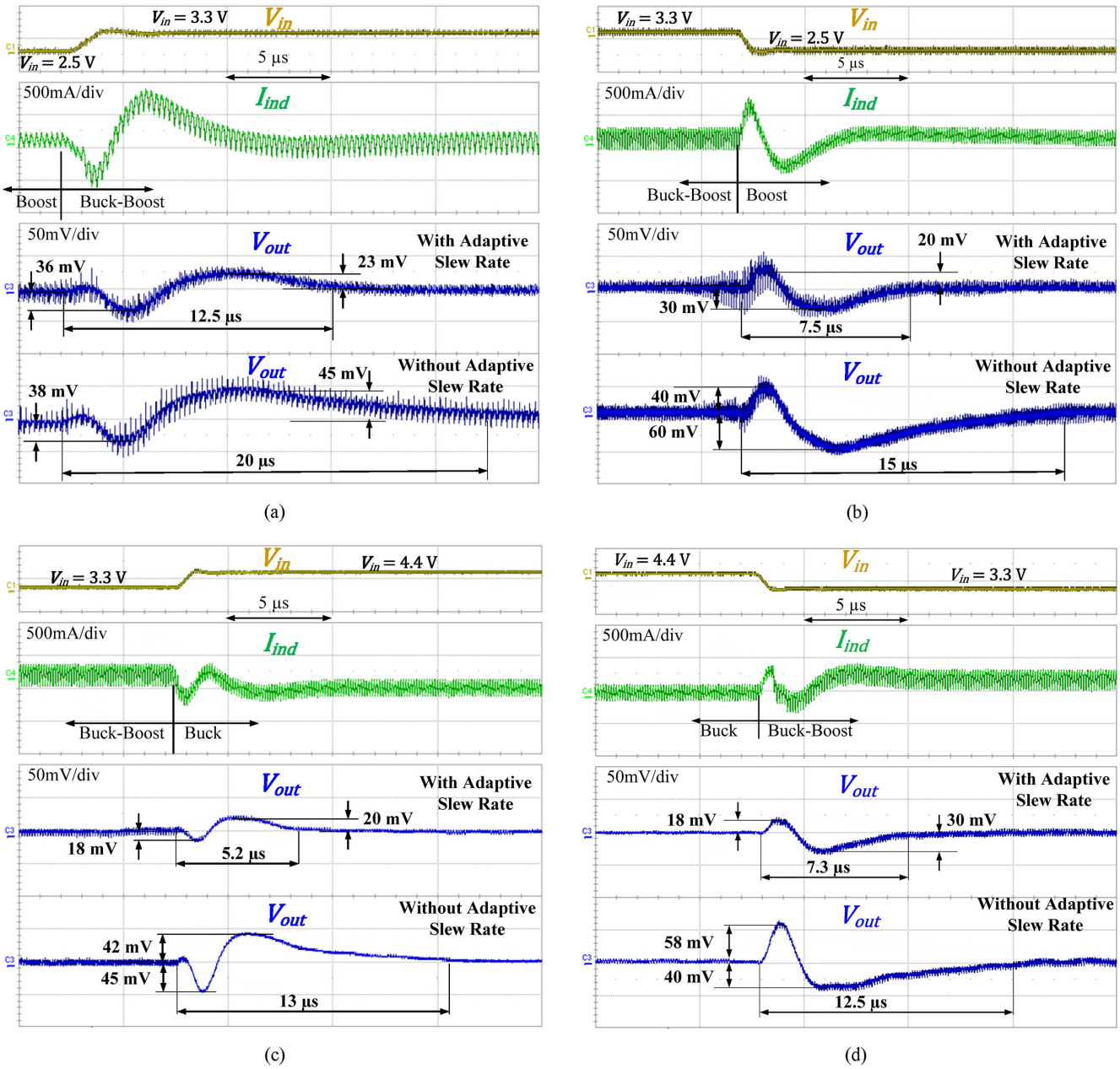

Fig. 9. Converter's measured output voltage and inductor current during mode transitions with and without the digital adaptive slew-rate control scheme: (a) boost to buck–boost, (b) buck–boost to boost, (c) buck–boost to buck, and (d) buck to buck–boost. Output voltage and load current are set to 3.3 V and 1 A.

a 130-nm standard CMOS process. The converter is designed to operate from an input between 2.3 and 5 V (i.e., Li-ion battery levels) and to generate a programmable output from 1.5 to 3.6 V, with a maximum load current of 1 A. The layout of the converter is shown in Fig. 8, where the total area is 1.36 mm^2, ∼50% of which is used for the controller circuit blocks and ∼50% is used for the power switches and their gate drivers.

Fig. 9 shows the measurement results of the converter's output voltage and inductor current waveforms during various mode transition events with and without the proposed digital adaptive slew-rate control scheme. All measurements are taken with the output voltage set to 3.3 V and the load current set to the maximum 1-A level. Fig. 9(a) and (b) shows the result as the input voltage is stepped from 2.5 to 3.3 V and then back to 2.5 V, which transitions the converter between the boost and buck–boost modes, while Fig. 9(c) and (d) shows the results as the input voltage is stepped from 3.3 to 4.4 V and then back to 3.3 V, which transitions the converter between the buck–boost and buck modes. As shown, the proposed adaptive slew-rate control significantly reduces the overshoot and undershoot (by 25%–60%) and the settling time (by 41.6%–60%), which leads to much more seamless mode transitions.

To demonstrate the impact of the adaptive slew-rate control on the dynamic response of the converter in cases where there are no mode transitions, Fig. 10 shows the converter's output in

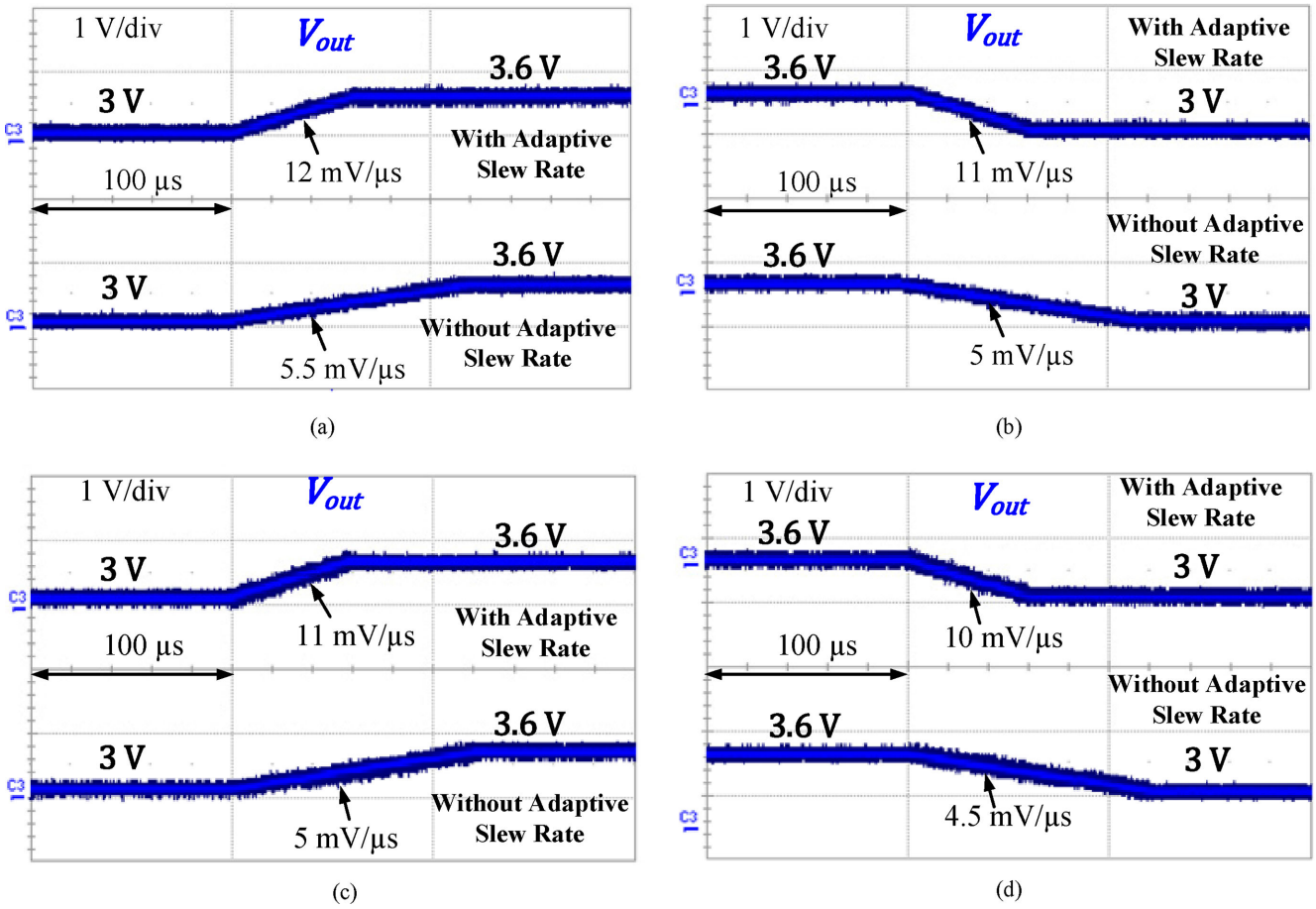

Fig. 10. Output of the converter in response to rising and falling output voltage steps between 3 and 3.6 V with and without the proposed adaptive slew-rate scheme: (a) and (b) in buck mode with 5-V input; and (c) and (d) in boost mode with 2.3-V input. A constant load resistance of 3.6 Ω has been used for all cases.

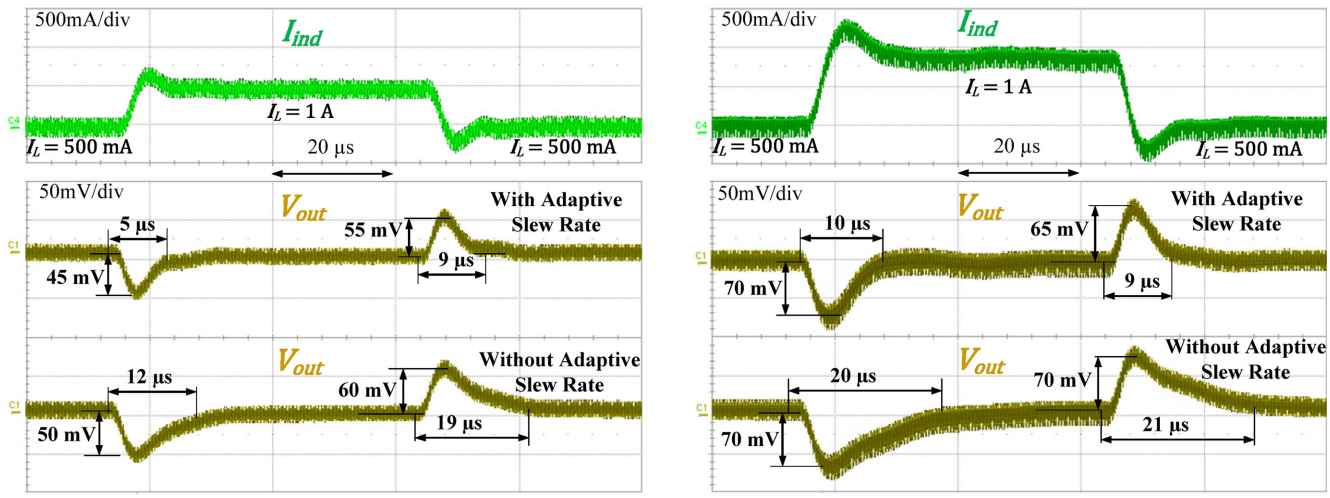

Fig. 11. Output of the converter in response to rising and falling load steps between 0.5 and 1 A with and without the proposed adaptive slew-rate scheme: (a) in buck mode; and (b) in boost mode.

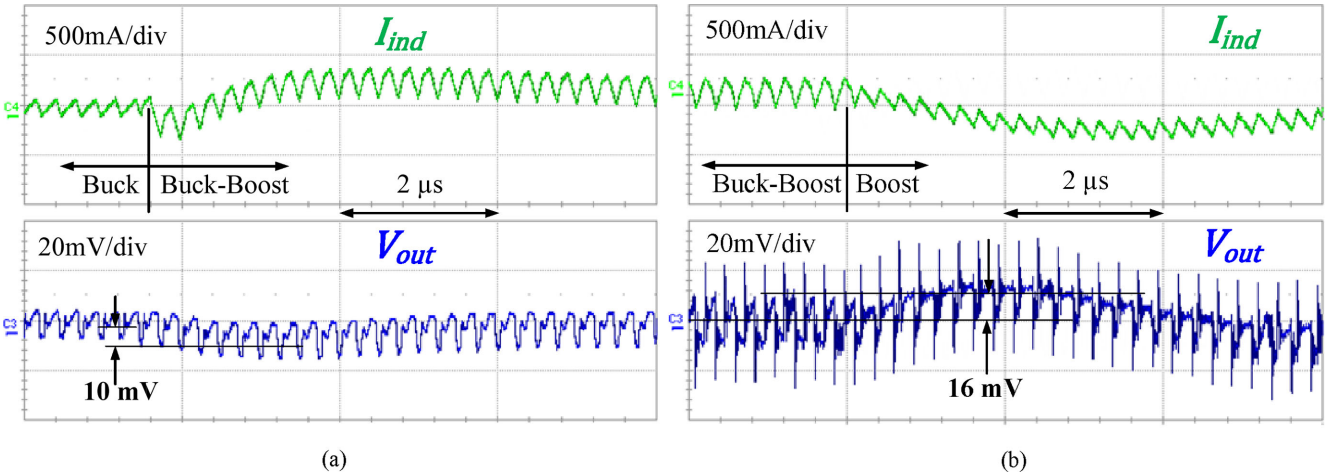

Fig. 12. Converter's response when the input voltage is ramped down from 5 to 2.3 V at 1 V/s: (a) during buck to buck–boost transition; and (b) during buck–boost to boost transition. The output voltage is 3.3 V and the load is 1 A.

response to rising and falling output voltage steps, while Fig. 11 shows the response to rising and falling load steps. Fig. 10(a) and (b) shows the response when the output is stepped between 3.0 and 3.6 V while the input is set to 5 V, which keeps the converter in the buck mode, while Fig. 10(c) and (d) shows the case when the input is set to 2.3 V, which keeps the converter in the boost mode. As shown, the adaptive slew-rate control significantly improves the rising and falling DVS response (by ∼50%) irrespective of the operation mode. Moreover, Fig. 11(a) shows the response when the load is stepped between 0.5 and 1 A, while the input is set to 5 V and the output is set to 3.3 V (i.e., buck mode), and Fig. 11(b) shows the case when the input is set to 2.3 V (i.e., boost mode). As shown, the adaptive slew-rate control significantly reduces the overshoot and undershoot (by 7.14%–10%) and the settling time (by 50%–58.33%) for both rising and falling load steps.

As explained in Section III-C, the proposed converter is designed to operate in the buck–boost mode if the minimum pulsewidth in the buck or the boost modes becomes shorter than 25 ns, which corresponds to 85% and 15% duty cycle in the buck and boost modes, respectively. Thus, for a 3.3-V output, and using (7) and (9), the mode transition thresholds V_{THBO} and V_{THBU} are 2.8 and 3.8 V, respectively. In order to demonstrate the effectiveness of the hysteretic mode detector in preventing false and repetitive mode transitions when the conversion ratio is fairly close to the boundaries between the various modes, the converter's response is examined as the input voltage is ramped down from 5 to 2.3 V at a very slow rate (1 V/s), while keeping the output voltage at 3.3 V and the load at 1 A. The slow input voltage ramp is used to ensure that the conversion ratio remains around the boundary between the different modes for an extended period of time to allow for observing false or repetitive transitions. Fig. 12(a) and (b) shows the case as the converter transitions from the buck to buck–boost modes and from the buck–boost to boost modes, respectively. As shown, only a single mode transition occurs in both cases with minimal disturbance to the output despite the slow input voltage change rate, which demonstrates the effectiveness of the hysteretic mode detector in ensuring seamless and glitch-free transitions between the modes.

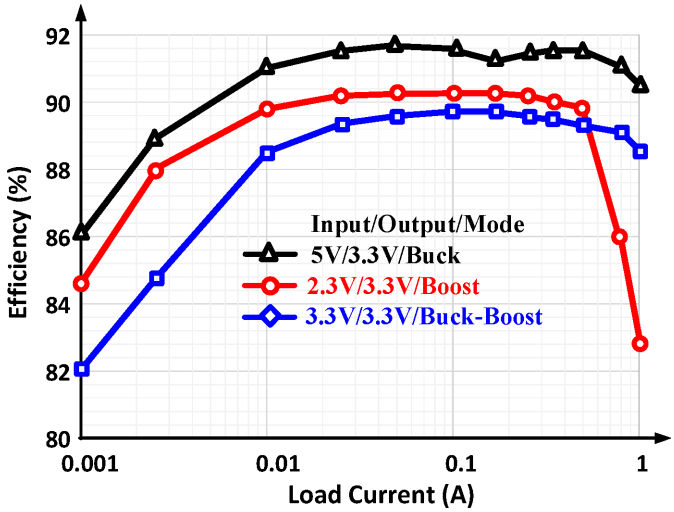

Fig. 13. Converter's measured efficiency versus load current for different operation modes.

Fig. 13 shows the measured efficiency of the converter versus load current in different modes. The converter achieves 91.7% peak efficiency in the buck mode and 82% minimum efficiency in the buck–boost mode at 1 mA load. This is because of the higher switching losses in the buck–boost mode resulting from toggling all four power switches. As switching losses dominate at light loads, the buck–boost mode offers lower efficiency than the buck or boost modes at light loads. At heavy loads (higher than 500 mA) where conduction losses dominate, the boost mode has the lowest efficiency, as can be clearly observed in Fig. 13. This is because for the same load, the boost mode has significantly higher input current (i.e., higher conduction losses) than the buck and the buck–boost modes, especially at high conversion ratio.

TABLE I
KEY PERFORMANCE METRICS OF THE PROPOSED CONVERTER AND A COMPARISON WITH OTHER PUBLISHED WORKS

		This Work	TPEL '20 [53]	TIEL '19 [9]	TPEL '17 [16]	TCAS-II '17 [54]	TPEL '14 [13]	ISSCC '11 [30]	TPEL '10 [32]
Control Scheme		**Peak-Current-Mode with Adaptive Slew-Rate**	Voltage-Mode	Peak-Current-Mode	Hysteretic Current-Mode	Voltage-Mode	Voltage-Mode	Average Current-Mode	Average Current-Mode
Technology (μm)		**0.13**	0.18	0.18	0.35	FPGA-based	0.18	0.5	0.25
Active Silicon Area (mm^2)		***2.8, **1.36**	**1.51	*5.79	*3.86	Discrete Design	*4	*7.5	*3.14
Input Voltage Range (V)		**2.3–5**	2.5–5	2.7–4.2	2.5–5	2.5–4.5	2.7–5.5	3–5.5	2.7–4.5
Output Voltage Range (V)		**1.5–3.6**	2.0–4.6	3.4	3.3	3.3	2–5	3.6	3.3
Maximum Load Current (A)		**1**	0.5	1.1	0.4	0.5	2	1.2	0.5
Inductor (μH)		**0.22**	3	4.7	1	4.7	1	2.2	4.7
Output Capacitor (μF)		**10**	20	10	10	22	33	10	47
Switching Frequency (MHz)		**6**	14	1	1.66	1	2.5	2	0.7
DVS Rate: 3 ↔ 3.6 V (mV/ μs)		**10-12**	Not Reported						
Efficiency	Minimum	**82% @ I_L = 1 mA**	83% @ I_L = 10 mA	82.9% @ I_L = 100 mA	80.4% @ I_L = 10 mA	72% @ I_L = 100 mA	80% @ I_L = 400 mA	78% @ I_L = 600 mA	86% @ I_L = 100 mA
	Peak	**91.7%**	94.8%	90.9%	98.1%	85.5%	91%	90.7%	96%
Load Step Response	Worst Case Condition: Boost Mode	**V_{out} = 3.3 V V_{in} = 2.3 V 0.5 ↔ 1 A**	V_{out} = 3.3 V V_{in} = 3.3 V 0.01 ↔ 0.42 A	V_{out} = 3.4 V V_{in} = 3 V 0.1 ↔ 1 A	V_{out} = 3.3 V V_{in} = 2.5 V 0.01 ↔ 0.4 A	V_{out} = 3.3 V V_{in} = 2.5 V 0. 1 ↔ 0.3 A	V_{out} = 3.3 V V_{in} = 3 V 0.05 ↔ 0.5 A	Not Reported	V_{out} = 3.3 V V_{in} = 2.5 V 0.08 ↔ 0.28 A
	Undershoot/Overshoot	**70 mV / 65 mV**	42 mV / 43 mV	300 mV / 250mV	80 mV / 50 mV	208 mV / 181 mV	72 mV / 40 mV		80 mV / 90 mV
	Settling Time	**10 μs / 9 μs**	65 μs / 75 μs	60 μs / 60 μs	50 μs / 70 μs	234 μs / 227 μs	40 μs / 40 μs		45 μs / 47 μs
Line Step Response	Worst Case Condition: Boost → Buck-Boost	**V_{out} = 3.3 V I_o = 1 A 2.5 ↔ 3.3 V**	V_{out} = 3.3 V I_o = 0.01 A 2.6 ↔ 5.0 V	Not Reported					V_{out} = 3.3 V I_o = 0.225 A 3.2 ↔ 3.5 V
	Undershoot/Overshoot	**36 mV / 23 mV**	87 mV / 95 mV						40 mV / 15 mV
	Settling Time	**12.5 μs / 7.5 μs**	200 μs / 240 μs						120 μs / 64 μs

*Total area with the pads. ** Total area without the pads.

Moreover, since the boost mode is used only when the battery voltage (i.e., the converter's input voltage) is too low, and given that the gate overdrive voltage of the power switches is derived from the input voltage, the power switches exhibit a much larger ON resistance, which further increases the conduction losses.

It is worth highlighting that although the buck–boost mode is a transitional state between the buck and the boost modes, its efficiency is actually quite critical. In fact, as mentioned earlier in this section, the proposed converter operates in the buck–boost mode if the output is set to 3.3 V and the input is between 2.8 and 3.8 V. Since the Li-ion battery range is from 2.3 to 5 V, the range in which the converter operates in the buck–boost mode is actually 37% of the full input voltage range of the converter, which is significant. Moreover, since the Li-ion battery spends most of its life in a given discharge cycle within the 2.8–3.6 V range, this also means that the converter will be operating in the buck–boost mode for an extended period of time. For the aforementioned reasons, the efficiency of the converter in the buck–boost is quite critical.

Table I summarizes the key performance metrics of the converter, along with a comparison with other published work. The proposed converter occupies much smaller silicon area, and offers a significantly better dynamic performance (in terms of settling time and overshoot and undershoot) due to its adaptive slew-rate control scheme. The proposed converter also features higher switching frequency and smaller inductor, which further improves its dynamic response.

VI. CONCLUSION

A digitally assisted peak-current-mode buck–boost converter for extending the battery life of mobile devices operating from Li-ion batteries has been proposed. The converter employs adaptive slew-rate control to enable fast response to dynamic events, such as load, line, and output voltage steps, with significantly reduced overshoots and undershoots and settling time. Moreover, a hysteretic mode detector is incorporated to prevent false and repetitive mode transitions under noisy operating conditions. Along with the adaptive slew-rate control, hysteretic mode detection ensures seamless mode transitions under all input, output, and load conditions.

ACKNOWLEDGMENT

The authors would like to thank Dialog Semiconductor Inc. for financial, logistical, and chip fabrication support.

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