A 15-W Quadruple-Mode Reconfigurable Bidirectional Wireless Power Transceiver With 95% System Efficiency for Wireless Charging Applications

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***Abstract*—In this article, a 15-W quadruple-mode reconfigurable wireless power-receiving unit with high efficiency for Inductive coupling and magnetic resonance-based standards, such as wireless power consortium (WPC), power matters alliance (PMA), alliance for wireless power (A4WP), and magnetic secure transmission (MST) applications is proposed. Quadruple-mode gate controller(QMGC) is proposed in quadruple-mode synchronous rectifier to manage sizes of core and drivers which results in maximum power conversion efficiency (PCE) for each mode based on conduction and switching losses. In QMGC, switchable zero voltage and current sensing block is proposed for WPC/PMA to maximize PCE regardless of load current variations. For A4WP mode, a digitally controlled delay adjustment block is adapted to minimize power consumption while compensating for delay which results in reverse leakage current and power loss. Finally, for MST mode, low power TX (LPTX) block is implemented to minimize current consumption so that burden on battery can be minimized. A high-resolution current sensor is proposed in low-drop out regulator to sense current for overcurrent limit and overcurrent protection. The measured PCE of proposed system at 15 W are 95.3% and 92.3% for WPC/PMA and A4WP mode, respectively. For MST, power consumption is reduced to 35% courtesy LPTX block.**

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***Index Terms*—Alliance for wireless power (A4WP), high efficiency, magnetic induction, magnetic resonance, magnetic secure transmission (MST), power matters alliance (PMA), quadruple-mode active rectifier, wireless power consortium (WPC), wireless power receiving (WPR) unit.**

I. Introduction

WIRELESS power transfer (WPT) technology has been appeared as one of an efficient and resourceful technologies among power transfer, especially near-field (nonradiative) techniques, for wireless charging of the radio-frequency identifications (RFIDs), electric vehicles, buried sensors, portable electronic devices, and implanted medical devices [1]–[3]. Near-field WPT systems are popular for providing high power conversion efficiency (PCE) over short range and mid-range applications. Near-field techniques are mainly divided into two categories: inductive and capacitive coupling technique for short-range applications and magnetic resonance coupling technique for mid-range applications. Two of the most effective standards for short range applications are wireless power consortium (WPC) [4] and power matters alliance (PMA) which uses inductive coupling method. Moreover, they are accessible by the consumers to supply wireless chargers. The WPC/PMA standards have low and adjustable frequency ranging from 87–357 kHz for WPT system [5]–[8]. On contrary, magnetic resonance method is utilized in alliance for wireless power (A4WP) [9], [10] standard, which transfers the power over longer distance (few centimeters) than inductive coupling method. Generally, A4WP standard operates at 6.78 MHz, which is considerably greater frequency than the frequency range of WPC/PMA. However, PCE of the magnetic resonance method is much lower than the inductive coupling method in a WPT system. [11] reports resonant regulating rectifier (3R) working at 6.78 MHz for resonant WPT applications. In [12], a wireless power receiver using 3-mode rectifier operating at 6.78 MHz is proposed. In [13], a WPT transmitter is presented that can concurrently operate at 200 kHz and 6.78 MHz to simultaneously power-up two receivers operating at different frequency standards. Hui *et al.* [14] summarize

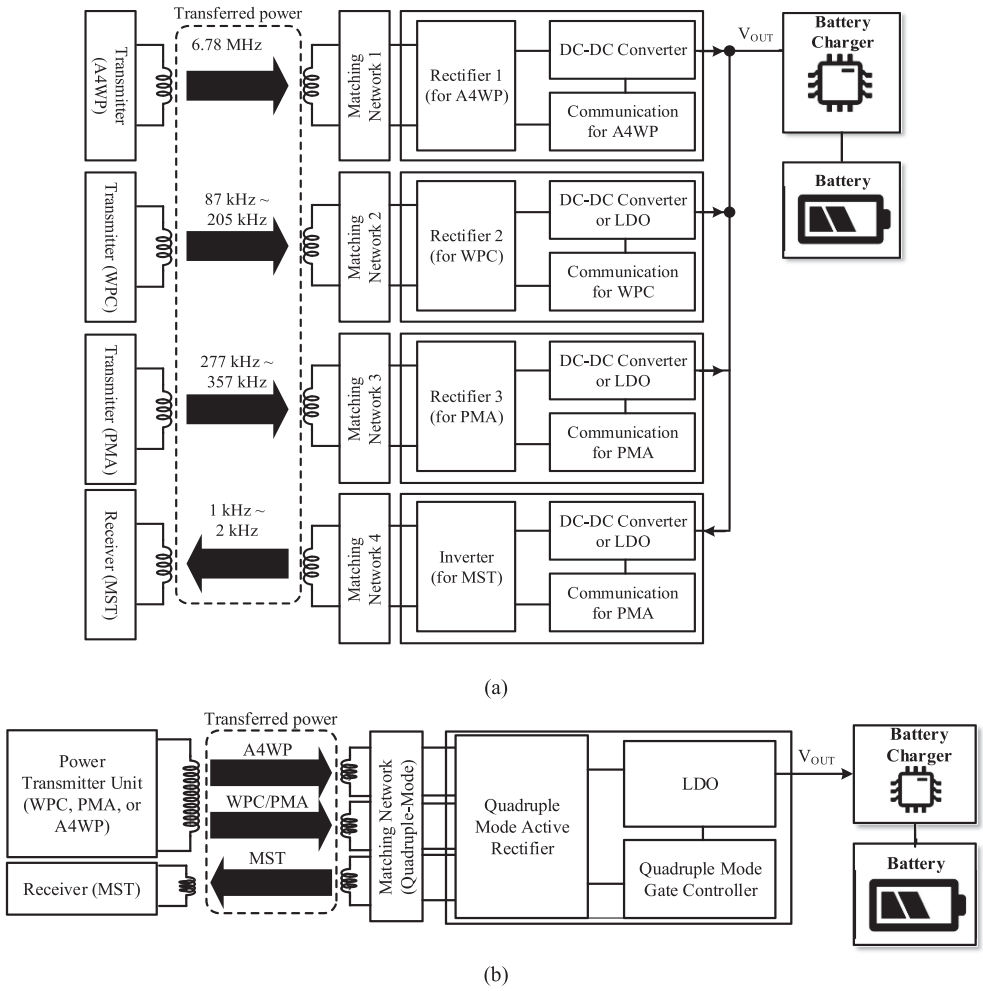


Fig. 1. Concept of the quadruple mode wireless power transceiver: (a) when it is implemented with separate systems; (b) when it is implemented as the proposed quadruple mode wireless receiving unit.

the wireless power research's operating principle into maximum power transfer and principles of maximum energy efficiency and how WPT system relates to them. In order to improve the convenience of a user, the WPT receiver must be capable of operating in the presence of any of the three wireless power transmitters (WPC, PMA, or A4WP). Furthermore, the WPT receiver must be highly efficient so that its high output power reduces the charging time of the user appliance. The devices which can operate at multiple standards provide remarkable benefits to operators and users. These multimode devices should have the ability to provide wireless charging without adding bulky hardware or long charging time. In [15], a multimode wireless power receiver unit charges the mobile from any of the three standards: WPC; PMA; or A4WP. On the other hand, if there are three individual ICs to separately support WPC/PMA and A4WP standards for the WPT system, there are drawbacks of larger area and increased cost [16]. In [17] and [18], a single resonator using lumped impedance matching and operating at two distinct frequencies for WPT is presented. The work in [17] operates at 6.78 and 13.56 MHz, while [18] operates at 11 and 36 MHz.

In addition to wireless power receiving (WPR) system supporting multiple standards, demands on the wireless power transceiver are also increased. Fig. 1(a) shows the concept of the wireless power transceiver. In wireless power transceiver, however, since the transmitter and the receiver are combined in a single chip, the current consumption and active area can be considerably saved compared to the separate transmitter and receiver systems, as shown in Fig. 1(b). As mentioned earlier, in case of implementing transmitter, several papers are presented for different applications such as A4WP power transmitter in wearable applications, or near field communication (NFC) applications [17], [18]. For mobile devices and wearable devices, WPT, NFC, and MST techniques have become significantly important as most of the applications support wireless charging, convenient mobile pay and digital wallet systems. Therefore, the proposed quadruple-mode wireless power receiving unit (WPRU) in this article supports four standards using single shared rectifier core to achieve high efficiency with smaller area. Since the rectifier can be used as the inverter, bidirectional ac/dc or dc/ac conversion can be achieved. Also, with the help of quadruple-mode gate controller (QMGC), the configuration and

high efficiency modes are automatically changed by sensing the detection of the three standards' operating frequencies.

Recently, transceiver's protection is becoming one of the major issues as WPT output power has been improved to lessen the multimode devices charging time. Heat flow from the transceiver must be insignificant when the output power is improved. For preventing these unwanted and undesirable accidents, a very accurate current sensing is needed to measure the output power and to limit the over-current which is defined from the system. In this article, a high-resolution current sensor is proposed to sense the output current and operates over current limit (OCL) and over current protection (OCP). The rest of the article is organized as follows. The architecture of the proposed quadruple-mode WPR system is explained in Section II. The sub-blocks implemented in proposed architecture are discussed in Section III. Section IV demonstrates the experimental results. Finally, in Section V, the proposed design is concluded.

II. Proposed Architecture of Quadruple-Mode WPR System

Fig. 2(a) presents a block circuit diagram of the proposed quadruple-mode reconfigurable wireless power-receiving unit (QWPRU), which is typically used to charge the mobile devices wirelessly. As shown in Fig. 2(b), power is delivered to the receiver's coils of the A4WP and WPC/PMA, by A4WP power transmitting unit (PTU) and WPC/PMA PTU, respectively. Meanwhile, the type of PTU can be selected by the QWPRU therefore it can take power from all kinds of PTU (WPC/PMA or A4WP), through the communication. For the MST application, battery voltage (VRECT) from the battery becomes the input, and the signals from QMGC drive the gates of power transistors (M_{N1}, M_{N2}, M_{N3}, M_{N4}) to generate the MST transmitting signals, V_{AC1} and V_{AC2}, as shown in Fig. 2(c). The QWPRU is composed of a quadruple-mode synchronous rectifier (QMSR), a low-drop out (LDO) regulator, a power-up circuit, a SAR Adc, a frequency detector, a digital logic block and a protection block. Furthermore, the quadruple-mode active rectifier produces dc power supply (V_{RECT}) from the received ac voltage (V_{AC}) with high efficiency. An output voltage (V_{OUT}) of 5 or 9 V, is provided by the dc–dc converter depending on the battery charger mode (normal or fast charging). In recent mobile devices, Li-Ion batteries are widely used, whose normal charging voltage is from 3 to 4.2 V, and input charging voltage and current are increased up to 9 V and 1 A for fast charging [19], [20]. The power-up circuit generated voltages are supply voltage (AVDD) and V_{TS}. The supply voltage to the internal circuitry is provided by the voltage AVDD while the thermal shutdown conditions are checked by V_{TS}. Subsequently, the overvoltage protection and thermal shutdown role is being done by the protection block. Data to the digital logic blocks are directed by the SAR Adc which first senses the analog information, such as V_{RECT}, V_{OUT}, and I_{OUT}. MST controls to start the Adc with start of conversion signal and Adc converts them into 12-bit digital data before transferring it to the digital logic block. When the data conversion is finished, Adc generates the end of conversion signal, and microcontroller unit (MCU) starts to compute from the data.

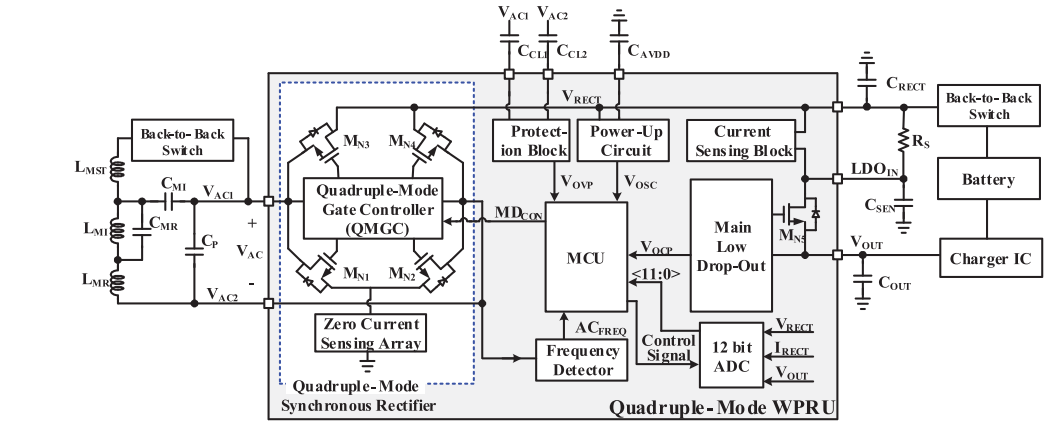
III. Proposed Architecture Building Blocks

A. Proposed Quadruple-Mode Synchronous Rectifier

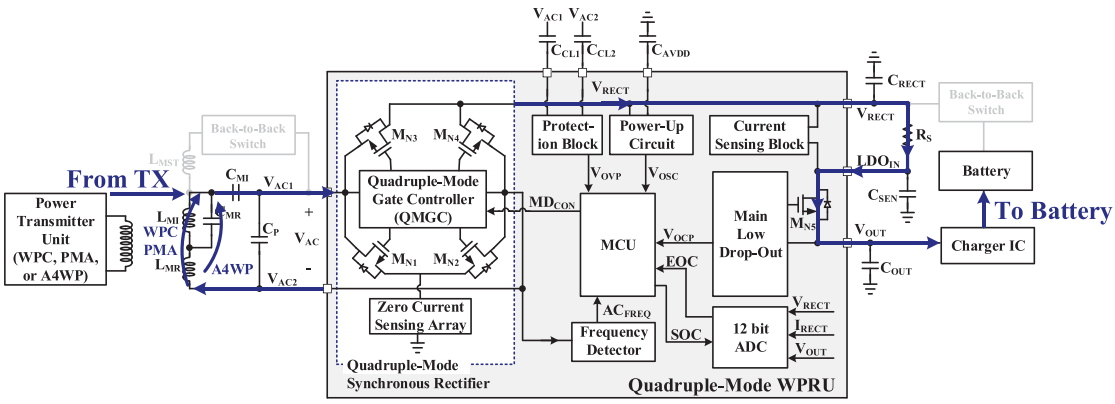
Fig. 3 shows the top block diagram of the proposed QMSR. The proposed QMSR has the QMGC to generate the input signals ($G_{I1} \sim G_{I4}$) of the drivers (LD1, LD2, HD1, and HD2). By QMGC, the proposed rectifier can produce the rectified voltage (V_{RECT}) in WPC, PMA, and A4WP mode. In MST mode, ac voltages (AC1, AC2) are generated for delivering power to the MST receiver. For the rectifier, R_{on} resistance of the rectifier core is very important to enhance the overall efficiency. Since the conduction loss is very critical for efficiency, R_{on} resistance should be very small in case of WPC and PMA modes. In order to reduce the R_{on}, LDMOS core should be designed as large as possible considering the overall layout size. When it comes to the A4WP mode, switching loss becomes more dominant than the conduction loss because of high frequency specification. In this case, proper size design is important considering the conduction loss and the switching loss. As a result, the overall core size becomes smaller than that of WPC and PMA modes. When the core size is decided in WPC and PMA modes, the core can be shared with A4WP and MST modes by dividing the core size. Only the driving mechanism is changed with different modes, supporting four modes using one core is possible with QMGC. As a result, overall size can be reduced over 80% compared to designing separate rectifier for each mode. When the ac signal inputs through frequency detector which consists of voltage limiter (VL), frequency detector sends the 1.5 V limited voltage signal ($\mathrm{ac_{FREQ}}$) to the MCU. MCU determines the current frequency and the mode by counting the $\mathrm{ac_{FREQ}}$ and controls the QMGC by mode control signal $\mathrm{MD_{CON}}$<1:0>. When the $\mathrm{MD_{CON}}$<1:0> is "00," "01," and "10," it represents the WPC/PMA mode, A4WP mode, and the MST mode, respectively.

The efficiency of the rectifier is mainly determined by the reverse leakage current, conduction loss and switching loss. Firstly, to avoid the reverse leakage current, core MOSFETs ($M_{N1} \sim M_{N4}$) should be turned-ON and turned-OFF properly with the timing of AC1 and AC2 by controlling the gate voltages ($G_{\mathrm{O1}} \sim G_{\mathrm{O4}}$). If G_{O1} and G_{O3}, or G_{O2} and G_{O4} are high at the same timing, the reverse leakage current will flow through M_{N1} and M_{N3}, or M_{N2} and M_{N4}, respectively, which result in the degradation of PCE of the rectifier. In WPC/PMA mode, to sense the reverse leakage current and generate the $G_{I1} \sim G_{I4}$, zero current sensing (ZCS) array is used to mirror the current flowing through M_{N1} and M_{N2}, and generate the corresponding voltages (V_{S1} and V_{S2}) of mirrored currents (I_{S1} and I_{S2}). The size of the mirroring MOSFETs (M_{S1} and M_{S2}) are designed and chosen as the ratio of 1/100 of the M_{N1} and M_{N2} to minimize the conduction loss through M_{N1} and M_{N2}. V_{S1} and V_{S2} become the input of the proposed SZVCS; and SZVCS generates the $\mathrm{O_{MD1\_1}}$ and $\mathrm{O_{MD1\_2}}$, which will be $G_{\mathrm{O1}} \sim G_{\mathrm{O4}}$ through the drivers.

The A4WP standard frequency is 6.78 MHz so that the parasitic capacitance becomes dominant compared to the WPC/PMA modes. The delays from circuit make the outputs of the driver ($G_{\mathrm{O1}} \sim G_{\mathrm{O4}}$) delayed so that M_{N1} to M_{N4} are not turned-ON and turned-OFF with the proper timing. It will generate the reverse



(a)



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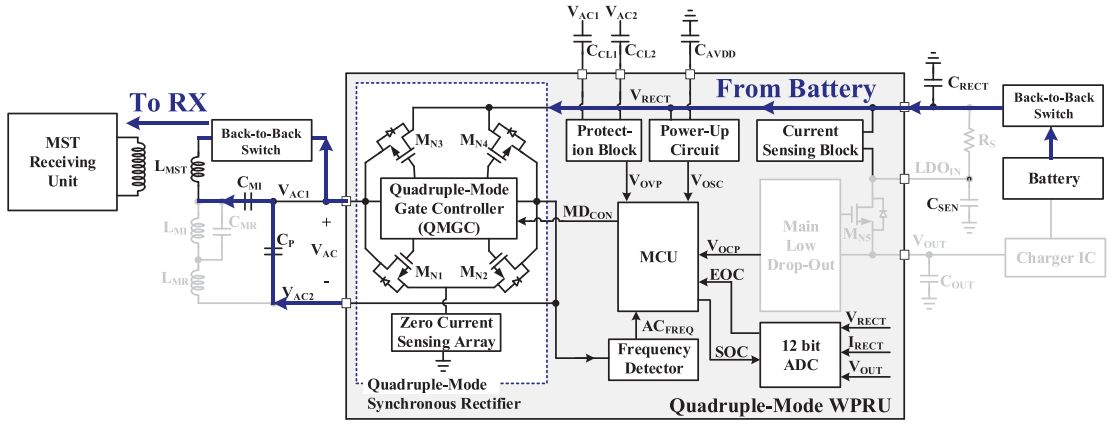

(c)

Fig. 2. (a) Block diagram of the proposed QWPRU. (b) Signal flow when operating in RX mode (WPC, PMA or A4WP). (c) Signal flow when operating in MST mode.

leakage current through M_{N1} and M_{N3}, or M_{N2} and M_{N4}, which will cause severe efficiency loss. In addition, consideration about the conduction loss cannot be matched with that of WPC/PMA modes. In WPC/PMA modes, to minimize the conduction loss and maximize the efficiency, the sizes of the core are intended to be made as huge as possible to reduce the $R_{\rm on}$ resistance. In the A4WP mode, however, when sizes of the core are large, the corresponding parasitic capacitances are increased so that the switching losses through $G_{\rm O1}$ to $G_{\rm O4}$ will generate the reverse leakage current. To make balance between conduction loss and

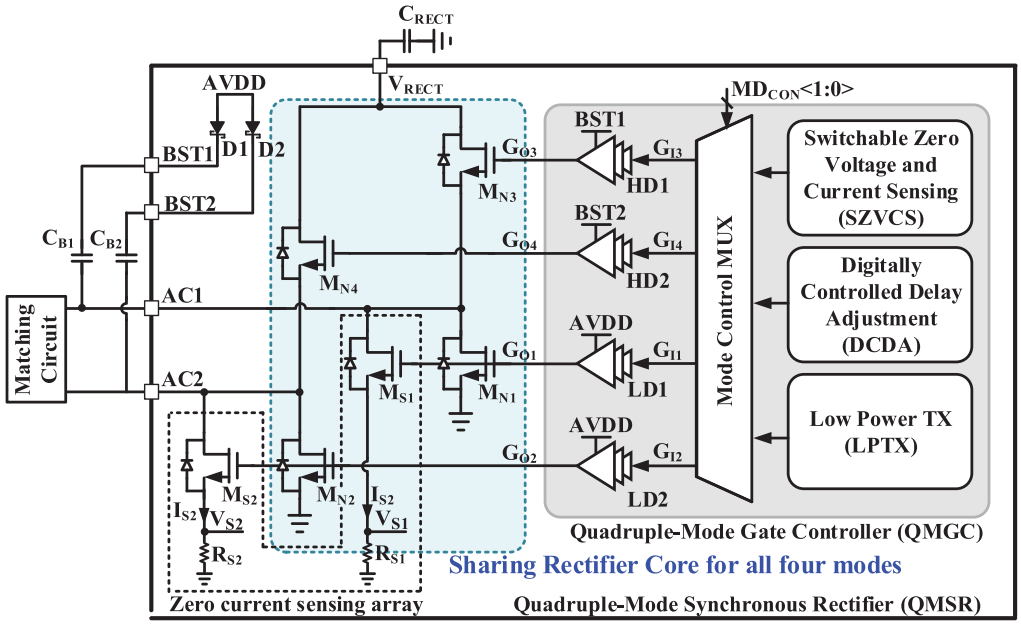

Fig. 3. Top block diagram of the proposed QMSR.

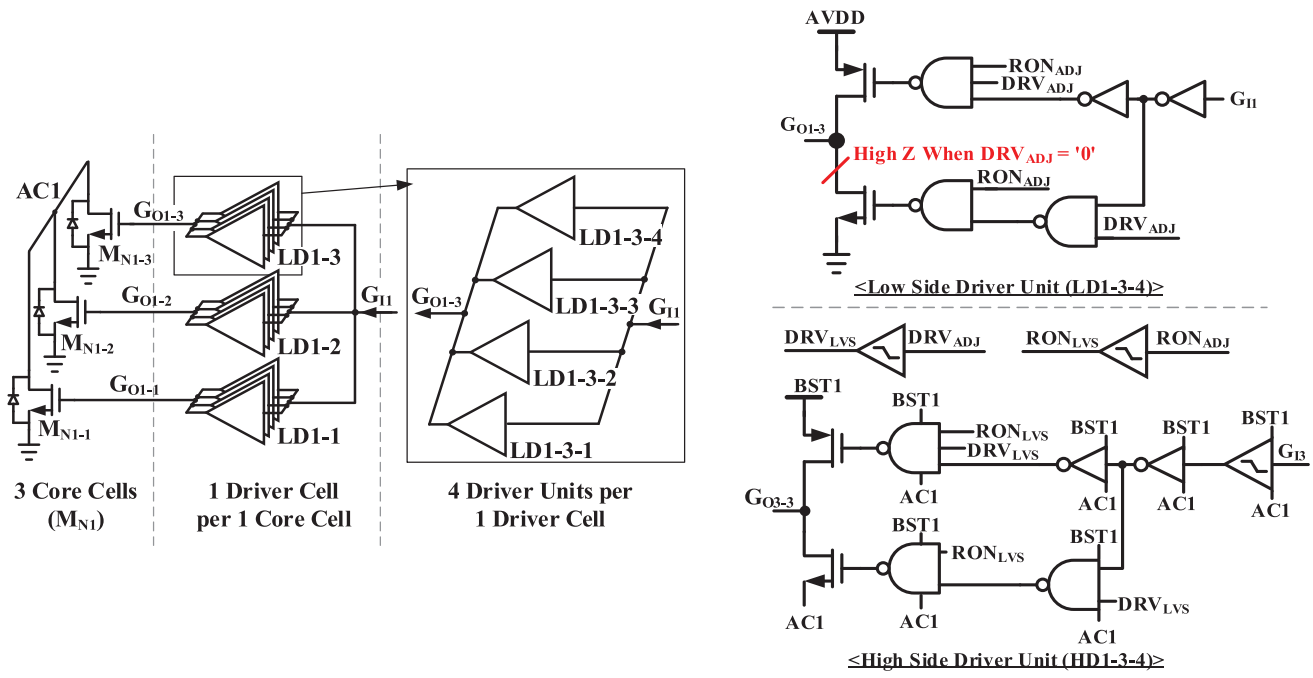

Fig. 4. Block diagram of the (a) overall driver architecture and (b) driver unit for the low side and high side.

switching loss and to maximize the conversion efficiency in all standards, sizes of the core and the sizes of the drivers can be controlled through QMGC. The size of the driver can be divided and controlled to 1/4, 2/4, 3/4, and 4/4. Similarly, for the core, it can be divided and controlled to 1/3, 2/3, and 3/3. In WPC/PMA/MST modes, the full size of the core and driver is used to minimize the conduction loss. In the A4WP mode, 2/3 of the core size and driver size are used considering the balance between conduction loss and switching loss through the simulation.

Fig. 4 explains about controlling the size of the driver and core. As can be seen from the Fig. 4(a), each core cell is driven by the single driver cell. The single driver cell is consisted of four driver units. If all of three driver cells are turned-ON

and driving the cores, the full size of core is operated for the synchronous operation. Fig. 4(b) is the detailed block diagram of the single driver unit. Strength of the driver is determined by the signal driver $(\mathrm{DRV})_{\mathrm{ADJ}}$, while $\mathrm{RON}_{\mathrm{ADJ}}$ has a role of enabling the core cell. For example, by the thermometer control of $\mathrm{DRV}_{\mathrm{ADJ}}<3{:}0>$, the strength can be controlled from 1/4, 2/4, 3/4 to 4/4. It affects the all driver cells simultaneously. $\mathrm{RON}_{\mathrm{ADJ}}$ is a enable signal of each driver cell from LD1-1 to LD1-3. By thermometer control of $\mathrm{RON}_{\mathrm{ADJ}}<2{:}0>$, three core cells of M_{N1} ($M_{N1\text{-}1}$, $M_{N1\text{-}2}$, and $M_{N1\text{-}3}$) can be turned on and off individually. The internal logics are implemented for making high impedance (high Z) when the driver unit is turned OFF to prevent avoiding output signals of other driver units. In the case of high side driver, since the signal should be level shifted for the boosting, level shifters are used for input signal G_{I3}, driver strength control signal $\mathrm{DRV}_{\mathrm{ADJ}}$, and the core size control signal $\mathrm{RON}_{\mathrm{ADJ}}$. All the logic gates inside are used as same as low side driver with the supply voltage (VDD) of BST1 (or BST2) and the ground (VSS) of AC1 (or AC2) since the V_{DS} and V_{GS} of the internal 5V MOSFETS can be guaranteed as 5 V.

B. Proposed Switchable Zero Voltage and Current Sensing (SZVCS)

Fig. 5(a) shows the block diagram of the proposed SZVCS. It is composed of zero voltage sensing (ZVS), ZCS, deglitch circuit, and mode selection block. In the magnetic resonance-based standard mode, such as WPC, PMA, MCU gives the $\mathrm{MD}_{\mathrm{CON}}<1{:}0>$ as "00" and the SZVCS starts to operate. For light load condition, $0 \sim 200$ mA, the $\mathrm{MD}_{\mathrm{OP}}$ is '0" so that the output of the ZVS (ZVS_SET) is selected from the mode selection block. ZVS directly gives the output voltage by comparing AC1 (or AC2) with V_{RECT}. In light load condition, comparator inside the ZCS (COMP2) may not detect the current from V_{S1} (or V_{S2}) since the amplitude of the V_{S1} is not large enough to be detected from the comparator reference voltage (V_{REFC}). Moreover, glitches from the system relatively affect the V_{S1} in the light load condition more than the heavy load condition so that the COMP2 cannot exactly compare the V_{CS1} and V_{REFC}. In order to solve the issues and for the stable operation of the rectifier, ZVS is used in the light load condition.

Using only ZVS at all load condition has the limited voltage-conversion efficiency since it requires large ac carriers across receiver (RX). To maximize the efficiency, when it comes to the heavy load condition, ZCS is used instead of ZVS by sensing zero current. Fig. 5(b) shows timing diagram of the proposed SZVCS. The zero current is detected from V_{CS1} and V_{REFC}, and ZCS_SET is generated. To generate stable ZCS output, De-glitch circuit is added after ZCS circuit. As mentioned, comparator may not produce the correct output signal when the glitches from the system affect the V_{CS1} or V_{REFC}. To prevent the issue, ZCS_SET and RST_{G1} from the deglitch circuit become the input of the D-flip flop in mode selection block and generates the $\mathrm{O}_{\mathrm{MD1\_1}}$. Same process is done for the $\mathrm{O}_{\mathrm{MD1\_2}}$ with AC2 and V_{S2}.

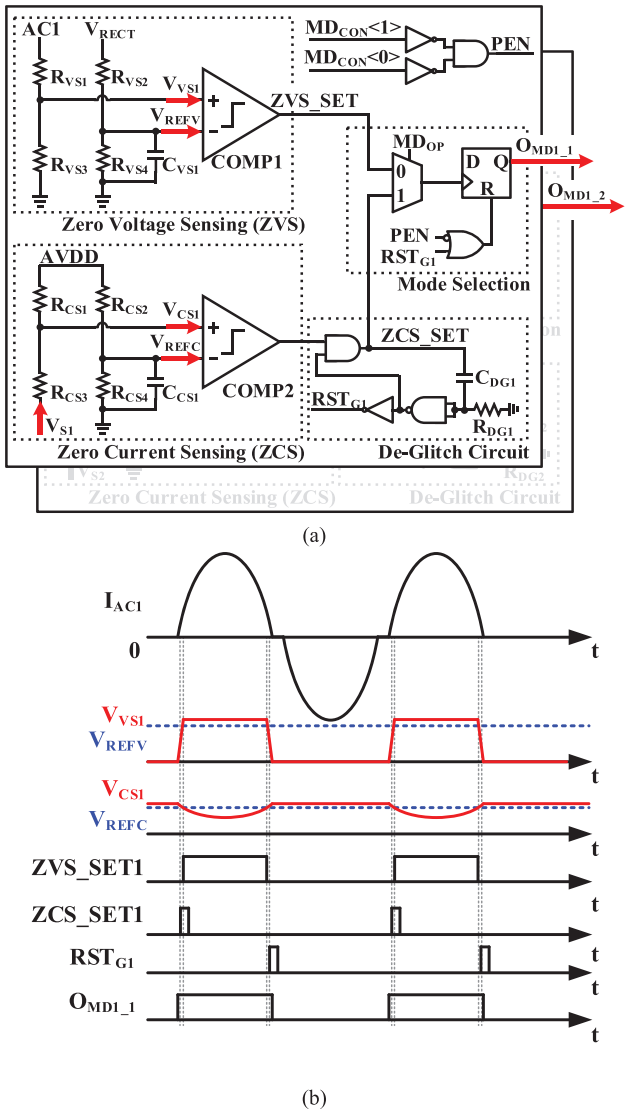

Fig. 5. Proposed SZVCS. (a) Block diagram. (b) Timing diagram.

C. Proposed Digitally Controlled Delay Adjustment (DCDA)

In A4WP mode, a DCDA block is presented to solve the problem of the reverse leakage current, which is caused by delays of internal circuits, including drivers, and to enhance the PCE. Fig. 6 shows block diagrams of the conventional analog delay locked-loop (DLL) with Replica delay and the proposed DCDA block. Fig.7 describes the timing diagram of the proposed DCDA. As it can be seen from Fig. 6(a), the analog DLL was frequently used to compensate for the internal circuit delay [21], [23]. A charge pump (CP), an analog phase detector (PD), and a voltage controlled delay line (VCDL) are used to implement the analog DLL. To calculate the circuit delay, replica delay is used, and the PD calculates the phase difference between limited ac voltage (V_{ACT}) and delayed signal through Replica delay (V_{REP}). Analog DLL can compensate for the delay with VCDL so that the resolution can be relatively high compared to the digital DLL. However, the replica delay needs the tuning

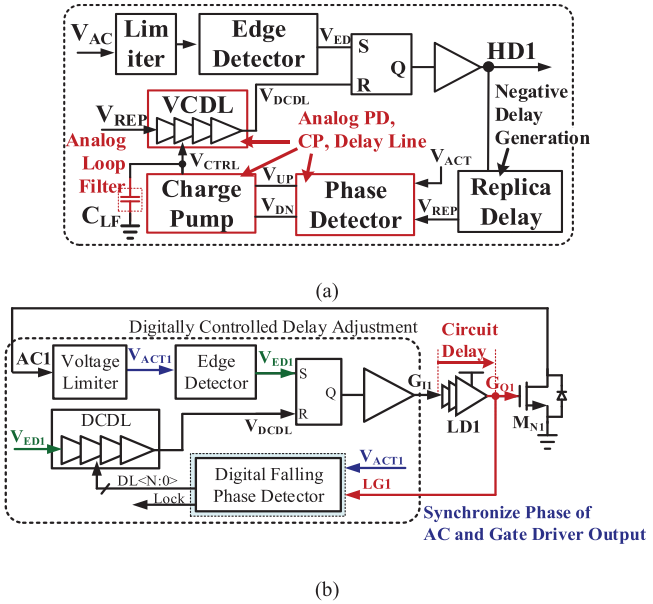

Fig. 6. Block diagram of the (a) conventional analog DLL with replica delay, and (b) proposed DCDA.

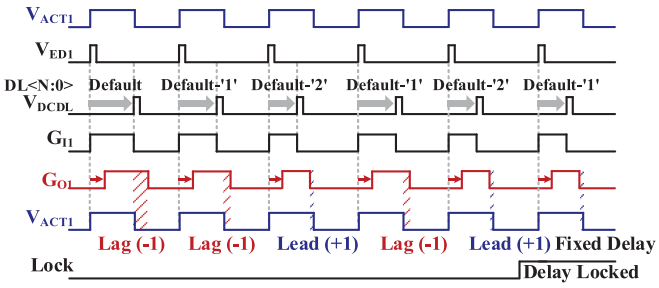

Fig. 7. Timing diagram of the DCDA.

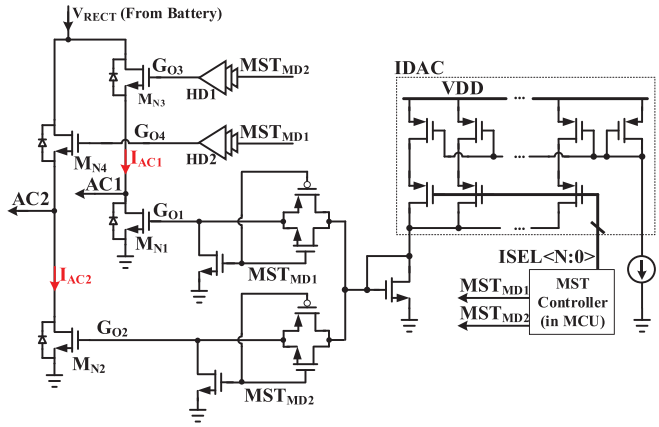

Fig. 8. Block diagram of the proposed LPTX block.

before the operation since it needs to calculate the circuit delay, and the size of the analog DLL is large compared to the digital DLL because of the analog Loop filter and the varactor inside the VCDL. Fig. 6(b) shows a block diagram of the proposed DCDA which is for the M_{N1}. This consists of a VL, edge detector (ED), SR Latch, digital controlled delay line (DCDL), and digital falling PD (DFPD). The purpose of DCDL shown in Fig. 6(b) is to synchronize the falling edge of *AC*1 and G_{O1}. From the DCDL, M_{N1} can be turned off at the exact time when the AC1 goes negative voltage and AC2 rises to positive voltage. Compared to the analog DLL shown in Fig. 6(a), since the output of the driver directly goes to the DFPD, the additional replica delay is not needed. Moreover, since there is no external loop filter and the varactor, the size can be reduced, and the overall current consumption also can be minimized.

As can be seen from the Fig. 7, DFPD is used to compare the falling edge of V_{ACT1} and G_{O1}, which are the limited voltage signal of AC1 and the final gate control signal of M_{N1}, respectively. First, through the VL, AC1 is limited as V_{ACT1}, and edge signal V_{ED1} is generated through ED. V_{ED1} becomes the input of DCDL and generates the V_{DCDL} by the delay cells inside the DCDL. SR latch generates the G_{I1} from V_{ED1} and V_{DCDL} and it becomes the input of the gate driver LD1. Since the LD1 has the circuit delay, G_{I1} is delayed as G_{O1}, and it causes the leakage current. Since the dominant reason of leakage current is the turn-OFF timing of M_{N1}, DFPD compares the V_{ACT1}, which represents the AC1 signal, and the G_{O1} to synchronize the falling edges of these two signals. As can be seen from the Fig. 7, DL<*N*:0> starts from default value and generates the default delay value. At the first comparison point, G_{O1} is lagging to the V_{ACT1}, the value of DL<*N*:0> becomes default-"1," and the delay is decreased. At the next timing, since G_{O1} is still lagging, DL<*N*:0> is decreased again and at the third point, it is leading the V_{ACT1} so the DL<*N*:0> becomes default-"1" again. From the DFPD, when the lag and the lead operations are repeated two times, lock signal is generated and the DFPD stops to compare and the delay is locked until the MCU resets the DCDL.

D. Low Power TX (LPTX)

When the rectifier operates as a transmitter, TX, the operation is same as a full bridge (FB) inverter. Figs. 8 and 9 illustrates the circuit block diagram of the proposed LPTX block and its timing diagram. MST controller in MCU generates $\mathrm{MST_{MD1}}$ and $\mathrm{MST_{MD2}}$ for the switching operation. M_{N1} and M_{N4} are turned ON simultaneously while M_{N2} and M_{N3} are turned OFF. Similarly, M_{N2} and M_{N3} are turned ON at the same time while M_{N1} and M_{N3} are turned OFF. The purpose of the LPTX is to reduce the I_{AC1} and I_{AC2} which flow through M_{N1} and M_{N2}, respectively. From the MST Controller, ISEL<*N*:0> is controlled by turning all the current sources from ON to gradually OFF from most significant bit (MSB) to least significant bit (LSB). At the beginning, ISEL<*N*:0> starts with its maximum value for the fast transition. While M_{N1} and M_{N4} are turned ON, with the conventional static dc operation, the current consumption must be relatively high since the longest on-duty cycle while MST communication is around 80 μs from the MST standard, and also, R_{on} resistance is minimized. The idea is to minimize the current consumption at the on-duty cycle. For that operation, MST Controller controls the G_{O1} and G_{O2} by controlling the

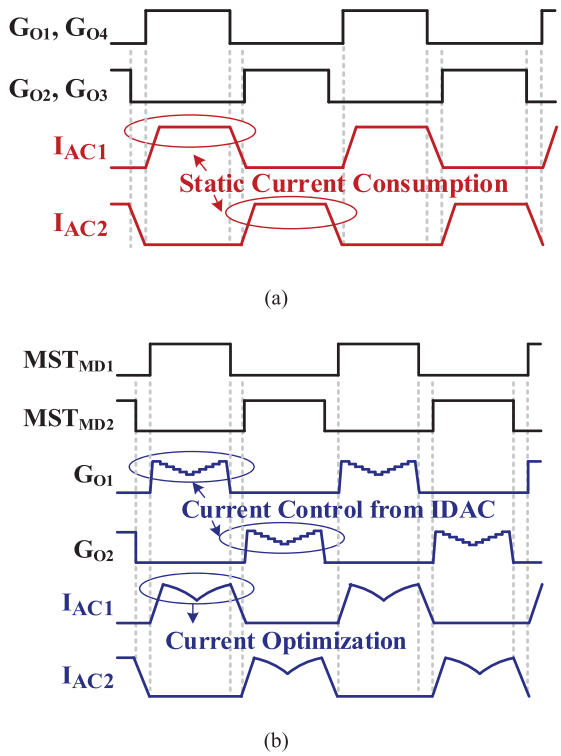

Fig. 9. Timing diagram of the proposed LPTX. (a) Conventional full driving. (b) Proposed low power driving.

current DAC (Current Digital to Analog Converter) (IDAC) from ISEL<*N*:0>. Fig. 9 shows the timing diagram of the proposed LPTX and its operation. As can be seen from the Fig. 9(b), the G_{O1} and G_{O2} can be controlled from IDAC by changing the ISEL<*N*:0> gradually. In the result, the slope of the I_{LG1} and I_{LG2} can be controlled and the current consumption can be reduced compared to the conventional MST operation illustrated in Fig. 9(a). From the simulation and measurement results, current consumption can be reduced up to 35% at the same test condition while maintaining the MST operation pass condition. The detailed results are discussed in Section IV.

E. Proposed Main Low Drop-Out With Current Sensor

Fig. 10 presents the circuit diagram of the main LDO (MLDO) regulator with current sensor. MLDO is implemented and placed after the rectifier so that it can generate the clean dc voltage from the VRECT. Since the N-type MOSFET is used for the MLDO, the CP is implemented and boosts the V_{OUT} voltage to turn on the M_{NLDO} so that V_{GS} of M_{NLDO} can be guaranteed as 5 V when the core MOS is turned ON. To provide the load current information and OCL operation, the proposed MLDO includes the current sensor. The proposed current sensor mirrors the main current from M_{NLDO} with the certain ratio. From the resistors *R*2 and *R*3, mirrored current is converted to V_{ILIM}. V_{ILIM} becomes the input of the current limit controller and is compared with V_{REF}. From the Current limit controller, feedback voltage signal (V_{FEED}) is selected between feedback voltage (VFB) and current limiter voltage (VILIM).

Fig. 11 illustrates the detailed block diagram of the current sensor and the current limit controller. In Fig. 11(b), when the V_{ILIM} exceeds the reference voltage of the comparator, the overall feedback voltage of the MLDO (V_{FEED}) is switched from V_{FB} to V_{ILIM}, so that the output current can be limited. By this hardware controlled OCL operation, the immediate reaction of the over current can be activated, otherwise it needs a certain time to wait until the Adc processes the current and the MCU provides the OCL signal to the MLDO.

IV. Experimental Results

The proposed chip is fabricated in 0.18 μm Bipolar-CMOS-DMOS (BCD) technology, using high-voltage MOSFET, five metals and on poly. The active die area of QWPRU IC 2.7 mm $\times$ 3.9 mm. Fig. 12 shows the microphotograph of the proposed chip.

Fig. 13 shows measurement environment of the proposed QWPRU IC. From the power amplifier and TX coil, the ac power is applied through the RX coil. From the RX coil and matching network, the proposed IC regulates the ac voltages into dc voltage. The output voltage, VOUT, is attached with an electronic load for measuring 15 W output power with 1.66 A, when the output voltage reaches 9 V.

Fig. 14 demonstrates the results obtained from the measurement of the proposed SZVCS. When the rectifier is in passive operation, the core power MOSFETs ($M_{N1} \sim M_{N4}$) are turned OFF and the current flows through the back diodes of power MOSFETs. As can be seen from the Fig. 14(a), the difference between ac signals (AC1, AC2) and V_{RECT} is relatively high compared to the difference when synchronous operation. That is because of the voltage drop of the back-diode, which is around 700 mV. When the rectifier is in synchronous operation, the power MOSFET is turned ON and its voltage drop is around 100 mV from the R_{on} resistance. Fig. 14(a) and (b) shows the two different conditions which are the light load condition and the heavy load condition. As mentioned in Section III-B, under 200 mA load condition, MCU sets the SZCVCS as the ZVS mode, which is the measurement result of Fig. 14(a) when the load current of 150 mA flows. Since the purpose of the ZVS operation is the stability, reference voltage of comparator in Fig. 5(a), V_{REFV}, is set as minimum so that the synchronous operation period is almost half of the passive operation. In the Fig. 14(b), which is operated as ZCS mode, load current of 1.2 A condition was measured so that the 15 W condition can be tested. For maximizing the efficiency, optimum value of reference voltage of ZCS comparator in Fig. 5(a), V_{REFC}, is selected and the almost every whole period can be operated as synchronous operation.

Fig. 15 presents the simulation results of the proposed DCDA. The output of the VL is V_{ACT1} which limits the ac input to 5 V voltage domain. From the V_{ACT1}, the DCDA generates the DCLK1, which is 1 of the 8 dividing clocks of V_{ACT1}. Since the Rectifier needs to be settled with the response time after the digital delay is changed, DCLK1 is used as digital clock of the DCDA to compensate for the response time. DCDA synchronizes the falling edge of the ac signal with the driver output signal (LG1). Since the DCLK1 and LG1 are the inverted

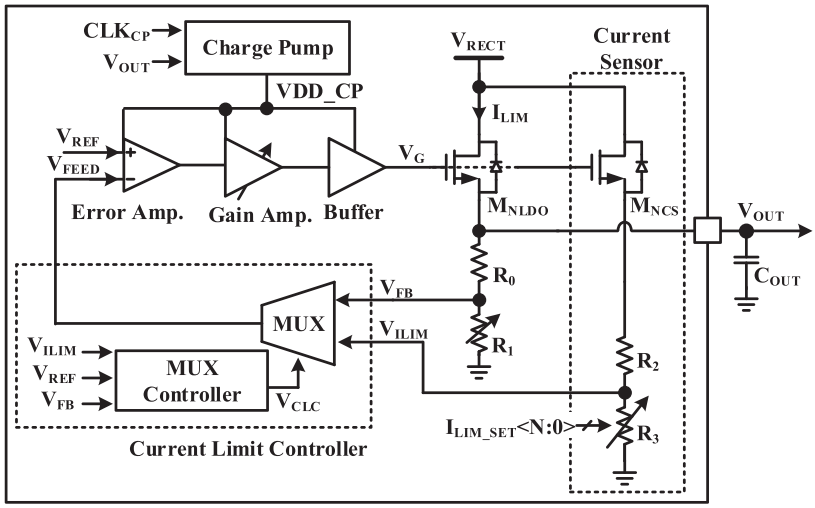

Fig. 10. Block diagram of the main LDO regulator.

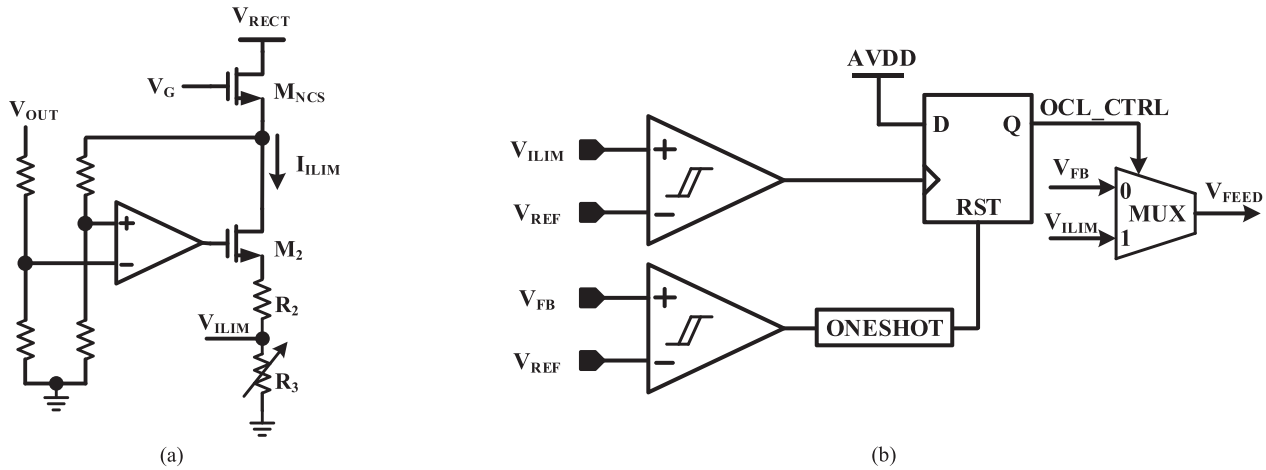

Fig. 11. Block diagram of the (a) current sensor and (b) current limit controller.

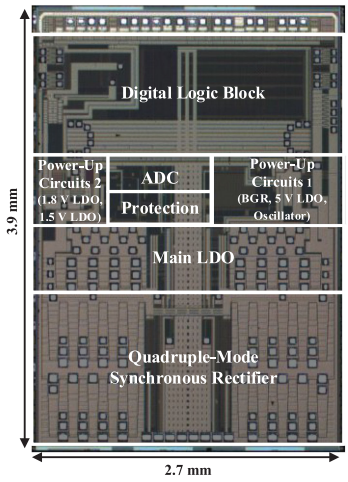

Fig. 12. Microphotograph of the proposed QWPRU chip.

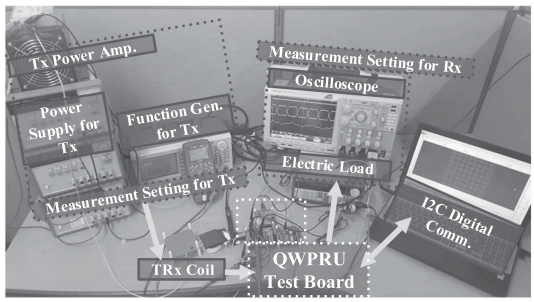

Fig. 13. Measurement environment of the proposed QWPRU IC.

phase signals of the ac signal and the driver output signal, the rising edge of both signals are compared, and when the DCLK1 is leading the LG1, the delay will be adjusted as +1, since the driver output needs to be delayed for synchronization.

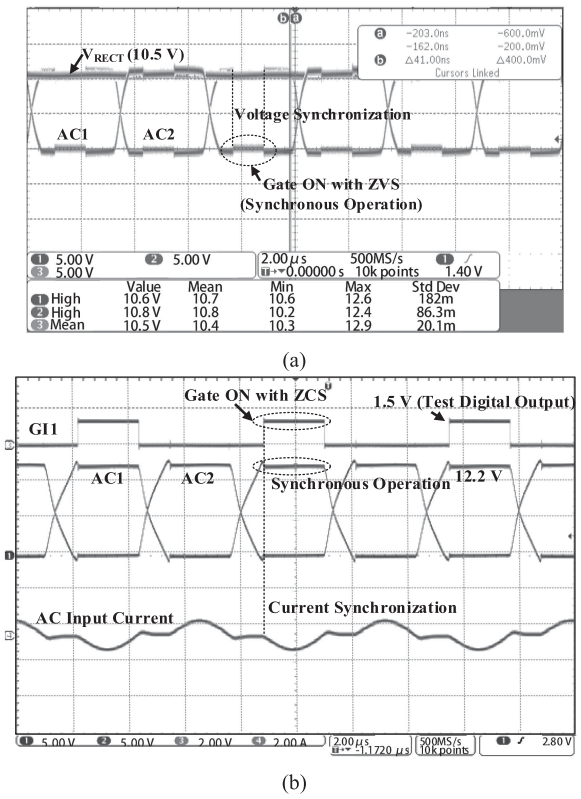

Fig. 14. Measurement result of the proposed SZVCS. (a) ZVS, and (b) ZCS operation.

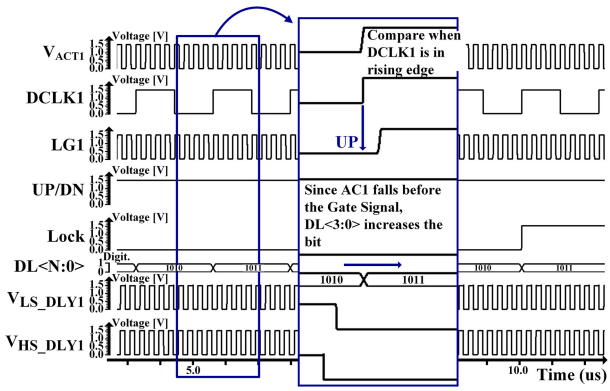

Fig. 15. DCDA simulation results.

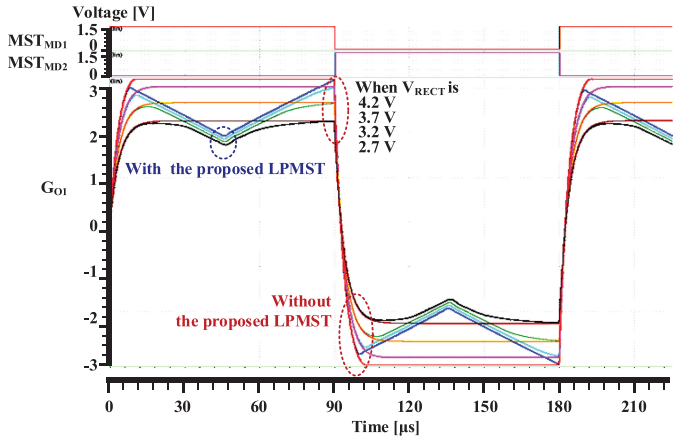

Fig. 16. Simulation waveforms of the proposed LPTX.

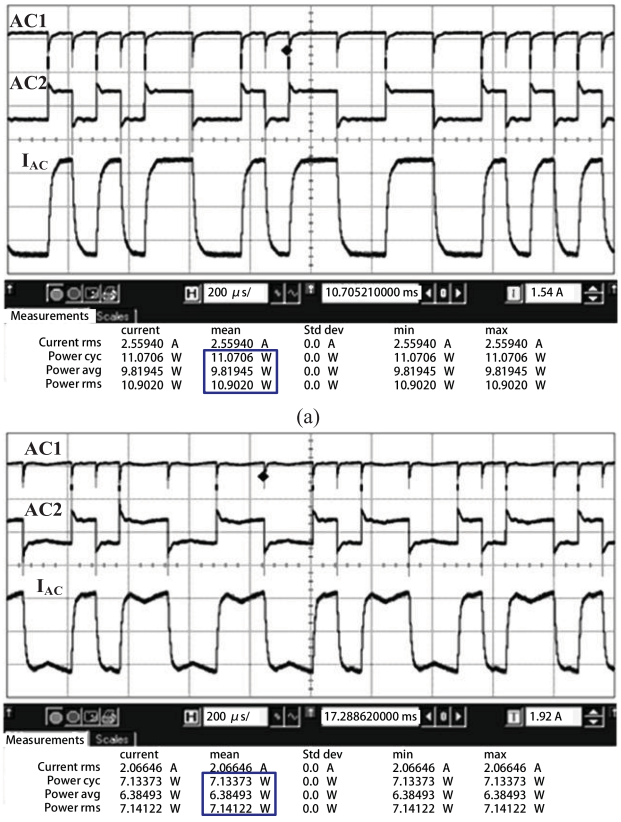

Fig. 17. (a) Conventional and (b) the proposed waveforms of the rectifier in MST mode.

Fig. 16 shows the simulation waveforms of LPTX when the V_{RECT} (Battery) is from 4.2 to 2.7 V considering battery discharge. Simulation has done with comparison between the proposed LPTX and the conventional MST mode operation (without the proposed LPTX). Through the simulation result, the proposed LPTX can operate in various battery situations, and it also always exceeds the threshold level for the transmission.

Fig. 17(a) and (b) present the measured waveform of the conventional and the proposed rectifier as the MST mode. As it can be seen from Fig. 17(a), the conventional current waveform of the rectifier has rectangular shape with static current while AC1 and AC2 are turned-ON and turned-OFF, respectively. From the oscilloscope calculator function, we can get the average and rms power consumption of the conventional MST mode and the proposed LPTX mode at the same measurement condition when the output voltage swing of AC1 and AC2 are 5 V. The average and rms power consumption of the conventional MST mode is 9.82 and 10.9 W, respectively, and in the proposed LPTX mode, 6.38 and 7.14 W, respectively. As can be seen from the calculation, both for the average and rms power consumption,

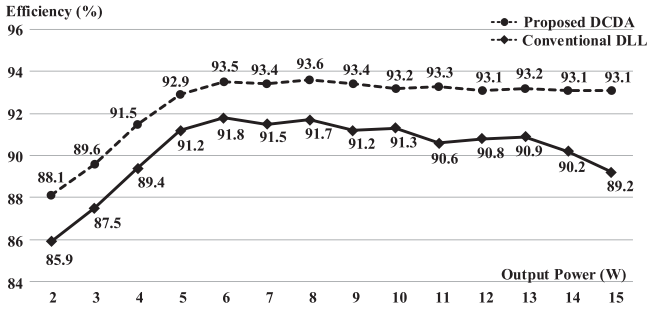

Fig. 18. Efficiency comparison of rectifier using the proposed DCDA and conventional analog DLL.

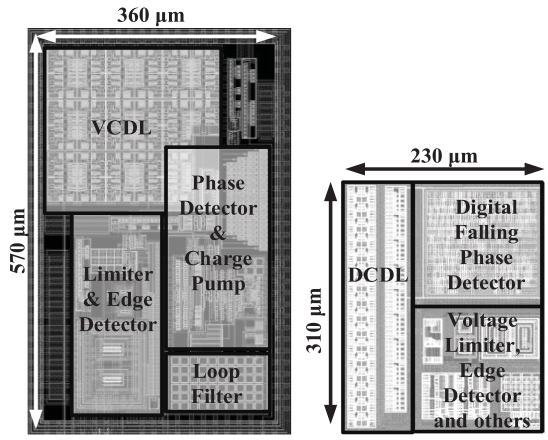

Fig. 19. Layout size comparison between (a) the conventional analog DLL and (b) the proposed DCDA.

the LPTX mode achieve over 35% less current consumption than the conventional MST mode.

Fig. 18 shows the efficiency comparison of the rectifier using the proposed DCDA and the conventional analog DLL. The measurement comparison has done with the test IC which was already implemented with analog DLL counterpart similar with [21]. The comparison is done with the same test condition when the output voltage V_{RECT} is 12 V. As it can be seen from the Fig. 18, when using the proposed DCDA, the efficiency is increased minimum by 2% compared to the conventional analog DLL. Fig. 19 shows the layout comparison of analog DLL and the proposed DCDA with the same process. As can be seen from the result, the size of the conventional analog DLL is 0.2 mm^2 while the size of the proposed DCDA is 0.07 mm^2, which achieves 65% size reduction. Moreover, the current consumption of analog DLL at the simulation level is 1 mA, while the proposed DCDA consumes 650 μA at the same simulation condition of V_{RECT} is 12 V. As a result, along with size reduction of 65% and the current consumption reduction of 35%, the efficiency of the proposed DCDA is increased 2% compared to analog DLL.

Fig. 20 shows the WPC efficiency results of rectifier and full path. The system efficiency is calculated from the input power of the rectifier to the output power of the rectifier and LDO.

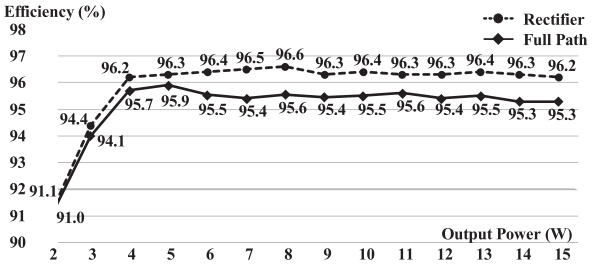

Fig. 20. WPC efficiency results of (a) rectifier and (b) full path.

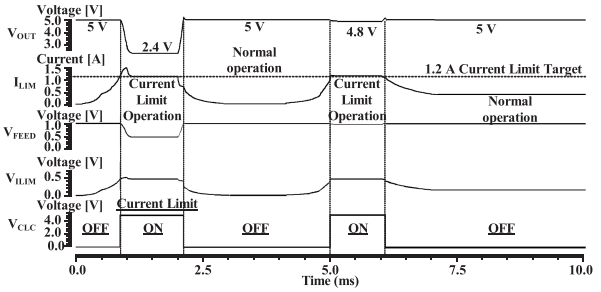

Fig. 21. Simulation result of the proposed current sensor.

TABLE I
COMPARISON OF REPORTED RELATED WPRUS AND THIS ARTICLE

Parameters	**This Work**	[16]	[21]	[22]
Technology	**0.18 µm BCD**	0.18 µm BCD	0.18µm BCD	0.35 µm BCD
Supported standards	**WPC, PMA, A4WP and MST**	WPC, PMA and A4WP	A4WP	A4WP
Input frequency	**85 ~ 500 kHz / 6.78 MHz**	85 ~ 500 kHz / 6.78 MHz	6.78 MHz	3.23 MHz /6.78 MHz
Maximum Efficiency of rectifier (%)	**96.2 @ 150 kHz 93.6 @ 6.78 MHz**	92.7 @ 150 kHz 91.7 @ 6.78 MHz	91.5	81 @ 3.23 MHz 74 @ 6.78 MHz
Maximum System Efficiency (%)	**95.3 @ 150 kHz 92.3 @ 6.78 MHz**	85.5 @ 150 kHz 84.5 @ 6.78 MHz	80.86	75
Max. Output Power (W)	**15**	9	5	3
Die Area (mm^2)	**10.66**	17.2	12.25	18.3

As it can be seen from the results, rectifier maintains efficiency over 96.2% from 4 to 15 W. When it comes to the RX full path, efficiency becomes 95.3% at 15 W from the ac input to the main LDO output (V_{OUT}).

The simulation result of the proposed current sensor has been presented in Fig. 21. When I_{LIM} exceeds the current limit target

level, which is 1.2 A in this simulation, current sensor senses the current and current limit controller changes the V_{CLC} from the V_{FB} to V_{ILIM}. As can be seen from the Fig. 21, V_{FEED} is changed from V_{FB} to V_{ILIM} as the V_{CLC} goes from 0 to 5 V. When V_{FEED} is changed to V_{ILIM}, the voltage goes down and the output voltage V_{OUT} also goes down from 5 to 2.4 V by the LDO feedback. When the current I_{LIM} goes down under current limit target level, V_{FEED} is again switched to V_{FB} and the normal MLDO operation can be done.

Table I gives the comparison of reported related WPRUs and this article. This article supports four different standards while other references support a maximum of three standards. From the standards, input frequency can be changed from 85–500 kHz and 6.78 MHz. The efficiency of the rectifier and system at the output level of 15 W is 96.2% and 95.3%, respectively, which is the highest among the references even though the maximum output power is 15 W. The die area of the proposed QWPRU is 10.66 mm^2, which is the smallest among other references.

V. Conclusion

This article presents a high efficiency 15 W QWPRU for wireless charging applications utilizing WPC, PMA, and A4WP, and magnetic secure transmission standards. The QMGC is implemented in the QMSR to manage the core sizes of the rectifier. The optimized core and driver sizes are selected to achieve maximum PCE for each mode in terms of conduction and switching losses. The SZVCS block is proposed in the QMGC for WPC/PMA modes to obtain maximum PCE regardless of the load current variations. The DCDA block is implemented for A4WP to minimize power consumption and sizes while compensating for the delay which results in the reduced reverse leakage current and power losses. Finally, for the MST mode, LPTX block is adapted to minimize the current consumption so that burden of the battery can be minimized. In LDO voltage regulator, a high-resolution current sensor is proposed to sense the current for OCL, OCP, and for output power calculation. The proposed chip is fabricated and implemented in 0.18 μm BCD technology, with an active area of 5.0 mm $\times$ 3.5 mm. The measurement results show that peak PCEs of the proposed system at 15 W are 95.3% and 92.3% for the WPC/PMA and A4WP mode, respectively.

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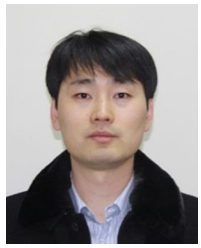

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