Modular Multilevel DC–DC Power Converter Topology With Intermediate Medium Frequency AC Stage for HVDC Tapping

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***Abstract*—This article proposes an isolated dc–dc modular multilevel converter (MMC) topology intended for tapping power from the high-voltage dc (HVdc) link. The proposed converter operates with two stages of power conversion, i.e., HVdc to ac and ac to medium-voltage dc, using an intermediate medium-frequency transformer. The proposed topology reduces the number of arms in MMC to two, along with a series *LC* passive filter tuned at a medium frequency at the primary side of the transformer. A high-voltage transformation ratio is possible in the proposed converter. Operation at the medium-frequency ac ensures the reduction in the size of the transformer and other passive elements. A sinusoidal level-shifted pulsewidth modulation technique is implemented for modulating the arm voltages of the converter, which results in a voltage close to the sine wave with small *dv/dt* being impressed across the transformer primary. The design of the passive filters is also included in the article. The operation of the converter is validated by the simulation of a 400 kV, 10 MW system, and a downscaled experimental prototype of 1 kW, 400 V system.**

***Index Terms*—DC–DC converter, high-voltage dc (HVdc), medium-voltage dc (MVdc), modular multilevel converter (MMC), passive *LC* filter.**

I. Introduction

HIGH-VOLTAGE dc (HVdc) technology is becoming a preferred choice in the long-distance high-power transmission, in particular after the introduction of a modular multilevel converter (MMC) [1], [2]. With the growing penetration of renewable energy sources, the next-generation HVdc transmission would demand the integration of renewable energy sources mainly from off-shore wind farms and photovoltaic generation [3], [4].

HVdc tapping stations are possible solutions in this direction and are established in order to extract or inject a small amount of power from/to the local ac grid, e.g., 1%–10% of the total capacity of the HVdc transmission line [5]–[7]. In the HVdc tapping, an HVdc network (e.g., hundreds of kilovolt) is interfaced with a medium-voltage dc (MVdc) network (tens of kilovolt) and a small amount of power exchange (e.g., hundreds of kilowatt to tens of megawatt) takes place [6], [7]. Fig. 1 shows the diagram of the HVdc tapping, where a dc–dc converter is an interface between the HVdc line and the local ac grid. One of the important requirements of the dc–dc converter in the HVdc tapping is to provide a high-voltage transformation ratio or high step ratio between the HVdc-side voltage V_H and MVdc-side voltage V_L.

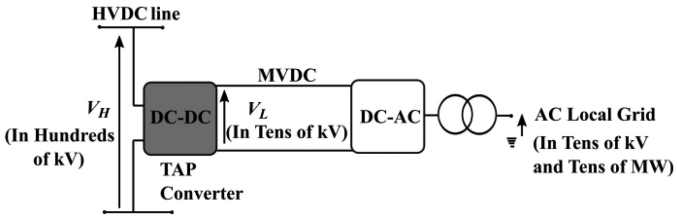

Fig. 1. HVdc tapping [6].

Significant research has been going on to implement MMC for the dc–dc power conversion [1]–[4]. A higher degree of modularity and flexible scalability are the key features of MMC, which make it well suited for HVdc applications.

In recent years, many MMC-based topologies are reported in the literature for interfacing high- and medium-voltage dc networks. Primarily, there are two kinds of MMC-based dc–dc topologies available, which can be classified under nonisolated [6], [8]–[10] and isolated versions [2], [11]–[16]. Another type of converters used in the HVdc applications is resonant dc–dc converters [17], [18]. These converters provide a high-voltage transformation ratio but they lack modularity in the structure.

Nonisolated MMC-based topologies have been reported in [8]–[10]. These converters are transformerless high-voltage dc–dc converters and are intended for the dc-grid interconnection (MVdc and HVdc). In these converters, an internal ac current (circulating current) flows in the arms to maintain the cell voltages balanced while transferring the dc power from the input HVdc side to the output MVdc side. Many of the nonisolated topologies require passive *LC* filters as a part of the converter to prevent the circulating ac current flowing into the dc side [6], [8], [9]. The magnitude of ac circulating current increases as the voltage transformation ratio increases, which reduces

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the efficiency of the converter, thereby limiting the application of these converters to a low voltage transformation ratio [6], [10].

In order to achieve a high-voltage transformation ratio, improve efficiency, and provide isolation, several MMC-based isolated topologies have been proposed for the HVdc application [2], [11]–[16]. Isolated topologies generally have two stages of power conversion, i.e., dc to ac and ac to dc with an intermediate medium-frequency transformer. Both Lüth *et al*. [2], and Jovcic and Zhang [11] propose an MMC-based dc–dc converter through an intermediate three-phase ac conversion, where six arms have been used in each MMC. When the tapped power from the HVdc link is small (e.g., hundreds of kilowatt to tens of megawatt), six arms of MMC may not be needed and a reduction in the number of arms of MMC is possible. A modification in this direction have been proposed in [12]–[14]. Kenzelmann *et al.* [12] discuss an MMC dc/dc converter with two MMCs (four arms of MMC) connected through a medium-frequency transformer.

Different switching strategies for running this converter are discussed in [13]. A further reduction to two arms of MMC is proposed in this article. In all the isolated dc–dc topologies, there is an intermediate ac transformer [2], [12]–[16]. Kenzelmann *et al.* [12] use the medium-frequency transformer but implements a square wave modulation technique, which will create a high *dv/dt* stress at the transformer terminals. A trapezoidal medium-frequency modulation technique has been proposed in [15] and [16] to provide a less *dv/dt* stress at the transformer terminals. In the proposed topology, the *dv/dt* stress has been further reduced by imposing a sinusoidal voltage waveform across the transformer primary.

In particular, for the HVdc tapping application, many MMC-based converters are proposed in the literature. A scalable dc–dc resonant converter has been proposed in [7], which contains a high-voltage valve consisting of series-connected switches and many series cells containing three switches and one capacitor. One drawback of this converter is the requirement of a large number of switches. An improved resonant multistage dc–dc converter is proposed in [18] with lesser number of components as compared with [7] and [19]. The drawbacks of these resonant converters are the lack of isolation and offer a high voltage or current stress on the devices.

This article proposes a new isolated MMC-based dc–dc converter topology, which uses only one leg (two arms) of MMC. It is an improvement over [12]–[14] in terms of reducing the arms of the converter. The proposed converter topology provides a high-voltage transformation ratio and is meant for tapping power from an HVdc line. The converter allows the bidirectional power flow with an intermediate medium-frequency transformer. A range of medium ac frequencies, such as 200 Hz, 250 Hz, 300 Hz, 350 Hz, 400 Hz, 450 Hz, 500 Hz and 1 kHz has been chosen as the intermediate ac frequencies in many existing isolated topologies [2], [12]–[15], while in this work 350 Hz has been chosen. A sinusoidal level-shifted (LS) pulsewidth modulation (PWM) is used to create a sinusoidal ac voltage at the primary side of the transformer. With many cells in the arm, the *dv/dt* stress at the transformer terminal will be substantially less. The main advantages of the proposed converter over other isolated converters can be summarized as follows.

1) A high-voltage transformation ratio is achieved.
2) It uses only one leg (two arms) of MMC, which significantly reduces the complexity and cost of the converter.
3) The voltages impressed across the transformer terminals are close to a sinewave with very less *dv/dt* stress.
4) Operation at the medium-frequency ac (350 Hz) will reduce the size of the transformer and other passive elements.

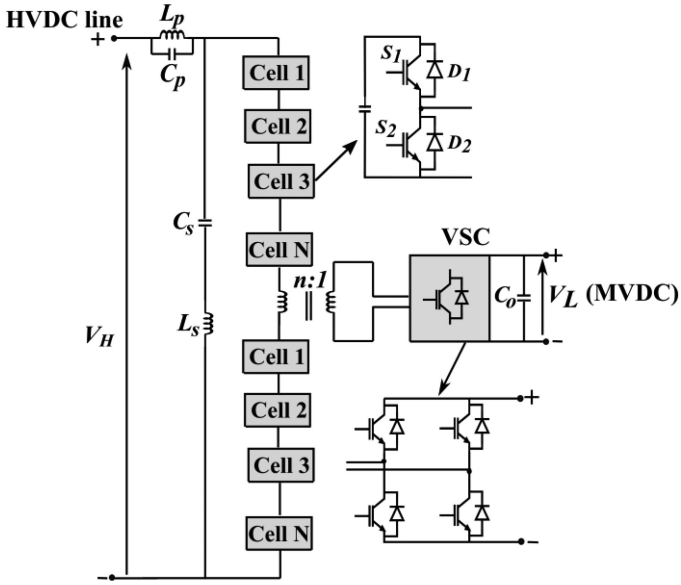

Fig. 2. Proposed MMC-based dc–dc converter.

II. Proposed DC–DC MMC

A. Converter Architecture

The proposed circuit topology of the MMC-based dc–dc converter is illustrated in Fig. 2. It consists of one dc–ac MMC with two arms and one ac–dc voltage source converter (VSC) interconnected through a transformer. Each arm of MMC has a number of cascaded power cells having either a half-bridge or full-bridge configuration. The proposed topology has been implemented by using half-bridge cells. MMC is connected to the HVdc side and VSC is connected to the MVdc side. The intermediate medium-frequency transformer is connected across the output of MMC arms. There are two filter circuits on the primary side, which are tuned at the fundamental medium-frequency ac. The series *LC* filter (L_s and C_s) is connected in parallel with the two arms of MMC. It provides a path for the fundamental medium-frequency ac current to circulate through both the arms of MMC and transformer but it prevents the flow of the dc current. The parallel *LC* filter (L_p and C_p) is connected in series with the HVdc lines and it is used to oppose the fundamental ac component of the current flowing into the HVdc line.

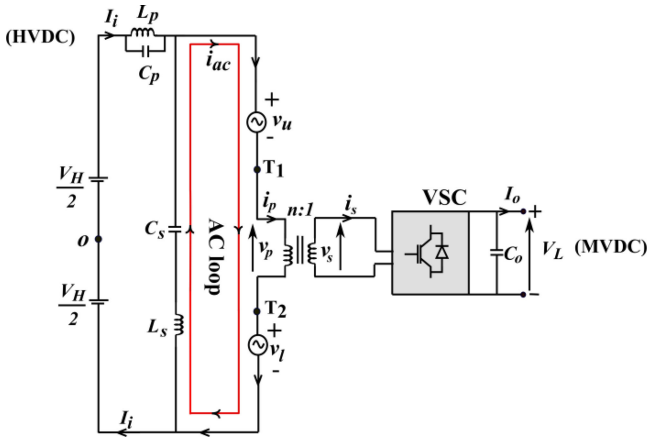

Fig. 3. Equivalent circuit diagram of the proposed converter.

B. Operating Principle

The equivalent circuit diagram of the proposed converter is shown in Fig. 3. The upper and lower arm cells are modulated using the sinusoidal PWM technique, and hence, can be represented as controllable voltage sources, i.e., $v_u(t)$ and $v_l(t)$ (neglecting the switching frequency harmonics). The primary and secondary voltages of the transformer are shown as $v_p(t)$ and $v_s(t)$ respectively. The dc voltage transformation ratio G_v of the proposed converter is given by

$$G_v = \frac{V_H}{V_L}. \tag{1}$$

Assuming the ideal switches in each power cell and negligible drop across the passive filters, the upper arm and lower arm instantaneous voltages of the MMC can be modulated to produce

$$v_u(t) = v_l(t) = v_{\text{arm}}(t) = \frac{V_H}{2}(1 - m_{a1}\sin\omega t) \tag{2}$$

where m_{a1} is the modulation index of the reference voltages of both the arms and ω is the fundamental ac frequency. As observed from (2), both the arm voltages have one dc and one ac component [see Fig. 4(a)].

The dc and ac components of the arm voltages are given as

$$V_{\text{dc}} = \frac{V_H}{2} \tag{3}$$

$$v_{\text{ac}}(t) = \frac{V_H}{2} m_{a1}\sin\omega t = \frac{V_{m1}}{2}\sin\omega t. \tag{4}$$

The voltage across the transformer primary $(v_p(t))$ is given by

$$v_p(t) = v_{T_1T_2}(t) = v_{T_1o}(t) - v_{T_2o}(t). \tag{5}$$

The voltage at $v_{T_1o}(t)$ and $v_{T_2o}(t)$ can be written as

$$v_{T_1o}(t) = \frac{V_H}{2} - v_u(t) = \frac{m_{a1}V_H\sin\omega t}{2} \tag{6}$$

$$v_{T_2o}(t) = -\frac{V_H}{2} + v_l(t) = -\frac{m_{a1}V_H\sin\omega t}{2}. \tag{7}$$

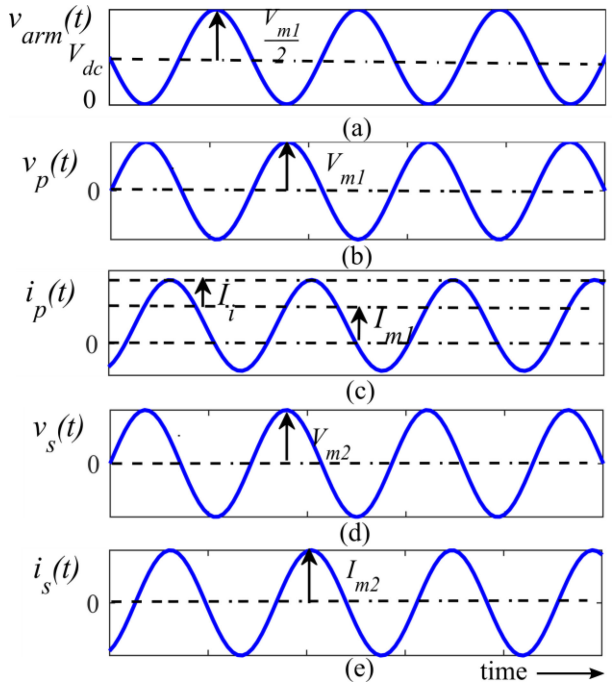

Fig. 4. Ideal waveforms. (a) Arm voltage. (b) Transformer primary-side voltage. (c) Arm current. (d) Transformer secondary-side voltage. (e) Transformer secondary-side current.

Thus, using (6) and (7) in (5), the voltage at the primary side of the transformer $(v_p(t))$ can also be written as

$$v_p(t) = m_{a1}V_H\sin\omega t = V_{m1}\sin\omega t \tag{8}$$

where V_{m1} is the peak amplitude of the ac voltage [see Fig. 4(b)]. Note that the voltage appearing across the transformer primary does not contain the dc voltage component present in the arms.

As $0 \le m_{a1} \le 1$, from (2), it can be said that [20]

$$0 \le v_u(t) \le V_H \tag{9}$$

$$0 \le v_l(t) \le V_H. \tag{10}$$

Thus, the voltage rating of both the upper and lower arm voltage sources is equal to V_H. If there are "N" number of power cells in each arm, then the voltage rating of each power cell will be $V_{\text{cell}} = \frac{V_H}{N}$. The fundamental ac voltage $(V_{m1}\sin\omega t)$ at the medium frequency causes a fundamental ac current to flow through the upper and lower arms of MMC, transformer, and the series *LC* filter circuit, which is shown as the ac loop in Fig. 3. During the process of the transfer of power from HVdc to MVdc, the cell capacitors in the arm will be charged/discharged. The fundamental ac current is essential to keep the cell capacitor voltages balanced [21]. The input dc current circulates through the arms of MMC, the transformer, and the parallel *LC* filter. In steady state, the current flowing through the arms of MMC and the transformer primary side has a dc and an ac component and is given by [22]

$$i_p(t) = i_{\text{ac}}(t) + I_i \tag{11}$$

where $i_{\text{ac}}(t)$ is the fundamental ac current and I_i is the input dc current, as shown in Fig. 4(c). The fundamental component

of the current, i.e., $i_{\rm ac}(t)$ can be written as

$$i_{\rm ac}\left(t\right) = I_{m1}\sin\left(\omega t - \varphi\right) \tag{12}$$

where I_{m1} is the peak value of the fundamental current in the primary side of the transformer and φ is the angle between the fundamental voltage and current.

The voltage at the secondary side of the transformer depends on the turns ratio (n:1) of the transformer [see Fig. 4(d)] and is given by

$$v_s\left(t\right) = V_{m2}\sin\omega t = \frac{v_p\left(t\right)}{n} = \frac{V_{m1}\sin\omega t}{n} \tag{13}$$

where V_{m2} is the peak value of the transformer secondary voltage. The current flowing through the secondary side of transformer $(i_s(t))$ is given by

$$i_s\left(t\right) = I_{m2}\sin\omega t \tag{14}$$

where I_{m2} is the peak amplitude of the fundamental current in the transformer secondary side [see Fig. 4(e)]. In the secondary side of the transformer, a medium-voltage VSC is connected, which acts as the ac–dc converter. The output dc voltage of the VSC obtained is

$$V_L = \frac{V_{m2}}{m_{a2}} \tag{15}$$

where m_{a2} is the modulation index of the reference voltages of the VSC. Using (8), (13), and (15) with $(m_{a2} = m_{a2} = 1)$, the voltage transformation ratio G_v of the proposed converter can be derived as

$$G_v = \frac{V_H}{V_L} = \frac{V_{m1}}{V_{m2}} = n. \tag{16}$$

From (16), it can be said that a high-voltage transformation ratio or step ratio (G_v) can be achieved in the proposed converter topology.

C. Arm Energy Balance

During the steady-state operation of the converter, the input power and output power of the converter are

$$P_{\rm in} = V_H I_i \tag{17}$$

$$P_{\rm out} = V_L I_o. \tag{18}$$

Neglecting the losses in the converter in steady state

$$P_{\rm in} = P_{\rm out}. \tag{19}$$

The magnitude of I_{m1} flowing in the arms of MMC is given by

$$I_{m1} = \frac{2P_{\rm out}}{V_{m1}\cos\varphi}. \tag{20}$$

For the proper operation of the proposed converter topology, the energy balancing of the upper and lower arm in the MMC is essential. The instantaneous power flowing into the upper arm and lower arms of MMC is described as

$$p_u = p_l = v_u i_p = p_{\rm arm}. \tag{21}$$

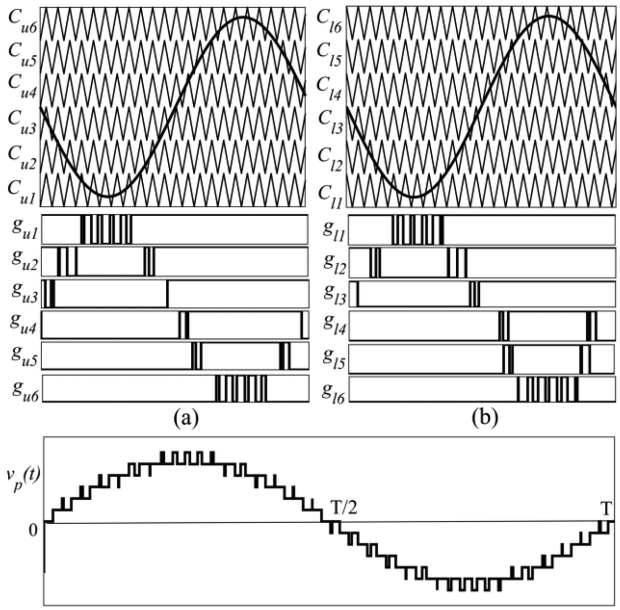

Fig. 5. LS-PWM technique. (a) Upper arm modulation. (b) Lower arm modulation.

By using arm voltage (2) and arm current (11) into (21), the instantaneous arm power $(p_{\rm arm})$ equation can be written as

$$p_{\rm arm} = \frac{V_H}{2}\left(1 - m_{a1}\sin\omega t\right) \times \left(I_{m1}\sin\left(\omega t - \varphi\right) + I_i\right). \tag{22}$$

The instantaneous arm power has both ac fundamental and dc component and can be written as

$$p_{\rm DC\_arm} = \frac{V_H I_i}{2} - \frac{1}{4}m_{a1}V_H I_{m1}\cos\varphi \tag{23}$$

$$p_{\rm AC_{arm}} = \frac{V_H I_{m1}}{2}\sin\left(\omega t - \varphi\right) - \frac{m_{a1}V_H I_i}{2}\sin\omega t + \frac{m_{a1}V_H I_{m1}}{4}\cos(2\omega t - \varphi). \tag{24}$$

In steady state, to ensure an arm energy balance, the average dc power of each arm $(p_{\rm DC\_arm})$ must be equal to zero. Thus

$$\frac{V_H I_i}{2} = \frac{1}{4}\left(m_{a1}V_H\right) I_{m1}\cos\varphi\,. \tag{25}$$

Equation (25) shows the essential condition for the arm energy balance [22].

D. PWM Technique and Sorting Algorithm

In the proposed topology, the LS sinusoidal PWM technique is implemented. If there are *N* number of power cells in each arm of MMC, *N* number of equally spaced identical triangular waves are required in LS-PWM. Fig. 5 shows the LS-PWM technique where the triangular carriers in the upper and lower arms are phase shifted by 180°. The phase shift between the carriers helps in increasing the number of levels at the converter output voltage. If there are *N* number of power cells in each arm of MMC, it is possible to produce $2N + 1$ number of levels at the converter output voltage by providing 180° phase shift between the upper and lower arm carriers. The implementation

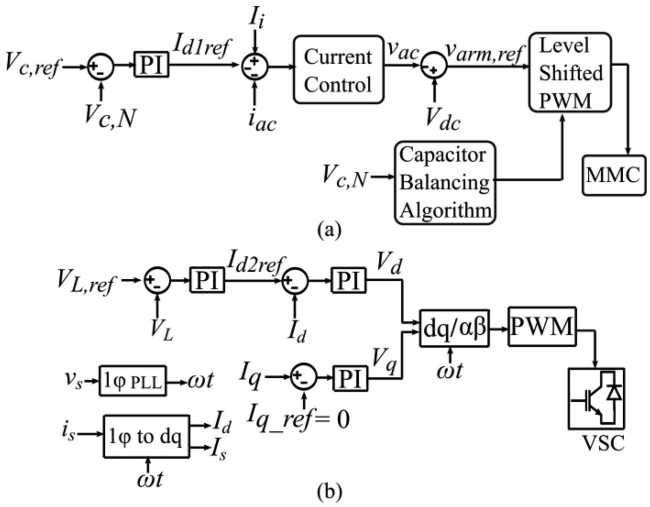

Fig. 6. Control block diagram. (a) MMC control scheme on the primary side of the transformer [23]. (b) VSC control scheme for ac to dc conversion in the secondary side of the transformer [16].

of the LS-PWM technique (see Fig. 5) results in the shifting of the effective switching frequency at the converter output voltage from f_s to $2f_s$.

The control block diagram of the MMC and the VSC in the proposed topology is shown in Fig. 6 [23]. In Fig. 6(a), the outer loop shows the average capacitor voltage control followed by a current controller, which generates the reference voltages of arms. The LS-PWM technique combined with voltage balancing is implemented to generate the required gate pulses for the MMC. The voltage balancing in the power cells is achieved by applying a well-known sorting algorithm [23]. Fig. 6(b) shows the conventional control scheme of VSC for the ac to dc conversion in the *d-q* reference frame [16]. In the secondary-side control scheme, the outer loop maintains the output dc voltage constant and the inner current loop controls the active power component while making the reactive component to zero to ensure the unity power factor at the transformer secondary side.

E. Filter Design

The impedance of the series *LC* filter ($Z_s(\omega)$) in the frequency domain is given by

$$Z_s(\omega) = (R_s + j\omega L_s) + \frac{1}{j\omega C_s}. \tag{26}$$

The tuning frequency (ω_{os}) of the series *LC* filter is given by

$$\omega_{os} = \frac{1}{\sqrt{L_s C_s}}. \tag{27}$$

The quality factor of the series filter inductor is given by

$$Q_s = \frac{\omega L_s}{R_s}. \tag{28}$$

In the proposed topology, the series *LC* filters are tuned at the fundamental medium ac frequency. Thus, this filter becomes a very low impedance path (ideally short circuit) for the fundamental ac frequency component and provides a very high impedance (ideally open circuit) for the dc component, as shown in Fig. 7(a) and (b), respectively. The impedance of the parallel *LC* filter ($Z_p(\omega)$) in the frequency domain is given by

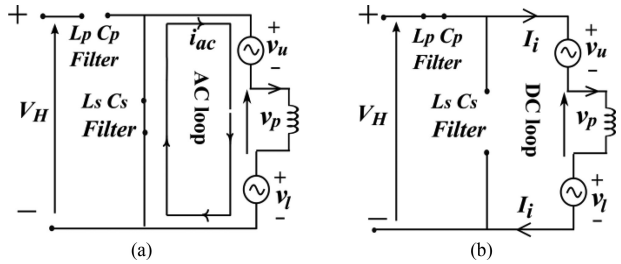

Fig. 7. Simplified equivalent circuit of the proposed converter at the primary side in ideal conditions. (a) AC equivalent circuit. (b) DC equivalent circuit.

$$Z_p(\omega) = \frac{R_p + j\omega L_p}{j\omega R_p C_p - \omega^2 L_p C_p + 1}. \tag{29}$$

The tuning frequency of the parallel *LC* filter is given by

$$\omega_{op} = \sqrt{\frac{1}{L_p C_p} - \left(\frac{R_p}{L_p}\right)^2}. \tag{30}$$

The quality factor of the parallel filter inductor is given by

$$Q_p = \frac{\omega L_p}{R_p}. \tag{31}$$

The parallel *LC* filter is also tuned at the fundamental ac frequency in the proposed topology. It provides a very high impedance (ideally open circuit) for the fundamental ac frequency component and acts as a low impedance (ideally short circuit) for the dc component, as shown in Fig. 7(a) and (b), respectively.

F. Sizing of Filter Components

The passive *LC* filters used in the distribution systems can be implemented in large sizes of several MVA ratings [24]. The size or cost of the passive *LC* filters depends on their VA ratings. The ac voltage imposed across the series *LC* filter is $v_p\ (t) = V_{m1}\ \sin\omega t$ and the current flowing through it is $i_{\rm ac}(t)\ = I_{m1}\ \sin(\omega t - \varphi)$. The VA rating of the series *LC* filter can be written as

$$S_{fs} = v_{p,\rm rms} \times i_{\rm ac,rms} = \frac{V_{m1}}{\sqrt{2}} \times \frac{I_{m1}}{\sqrt{2}}. \tag{32}$$

The voltage imposed across the parallel *LC* filter is very small. The current flowing through the parallel filter is dc, i.e., I_i. Thus, the VA rating of the parallel *LC* filter is very small. The size or cost of filter inductors can be evaluated from their area products and the cost or size of filter capacitors depend on their VA rating [25], [26]. The calculation of the area product of the filter inductors is given in Appendix B.

G. Variation of Filter Parameters

The sharpness of tuning depends on the quality factor Q of the filters. Tuning factor δ of a filter is defined as the amount

TABLE I
VARIATION OF PARAMETERS

Parameters	Value (%)
Frequency (Δf)	±1%
Inductance (ΔL)	±2%
Capacitance (ΔC)	±5%

TABLE II
PARAMETERS OF THE PROPOSED CONVERTER

Converter Parameters	Simulation	Experiment
Power Rating, $\|P\|$	10 MW	1 kW
HVDC voltage, V_H	400 kV	400 V
MVDC voltage, V_L	50 kV	200 V
Number of cells in each arm, N	6	3
Fundamental frequency, f	350 Hz	350 Hz
Switching frequency in MMC, f_s	2 kHz	2 kHz
Carrier frequency in VSC, f_c	2 kHz	2 kHz
Cell Capacitance, C	6 mF	1 mF
Series filter inductance, L_s	2.5 mH	1 mH
Series filter capacitance, C_s	82.6 µF	206 µF
Parallel filter inductance, L_p	2.5 mH	1 mH
Parallel filter capacitance, C_p	82.6 µF	206 µF
Transformer turns ratio, *n:1*	8:1	2:1

of detuning from the nominal tuned frequency and can be written a

$$\delta = \frac{\omega - \omega_o}{\omega_o} \tag{33}$$

where $\omega_{os} = \omega_{op} = \omega_o$. Due to aging or temperature rise, there may be variations on the values of *L* and *C*. Under such conditions, the tuning factor δ can also be expressed as [27]

$$\delta = \frac{\Delta f}{f} + \frac{1}{2}\left(\frac{\Delta L}{L} + \frac{\Delta C}{C}\right). \tag{34}$$

Table I illustrates the maximum variation of the parameters in industrial filters [24], [27].

The impedance of the series *LC* filter can be rewritten in terms of the nonidealities, such as quality factor Q_s and tuning factor δ, and it is given by

$$Z_s(\omega) = R_s + jQ_sR_s\left(\frac{\delta(2+\delta)}{(1+\delta)}\right). \tag{35}$$

Similarly, the impedance of the parallel *LC* filter can be rewritten as

$$Z_p(\omega) = \frac{R_p + j(1+\delta)Q_pR_p}{1-(1+\delta)^2 + j\frac{(1+\delta)}{Q_p}}. \tag{36}$$

The impact of the filter parameter variation on the performance of the proposed converter topology is analyzed. The tuned filter component values given in the simulation parameters in Table II are used for the analysis. Consider that the filter capacitance increases by 5%, filter inductance increases by 2%, and fundamental ac frequency increases by 1%. Using (34), the tuning factor δ calculated is 0.045. The quality factors of both the filters are chosen, such as $Q_s = Q_p = 60$.

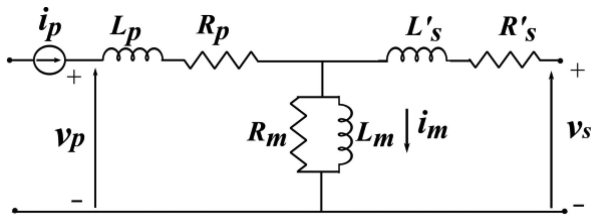

Fig. 8. Equivalent circuit diagram of the power transformer.

At the tuning frequency, the impedance of the series *LC* filter calculated using (26) and (28) is equal to 0.09 Ω, whereas considering the parameter variations given in Table I, the impedance of the series *LC* filter calculated using (35) is 0.48 Ω. That means at the fundamental frequency, the impedance offered by the series *LC* filter increases to 0.48 from 0.09 Ω. Similarly, the parallel *LC* filter impedance at the tuning frequency is 336 Ω [using (29) and (31)] and the impedance of the parallel *LC* filter calculated using (36) is 61 Ω. However, considering these parameters' variations, the fundamental current continues to flow through the series *LC* filter (not through the HVdc line). Hence, the performance of the proposed converter is not affected significantly with the variations of the filter parameters given in Table I.

H. Analysis of DC Current Through the Transformer

The equivalent circuit diagram of the power transformer is shown in Fig. 8, where symbols have the usual meaning. As seen in (11), the primary-side current i_p has a dc and an ac component. From Fig. 8, it can be observed that I_i cannot flow into the secondary side as L_m is shorted at dc. The current flowing through L_m has a magnetizing ac component and a dc component I_i. As a result, the flux developed in the core has a dc and an ac component given by

$$\phi_T = \phi_{\mathrm{AC}} + \phi_{\mathrm{DC}} \tag{37}$$

where ϕ_{DC} is the dc component, ϕ_{AC} is the fundamental ac component, and ϕ_T is the total flux. ϕ_{AC} is responsible to produce the induced electromotive force on the secondary side of the transformer. The presence of dc bias in the total flux will cause a flux imbalance in the core and the transformer may operate in the saturation region of the hysteresis loop [25], [28]. To bring the core back to operate in the linear region, the airgap is introduced in the magnetic path of the flux. The core with airgap can tolerate a higher dc current and operate in the linear region, which can be seen in Fig. 9. The design of the medium-frequency transformer with airgap is described in Appendix A.

III SIMULATION RESULTS

To verify the performance and effectiveness of the proposed converter, a simulation model rated 10 MW, 400 kV is simulated in MATLAB Simulink. The detailed parameters of the simulation of the proposed converter are listed in Table II.

On the high-voltage side, an MMC is connected to a 400 kV HVdc link, and on the medium-voltage side, a VSC is connected

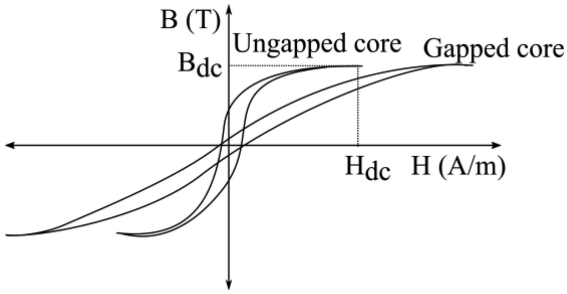

Fig. 9. Hysteresis loop.

to 50 kV via a 350 Hz, 10 MVA transformer. The simulated waveforms for the proposed converter are shown in Fig. 10. Fig. 10(a) shows the input and output dc voltages. The input HVdc V_H is 400 kV and the output medium dc voltage (V_L) obtained is 50 kV. The proposed converter provides a high-voltage transformation ratio, i.e., 8. The dc currents in both HVdc and MVdc sides are shown in Fig. 10(b). In steady state, the proposed converter transfers a rated power of 10 MW. As $P_{\text{in}} = P_{\text{out}}$, the input dc current I_i magnitude in the HVdc side is 25 A, whereas in the MVdc side, the output dc current I_o magnitude is 200 A. Fig. 10(c) and (d) illustrates the upper arm and lower arm voltages, respectively. The sinusoidal LS-PWM technique is implemented with the sorting algorithm as explained earlier. The arm voltages have seven levels of voltages corresponding to six number of power cells in each arm. Both the upper and lower arm voltages have a dc component of 200 kV and an ac component of 200 kV as per (2).

Under the steady-state operation, all power cell capacitors are balanced and each maintains a voltage of $\frac{V_H}{N}$, i.e., 66.67 kV. Fig. 10(e) shows the transformer primary voltage, which has a peak amplitude of 400 kV as per (8).

The arm current flowing through the primary side of the transformer is shown in Fig. 10(f). It has an ac component and a dc component as per (11). The peak amplitude of the ac component is 50 A and the dc magnitude is 25 A. Fig. 10(g) illustrates the secondary voltage of peak magnitude 50 kV corresponding to 8:1 turns ratio of the transformer. The ac current flowing through the secondary side of the transformer is shown in Fig. 10(h), whose peak amplitude is 400 A.

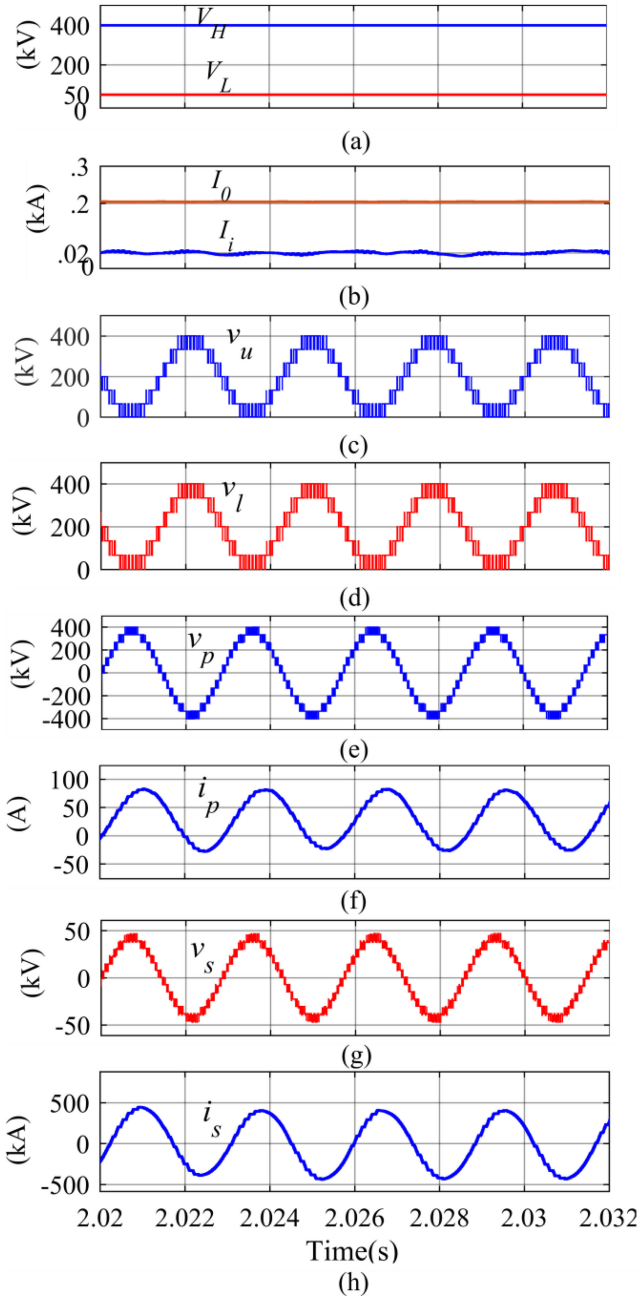

Fig. 10. Converter waveforms with computer simulation. (a) HVdc and MVdc voltages. (b) HVdc and MVdc currents. (c) Upper arm voltage. (d) Lower arm voltage. (e) Transformer primary-side voltage. (f) Arm current. (g) Transformer secondary-side voltage. (h) Transformer secondary-side current.

IV. Experimental Results

A downscaled laboratory prototype has been built with maximum power and high-side voltage of 1 kW and 400 V, respectively, as shown in Fig. 12. In the experimental setup, there are three half-bridge cells in each arm of the proposed dc–dc MMC.

The cells of the proposed converter consist of the Intelligent Power Module IGCM15F60GA of Infineon, electrolytic capacitors, and the gate drive circuits. Both the series and parallel *LC* filters are composed of laminated core inductors and ac capacitors. The load used in the converter is a resistive load. TMS320F28377S DSP controller of Texas Instruments is used to generate gate pulses. The experimental parameters are listed in Table II. On the high-voltage side, an MMC is connected to 400 V and on the medium-voltage side, a VSC is connected to 200 V via a 350 Hz, 1 kVA transformer in the experiment. The experimental waveforms are shown in Fig. 11.

Fig. 11(a) (i) illustrates the input dc bus voltage V_H, whose magnitude is 400 V and the input dc current I_i of magnitude 2.5 A is shown in Fig. 11(a) (ii). Fig. 11(b) (i) shows the upper arm voltage, whose peak amplitude is 380 V. Each arm voltage has four voltage levels corresponding to three number of power cells. Each arm voltage has a dc component of 200 V and an ac component of 180 V (peak amplitude), as per (2), where $m_{a1} = 0.9$. Fig. 11(b) (ii) shows the current flowing

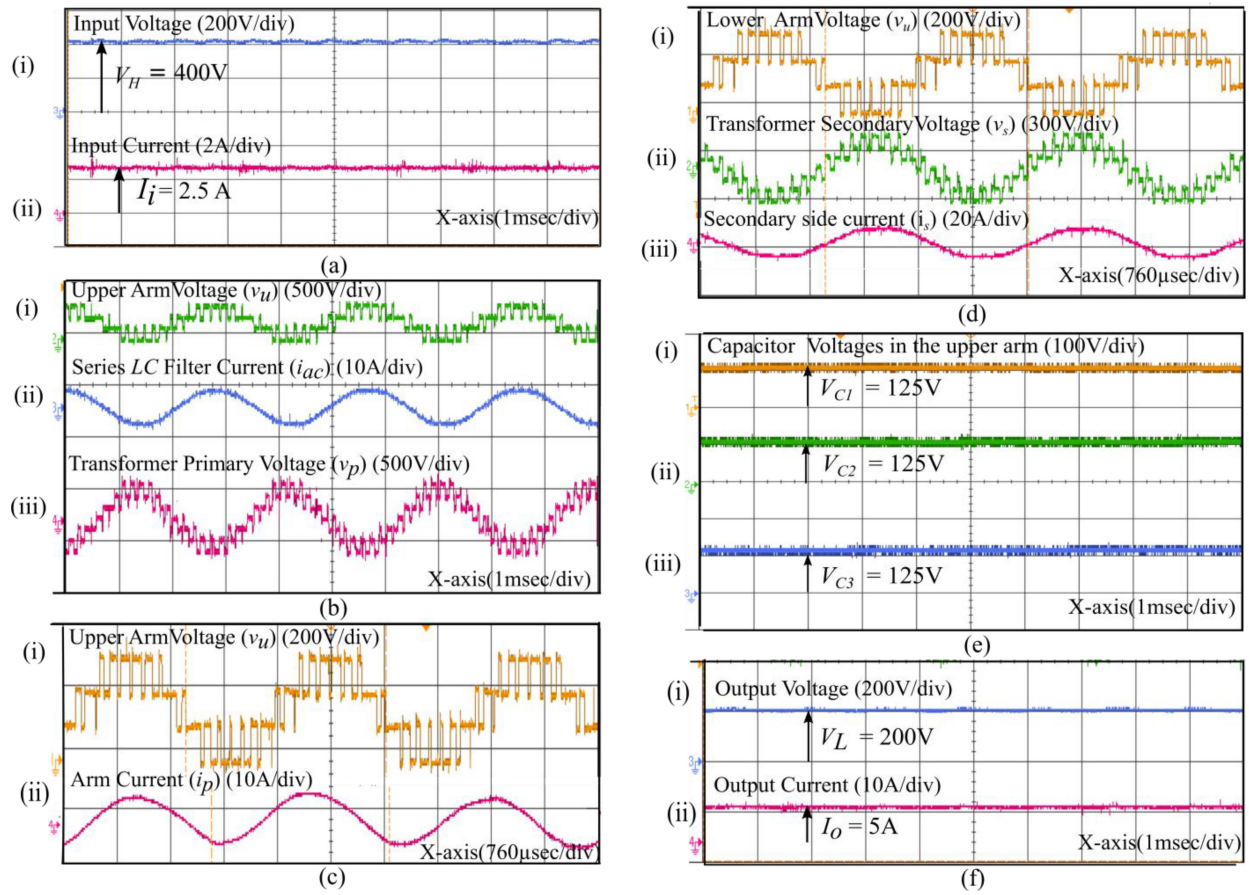

Fig. 11. Experimental results. (a) (i) Input dc bus voltage [200 V/div] and (ii) input dc current [2 A/div]. (b) (i) Upper arm voltage of MMC [500 V/div], (ii) series filter current [10 A/div], and (iii) transformer primary voltage [500 V/div]. (c) (i) Upper arm voltage of MMC [200 V/div] and (ii) transformer primary current [10 A/div]. (d) (i) Lower arm voltage of MMC [200 V/div], (ii) transformer secondary voltage [300 V/div], and (iii) transformer secondary current [10 A/div]. (e) Upper arm cell capacitor voltages [100 V/div]. (f) (i) Output voltage [200 V/div] and (ii) output current [10 A/div].

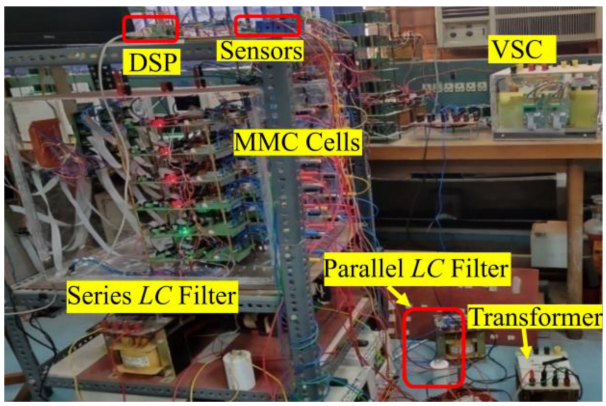

Fig. 12. Experimental setup.

through the arms, transformer, and series *LC* filter $i_{\rm ac}$ with a peak amplitude of 5 A. Fig. 11(b) (iii) illustrates the primary-side voltage of the transformer v_p with a peak amplitude of 360 V. The upper arm voltage is shown in Fig. 11(c) (i). Fig. 11(c) (ii) shows the arm current i_p transformer, which has a dc component of 2.5 A and an ac component 5 A. Fig. 11(d) (i) illustrates the lower arm voltage. Fig. 11(d) (ii) shows the transformer secondary-side voltage v_s with a peak amplitude of 180 V corresponding to 2:1 turns ratio. The current flowing in the transformer secondary side i_s is shown in Fig. 11(d) (iii). The three upper arm cell capacitor voltages are shown in Fig. 11(e), where the capacitor voltages are balanced, and each cell capacitor maintains a voltage magnitude of 125 V. The output dc voltage and current are shown in Fig. 11(f) (i) and (f) (ii), respectively. The magnitude of output dc voltage V_L is 200 V and the output dc current I_o magnitude is 5 A.

V. Conclusion

An isolated dc–dc MMC topology is presented in this article. The proposed topology can achieve a high-voltage transformation ratio. The converter utilizes only two arms of MMC and a passive filter with a medium-frequency transformer. The ac circulating current at medium frequency circulates through the arms of MMC, transformer, and the series *LC* filter. The operation of the converter and design of passive elements have been included in the article. The proposed converter is suitable for exchanging tens of megawatt power with the existing HVdc line. Therefore, the converter can be used to feed the isolated local ac grids in the vicinity to the HVdc line or integrate the renewable energy source directly to the HVdc grid.

APPENDIX A

A 10 MVA, 400 kV/50 kV (peak), 1-phase, core-type transformer operating at a frequency of 350 Hz is designed by assuming the following data.

1) voltage per turn v_t is 200 V (rms);
2) the peak magnitude of magnetizing ac current I_m is 1% of the secondary current peak magnitude, i.e., 4 A;
3) space factor K_w is 0.21;
4) current density J is 0.3 A/mm^2.

The material selected for the transformer core is the electrical steel core (Lite Carlite, M-2). The maximum flux density B_m before saturation of the core is 1.5 T and permeability μ_m of the core is 1.89×10^{-3} H/m. Using the above-mentioned data, the transformer design with dc bias in the primary current follows these three steps.

1) The cross-sectional area of the core A_i and the mean magnetic path length l_m is calculated.
2) The operating peak flux density B_{T_peak} can be checked using the previous data obtained in step 1. If B_{T_peak} is much greater than B_m, the airgap can be introduced to bring the core back to the linear operating region.
3) The window area A_w, window height H_w, and width W_w can be calculated.

The magnetizing inductance L_m can be calculated as

$$L_m = \frac{V_{m1}}{\omega I_m} = \frac{V_{m1}}{2\pi f I_m} = \frac{400 \times 10^3}{2 \times \pi \times 350 \times 4} = 45.47\text{H}.$$

Using $\text{volt/turn}\ (v_t)$, the number of turns in the primary side n_p can be calculated as $n_p = \frac{400\times10^3}{\sqrt{2}\times200} = 1415$. Similarly, the number of turns in the secondary side n_s is 177. The cross-sectional area of the core A_i can be calculated as

$$A_i = \frac{v_t}{4.44 B_m f} = \frac{200}{4.44 \times 1.5 \times 350} = 0.084\text{m}^2.$$

The mean magnetic path length l_m can be found out by using A_i, L_m, μ_m , and n_p. It is given by

$$l_m = \frac{{n_p}^2 \mu_m A_i}{L_m} = \frac{1415^2 \times 1.89 \times 10^{-3} \times 0.084}{45.47} = 7\ \text{m}.$$

Using the above-mentioned data, the flux density condition can be checked whether $B_{T\_\text{peak}} < B_m$. As the dc current flows through L_m, the total peak flux ϕ_{T_peak} [see (37)] can be written as

$$\phi_{T_\text{peak}} = \frac{\text{mmf}}{\text{reluctance}} = \frac{n_p\left(I_i + \frac{\Delta I_m}{2}\right)}{R_c}$$

where $R_c = \frac{l_m}{\mu_m A_i}$ and ΔI_m is the peak to peak change in the magnetizing current, i.e., 8 A. Thus, the total peak flux density magnitude B_{T_peak} can be calculated as

$$B_{T\_\text{peak}} = \frac{\phi_{T_\text{peak}}}{A_i} = \mu_m \frac{n_p\left(I_i + \frac{\Delta I_m}{2}\right)}{l_m} = 11.07\ \text{T}.$$

B_{T_peak} obtained above is much greater than B_m, the core will operate in the saturation region. An airgap of length l_g can be introduced in the core to sustain the dc flux. With airgap, ϕ_{T_peak} can be rewritten as

$$\phi_{T_\text{peak}} = \frac{\text{mmf}}{\text{reluctance}} = \frac{n_p\left(I_i + \frac{\Delta I_m}{2}\right)}{R_c + R_g}$$

where R_g is the reluctance of airgap. The airgap length chosen is $l_g = 30$ mm. Thus, B_{T_peak} with airgap can be calculated as

$$B_{T\_\text{peak}} = \frac{n_p\left(I_\text{DC} + \frac{\Delta I_m}{2}\right)}{\frac{l_m}{\mu_m} + \frac{l_g}{\mu_0}} = 1.48\ \text{T}.$$

Since $B_{T\_\text{peak}} < B_m$, the core operates in the linear region. Hence, the dimension of the core can be designed. The total conductor area is $A_C = K_w A_w$, where K_w is the window space factor and A_w is the window area. A_C can also be written as

$$A_c = \left(\frac{i_p n_p}{J}\right) + \left(\frac{i_s n_s}{J}\right).$$

Assume the same ac MMF (ampere turns) in the primary and secondary windings, i.e., $i_\text{ac} n_p = i_s n_s = \text{AT}$, and the dc MMF in the primary winding is half of the AC MMF, i.e.,0.5 AT [according to (25)], the total MMF in the primary winding is 1.5 AT. The total conductor area can be defined as

$$A_c = 2.5\text{AT}/J = K_w A_w.$$

The MVA rating of the transformer can be written as

$$Q = v_t \text{AT} \times 10^{-6} = 4.44 B_o A_i f \frac{J K_w A_w}{2.5} \times 10^{-6}.$$

From the above-mentioned equation, the value of A_w calculated is 2 m^2.

Assume the ratio of window height to window width is 2. The window area can also be written as

$$A_w = (H_w + l_g) W_w = (2W_w + l_g) W_w = 2\ \text{m}^2.$$

Solving the above-mentioned equation, the value of W_w is found to be $1\ \text{m}$ and $H_w = (2 \times W_w) + l_g = 2.03$ m.

APPENDIX B

In the proposed topology, the series filter inductor L_s carries the fundamental ac current and its design is similar to an ac transformer. The voltage rating of L_s is half of the voltage rating of the whole series filter, i.e., $v_{p,\text{rms}}/2$. The cross-sectional core area of L_s can be defined as

$$A_{cfs} = \frac{v_{p,\text{rms}}/2}{4.44 N_{fs} B_{os} f}$$

where N_{fs} is the number of turns and B_{os} is the operating flux density.

The winding window area A_{wfs} of L_s can be defined as

$$A_{wfs} = \frac{a_{cfs}}{K_w} = \frac{N_{fs} i_{\text{ac,rms}}}{J_s K_{ws}}$$

where a_{cfs} is the conductor area, J_s is the current density of the copper wire, and K_{ws} is the window space factor. The area product A_{pfs} of L_s is given by

$$A_{pfs} = A_{wfs} A_{cfs} = \frac{(v_{p,\text{rms}}/2) i_{\text{ac,rms}}}{4.44 J_s K_{ws} B_{os} f}.$$

The magnetic material selected for L_s is the silicon steel core and $B_{os} = 1.5$ T. Assume $J_s = 0.5$ MA/m^2 and $K_{ws} = 0.3$. The area product of L_s is calculated as $A_{pfs} = 0.014$ m^4.

The parallel filter inductor L_p carries the dc current and its design is given in the following part. The energy stored in L_p is

$$E_{Lp} = \frac{1}{2} L_p {I_i}^2 = \frac{1}{2} \times 2.5 \times 10^{-3} \times 25^2 = 0.78 \text{ Ws}$$

The area product of the parallel filter inductor is defined as [25]

$$A_{pfp} = \frac{2 \times E_{Lp}}{B_{op} \times J_p \times K_{wp}}$$

where J_p is the current density of the copper wire and K_{wp} is the window space factor of L_p. The magnetic material chosen for L_p is the permalloy powder core and $B_{op} = 0.3$ T. Assume $J_p = 0.5$ MA/m^2 and $K_{ws} = 0.3$. The area product of the parallel filter inductor is calculated as

$$A_{pfp} = \frac{2 \times E_{Lp}}{B_{op} \times J \times K_w} = 3.46 \times 10^{-5} \text{ m}^4.$$

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