Modular Equalization System Using Dual Phase-Shift-Controlled Capacitively Isolated Dual Active Bridge Converters to Equalize Cells and Modules in Series-Connected Lithium-Ion Batteries

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***Abstract*—Conventional lithium-ion battery (LIB) packs comprising series-connected modules need cell and module equalizers separately, resulting in increased system complexity. This article proposes a modular equalization system using dual phase-shift (DPS)-controlled capacitively isolated dual active bridge (CIDAB) converters. Each module contains an intramodule CIDAB converter that performs direct cell-to-cell equalization. Meanwhile, switching legs of adjacent modules' CIDAB converters are connected through an *LC* tank to configure an intermodule CIDAB converter that equalizes module voltages. The switching legs of CIDAB converters are utilized for both the intra- and intermodule equalizers, achieving the simplified system. Based on the proposed DPS control, the PS angles of both the intra- and intermodule CIDAB converters are manipulated to perform cell and module equalization. The prototype of the proposed modular equalization system for two LIB modules, each consisting of 12 cells was built and tested. Cells and module voltages in the proposed system were sufficiently equalized, demonstrating the efficacy of the proposed equalization system.**

***Index Terms*—Capacitive isolation, dual active bridge converter, equalization, lithium-ion battery (LIB), voltage imbalance.**

I. Introduction

A. Cell Imbalance and Equalizers for Lithium-Ion Batteries

LITHIUM-ION battery (LIB) cells are connected in series to form a pack or module to meet the voltage requirement of loads. Individual cell voltages gradually become imbalanced due to characteristic mismatches, such as capacity, internal impedance, self-discharge rate, coulombic efficiency, and ambient temperatures [1], [2]. In voltage-imbalanced LIB modules, some cells with high or low voltages might be overcharged or -discharged beyond safety boundaries specified by manufacturers. Charging and discharging LIB cells beyond safety boundaries may trigger premature irreversible degradation or hazardous consequences, such as fire or, in the worst case, an explosion.

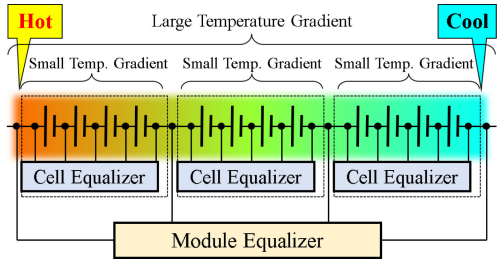

Fig. 1. Modular battery structure and its uneven temperature distribution.

In large-scale LIB packs, such as electric vehicles, a modular structure is a mainstream. Several dozen cells are connected in series to form a module, and then multiple modules are connected in series to form a large pack or string, as illustrated in Fig. 1. In such large-scale systems, in addition to cell voltage imbalance in each module, module voltage imbalance is also very likely due to uneven temperature distribution. Cell temperatures in each module are relatively even because of the small geometry of modules. Module temperatures, on the other hand, are prone to be uneven due to their large geometry. In general, the uneven temperature distribution is cited as a top concern that accelerates voltage imbalance as well as premature degradation [2]–[4]. To operate LIB systems safely for years, cell and module voltage equalizations are indispensable to mitigate or even eliminate such voltage imbalance.

Various kinds of voltage equalizers, also known as balancers, have been proposed for series-connected LIBs. Several kinds of equalization architectures, such as adjacent cell-to-cell architectures using nonisolated bidirectional converters [see Fig. 2(a)], such as PWM converters [5]–[7] and switched capacitor converters [8]–[13], module-to-cell architectures using single-input–multiple-output converters [see Fig. 2(b)] [14]–[26], module-to-cell architecture using isolated converters [see Fig. 2(c)] [27], etc., have been proposed. These architectures and circuit topologies are relatively simple. However, since the numbers of passive components, such as inductors, capacitors, and transformers, are proportional to the cell count n, these equalizers are prone to be bulky as n increases.

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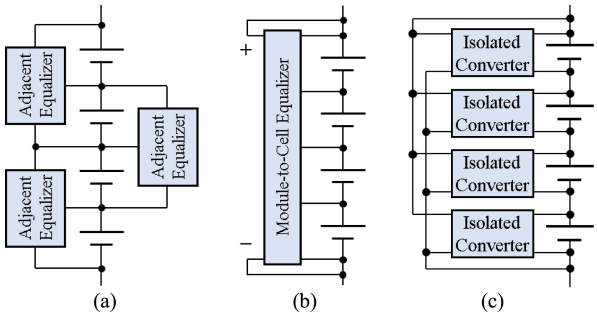

Fig. 2. Cell equalization architectures. (a) Adjacent cell-to-cell architecture with nonisolated bidirectional converters. (b) Module-to-cell architecture with single-input–multiple-output converter. (c) Module-to-cell architecture with isolated converters.

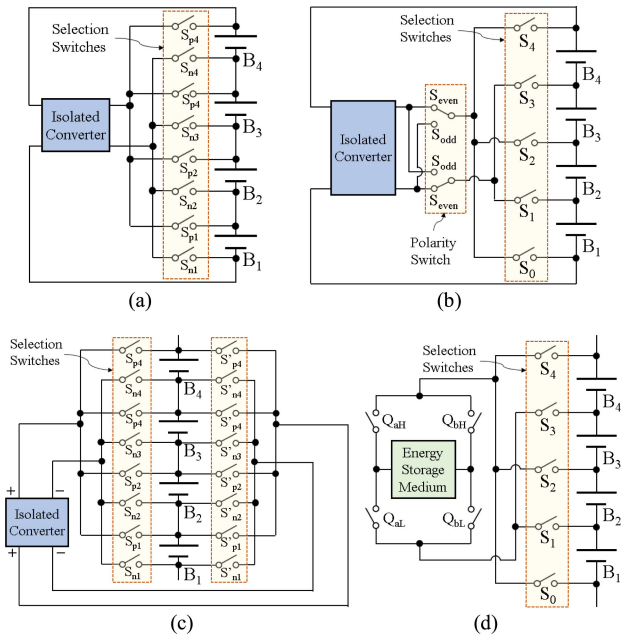

Fig. 3. Equalization architectures with selection switches. (a) Module-to-cell architecture. (b) Module-to-cell architecture with polarity switches. (c) Direct cell-to-cell architecture with unidirectional converter. (d) Direct cell-to-cell architecture with energy storage medium.

B. Cell Equalizers With Selection Switches

Among conventional equalization architectures is the direct cell-to-cell or module-to-cell architecture using selection switches, as shown in Fig. 3. Although numerous selection switches are necessary, the passive component count can be considerably reduced in comparison with other equalization architectures. The reduced passive component count is an attractive feature from the viewpoint of circuit volume because passive components (especially magnetic components) are rather bulkier than semiconductor devices.

Representative cell equalizers with selection switches are shown in Fig. 3. Selection switches in these topologies are a bidirectional switch consisting of two MOSFETs connected back-to-back to block bidirectional current flow. The most charged cell (or the least charged cell) in a module is selected as a target cell by the selection switches to connect a converter. In the module-to-cell architecture [see Fig. 3(a)], an isolated converter transfers energy between a target cell and module [28]–[31]. With polarity switches, as shown in Fig. 3(b), the selection switch count can be reduced as low as $n + 5$ [32]. However, since the energy transfer in the module-to-cell architectures is limited between the module and a target cell, some cells in a module are unnecessarily charged and discharged in the course of equalization, resulting in a slowed equalization process and reduced overall efficiency. Furthermore, in addition to the necessity of a bulky transformer, isolated converters in these module-to-cell equalization architectures must be rated for the full module voltage as it is directly connected to the module.

The direct cell-to-cell architecture using a unidirectional converter [see Fig. 3(c)] can directly transfer energy between target cells [33], [34], but the increased selection switch count ($4n$) is a major drawback. The direct cell-to-cell architecture with an energy storage medium [see Fig. 3(d)], such as a capacitor, inductor, and resonant tank, can reduce the selection switch count as low as $n + 1$ [35]–[40]. However, since selection switches in many existing topologies have to operate at a high frequency in conjunction with four unidirectional switches (Q_{aH}, Q_{aL}, Q_{bH}, and Q_{bL}), numerous high-frequency gate drivers are necessary, increasing the system cost and complexity—selection switches in other architectures can operate at a low frequency, and high-frequency gate drivers are not necessary.

Although equalizers with selection switches achieve miniaturized circuit thanks to the reduced passive component counts, voltage stresses of selection switches are prone to soar as the number of cells in a string increases. Switches at the furthest ends of the string, for example, are exposed to a full string voltage.

C. Conventional Modular Equalization Systems

Multilayer or modular equalization systems (hereafter referred to as modular systems) have been proposed for large-scale systems to realize good modularity (or scalability) and fast equalization performance [41]–[48], as illustrated in Fig. 1. In such systems, LIB cells in each module are equalized by cell-level equalizers, and module equalizers unify module voltages. The design of cell-level equalizers and the number of cells in each module are fixed and unchanged while the system can be flexibly scaled up by adding modules and module-level equalizers. Any kinds of equalizers can be employed as cell- and module-level equalizers. Conventional modular systems [42], [48] simply employ cell- and module-level equalizers separately, hence increasing the system complexity and cost. Equalization systems in [43], [45], and [47] can reduce the number of module-level equalizers by using a multiwinding transformer-based converter, but the existence of the multiwinding transformer is often cited as a major concern that increases the design difficulty and impairs the modularity [49].

D. Research Objective

This article proposes a novel modular equalization system based on equalizers with selection switches. A direct-cell-to-cell equalizer with selection switches using a capacitively isolated

dual-active bridge (CIDAB) converter is employed as an intramodule equalizer. Meanwhile, by adding an *LC* tank between adjacent switching legs of adjacent modules' CIDAB converters, a CIDAB-based intermodule equalizer is configured without adding active switches. With the proposed dual phase-shift (DPS) control technique, phase-shift (PS) angles of not only the intramodule CIDAB converter but also the intermodule CIDAB converter are manipulated to perform cell and module equalization.

The rest of this article is organized as follows. Section II presents the proposed modular equalization system and its major features. Section III discusses operation principles of the cell equalization mode and module equalization mode, separately, followed by the equalization algorithms in Section IV. Section V discusses a design example of the CIDAB converter for LIB modules consisting of 12 cells connected in series. The experimental results of the proposed modular equalization system for two modules will be presented in Section VI. The proposed and conventional equalizers will be compared from the viewpoint of component counts and reported efficiency in Section VII.

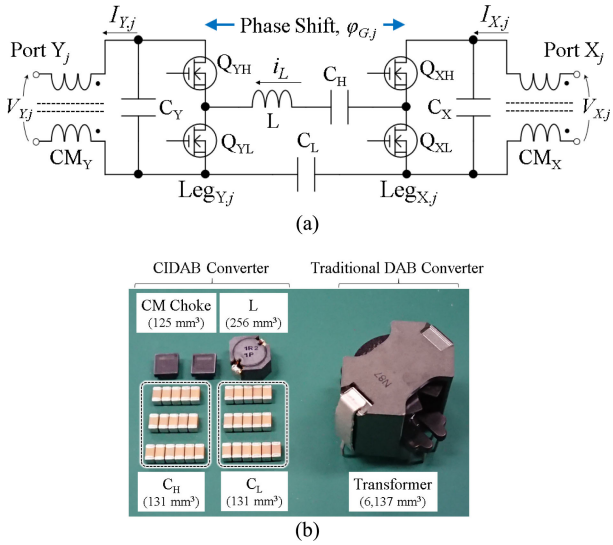

Fig. 4. (a) Half-bridge CIDAB converter. (b) Key passive components necessary in the CIDAB converter and the traditional transformer-based DAB converter.

II. Proposed Modular Equalization System

The proposed modular equalization system consists of series-connected LIB modules, each comprising two groups of series-connected cells, CIDAB converter, and switch module. This section explains the CIDAB converter and switch modules, which are the key components of the proposed system, followed by the system configuration.

A. Capacitively Isolated Dual Active Bridge Converter

An isolated converter is indispensable to transfer energy between cells at different voltage levels. Isolated converters, such as flyback converters and DAB converters, are generally employed in conventional battery cell equalization systems, but each isolated converter requires a bulky lossy transformer. In the proposed equalization system, instead of traditional transformer-based isolated converters, CIDAB converters are employed to achieve reduced circuit volume. Energy densities of discrete capacitors are reportedly in the range of more than three orders of magnitude over that of similarly scaled magnetic components [50], [51]. Previous studies reported the reduced circuit volume of the resonant converters thanks to the capacitive isolation [52], [53].

The half-bridge CIDAB converter is shown in Fig. 4(a). Two switching legs ($\mathrm{Leg}_{X.j}$ and $\mathrm{Leg}_{Y.j}$) are isolated by capacitors C_H and C_L, instead of a transformer. The fundamental operation principle of the CIDAB converter is very similar to that of conventional DAB converters. The high- and low-side switches are driven with 50% duty cycle in a complementary manner while the phase-shift angle $\varphi_{G.j}$ between $\mathrm{Leg}_{X.j}$ and $\mathrm{Leg}_{Y.j}$ is manipulated to adjust the magnitude and direction of power transfer between Ports X_j and Y_j. Switches in the CIDAB converter can be turned-ON and -OFF at zero-voltage switching (ZVS), similar to conventional DAB converters. Although common-mode (CM) chokes are necessary to suppress CM currents, these can be tiny in comparison with an isolation transformer.

Fig. 4(b) exemplifies the comparison of key passive components necessary in the CIDAB converter and conventional half-bridge DAB converter for the same power rating of 50 W. Switches and smoothing capacitors (C_X and C_Y), which are common to both converters, are excluded. Although the number of passive components necessary increases, the passive component volume would be reduced by 90%.

B. Switch Module

The switch module, which selects target cells depending on voltage imbalance conditions, consists of selection switches (S_{Xi} and S_{Yi}, where $i = 1, \ldots, 4$) and polarity switches ($\mathrm{S}_{X\mathrm{odd}}$, $\mathrm{S}_{X\mathrm{even}}$, $\mathrm{S}_{Y\mathrm{odd}}$, and $\mathrm{S}_{Y\mathrm{even}}$), as shown in Fig. 5. Each switch comprises two *N*-channel MOSFETs connected back-to-back, and each module contains $n + 12$ switches (n is the cell count in each module).

The selection switches literally select target cells or a whole group while polarity switches match the voltage polarities of the target cells and CIDAB converter. For example, to select the odd-numbered cell of B_{X1}, the selection switches of S_{X1} and S_{X2} and the polarity switch of $\mathrm{S}_{X\mathrm{odd}}$ are turned ON. To select the even-numbered cell of B_{X2}, on the other hand, the selection switches of S_{X2} and S_{X3} and the polarity switch of $\mathrm{S}_{X\mathrm{even}}$ are turned ON.

C. System Configuration

The proposed modular equalization system for two LIB modules, each consisting of eight cells connected in series, is illustrated in Fig. 5. Each module contains a switch module and an intramodule CIDAB converter that performs cell equalization. Series-connected cells in each module are subdivided into two groups of Group X_j and Y_j ($j = 1, 2, \ldots, m$, where m is the

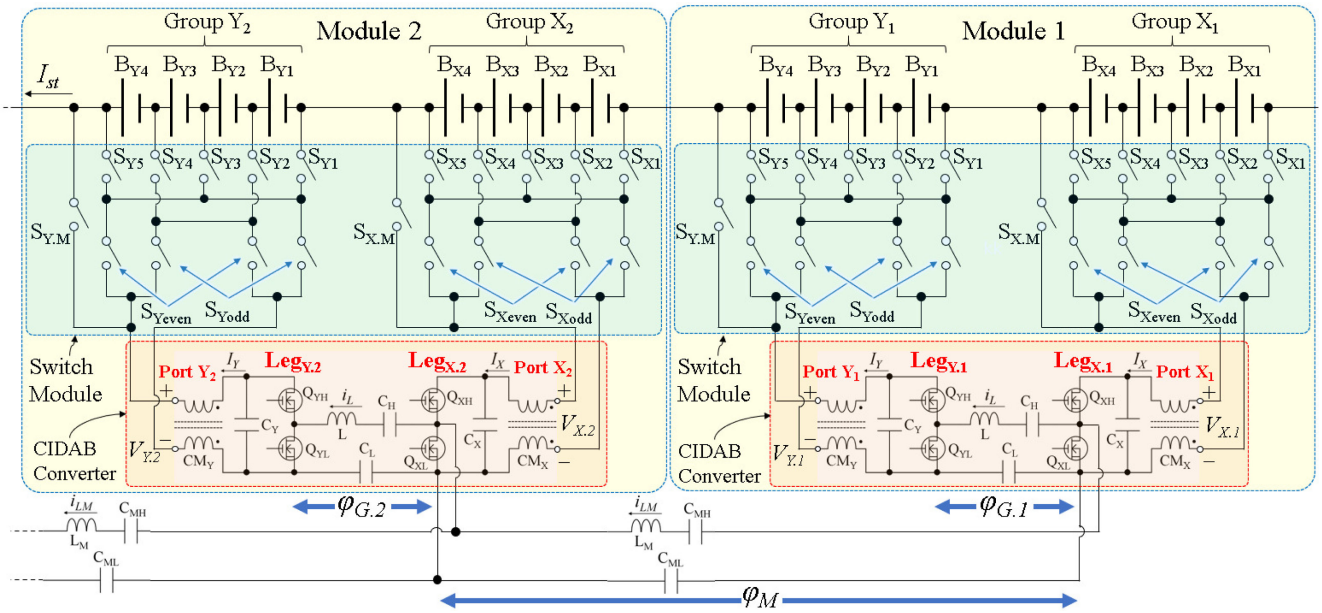

Fig. 5. Proposed modular equalization system using selection switches and capacitively-isolated DAB converter.

number of modules), and are connected to Port X_j and Y_j of the CIDAB converter.

Each CIDAB converter contains two switching legs of $\text{Leg}_{X.j}$ and $\text{Leg}_{Y.j}$. An *LC* tank consisting of C_{MH}, C_{ML}, and L_M is added between adjacent Leg_X's to configure an intermodule CIDAB converter that performs module equalization. No additional switches are necessary for the intermodule equalizer because $\text{Leg}_{X.j}$ is utilized for both the intra- and intermodule CIDAB converters.

To perform cell and module equalizations, two control freedoms are necessary. A DPS control technique is also proposed for the modular equalization system. The DPS control technique manipulates not only the PS angel $\varphi_{G.j}$ of each intramodule CIDAB converter to equalize cell voltages (or group voltages) but also the PS angel φ_M between adjacent Leg_X's (i.e., the PS angle of the intermodule CIDAB converter) to balance module voltages.

D. Features

The most prominent feature is that the intermodule CIDAB converter can be configured by simply adding an *LC* tank between adjacent modules. Since no additional active switches are necessary, the number of switching legs as well as gate driver circuits can be reduced in comparison with conventional systems, hence contributing to the simplified circuit. The reduced circuit volume of the converter thanks to the capacitive isolation is also a benefit.

The proposed equalization system is fully modular and offers good modularity or scalability. The number of cells in each module and module design are fixed, whereas the number of modules can flexibly be changed to meet system requirements. The number of modules can be arbitrarily extended by simply neither adding *LC* tanks without redesigning the modules nor adding active switches.

The major drawback of the proposed system is that switching in each module should occur synchronously for the intermodule CIDAB converters to properly operate. In other words, the proposed modular equalization architecture should be a centralized system, not distributed one, posing wiring and communication issues. The development of distributed modular equalization systems will be of primary importance in our future works.

III. Equalization Mode

The proposed modular equalization system operates either in the cell equalization mode or module equalization mode. The cell and module equalization modes do not coincide. Although cells and modules cannot be equalized simultaneously, equalizing cells and modules separately slowly would be satisfactory. As long as batteries are properly designed and manufactured, the mismatch in voltage or state-of-charge grows very slowly in practical use. Previous works reported that an equalization current equivalent to one-hundredth of charging or discharging current is sufficient to preclude voltage imbalance [54], [55].

Images of the cell and module equalization modes are illustrated in Fig. 6(a) and (b), respectively.

A. Cell Equalization Mode

Target cells (the least charged cell and the most charged cell) in each module are selected by the switch module so that the intramodule CIDAB converter directly transfers power from the most charged cell in a group to the least charged cell in another group. The magnitude and direction of power transfer in the jth module ($j = 1, 2, \ldots, m$) are adjusted by the PS angle $\varphi_{G.j}$ between $\text{Leg}_{X.j}$ and $\text{Leg}_{Y.j}$. Meanwhile, the PS angle φ_M between adjacent modules' CIDAB converters is set to be zero so that the module equalization does not take place.

The input and output currents (or $I_{X.j}$ and $I_{Y.j}$) of the intramodule CIDAB converter in the cell equalization mode are

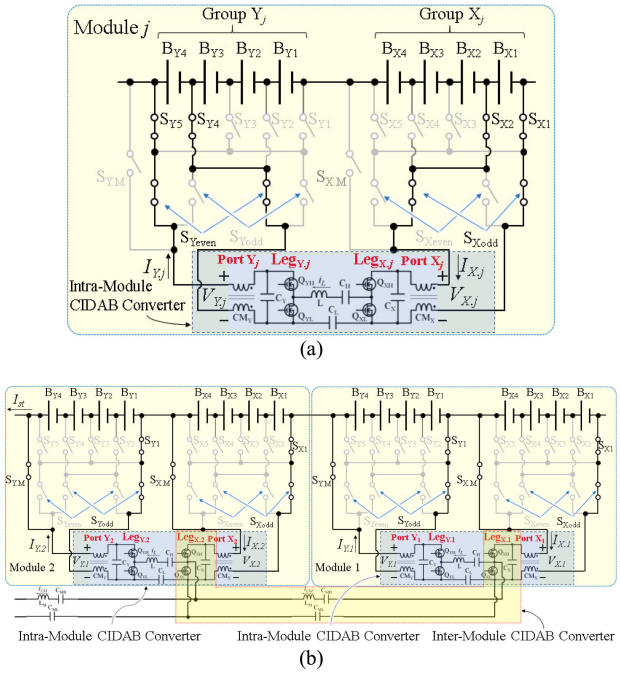

Fig. 6. Equalization modes. (a) Cell equalization mode. (b) Module equalization mode.

given by

$$\begin{cases} I_{X.j} = \dfrac{V_{Y\text{cell}.j}}{2f_sL}\, d_{\varphi G.j}\,|0.5 - d_{\varphi G.j}| \\ I_{Y.j} = \dfrac{V_{X\text{cell}.j}}{2f_sL}\, d_{\varphi G.j}\,|0.5 - d_{\varphi G.j}| \end{cases} \tag{1}$$

where f_s is the switching frequency, L is the inductance, and $V_{X\text{cell}.j}$ and $V_{Y\text{cell}.j}$ are the voltages of cells connected to Ports X_j and Y_j, respectively. $d_{\varphi G.j}$ is the PS duty cycle of the intramodule CADAB converter defined as

$$d_{\varphi G.j} = \frac{\varphi_{G.j}}{2\pi}\,. \tag{2}$$

B. Module Equalization Mode

Whole groups are selected by $\mathrm{S}_{X.M}$, S_{X1}, $\mathrm{S}_{Y.M}$, and S_{Y1} of the switch module, and the intermodule CIDAB converter transfers power between adjacent Group X's. The PS angle φ_M between adjacent Leg_X's is manipulated to determine the magnitude and direction of power transfer between adjacent Group X's. However, since the intermodule CIDAB converter is configured between adjacent Group X's, voltage imbalance between Groups X_j and Y_j occurs to some extent. To balance the group voltages, $\varphi_{G.j}$ should also be manipulated at the same time. Thus, the module equalization mode simultaneously manipulates $\varphi_{G.j}$ and φ_M (i.e., the DPS control) so that the intramodule CIDAB converter transfers power between Groups X_j and Y_j in each module.

$\mathrm{Leg}_{X.j}$ is shared by both the intra- and intermodule CIDAB converters, which complicates the analysis of the module equalization mode. To simplify the analysis, the shared $\mathrm{Leg}_{X.j}$ can be equivalently separated. The equivalent circuit of the intra- and intermodule CIDAB converters is shown in Fig. 7, in which

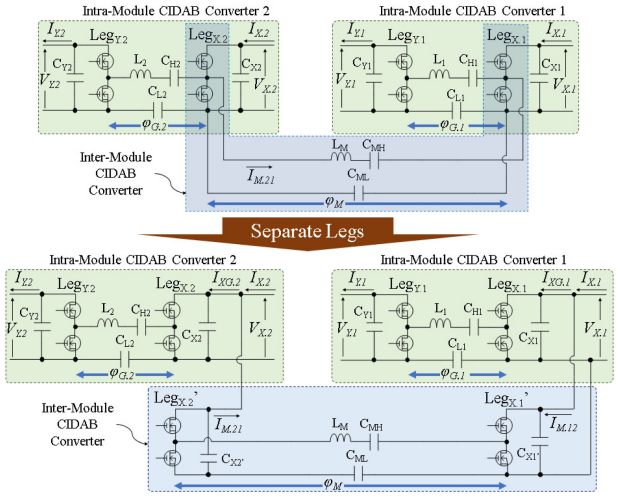

Fig. 7. Equivalent circuit of intra, and intermodule CIDAB converters in module equalization mode.

the intra- and intermodule CIDAB converters have separate switching legs of $\mathrm{Leg}_{X.j}$ and $\mathrm{Leg}_{X.j}$'. This figure suggests that the port current of $I_{X.j}$ contains not only the group equalization current by the intramodule CIDAB converter ($I_{XG.j}$) but also the module equalization current due to the intermodule CIDAB converter ($I_{M.j(j+1)}$ and $I_{M.(j+1)j}$). Meanwhile, the port current of $I_{Y.j}$ is equal to the group equalization current of $I_{YG.j}$.

The input and output currents ($I_{XG.j}$ and $I_{YG.j}$) of the intramodule CIDAB converter due to the group equalization is expressed as

$$\begin{cases} I_{XG.j} = \dfrac{V_{YG.j}}{2f_sL}\, d_{\varphi G.j}\,|0.5 - d_{\varphi G.j}| \\ I_{YG.j} = \dfrac{V_{XG.j}}{2f_sL}\, d_{\varphi G.j}\,|0.5 - d_{\varphi G.j}| \end{cases} \tag{3}$$

where $V_{XG.j}$ and $V_{YG.j}$ are, respectively, the voltages of Groups X and Y in the jth module.

Similarly, the input and output currents ($I_{M.j(j+1)}$ and $I_{M.(j+1)j}$) of the intermodule CIDAB converter due to the module equalization is expressed as

$$\begin{cases} I_{M.j(j+1)} = \dfrac{V_{XG.(j+1)}}{2f_sL_M}\, d_{\varphi M}\,|0.5 - d_{\varphi M}| \\ I_{M.(j+1)j} = \dfrac{V_{XG.j}}{2f_sL_M}\, d_{\varphi M}\,|0.5 - d_{\varphi M}| \end{cases} \tag{4}$$

where $d_{\varphi M}$ is the PS duty cycle of the intermodule CIDAB converter defined as

$$d_{\varphi M} = \frac{\varphi_M}{2\pi}\,. \tag{5}$$

IV. Equalization Algorithm

As explained in the previous sections, the proposed modular equalization system operates either in the cell equalization mode or module equalization mode, and these two equalization modes do not coincide. The cell and module equalization modes are performed independently with separate algorithms.

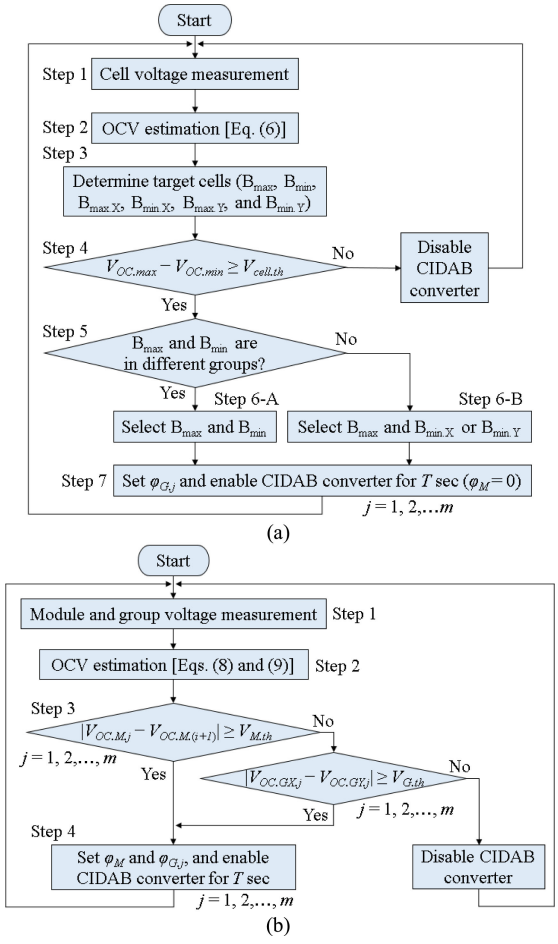

Fig. 8. Equalization algorithms in (a) cell and (b) module equalization modes.

A. Cell Equalization Mode

The flowchart of the cell equalization algorithm is shown in Fig. 8(a). First, all cell voltages are measured in Step 1 to estimate open-circuit voltages (OCVs) of cells. A voltage drop due to an internal impedance of a cell needs to be compensated based on a nonlinear impedance model to accurately estimate OCVs [56], [57]. However, to simplify the OCV estimation, cells can be equivalently treated as a series connection of a voltage source and an internal resistance. Step 2 employs the following equation to estimate the OCV of the ith cell in each module:

$$V_{\mathrm{OC}.i} = V_{\mathrm{cell}.i} + r\left(I_{\mathrm{eq}} + I_{\mathrm{st}}\right) \tag{6}$$

where $V_{\mathrm{cell}.i}$ is the voltage of the ith cell in a module, r is the internal resistance, and I_{st} is the string current. I_{eq} is the equalization current supplied to/from the intramodule CIDAB converter

$$I_{\mathrm{eq}} = \begin{cases} I_{X.j} \\ -I_{Y.j} \\ 0 \end{cases} \tag{7}$$

where $I_{X.j}$ and $I_{Y.j}$ in the cell equalization mode are given in (1).

Based on the estimated OCVs, target cells that will be selected by the switch module are determined in Step 3. The target cells include the most charged cell and the least charged cell in the module ($\mathrm{B_{max}}$ and $\mathrm{B_{min}}$), and the most charged cells and the least charged cells in Groups X_j and Y_j ($\mathrm{B_{max.}}_X$, $\mathrm{B_{max.}}_Y$, $\mathrm{B_{min.}}_X$, and $\mathrm{B_{min.}}_Y$).

Step 4 judges whether cells are balanced. If the largest OCV difference among cells in a module exceeds a threshold voltage level, the cell equalization starts. The difference between OCVs of $\mathrm{B_{max}}$ and $\mathrm{B_{min}}$ (i.e., $V_{\mathrm{OC.max}} - V_{\mathrm{OC.min}}$) is calculated and compared with the threshold voltage of $V_{\mathrm{cell.th}}$. If $V_{\mathrm{OC.max}} - V_{\mathrm{OC.min}} < V_{\mathrm{cell.th}}$, the intramodule CIDAB converter is disabled to stop cell equalization. If $V_{\mathrm{OC.max}} - V_{\mathrm{OC.min}} \geq V_{\mathrm{cell.th}}$, the operation moves toward cell equalization by manipulating the switch module and activating the CIDAB converter.

The equalization process differs depending on whether $\mathrm{B_{max}}$ and $\mathrm{B_{min}}$ exist in different groups because the intramodule CIDAB converter cannot transfer power between cells in the same group. Step 5 judges whether $\mathrm{B_{max}}$ and $\mathrm{B_{min}}$ exist in the same group. If $\mathrm{B_{max}}$ and $\mathrm{B_{min}}$ exist in different groups (e.g., $\mathrm{B_{max}}$ in Group X_j and $\mathrm{B_{min}}$ in Group Y_j), the operation moves to Step 6-A so that the switch module selects $\mathrm{B_{max}}$ and $\mathrm{B_{min}}$ as the target cells. On the other hand, if $\mathrm{B_{max}}$ and $\mathrm{B_{min}}$ exist in the same group, the operation moves to Step 6-B, in which the switch module selects $\mathrm{B_{max}}$ and either $\mathrm{B_{min.}}_X$ or $\mathrm{B_{min.}}_Y$ that does not exist in the same group as $\mathrm{B_{max}}$.

Examples of Steps 6-A and 6-B for a module consisting of eight cells are illustrated in Fig. 9. In the example case of Step 6-A in Fig. 9(a), B_{Y3} and B_{X2} are the most and the least charged cells, respectively. B_{X4} is the most charged cell in Group X, and B_{Y1} is the least charged cell in Group Y. Since B_{Y3} ($\mathrm{B_{max}}$) and B_{X2} ($\mathrm{B_{min}}$) exist in different groups, these cells are selected as the target cells. In the example case of Step 6-B in Fig. 9(b), B_{Y3} and B_{Y1} are the most and the least charged cells in the module, respectively, while B_{X4} and B_{X1}, respectively, are the most and the least charged cells in Group X. In this case, B_{Y3} is selected as the target cell of $\mathrm{B_{max}}$ to supply energy. B_{Y1} is the least charge cell ($\mathrm{B_{min}}$) in the module, but it cannot be selected because it exists in the same group. Instead, the least charged cell in the other group (B_{X1}) is selected as the target cell to receive energy.

Once the target cells are determined and selected, the intramodule CIDAB converter is enabled with setting $\varphi_{G.j}$ properly in Step 7. Meanwhile, φ_M should be zero so that no power transfer between modules occurs. The series of steps in Fig. 8(a) is performed for all modules and is repeated every T s as long as $V_{\mathrm{OC.max}} - V_{\mathrm{OC.min}}$ is greater than $V_{\mathrm{cell.th}}$. If $V_{\mathrm{OC.max}} - V_{\mathrm{OC.min}}$ becomes lower than $V_{\mathrm{cell.th}}$, cells are judged to be equalized well, and the CIDAB converter is disabled.

B. Module Equalization Mode

Contrary to the cell equalization mode, the module equalization algorithm does not need to detect targets because whole groups and modules are selected to exchange power, as illustrated in Fig. 6(b).

The flowchart of the module equalization is shown in Fig. 8(b). The module and group voltages are measured in Step 1 to estimate OCVs. As mentioned in Section III-B, the input and output currents of the CIDAB converter (i.e., $I_{X.j}$ and $I_{Y.j}$) contain not

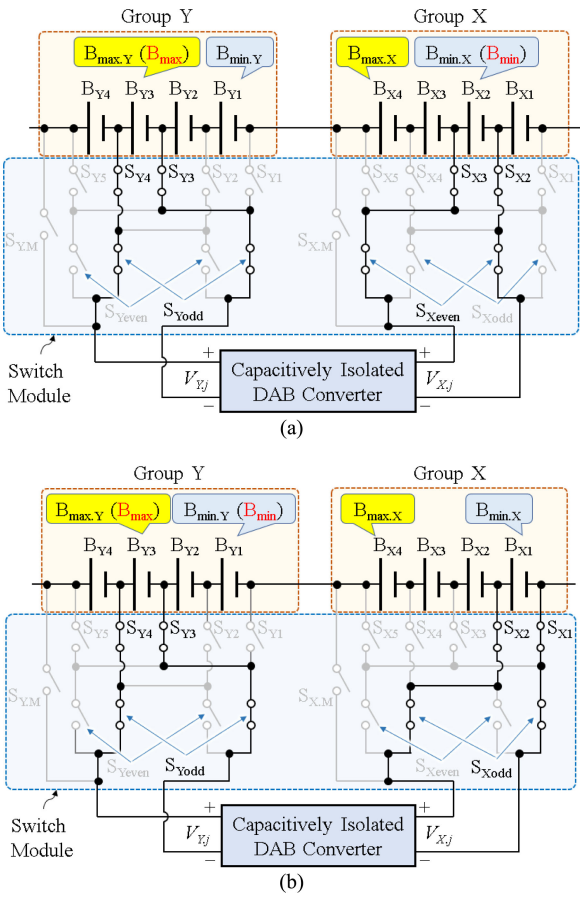

Fig. 9. Examples of (a) Step 6-A and (b) Step 6-B in cell equalization mode.

only the current due to the group equalization ($I_{GX.j}$ and I_{GYj}) but also the current due to the module equalization ($I_{M.j(j+1)}$ and $I_{M.(j+1)j}$), as expressed by (3) and (4). Hence, OCVs of groups and modules should be estimated by compensating the voltage drops due to both the group equalization and module equalization.

Similar to the simple model used for the cell OCV estimation, the OCVs of group X_j and Y_j in the jth module, $V_{OC.GX.j}$, and $V_{OC.GY.j}$, are estimated in Step 2 based on the following model:

$$\begin{cases} V_{OC.GX.j} = V_{GX.j} + \frac{n}{2} r \\ \quad \times \left(I_{GX.j} + I_{M.j(j+1)} - I_{M.(j-1)j} + I_{st} \right) \\ V_{OC.GY.j} = V_{GY.j} + \frac{n}{2} r \left(-I_{GY.j} + I_{st} \right). \end{cases} \tag{8}$$

The OCV of the jth module, $V_{OC.M.j}$, is the sum of $V_{OC.GX.j}$ and $V_{OC.GY.j}$. From (8)

$$V_{OC.M.j} = V_{OC.GX.j} + V_{OC.GY.j} = V_{M.j} + \frac{n}{2} r \times \left(I_{GX.j} - I_{GY.j} + I_{M.j(j+1)} - I_{M.(j-1)j} + 2I_{st} \right). \tag{9}$$

Step 3 judges whether modules and groups are balanced. If the OCV difference between adjacent modules or Group X_j and Y_j in each module exceeds a threshold voltage level, the module equalization starts. First, the absolute value of the OCV difference between adjacent modules (i.e., $|V_{OC.M.j} - V_{OC.M.(j+1)}|$) is calculated to be compared with the threshold level $V_{M.th}$ of the module equalization. If $|V_{OC.M.j} - V_{OC.M.(j+1)}| \geq V_{M.th}$ is yes, the operation moves to the next step. If no, the OCV difference between Group X_j and Y_j (i.e., $|V_{OC.GX.j} - V_{OC.GY.j}|$) is also calculated to be compared with the threshold level $V_{G.th}$ of the group equalization.

In Step 4, if either of $|V_{OC.M.j} - V_{OC.M.(j+1)}| \geq V_{M.th}$ or $|V_{OC.GX.j} - V_{OC.GY.j}| \geq V_{G.th}$ is detected, the CIDAB converter is enabled with properly setting both $\varphi_{G.j}$ and φ_M depending on voltage imbalance conditions. For example, if $V_{OC.M.j} > V_{OC.M.(j+1)}$, φ_M should be positive arbitrary value for the intermodule CIDAB converter to transfer power from jth module to $(j+1)$th one. If $V_{OC.GX.j} < V_{OC.GY.j}$, $\varphi_{G.j}$ should be negative so that the intramodule CIDAB converter delivers power from Group Y to X. On the other hand, if the calculated OCV differences are smaller than threshold levels, the CIDAB converter is disabled to stop the module equalization.

This course of the module equalization is performed for all modules until all module and group voltages are balanced.

V. Design Example

This section presents a design example of the CIDAB converter for LIB modules consisting of 12 cells connected in series. Component values are determined so that $I_{X.j} = I_{Y.j} = 1.0$ A in the cell equalization mode and $I_{XG.j} = I_{YG.j} = I_{M.j(j+1)} = I_{M.(j+1)j} = 1.0$ A in the module equalization mode when $V_{Xcell.j} = V_{Ycell.j} = 4.2$ V and $V_{XG.j} = V_{XG.(j+1)} = V_{YG.j} = 25.2$ V (4.2 V/cell). The switching frequency is $f_s = 100$ kHz.

A. Inductance

Denominators in (1) and (3), which yield $I_{X.j} = I_{Y.j}$ in the cell equalization mode and $I_{XG.j} = I_{YG.j}$ in the module equalization mode, are the same, whereas $V_{Xcell.j}$ and $V_{Ycell.j}$ (= 4.2 V) in the nominator in (1) is one-sixth of $V_{XG.j}$ and $V_{YG.j}$ (= 25.2 V). Therefore, $d_{\varphi G.j}$ in (1) must be rather larger than that in (3) in order to fulfill $I_{X.j} = I_{Y.j} = 1.0$ A and $I_{XG.j} = I_{YG.j} = 1.0$ A. Here, $d_{\varphi G.j}$ is assumed to be 0.167 (i.e., $\varphi_{G.j} = 60°$) in the cell equalization mode. From (1), L is determined as

$$L = \frac{4.2\text{ V}}{2 \times 100\text{ kHz} \times 1.0\text{ A}} 0.167 \left| 0.5 - 0.167 \right| \rightarrow L = 1.2\ \mu\text{H}. \tag{10}$$

Voltage values in nominators (i.e., $V_{XG.j}$, $V_{YG.j}$, and $V_{XG.(j+1)}$) in (3) and (4) are 25.4 V. Since (3) and (4) are expressed in the very similar form, operating the converter with $d_{\varphi M} = d_{\varphi G.j} = 0.167$ is considered preferable. Applying $d_{\varphi M} = d_{\varphi G.j} = 0.167$ into (3) and (4) yields

$$L_M = 1.2\ \mu\text{H}. \tag{11}$$

B. Capacitance

According to (1) and (3), the input and output currents of the CIDAB converter are dependent on L or L_M and are independent on capacitances of C_H and C_L or C_{MH} and C_{ML}, as long as these passive components do not resonate. To avoid resonant operations, capacitances of C_H, C_L, C_{MH}, and C_{ML} should be large enough so that the resonant frequency of L and the series

connection of C_H–C_L (or L_M and C_{MH}–C_{ML}) is at least lower than one-fifth of f_s. Given dc bias characteristics of ceramic capacitors, the capacitance C of C_H, C_L, C_{MH}, and C_{ML} should have enough margins. Here, C is determined to be 1.5 times larger than the theoretical value

$$\frac{1}{2\pi\sqrt{\frac{LC}{2\times 1.5}}} = \frac{f_s}{5} \rightarrow C = 160\ \mu\mathrm{F}. \tag{12}$$

C. Voltage Stress of Capacitors

In this section, all cell voltages and group voltages are assumed equal to be V_{cell} and V_G, respectively. In the cell equalization mode, voltages of C_H and C_L, V_{CH} and V_{CL}, vary depending on which cells are selected. V_{CH} and V_{CL} become the highest when the most distantly located cells [e.g., B_{X1} and B_{Y4} in the case of Fig. 6(a)] are selected. In the module equalization mode [see Fig. 6(b)], on the other hand, V_{CH} and V_{CL} are equal to the group voltage V_G. V_{CH} and V_{CL} in the cell and group equalization modes are summarized as

$$V_{\mathrm{CH}},\ V_{\mathrm{CL}} = \begin{cases} (n-1)\,V_{\mathrm{cell}} & (\text{Cell Equalization}) \\ V_M - V_{\mathrm{cell}} & (\text{Module Equalization}) \end{cases} \tag{13}$$

where n is the number of cells in a module (i.e., $n = 12$ for the 12-cell module). This equation suggests that V_{CH} and V_{CL} in the cell equalization mode are higher than those in the module equalization mode. According to the given design target, the voltage rating of C_H and C_L can be determined as

$$V_{\mathrm{CH}}\ , V_{\mathrm{CL}} = (12-1)\ \times 4.2\ \mathrm{V}\ =\ 46.2\ \mathrm{V} \rightarrow 100\ \mathrm{V}. \tag{14}$$

Since $\mathrm{C_{MH}}$ and $\mathrm{C_{ML}}$ are connected between adjacent Group X's, their voltages, V_{CMH} and V_{CML}, are equal to the module voltage V_M

$$V_{\mathrm{CMH}},\ V_{\mathrm{CML}} = V_M\ =\ 50.4\ \mathrm{V} \rightarrow 100\ \mathrm{V}. \tag{15}$$

From (14) and (15), ceramic capacitors with a rated voltage of 100 V are selected for C_H, C_L, C_{MH}, and C_{ML}.

VI. Experimental Results

A. Prototype

The proposed modular equalization system for two modules, each comprising 12 cells connected in series, was built. The CIDAB converter and switch module were separately built, and these were connected using D-sub connectors. The prototypes of the CIDAB converter and switch module are shown in Fig. 10(a) and (b), respectively. Circuit components are listed in Table I. The LC tank for the intermodule CIDAB converter (L_M, C_{MH}, and C_{ML}) was mounted on the switch module board. The switches in the CIDAB converter were driven with 50% duty cycle at $f_s = 100$ kHz.

B. Characteristics of CIDAB Converter

Before performing equalization tests, characteristics of the CIDAB converter in the cell and module equalization modes were individually measured. In the cell equalization mode, Ports X and Y of the CIDAB converter are connected to a cell through

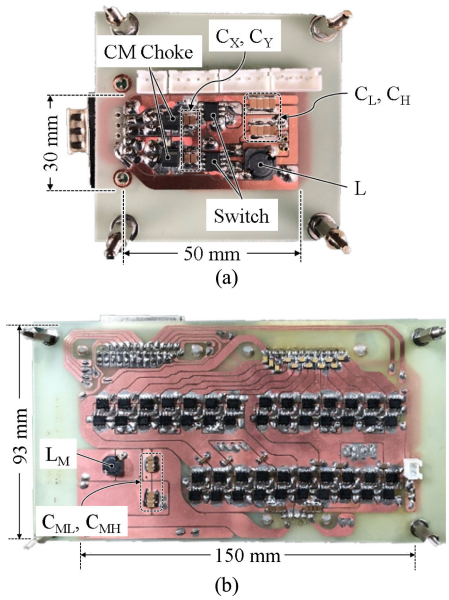

Fig. 10. Photographs of (a) CIDAB converter and (b) switch module.

TABLE I
Component List of CIDAB Converter and Switch Module

	Component	Value
CIDAB Converter	$\mathrm{Q_{XH}}$, $\mathrm{Q_{XL}}$, $\mathrm{Q_{YH}}$,$\mathrm{Q_{YL}}$	IRF7351PbF, R_{on} = 17.8 mΩ
	L	1.2 μH
	$\mathrm{C_H}$, $\mathrm{C_L}$	Ceramic Capacitor, 10 μF × 16
	$\mathrm{C_X}$, $\mathrm{C_Y}$	Ceramic Capacitor, 22 μF × 8
	Common Mode Choke	DLW5BTM102SQ2L
	Gate Driver	UCC27201D
Swith Module	$\mathrm{S_X}$, $\mathrm{S_Y}$, $\mathrm{S_{even}}$, $\mathrm{S_{odd}}$	FDS2572, R_{on} = 47 mΩ
	$\mathrm{L_M}$	1.2 μH
	$\mathrm{C_{MH}}$, $\mathrm{CM_L}$	Ceramic Capacitor, 10 μF × 16
	Gate Driver	Si8751AB-IS

the switch module, as exemplified in Fig. 6(a). In the module equalization mode, on the other hand, whole Groups X and Y are connected to the CIDAB converter [see Fig. 6(b)]. Hence, the CIDAB converter was tested with $V_{X.j} = V_{Y.j} = 4.2$ V and $V_{XG.j} = V_{YG.j} = 25.2$ V ($= 4.2$ V $\times$ 6 cells) for the cell and module equalization modes, respectively.

Measured output current (i.e., $I_{Y.j}$) characteristics are shown in Fig. 11. The experimental results agreed very well with the theoretical characteristics, verifying the operation of the prototype of the CIDAB converter.

Measured waveforms in the cell equalization mode with $\varphi_{G.j} = 60°$ and the module equalization mode with $\varphi_M = 12°$ are shown in Fig. 12(a) and (b). $I_{Y.j}$ was nearly 1.0 A in both cases, but the current slope in the module equalization mode was steeper because of the higher input and output voltages of 25.2 V.

The measured power conversion efficiencies in the cell and module equalization modes are shown in Fig. 13(a) and (b), respectively. Theoretical efficiencies calculated based on loss models are also shown. The theoretical loss model is discussed

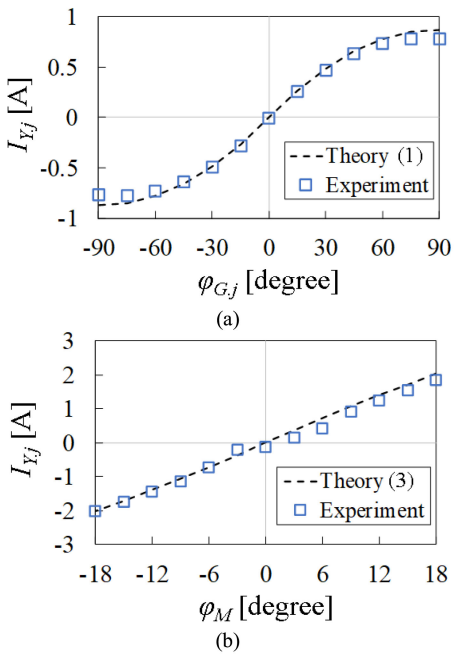

Fig. 11. Measured output current characteristics of CIDAB converter in (a) cell and (b) module equalization modes.

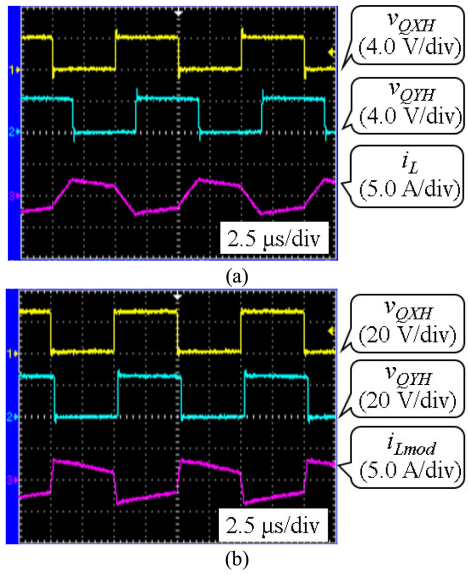

Fig. 12. Measured operation waveforms of CIDAB converter in (a) cell equalization mode with $\varphi G.j = 60°$ and (b) module equalization mode with $\varphi M = 12°$.

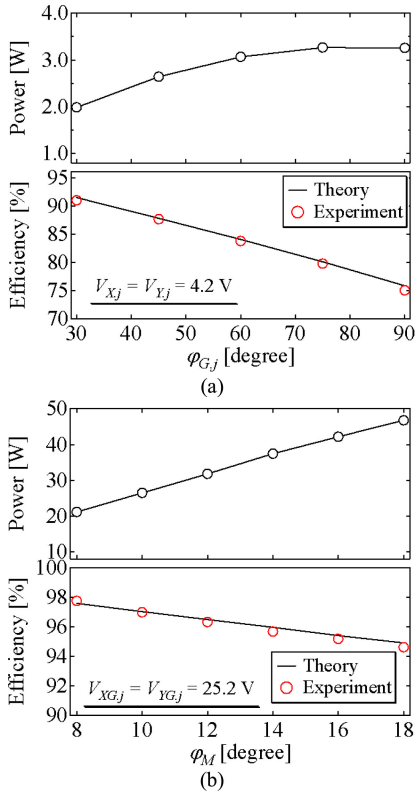

Fig. 13. Measured power conversion efficiencies of CIDAB converter in (a) cell and (b) module equalization modes.

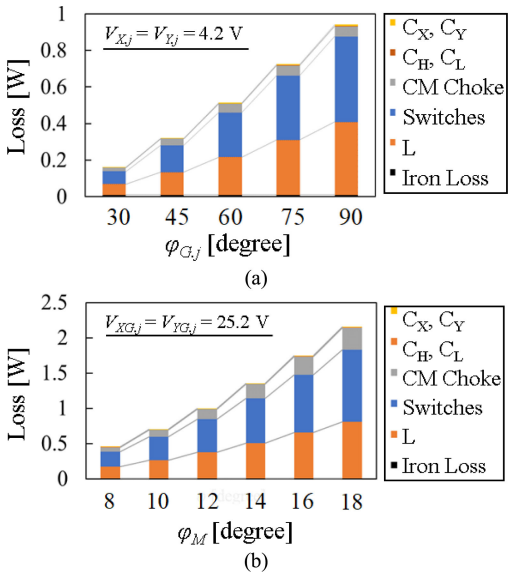

Fig. 14. Estimated loss breakdowns of CIDAB converter in (a) cell and (b) module equalization modes.

in the following paragraph. Similar to traditional transformer-based DAB converters, the measured efficiencies of the CIDAB converter decreased with $\varphi_{G.j}$ and φ_M due to increased circulating currents. The measured and calculated efficiencies agreed well, verifying the loss models.

The loss breakdowns estimated by the theoretical loss models are shown in Fig. 14. Switching losses were assumed zero thanks to the ZVS operations. Except for the iron loss, all losses were Joule losses, which were the product of resistance and the square of an rms current. The iron loss of L was calculated based on Steinmetz's equation [58]. The Joule losses of L, C_H, and C_L were calculated using an rms current of L, $I_{L.\mathrm{rms}}$. Since every switch conducts during half the switching period, the rms switch currents are equal to $I_{L.\mathrm{rms}}/\sqrt{2}$. The rms currents of the CM chokes are equal to $I_{X.j}$ and $I_{Y.j}$ in the cell equalization mode (3) or $I_{XG.j}$ and $I_{YG.j}$ in the module equalization mode

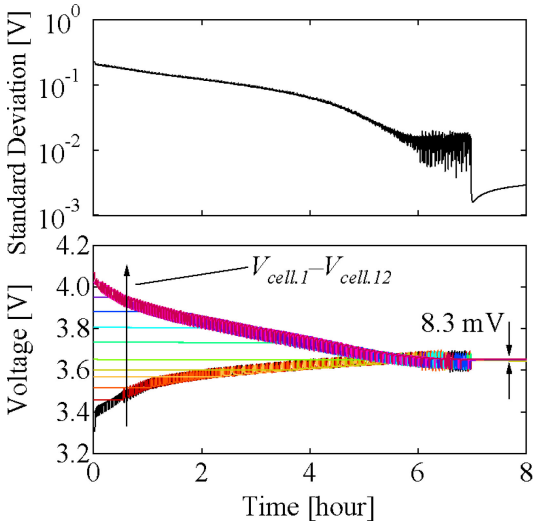

Fig. 15. Resultant voltage and standard deviation profiles of 12 cells in cell equalization mode.

(4). The rms currents of C_X and C_Y were obtained from the simulation analysis.

The estimated breakdowns revealed that Joule losses of the switches and inductors were dominant while losses of capacitors were negligibly small. Hence, employing switches and inductors with lower resistance is an effective way to improve the power conversion efficiencies.

C. Cell Equalization

The cell equalization test was performed using 12 cylindrical cells, each with a typical capacity of 3350 mAh (NCR18650B, Panasonic). Initial OCVs were intentionally imbalanced in the range of 3.31–4.07 V, corresponding to the state-of-charge variation of 2%–96%. The cell equalization was performed with $\varphi_{G.j} = \pm 60°$ and $V_{\mathrm{cell.th}} = 10$ mV. A compact data acquisition system (Compact DAQ, National Instruments) with voltage input modules (NI-9221) and digital I/O modules (NI-9403) was used as a control platform. The equalization algorithm (see Fig. 8) was implemented with LabVIEW.

The resultant cell equalization profiles are shown in Fig. 15. Cells with high initial voltages supplied power to the CIDAB converter, and their voltage decreased. At the same time, cells with low initial voltages received power from the CIDAB converter, and their voltage increased. Thanks to this energy redistribution through the CIDAB converter, cell voltages gradually converged, and the voltage imbalance decreased as low as 8.3 mV. The calculated standard deviation of cell voltages at the end of the cell equalization test was 2.9 mV, demonstrating the cell equalization performance of the proposed equalizer.

D. Module Equalization

The module equalization test was performed for two modules, each consisting of 12 cells connected in series. The experimental setup is shown in Fig. 16. Initial OCVs of the modules and groups were imbalanced in the range of 43.63–46.82 V and 20.95–23.71 V, respectively. The module equalization test was

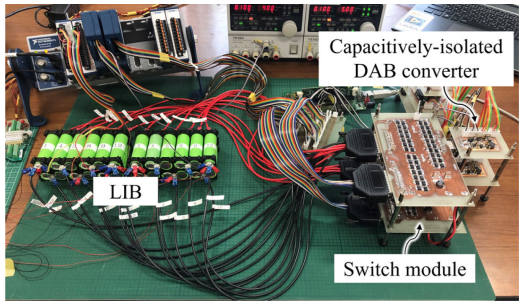

Fig. 16. Experimental setup for module equalization test using two LIB modules, each consisting of 12 cells connected in series.

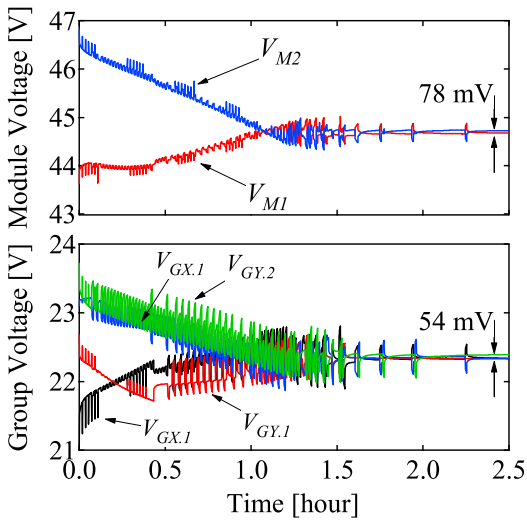

Fig. 17. Resultant voltage and standard deviation profiles of two modules in module equalization mode.

performed with $\varphi_{G.j} = \varphi_M = \pm 12°$ and $V_{M.\mathrm{th}} = V_{G.\mathrm{th}} = 80$ mV.

The recorded module equalization profiles are shown in Fig. 17. The module and group voltages converged simultaneously. Group and module voltages were nearly equalized at 1.6 h. The voltage mismatches of the groups and modules decreased as low as 54 and 78 mV, respectively, at the end of the test, thus sufficiently eliminating the voltage imbalance.

VII. Comparison With Conventional Equalizers

This section compares the proposed and conventional equalizers from the viewpoint of component counts and reported efficiency. Since the proposed modular equalization system consists of two levels (i.e., the cell-level equalization in each module and module-level equalization), the comparison is performed not only for the system but also for intramodule equalizers.

Since each switch requires an auxiliary circuit, including a driver and its power supply, the switch count can be a good index to represent the circuit complexity. The circuit volume is chiefly dependent on passive component counts, especially bulky magnetic component counts. Equalization speed or time, on the other hand, cannot be fairly compared and hence is excluded from the comparison because it is dependent on

TABLE II
COMPARISON BETWEEN INTRAMODULE EQUALIZER AND CONVENTIONAL EQUALIZERS

Topology	Switch	Selection Switch	L	C††††	D	Transformer	Reported Efficiency
[31]	2	$2n$	-	-	2	2	-
[32]	1	$n+5$	-	-	1	1	-
[33]	2	$2n$	-	-	2	2	-
[34]	2	$2n+10$	2	3	2	-	60%
[35]	$2(n+1)$	-	1	-	$2(n+1)$	-	-
[36]	4 BS†	$n+1$ ††	1	1	-	-	80%
[37]	2 BS†	$n+1$ ††	-	-	-	1	80.4%
[39]	4 BS†	$2n$	1	1	-	-	87.9% (peak)
[40]	5	$2(n+1)$ Relays	2	1	4	-	-
Proposed	4	$n+12$	1 (L) + 2 (CMC†††)	2	-	-	84% (average)

†BS (bidirectional switch). ††Must operate at high frequency.
†††CMC (common-mode choke), ††††Smoothing capacitors excluded.

TABLE III
COMPARISON BETWEEN PROPOSED AND CONVENTIONAL MODULAR EQUALIZATION SYSTEMS

Topology	Module Equalizer	Cell Equalizer	Switch	Selection Switch	L	C††	D	Transformer	Reported Efficiency
[28]	Forward Converter	Flyback Converter	m	mn	-	-	n	$mn+m$	81.6% (average)
[29]	SCC	SCC	$2mn+2m$	-	-	$m(n-1)$ $+(m-1)$	-	-	-
[29]	SCC	Multi-Winding Flyback Converter	$3m$	-	-	$m-1$	mn	m (n Secondary Windings)	-
[42]	PWM Converter	PWM Converter	$2m(n-1)$ $+2(m-1)$	-	$m(n-1)$ $+(m-1)$	-	-	-	-
[43]	Multidirectional Multiport Converter	PWM Converter	$2m(n-1)$ $+2m$	-	$m(n-1)$	$2m$	-	1 (m Secondary Windings)	89.7% (average)
[45]	Flyback Converter	Flyback Converter	mn	-	-	-	-	m (n Secondary Windings)	89.4% (peak)
[47]	Forward Converter	Forward Converter	mn	-	-	-	1	m (n Secondary Windings)	95.6% (peak)
[48]	SCC	Multi-Winding Flyback Converter	$mn+2m$	-	-	$m-1$	m	m (n Secondary Windings)	83.3% (average)
Proposed	CIDAB Converter	CIDAB Converter	$4m$	$m(n+12)$	$2m-1$ (L) + $2m$ (CMC†)	$2(2m-1)$	-	-	Cell: 84% (average) Module: 96

†CMC (common mode choke). ††Smoothing capacitors excluded.

various factors, such as numbers of cells and modules, initial imbalance condition, equalization current, cell capacity, etc.

The intramodule equalizer in a single module in the proposed system is compared with conventional equalizers using selection switches, as shown in Table II, where n is the cell count. Conventional equalizers based on flyback converters [31]–[33] need a transformer, and, therefore, these topologies would be bulky. Transformerless topologies [34], [39], [40] contain $2n$ selection switches, and their circuit complexity is prone to soar as n increases. Although the equalizers in [36] and [37] can reduce the number of selection switches as low as $n+1$, high-frequency gate drivers are necessary to drive these selection switches, likely increasing the complexity and cost of drive circuits. Meanwhile, the intramodule equalizer in the proposed system is transformerless, and its selection switches can operate at a low frequency, similar to those in [31]–[35]. In comparison with the conventional equalizers with $2n$ selection switches from the viewpoint of the selection switch count, the proposed intramodule equalizer is advantageous for modules comprising more than 12 cells.

The proposed modular equalization system is compared with conventional modular systems, as shown in Table III where m is the module count. Most of the conventional systems are based on isolated converters, such as flyback converters and forward converter, and require transformers or multiwinding transformers that lead to the increased circuit volume, cost, and design difficulty. Although the conventional systems in [29] and [42] are transformerless, passive component counts are proportional to n, likely increasing the circuit volume. The proposed modular equalization system, on the other hand, not only is transformerless but also can reduce the passive component count and, therefore, would be advantageous to achieve circuit miniaturization. Although $m(n+12)$ selection switches are necessary, these switches can be slow and do not need high-frequency gate drivers.

VIII. Conclusion

This article has proposed the modular equalization system consisting of multiple LIB modules connected in series. Cells in each module are subdivided into two groups, and each module contains a selection switch module and an intramodule CIDAB converter that performs direct cell-to-cell equalization. The switching legs of adjacent modules' CIDAB converters are connected through an *LC* tank to configure an intermodule equalizer that performs the module equalization. Based on the DPS control technique, the PS angles of both the intra- and intermodule CIDAB converters are manipulated to perform the cell and module equalization. The proposed equalization system offers good scalability as the design of the intramodule equalizer is fixed while intermodule equalizers can be configured without the need for additional active switches.

The proposed modular equalization system operates either in the cell or module equalization modes, and these modes do not coincide. In the cell equalization mode, the target cells in each module are determined based on calculated SOCs and are selected by the switch module. The intramodule CIDAB converter transfers power between the selected target cells to perform cell equalization. In the module equalization mode, on the other hand, whole groups are selected in each module, and both the intra- and intermodule CIDAB converters simultaneously operate to perform the module equalization.

The experimental prototype for two LIB modules, each consisting of 12 cells connected in series, was built. The cell and module equalization tests were separately carried out from voltage imbalanced conditions. The cell and module voltages were sufficiently equalized, demonstrating the equalization performance of the proposed modular equalization system.

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