Mitigation of Ground Leakage Current of Single-Phase PV Inverter Using Hybrid PWM With Soft Voltage Transition and Nonlinear Output Inductor

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***Abstract*—A single-phase transformerless full-bridge photovoltaic grid-tie inverter is presented. It utilizes 1) a virtual ground technique to mitigate ground leakage current, 2) a hybrid pulsewidth modulation (HPWM) scheme to profile the output current and prevent sudden changes in the common-mode voltage, and 3) a nonlinear output inductor to attenuate current ripple around zero crossings and minimize filter size. The HPWM is effectively the same as unipolar PWM (UPWM), but with soft voltage transition modulation introduced around the zero crossings. Apart from low switching losses, the output filter is implemented with a minimum number of components to achieve high attenuation of ripple current. By deriving the switching trajectory, a mathematical model is formulated, and the ground leakage current and the output current with the traditional UPWM and the proposed HPWM schemes are compared. The output current harmonics caused by the nonlinear output inductor is analyzed by the Volterra theory. A 340 W, 380 Vdc/110 V ac, 50 Hz prototype has been built and evaluated.**

***Index Terms*—Ground leakage current, nonlinear inductor, photovoltaic (PV), pulsewidth modulation (PWM), transformerless inverters, virtual ground (VG).**

NOMENCLATURE

$v_{\rm dc}$	Input dc voltage
$V_{\rm dc}$	Average value of $v_{\rm dc}$
i_g	Output current of the inverter
$C_{\rm lk}$	Ground leakage capacitance
$i_{\rm lk}$	Ground leakage current
$I_{\rm lk\_rms}$	rms value of $i_{\rm lk}$
v_g	Grid voltage
V_g	rms value of v_g
$i_{\rm ref}$	Output current reference
$I_{\rm ref}$	rms value of $i_{\rm ref}$
ω_g	Angular frequency of v_g
ΔI_{Lc}	Current ripple of L_c
$T_{\rm sw}$	Switching period
$f_{\rm sw}$	Switching frequency ($=1$ / $T_{\rm sw}$)
i_{Lg}	Current through the inductor L_g
i_{Lc}	Current through the inductor L_c
i_{C1}	Current through the inductor L_{C1}
i_{Lg_HF}	High-frequency component of i_{Lg}
i_{Lc_HF}	High-frequency component of i_{Lc}
i_{C1_HF}	High-frequency component of i_{C1}
$v_{\rm cm}$	Common-mode (CM) voltage
$v_{\rm dm}$	Differential-mode (DM) voltage
α	Ratio between L_g and L_c
f_o	Resonant frequency of LCL filter
$N_{\rm sw}$	Total number of switching cycles in zero-crossing region
$T_{\rm SVT}$	Duration of the soft voltage transition period
λ	Number of switching cycles in $T_{\rm SVT}$
$L_{g,\max}$	Inductance of $L_g$when $i_{Lg}=0$
N_{Lg}	Number of turns of the coil in L_g

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I. INTRODUCTION

GRID-TIE voltage source inverters (VSIs) have been widely used in distributed power generation systems, such as photovoltaic (PV) systems [1]. Among different inverter topologies, the full-bridge (FB) topology is popular for its simple structure and fewer switching devices. Transformerless FB VSI is preferable as it does not have bulky, costly, and lossy isolation transformer. However, mitigation of ground leakage current caused by the high-frequency (HF) switching of the switches in the FB is a key design challenge, especially in installations with considerable parasitic capacitance [2]. To ensure safe operation, many industrial standards impose limits on the ground leakage current [3].

Extensive literature is devoted to various ground leakage current mitigation techniques. They can be divided into three major approaches, including modulation schemes, circuit topologies, and virtual ground (VG) techniques.

There are three popular modulation schemes. They are bipolar PWM (BPWM) (two-level switching scheme), unipolar PWM (UPWM) (three-level switching scheme with one leg switching at the grid frequency), and double-frequency unipolar PWM

TABLE I
COMPARISON BETWEEN PRIOR ART AND PROPOSED INVERTER

Ref	Power	Switching frequency	Number of switches	Leakage capacitance tested	Efficiency	THDi	Total output filter inductance	Additional capacitance	RMS leakage current	EMI filter
AVG [10]	100W - 950W	20kHz	6	220nF	95.3% - 96.3%	5% - 20%	1mH	5μF	130mA - 170 mA	No
VG1 [11]	100W - 1kW	20kHz	4	100 nF	97.5% - 99.0%	-	6mH	10μF	15 mA	No
VG2 [12]	100W - 500W	20kHz	5	75nF	92.5% - 97.0%	2.1% @ 500W	8.8mH	0.34 μF + 940 μF	N.A.	No
VG3[9]	10kW	20kHz	4	10nF	N.A.	-	7.75mH	17.8 μF	1.4mA†	No
Proposed inverter	400W	20kHz	4	220 nF	96.5% - 97.5%	1.6% - 3.5%	1.6mH - 6.72mH*	4.7 μF	98mA - 105mA	No

*Physical size is similar to a 1.6 mH inductor.
†Simulation result.

(DUPWM) scheme (three-level switching scheme with two legs switching at HF) [4]. BPWM generally causes high switching loss and current ripples [5]. By adding extra switching devices, new topologies, such as HERIC, H5, H6, etc., have been proposed and UPWM scheme is applied [6], [7]. Although UPWM exhibits low switching loss, at least one extra switching device, acting as a bidirectional blocking switch, is needed.

By connecting the midpoint of the dc input capacitor to the neutral point, passive VG techniques can reduce the ground leakage current of three-phase inverters [8], [18]. For single-phase inverters, a capacitor-center-tapped (CCT) technique is proposed in [9]. Two series capacitors are connected to the dc side with their mid-point connected to the neutral to create a low impedance path for the HF current ripples. DUPWM is applied to both legs, which are switched at HF. The output filter has to be symmetrical and thus consists of six components, forming two symmetrical LCL filters.

An active virtual ground (AVG) technique with two low-frequency-switched devices introduced on the output side is proposed in [10]. Since the UPWM is used, the switching loss can be reduced. An LCL filter equivalence is formed with the added switches and does not require using additional grid-side inductor. The AVG technique can attenuate the ground leakage current with three filter components only and the UPWM scheme. However, two extra switching devices are needed.

An FB topology with a passive VG capacitor, C_1, and a minimum number of output filter components to attenuate common-mode (CM) ground leakage current is presented. The switches in the FB are modulated by a hybrid pulsewidth modulation (HPWM) scheme, which is extended from UPWM with soft voltage transition modulation (SVTM) introduced around the zero crossings. Apart from shaping the output current, it also prevents sudden changes in the CM voltage. A nonlinear output inductor is used to attenuate ripple current around zero crossings. A comparison with prior arts using VG and AVG techniques is given in Table I. The proposed architecture has been demonstrated on a 340 W, 380 V dc/110 V ac, 50 Hz inverter prototype.

II. SYSTEM ARCHITECTURE AND MODULATION SCHEME

Fig. 1 shows the proposed FB inverter with an LCL filter, formed by the inductor L_c, nonlinear inductor L_g, and a VG capacitor C_1. $S_1 \sim S_4$ form an FB. L_c and L_g are both converter-side inductors. The inductance of L_g increases with its decreasing current. C_1 is connected between the grid-side node of L_c and the reference of the dc input. The value of C_1 is designed to be much larger than the typical value of the leakage capacitance $C_{\rm lk}$ so that the ripple current, generated by the FB, will dominantly flow through C_1. Thus, L_c, L_g, and C_1 form an LCL filter equivalence.

The output current i_g is regulated by an average current controller, in which a proportional resonant (PR) control with the dc voltage feedforward is used. The operation is described in detail in [13]. A sinusoidal phase-locked loop is used to provide phase information of the grid voltage. The output current reference is determined by multiplying $I_{\rm ref}$ with the grid voltage. The modulating signal v_m is generated by combining the output of the PR controller $v_{\rm PR}$ with the output of the feedforward controller $v_{\rm ff}$. The modulating signals for the two legs, $v_{m,a}$ for leg A and $v_{m,b}$ for leg B, respectively, are derived from v_m. The gate signals for the switches S_1 and S_3 are generated by comparing $v_{m,a}$ with the carrier signal $v_{{\rm TRI},a}$, while the gate signals for the switches S_2 and S_4 are generated by comparing $v_{m,b}$ with the carrier signal $v_{{\rm TRI},b}$.

The waveforms of $v_{m,a}$ and $v_{m,b}$ with UPWM are shown in Fig. 2(a) and that with HPWM are shown in Fig. 2(b).

II. System Architecture and Modulation Scheme

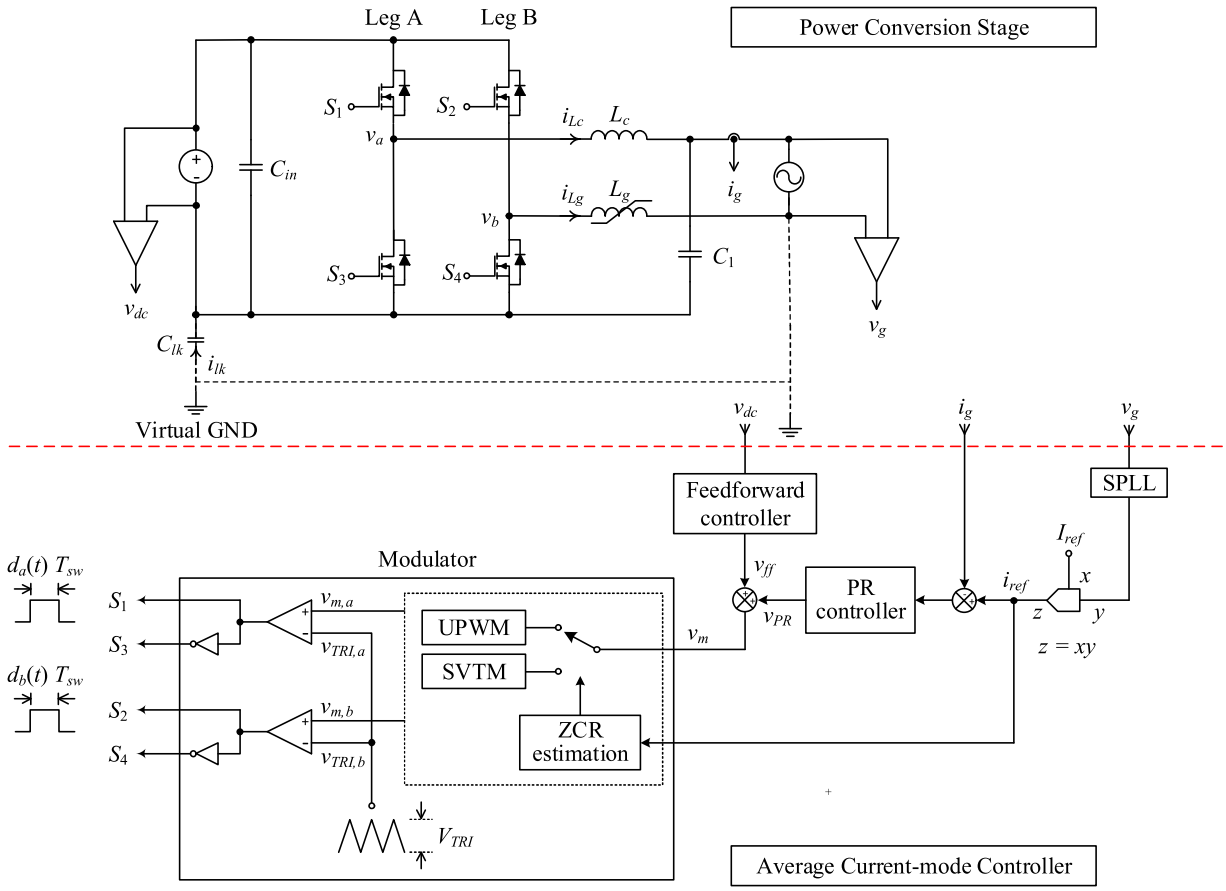

Fig. 1. Architecture of the proposed single-phase transformerless FB inverter with a VG capacitor.

HPWM has two PWM modulation schemes [4]. It is the same as UPWM in nonzero-crossing regions (NZCRs). It is different from UPWM that it has soft voltage transition introduced in the zero-crossing regions (ZCRs).

In the NZCRs, $v_{m,a}$ is derived from v_m as follows:

$$v_{m,a}(t) = \begin{cases} v_m(t) & +\text{ve half cycle} \\ 1 + v_m(t) & -\text{ve half cycle} \end{cases} \tag{1}$$

$$v_{m,b}(t) = \begin{cases} 0 & +\text{ve half cycle} \\ 1 & -\text{ve half cycle.} \end{cases} \tag{2}$$

The duty cycle of S_1, $d_a(t)$, is

$$d_a(t) = \frac{1}{V_{\text{TRI}}}\, v_{m,a}(t) \tag{3}$$

where V_{TRI} is the peak value of $v_{\text{TRI},a}$.

The duty cycle of S_3 is the complement of S_1. The duty cycle of S_2, $d_b(t)$, is

$$d_b(t) = \frac{1}{V_{\text{TRI}}}\, v_{m,b}(t) \tag{4}$$

where V_{TRI} is the peak value of $v_{\text{TRI},b}$.

The modulation is center aligned [4]. The duty cycle of S_4 is the complement of S_2.

In the ZCRs, an SVTM scheme is proposed [shown in Fig. 3(b)]. Instead of changing from 0 to 1 in UPWM, the duty cycle of S_2, i.e., $d_b(t)$ is gradually changed between 0 and 1 in N_{sw} cycles. The duty cycle of S_2 in ith switching cycle, $d_b[i]$, is

$$d_b[i] = \begin{cases} \frac{i}{N_{\text{sw}}} & \text{ZCR (from } +\text{ve to } -\text{ve half cycle)} \\ 1 - \frac{i}{N_{\text{sw}}} & \text{ZCR (from } -\text{ve to } +\text{ve half cycle)} \end{cases} \tag{5}$$

where $i = 1, 2, \ldots, N_{\text{sw}}$.

In order to ensure that the average output voltage of the FB is unaffected by the SVTM, the duty cycle of S_1 is offset by $d_b[i]$. Take the zero-crossing point as datum. The duty cycle of S_1 in the ith switching cycle, $d_a[i]$, equals

$$d_a[i] = \frac{1}{V_{\text{TRI}}}\, v_{m,a}((i - \frac{N_{\text{sw}}}{2})T_{\text{sw}}) + d_b[i]. \tag{6}$$

With the same v_m shown in Fig. 3(a)–(c) illustrates the variations of the duty cycles of the gate signals for S_1 and S_2 with SVTM and UPWM, respectively. UPWM is the case when $N_{\text{sw}} = 0$. It can be observed that the duty cycles of S_1 and S_2 do not change abruptly with the SVTM, resulting in a smooth transition of the CM voltage.

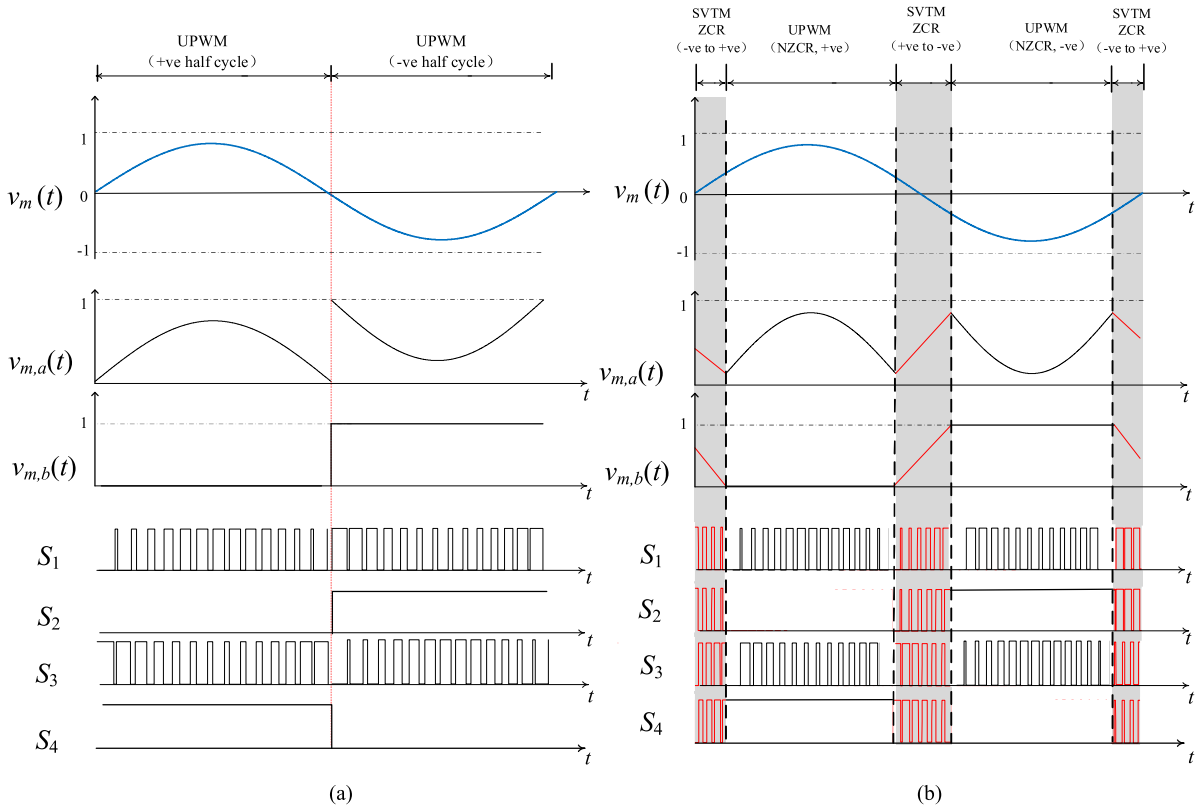

Fig. 2. Key waveforms under UPWM and HPWM schemes. (a) UPWM scheme. (b) HPWM scheme.

Hence, as shown in Fig. 1, the controller will switch the modulation scheme between the UPWM and the proposed SVTM in the NZCR and ZCR.

III. Operation in NZCR

In this section, the ground leakage current of the inverter operating in the NZCR is first derived and then its mitigation with the VG technique is discussed.

Fig. 4 shows the equivalent circuit model in HF operation. As shown in Fig. 4(a), the output voltages of legs A and B are v_a and v_b with the respect to the negative dc, respectively. They are represented by two independent voltage sources. In Fig. 4(b), since v_a consists of HF components and v_b consists of LF components, only v_a is taken into account. v_b equals to 0 in +ve half cycle and to $V_{\rm dc}$ in −ve half cycle. L_c, C_1, and L_g form an LCL filter. The VG capacitor C_1 is connected in parallel with the leakage capacitor $C_{\rm lk}$. Its value is designed to be much larger than $C_{\rm lk}$. Dominant HF current will then flow through C_1 and thus the ground leakage current $i_{\rm lk\_HF}$ is reduced. Although L_c and L_g are both converter-side inductors, it is unnecessary to ensure that their values are the same, different from the prior art using symmetrical filters that require them to be similar. *L. Mains* is the grid inductance.

In order for i_g to follow $i_{\rm ref}$, the duty ratio, *D*, is approximated by

$$D\,(t) = v_m(t) \approx \frac{v_g(t)}{V_{\rm dc}} \tag{7}$$

where $v_g(t) = \sqrt{2}\,V_g\ \cos\ \omega_g t$.

The peak-to-peak current HF ripple of $L_{\rm c}$, ΔI_{Lc}, is

$$\begin{aligned}|\Delta I_{Lc}(t)| &= |D(t)|\,T_{\rm sw}\,\frac{[V_{\rm dc} - |v_g(t)|]}{L_c} \\ &= \frac{V_{\rm dc}\,T_{\rm sw}\,[1-|D(t)|]\,|D(t)|}{L_c}.\end{aligned} \tag{8}$$

Based on Fig. 4(b)

$$\begin{aligned}i_{\rm lk\_HF}(t) &= i_{Lc\_HF}(t) - i_{Lg\_HF} - i_{C1\_HF}(t) \\ &= i_{Lc\_HF}(t)\,\frac{H(\omega)}{G(\omega)}\end{aligned} \tag{9}$$

where $-\omega^3 C_1 C_{\rm lk}$L_Mains$+\omega^2(L_g\,C_{\rm lk}+L_g\,C_1+C_1\,L.\,Mains)$ $-\,1$ and $H(\omega) = \omega^2 L_g\,C_{\rm lk}$.

In the following discussion, L_Mains is assumed to be zero. $i_{\rm lk}$ dominantly consists of HF component. Its rms value is close to the rms value of $i_{\rm lk\_HF}$. Based on (8) and (9), $I_{\rm lk\_rms}$ can be approximated by

$$\begin{aligned}I_{\rm lk\_rms} &\approx \sqrt{\frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} i_{\rm lk\_HF}^2(\omega_{\rm g}\,t)\;d(\omega_{\rm g} t)} \\ &= \frac{1}{\sqrt{6}}\,(V_{\rm dc} - \sqrt{2}V_g)\,\frac{V_g\ T_{\rm sw}\ C_{\rm lk}}{V_{\rm dc} L_c\ (C_1 + C_{\rm lk})}.\end{aligned} \tag{10}$$

Thus, $i_{\rm lk}$ reduces as C_1 increases.

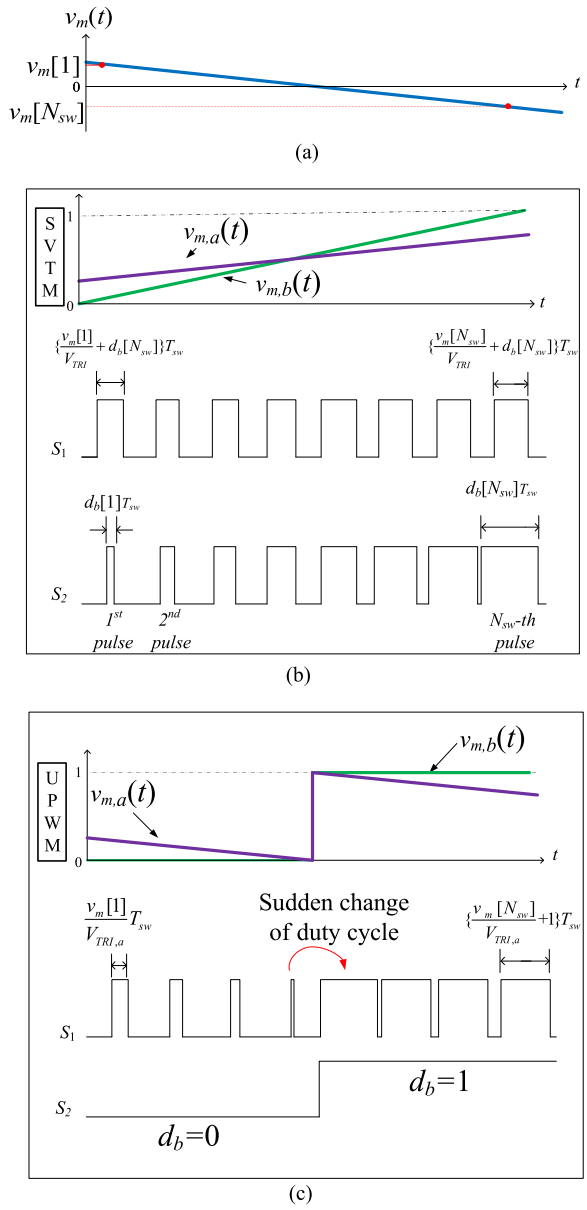

Fig. 3. Inverter output voltage around zero ac current. (a) Modulating signal generated by the controller. (b) Soft voltage transition modulation feature of HPWM. (c) Unipolar PWM.

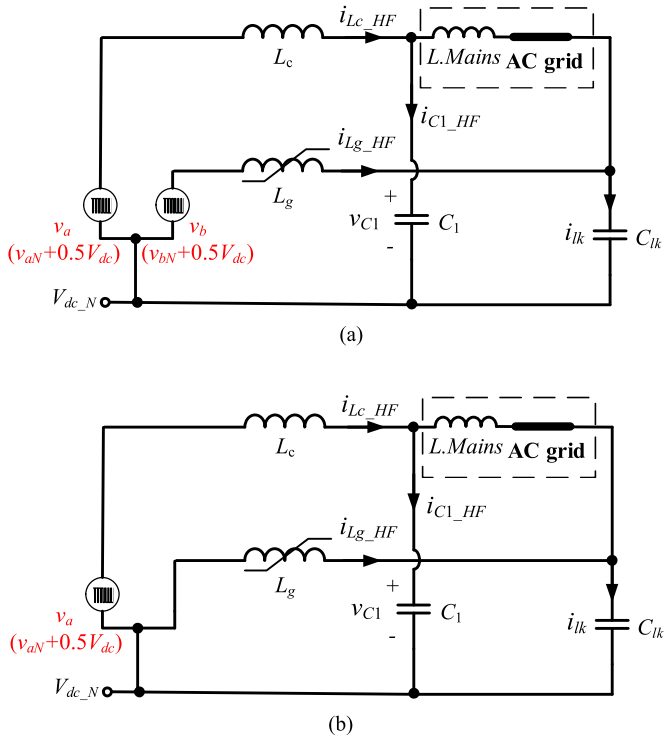

Fig. 4. High-frequency equivalent circuit. (a) Phase-leg voltages represented by two voltage sources. (b) Model in +ve NZCRs.

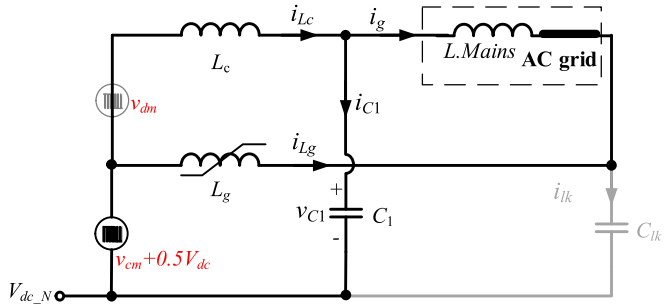

Fig. 5. Equivalent circuit in ZCR.

IV. Operations in ZCR

By studying the state trajectories, the grid currents of the inverter using traditional UPWM and the proposed SVTM scheme around the ZCR are studied. It will be shown that UPWM causes grid current oscillation upon changing the grid voltage polarity and the proposed SVTM scheme can avoid such oscillation.

A. Equivalent Circuit Model

v_a and v_b are expressed in terms of the CM voltage $v_{\rm cm}$ and the differential-mode voltage $v_{\rm dm}$ as

$$v_a = v_{aN} + \frac{1}{2}V_{\rm dc} = v_{\rm cm} + \frac{1}{2}\,v_{\rm dm} + \frac{1}{2}V_{\rm dc} \qquad (11)$$

$$v_b = v_{bN} + \frac{1}{2}V_{\rm dc} = v_{\rm cm} - \frac{1}{2}\,v_{\rm dm} + \frac{1}{2}V_{\rm dc} \qquad (12)$$

where v_{aN} and v_{bN} are the terminal voltages of two-phase legs with respect to the mid-point of dc (neutral line of ac).

Fig. 5 shows the equivalent circuit model. For the sake of simplicity in the analysis, the duration of the ZCR is very short that the grid voltage is assumed to be zero. The equivalent circuits connected across $v_{\rm cm}$ and $v_{\rm dm}$ are analyzed by applying superposition theorem. For $v_{\rm cm}$, the equivalent circuit is an LC circuit formed by $(C_1 \,//\, C_{\rm lk}) - (L_{\rm c} \,//\, L_{\rm g})$. For $v_{\rm dm}$, it is an LCL circuit formed by $L_{\rm c} - (C_1 \,//\, C_{\rm lk}) - L_{\rm g}$. Thus, when there is step change of $v_{\rm cm}$, an oscillatory response will appear.

Fig. 6 shows the waveforms of v_a, v_b, $v_{\rm cm}$, and $v_{\rm dm}$ with UPWM and SVTM around ZCR changing from positive to negative [Fig. 2(b)]. Fig. 6(a) shows that the cycle average value of $v_{\rm cm}$ (red dotted line) has a step voltage change. Fig. 6(b)

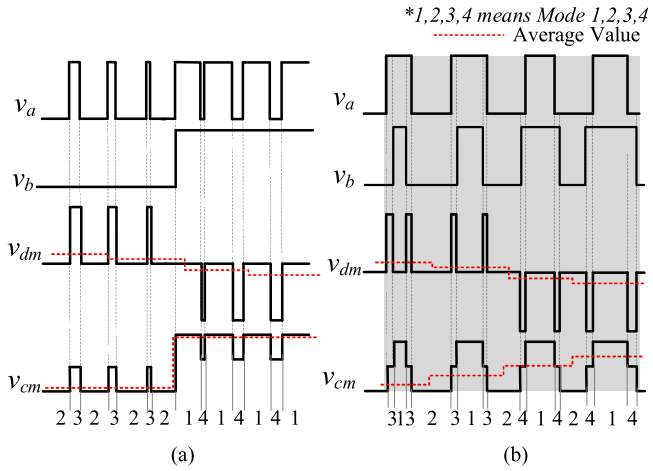

Fig. 6. Key waveforms around the ZCR changing from positive to negative half line cycle. (a) UPWM. (b) SVTM.

shows that the average value of $v_{\rm cm}$ increases gradually. This can avoid causing current oscillation. $v_{\rm dm}$ is ignored in Fig. 5 as its magnitude is much smaller than $v_{\rm cm}$. As $C_1 >> C_{\rm lk}$, it is also assumed that $i_{\rm lk} \approx 0$ and $C_{\rm lk}$ is ignored in the analysis.

B. Derivation of State Trajectories

Based on the equivalent circuit model in Fig. 5

$$\frac{d\,v_{C1}(t)}{d\,t} = \frac{i_{Lg}(t) + i_{Lc}(t)}{C_1} \tag{13}$$

$$\frac{d\,i_{Lc}(t)}{d\,t} = \frac{v_a(t) - v_{C1}(t)}{L_c} \tag{14}$$

$$\frac{d\,i_{Lg}(t)}{d\,t} = \frac{v_b(t) - v_{C1}(t)}{\alpha\,L_c} \tag{15}$$

$$i_{Lg}(t) = \frac{1}{1+\alpha}\, i_{C1}(t) \tag{16}$$

where $v_a = u_1\, V_{\rm dc}$, $v_b = u_2\, V_{\rm dc}$, and $\alpha = L_g/L_c$. Note that *L. Mains* is included in L_g in the following analysis.

u_1 and u_2 depend on the states of the four switches

$$u_1 = \begin{cases} 1,\ S_1 \text{ on and } S_3 \text{ OFF} \\ 0,\ S_1 \text{ off and } S_3 \text{ ON} \end{cases} \tag{17}$$

and

$$u_2 = \begin{cases} 1,\ S_2 \text{ on and } S_4 \text{ OFF} \\ 0,\ S_2 \text{ off and } S_4 \text{ ON} \end{cases}. \tag{18}$$

By combining (13)–(15)

$$\frac{d^2\,v_{C1}}{d\,t^2} = \frac{1}{C_1\,L}[v_a(t) + \frac{1}{\alpha}\,v_b(t) - \frac{\alpha+1}{\alpha}\,v_{C1}(t)]. \tag{19}$$

Equation (19) gives

$$v_{C1}(t) = \sqrt{[v_{C1}(0) - \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2)]^2 + [\frac{i_{C1}(0)}{\omega_0\ C_1}]^2}$$
$$\sin(\omega_0 t + \beta) + \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2) \tag{20}$$

$$i_{C1}(t) = \omega_0\ C_1$$
$$\sqrt{[v_{C1}(0) - \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2)]^2 + [\frac{i_{C1}(0)}{\omega_0\ C_1}]^2}$$
$$\times \cos(\omega_0 t + \beta) \tag{21}$$

where $v_{C1}(0)$ and $i_{C1}(0)$ are the voltage and current of C_1 at the start of every switching cycle, respectively, and

$$\omega_0 = \sqrt{\frac{L_c + L_g}{L_c L_g C_1}}$$

$$\beta = \tan^{-1}\left[\frac{i_{C1}(0)}{\omega_0\, C_1\, [v_{C1}(0) - \frac{\alpha}{\alpha+1}\frac{V_{\rm dc}}{2}(u_1 + \frac{1}{\alpha}u_2)]}\right].$$

Thus, v_{C1} and i_{C1} can be expressed in the form of a standard equation of an ellipse as

$$[v_{C1}(t) - \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2)]^2 + \frac{{i_{C1}}^2(t)}{(\omega_0\ C_1)^2}$$
$$= [v_{C1}(0) - \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2)]^2 + [\frac{i_{C1}(0)}{\omega_0\ C_1}]^2. \tag{22}$$

The center of the ellipse is $[\frac{\alpha}{\alpha+1}\ V_{\rm dc}\ (u_1 + \frac{1}{\alpha}\,u_2), 0]$. Based on (16), v_{c1} and i_{Lg} can also be expressed as

$$[v_{C1}(t) - \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2)]^2 + [\frac{(1+\alpha)\ i_{Lg}(t)}{\omega_0\ C_1}]^2$$
$$= [v_{C1}(0) - \frac{\alpha}{\alpha+1}V_{\rm dc}(u_1 + \frac{1}{\alpha}u_2)]^2 + [\frac{(1+\alpha)\ i_{Lg}(0)}{\omega_0\ C_1}]^2. \tag{23}$$

There are four possible operating modes as shown in Fig. 7. They are Modes 1, 2, 3, and 4. Based on (23), Fig. 8 shows their trajectories on $i_{Lg}-v_{C1}$ plane. The operations of the four modes are described as follows.

1) *Mode 1:* With S_1 and S_2 ON, and S_3 and S_4 OFF ($u_1 = u_2 = 1$), the trajectory moves along an elliptical path at the angular speed of ω_0 clockwise with the center at ($V_{\rm dc}$, 0).
2) *Mode 2:* With S_1 and S_2 OFF, and S_3 and S_4 ON ($u_1 = u_2 = 0$), the trajectory moves along another elliptical path at the angular speed ω_0 clockwise with the center at (0, 0).
3) *Mode 3:* With S_1 and S_4 ON, and S_2 and S_3 OFF ($u_1 = 1$, $u_2 = 0$), the trajectory moves along another elliptical path at the angular speed ω_0 clockwise with the center at $([\alpha/(\alpha+1)]\,V_{\rm dc},\ 0)$.
4) *Mode 4:* With S_2 and S_3 ON, and S_1 and S_4 OFF ($u_1 = 0$, $u_2 = 1$), the trajectory moves along another elliptical path at the angular speed ω_0 clockwise with the center at $([1/(\alpha+1)]\,V_{\rm dc},\ 0)$.

Thus, the trajectories under the UPWM and SVTM schemes can be obtained by combining the above four possible trajectories.

C. State Trajectories Under UPWM

Take the zero-crossing point changing from the positive half to the negative half line cycle (+ve to −ve) as an example. The

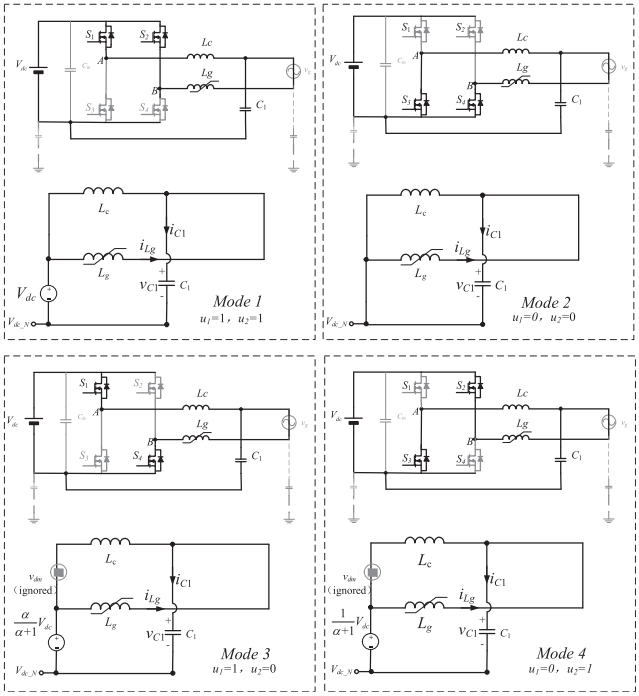

Fig. 7. Equivalent circuits of the four modes.

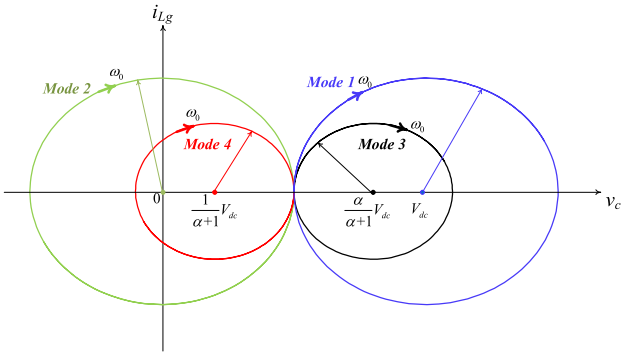

Fig. 8. Trajectories in Modes 1, 2, 3, and 4.

initial values of i_{C1} and v_{C1} are both zero. As shown in Fig. 6(a) S_2 is constantly ON with S_1 and S_3 switched at HF after the zero-crossing point. The inverter goes through Modes 1 and 4 repeatedly. Fig. 9 shows the trajectory of 10 switching cycles after the zero crossing.

As the duration of Mode 4 is much shorter than Mode 1, the peak value of i_{Lg}, $\hat{I}_{Lg,\,\mathrm{UPWM}}$, can be approximated by

$$\hat{I}_{Lg,\,\mathrm{UPWM}} = \frac{\omega_0\, C_1}{\alpha+1}\, V_{\mathrm{dc}}. \tag{24}$$

Thus, i_{Lg} exhibits oscillation with the natural resonance frequency of LCL filter, f_0

$$f_0 = \frac{1}{2\,\pi}\sqrt{\frac{L_c+L_g}{L_c L_g C_1}}. \tag{25}$$

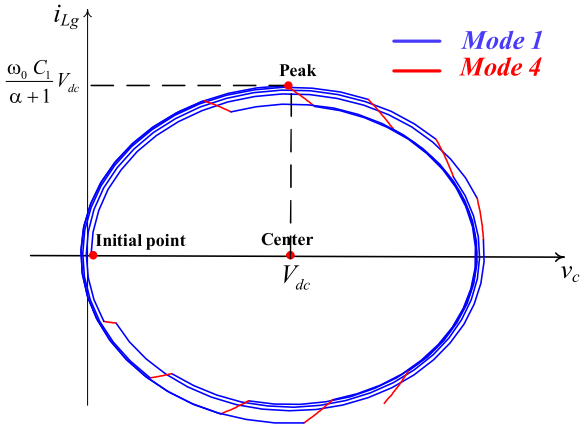

Fig. 9. Trajectories of UPWM in ZCR.

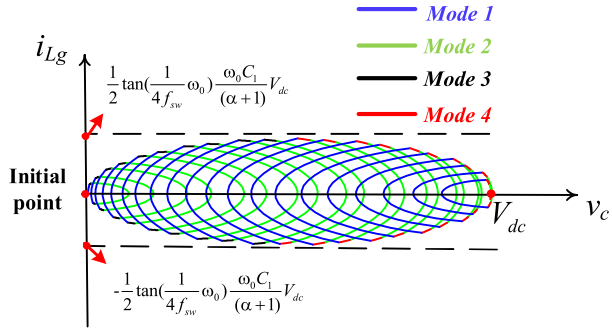

Fig. 10. Trajectories of SVTM in ZCR.

If the filter does not have damping resistor, the grid current will exhibit the above filter oscillation. Hence, the VG technique is unsuitable for inverters operating with UPWM.

D. State Trajectories Under SVTM

Under the SVTM scheme, the inverter will change between the combinations of Modes 1, 2, and 3 in the ZCR of the positive line cycle and Modes 1, 2, and 4 in the ZCR of the negative line cycle. Fig. 10 shows the trajectories changing from the positive to negative half cycle.

The peak value of the HF ripple in i_{Lg}, $\hat{I}_{Lg,\,\mathrm{SVTM}}$, can be shown to be

$$\hat{I}_{Lg,\,\mathrm{SVTM}} \approx \frac{1}{2}\tan\left(\frac{1}{4f_{\mathrm{sw}}}\omega_0\right)\frac{\omega_0 C_1}{(\alpha+1)}V_{\mathrm{dc}}. \tag{26}$$

By comparing (26) with (24),

$$\frac{\hat{I}_{Lg,\mathrm{SVTM}}}{\hat{I}_{Lg,\mathrm{UPWM}}} = \frac{1}{2}\tan\left(\frac{1}{4f_{\mathrm{sw}}}\omega_0\right). \tag{27}$$

In general, f_o ranges from 3 to 6 kHz. If the switching frequency is 20 kHz, the peak value of i_{Lg} can be reduced by $8 \sim 10$ times. Further reduction can be achieved with a higher switching frequency.

As illustrated in Fig. 6, the proposed SVTM reduces the rate of rise of v_{cm} by extending the duration of the ZCR in Fig. 2 in order to reduce the low-frequency current ripple in i_{Lg}. Let λ be the ratio between the duration of the soft-voltage transition

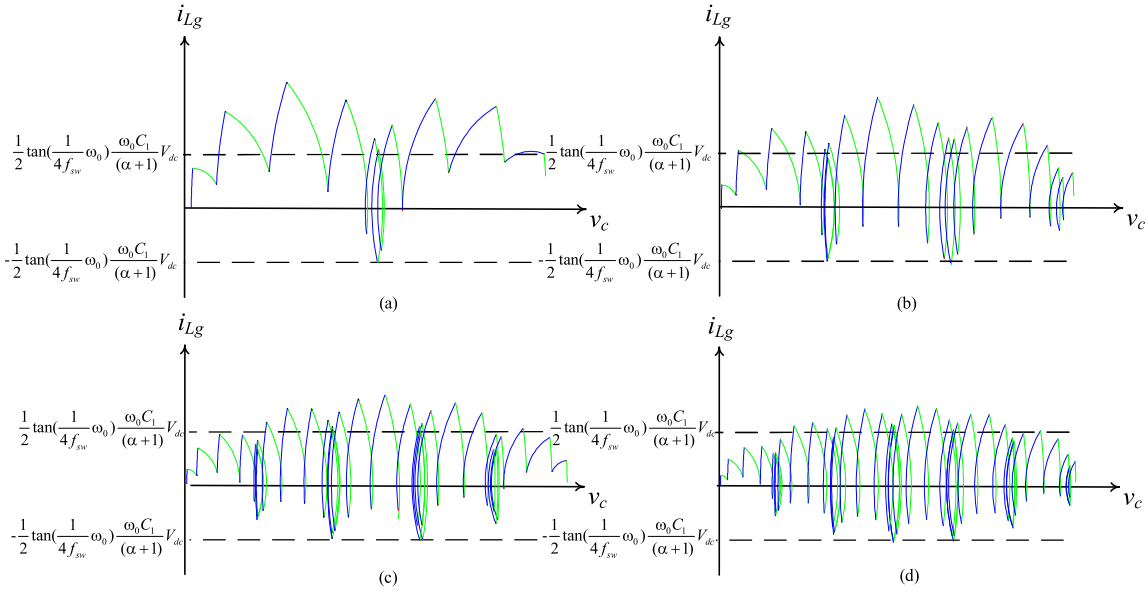

Fig. 11. Trajectories with different values of λ.

TABLE II
COMPONENT VALUES USED IN THE ANALYSIS

Component	Value	Component	Value
C_1	4.7 μF	L_g	6.72 mH
L_c	600 μH	T_0	326.22 μs
T_{sw}	50 μs	ω_0	19653.79 rad/s

period, $T_{\rm SVT}$, and T_0. It is defined as

$$\lambda = \frac{T_{\rm SVT}}{T_0} = \frac{N_{\rm sw}\ T_{\rm sw}}{T_0}. \tag{28}$$

Fig. 11 shows the trajectories when $\lambda = 0.76636$ ($N_{\rm sw}$= 10), $\lambda = 3.06546$ ($N_{\rm sw} = 20$), $\lambda = 4.5982$ ($N_{\rm sw} = 30$), and $\lambda = 6.1309$ ($N_{\rm sw} = 40$), respectively. The values of the filter components are tabulated in Table II. It can be seen from Fig. 11 that, when $\lambda = 0.766$, the envelop of the trajectories is nonelliptical. As λ increases to 4.5, the envelop becomes elliptical, giving less current harmonics. However, the duration $T_{\rm SVT}$ is limited by the maximum duty cycle of S_1 and S_3 when $d_a = 0.5$. Thus, the maximum value of $T_{\rm SVT}$, $T_{\rm SVT,max}$, is

$$\frac{V_m}{V_{\rm tri}}\ \sin\ \omega_g\,(\frac{T_{\rm SVT,max}}{2}) = 0.5$$

$$T_{\rm SVT,max} = \frac{2}{\omega_g}\ \sin^{-1}\ \frac{V_{\rm tri}}{2\ V_m}. \tag{29}$$

Thus, (29) gives the limit of the duration of the SVT.

V. EFFECTS OF NONLINEAR OUTPUT INDUCTOR

Based on (26), the output ripple current can be reduced by increasing the value of α, that is, with a larger value of L_g. In order to maintain the ratio of the ripple current to the cycle average current small, the value of L_g should be large in low-current current operation (i.e., ZCR) and can be small in high-current operation (i.e., NZCR). Hence, a nonlinear inductor that meets the abovementioned requirement is used. The volume of the inductor can be made smaller with nonlinear inductor, as compared with a fixed value inductor. This can optimize the size, weight, and cost of L_g.

A. Magnetic Cores With Distributed Airgaps Versus Concentrated Airgaps

The nonlinear inductor can be fabricated by the powder core with distributed airgaps or the magnetic core with concentrated airgaps, such as the gapped MnZn ferrite core. These two kinds of cores are compared as follows.

1) Power Loss: Concentrated airgaps generate fringing flux, while powder cores are manufactured with very fine particles and the airgaps are distributed and fringing flux can be highly eliminated [14]. The additional power loss caused by fringing flux of the inductor involves winding loss and core loss. The winding loss increases because the leakage magnetic flux crosses windings and voltage is induced within conducting material. Therefore, the eddy current generated by the induced voltage reduce the effective cross-sectional area of conductor for the current flow, thereby increasing the effective resistance [24], [25]. The core loss is also caused by the fringing flux because the fringing flux strikes the core, perpendicular to the laminations, and sets up eddy currents in cores [23].

Ungapped ferrite cores have a lower power loss density than powder cores. However, if a ferrite core is gapped to prevent from saturation, its power loss density will significantly increase [14]. The overall loss of inductors is thus dependent on many intrinsic and extrinsic factors, such as core shapes and materials, gap length, fabrication, operating environment, etc. [23].

2) Soft-Saturation Property: For toroidal powder cores, magnetic saturation occurs from the inner magnetic path to the outer magnetic path as the inductor current increases [14]. The inductance will also drop. Fig. 12 shows the dc superposition

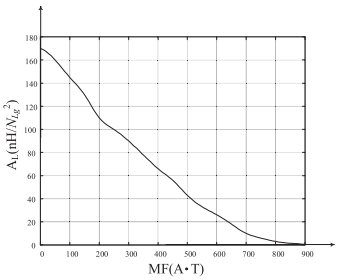

Fig. 12. Typical dc bias performance of a toroid powder core [17].

characteristic of a typical toroidal powder core [17]. N_{Lg} is the total number of turns of the coil in L_g. The inductance coefficient,$\mathrm{A_L}$, is the self-inductance generated in per squared turns of winding with the core structure. $\mathrm{A_L}$ gradually drops with the increase in the magnetomotive force (Ampere-Turn). Although the inner path saturation occurs at low inductor current, the saturation flux density for the outer path is high. L_g can be designed to maintain necessary inductance, even if the inductor current is very high.

For inductors that use high permeability magnetic cores with concentrated airgaps, when the maximum flux density exceeds the core saturation limit determined by the core material, the inductance will drop rapidly [14]. The nonlinear inductor in the proposed inverter should avoid changing abruptly to reduce low-order harmonics. This point will be further discussed in Section V-B.

3) Simple Design and Fabrication: As the dc bias curve of the powder cores can be obtained from manufacturers, the number of turns of the coil can be designed easily by considering necessary relationship between the inductance and inductor current. Conversely, the process of designing a nonlinear inductor with a gapped magnetic core is relatively complicated because the properties of gapped magnetic cores are sensitive to the gap width and coil arrangement.

Based on considering 2) and 3) above, powder core is chosen for L_g.

B. Fabrication of Nonlinear Inductor With Powder Cores

The inductances at the peak current and zero current, that is, $L_{g,\min}$ and $L_{g\_\max}$, respectively, are considered in the design of L_g. As discussed in [14], the permeability is quite constant if the operating frequency is far below the self-resonate frequency (SRF) with the parasitic capacitance taken into account. The SRF of the nonlinear inductor is usually around 1 MHz. Therefore, for a given value of N_{Lg}, the relationships between the value of L_g and the dc current through L_g, I_{Lg}, can be derived by the dc superposition characteristic (Fig. 12) as follows without considering the variation of the switching frequency:

$$L_g = \mathrm{A_L}\, {N_{Lg}}^2 \tag{30}$$

$$I_{Lg} = \frac{\mathrm{MF}}{N_{Lg}}. \tag{31}$$

Based on Fig. 12, Fig. 13 shows the characteristics between L_g and I_{Lg} under different values of N_{Lg}. The solid lines show the value of L_g with single powder core [Fig. 14(a)] and

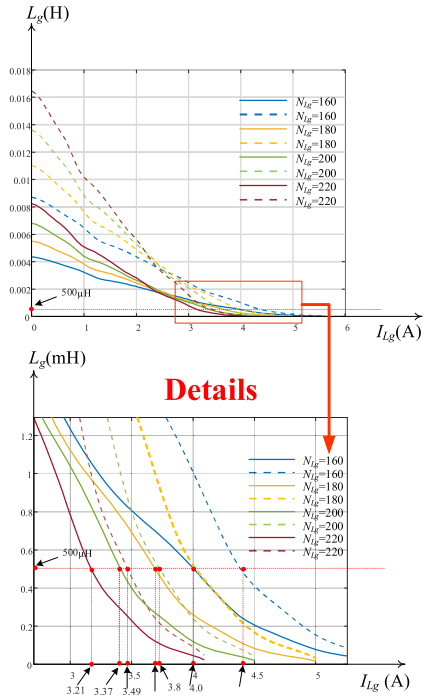

Fig. 13. Inductance value of L_{g} depending on the inductor current.

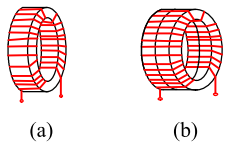

Fig. 14. Fabrication arrangements for the nonlinear inductor. (a) With single core. (b) With dual cores.

dotted lines show the value of L_g with two stacked powder cores [Fig. 14(b)]. It can be observed that the inductance value decreases faster with a larger N_{Lg}. $L_{g\_\max}$ can be increased by increasing N_{Lg}. $L_{g,\min}$ can be ensured by using multiple power cores. By adjusting N_{Lg} and the number of stacked cores, the desired performance of L_g can be realized.

Fig. 15(a) shows two inductors fabricated by the same type of powder core with different number of N_{Lg} and different number of stacked cores. The size of nonlinear inductor is almost the same as a fixed-value inductor with the inductance of$L_{g_\min}$. Fig. 15(b) shows their calculated and measured inductances versus their current. They have the same value of $L_{g\_\max}$, which is equal to 6.72 mH. The maximum inductor current is 5 A. The first inductor L_a has $N_{Lg} = 141$ and is fabricated with two stacked cores. The value of $L_{g,\min}$ of L_a is 1.6 mH. The second inductor L_b has $N_{Lg} = 200$ and is fabricated with single core. The value of $L_{g,\min}$ of L_a is 0.8 mH.

C. Analysis of the Nonlinear Effect

In Fig. 13, the effective value of L_g, L_{eff}, is approximated by a linear relationship with its current

$$L_{\mathrm{eff}} \approx L_{g,\max} - k_0\ |i_{Lg}| \tag{32}$$

where k_0 is the rate of change of inductance with current.

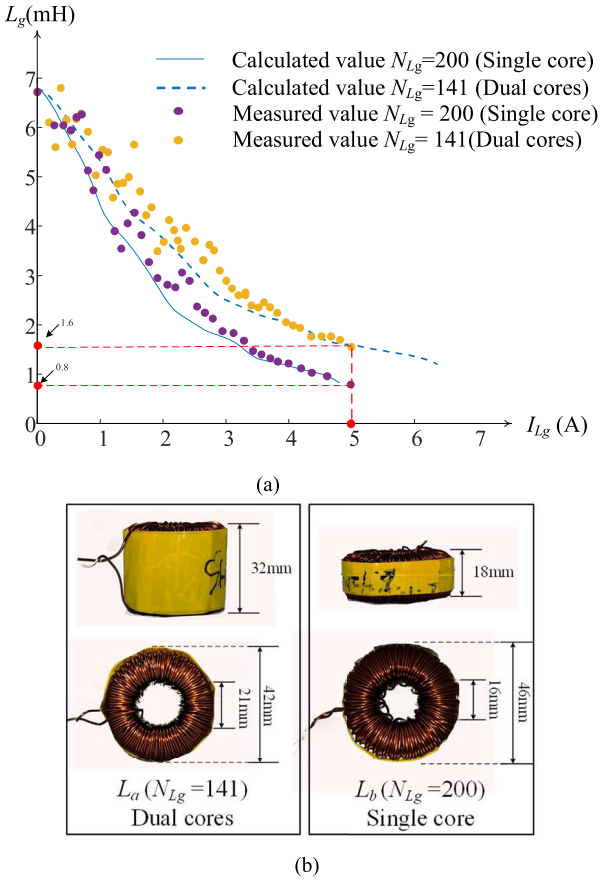

Fig. 15. Inductances and photos of two fabricated nonlinear inductors. (a) Calculated and measured inductance. (b) Photos.

The flux linkage φ is expressed as nonlinear relationships with the inductance and current as

$$\varphi(t) = L_1\, i_{Lg}(t) + L_2\, {i_{Lg}}^2(t) \tag{33}$$

where

$L_1 = L_{g,\max}$ and $L_2 = -k_0$, when $i_{Lg}(t) \geq 0$;
$L_1 = L_{g,\max}$ and $L_2 = k_0$, when $i_{Lg}(t) < 0$.

Distortion of the inductor current is studied by using the Volterra theory [13]. φ is expressed as a truncated series of linear and nonlinear responses of the inductor

$$\varphi(t) \approx \sum_{i=1}^{5} \varphi_i(t) \tag{34}$$

where

$$\begin{cases} \varphi_1(t) = L_1\, i_1(t) \\ \varphi_2(t) = L_2\, {i_1}^2(t) \\ \varphi_3(t) = 2\, L_2\, i_1(t)\, i_2(t) \\ \varphi_4(t) = 2\, L_2\, i_1(t)\, i_3(t) + L_2\, {i_2}^3(t) \\ \varphi_5(t) = 2\, L_2\, i_1(t)\, i_4(t). \end{cases} \tag{35}$$

As explained in [13], $i_i(t)$ in (36) can be considered as external disturbances. Each one can be expressed as

$$\begin{cases} i_1(t) = \frac{\int V_L dt}{L_1} \\ i_2(t) = \frac{L_2}{L_1} {i_1}^2(t) \\ i_3(t) = 2\frac{{L_2}^2}{{L_1}^2} {i_1}^3(t) \\ i_4(t) = 5\frac{{L_2}^3}{{L_1}^3} {i_1}^4(t) \\ i_5(t) = 10\frac{{L_2}^4}{{L_1}^4} {i_1}^5(t). \end{cases} \tag{36}$$

i_{Lg} can be written as

$$i_{Lg}(t) \approx\ i_1(t) + i_d(t) \tag{37}$$

where $i_d(t) = \sum_{i=2}^{5} i_i(t)$ is the component introduced by the nonlinear properties of the inductor.

By conducting Fourier transformation of i_d

$$\mathcal{F}[i_d(t)] = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \sum_{i=2}^{5} i_i(t)\, e^{jn\omega_g t} d(\omega_g\, t) + \frac{1}{\pi} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \sum_{i=2}^{5} i_i(t)\, e^{n\omega_g t} d(\omega_g\, t) \tag{38}$$

with $i_1(t) = I_1\ \cos\ \omega_g\, t$ in (36).

Based on (33), $L_2 = k_0$ in the first term of (38), while $L_2 = -k_0$ in the second term of (38). Therefore,

$$\mathcal{F}[i_2(t)] = \mathcal{F}[i_4(t)] = 0\ . \tag{39}$$

Thus, the disturbances in (36) only have effects when *i* is an odd number. It should be noted that the expression of the power *n* of the cosine terms in (36) is

$$\cos^n(\omega_g t) = \frac{1}{2^n} \sum_{m=0}^{n} C_n^m \cos[(n-2m)\, \omega_g t]. \tag{40}$$

Based on (36), (38), and (40), the nonlinear properties of $L_g$introduces low-order odd current harmonics. If a 50 Hz sinusoidal voltage is applied to the output filter, fundamental component and third- and fifth-order harmonics will result [13]. In other words, the frequency characteristic of the LCL filter varies with the grid frequency. Hence, a PR controller, as shown in Fig. 1, is used as it can perform the output current regulation at the predefined grid frequency, so as to achieve low current harmonics. However, if k_0 in (32) is large, L_g will change abruptly with a small change of its current. Based on (33) and (36), this will introduce more low-order harmonics and the PR controller may not be able to significantly eliminate low-order harmonics, leading to high current total harmonic distortion (THDi). That is why soft saturation is preferred.

VI. Simplified Design Guideline

The values of L_c, C_1, and L_g are designed by considering the following design criteria and parameters:

$\Delta I_{\rm lim}$	Maximum allowable ripple current in L_c;
$\rm V_{dc}$	Input dc voltage;
f_{sw}	Switching frequency of the FB;
$C_{\rm lk,max}$	Maximum ground leakage capacitance;
$f_{o,\rm center}$	Center resonant frequency of the filter;

$f_{o,\min}$ Minimum filter resonant frequency;
$f_{o,\max}$ Maximum filter resonant frequenc y.

Step 1: Design of L_c

Based on (8), ΔI_{Lc} is maximum when $M_r = 0.5$. Thus

$$L_c \geq \frac{V_{\rm dc}}{4\, f_{\rm sw}\, \Delta I_{\rm lim}}. \tag{41}$$

Step 2: Design of C_1

Since the function of C_1 is used to share major ripple current generated by the FB, the value of C_1 is designed to be no less than 10 times the value of $C_{\rm lk,max}$.

Step 3: Design of L_g

L_g is designed by considering the resonant frequency of the LCL filter equivalence, f_o. After the values of C_1 and L_c are chosen, the variation range of the value of L_g is determined by the relationships between C_1 and L_g that give respective f_o. The range of f_o should be chosen by considering the following factors:

1) f_o should be chosen in a range insensitive to L_g.
2) In order to ensure smooth transition of v_{C1} in ZCRs, λ should be larger than 4.5, with $T_o = \frac{1}{f_{o\min}}$ in (28).
3) In order to assure the control stability, active damping should be used if the range of f_o covers one-sixth of the switching frequency, $f_{\rm sw}$, or below [27], [26].

$f_{o\min}$ and $f_{o\max}$ are designed after the range f_o is chosen. The filter resonant frequency will be maximum at the peak of the grid current. Thus, based on (25), the minimum value of L_g, $L_{g,\min}$, is

$$L_{g,\min} = \frac{L_c}{4\pi^2 {f_{o,\max}}^2\, L_c\, C_1 - 1}. \tag{42}$$

Based on (25), the maximum value of L_g, $L_{g,\max}$, is

$$L_{g,\max} = \frac{L_c}{4\pi^2 {f_{o,\min}}^2\, L_c\, C_1 - 1}. \tag{43}$$

For illustration, Fig. 16 shows the relationships between C_1 and L_g that give respective resonant frequency when L_c= 600 μH, C_1= 4.7 μF, and $f_{\rm sw}$= 20 kHz. The following three points can be noted.

1) In order to avoid f_o entering the region on the left-hand side of the black dotted line, $f_{o,\rm center}$ is chosen to be $f_{\rm sw}$/6, 3.3 kHz, and the resonant frequency varies between ±10% of the center resonant frequency. The operating range is represented by the red solid line with $f_{o\_\min} = 3$ kHz, $f_{o\_\max} = 3.5$ kHz.
2) With $N_{\rm sw} = 40$, λ = 6. The proposed inverter can make a smooth transition of v_{C1} in ZCRs.
3) Active damping needs to be applied.

Thus, if the grid current varies from zero to 5A, $L_{g,\min}$= 1.6 mH at 5 A and $L_{g,\max}$= 6.72 mH at 0 A. Based on the calculated values of $L_{g,\min}$ and $L_{g,\max}$, the magnetic core and the number of turns of the coil are obtained by adjusting N_{Lg} and the number of magnetic cores, as analyzed in Section V.

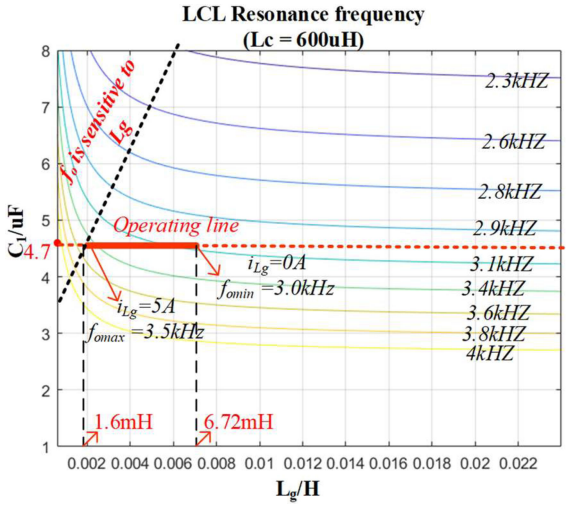

Fig. 16. Relationships between C_1 and L_g.

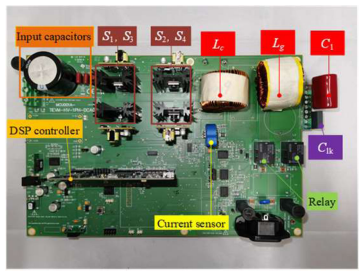

Fig. 17. Photograph of the proposed inverter prototype.

TABLE III
COMPONENT VALUES

Component	Value / Part No.	Component	Value / Part no.
S_1,S_3	SCT2120AFC	S_2,S_4	IGP20N65H5
C_{in}	470μF	$L_{g,\max}$	6.72mH
C_1	4.7μF	$L_{g,\min}$	1.6 mH
L_c	600μH	N_{Lg}	200 turns
Core of L_g	MAGNETICS, 0077254A7, dual stacked cores		

VII. EXPERIMENTAL VERIFICATION

A 340 W, 380 V dc/110 V ac, 50 Hz, prototype has been built and evaluated. Fig. 17 shows the photograph of the prototype. Table III shows the part number or value of the key components in Fig. 1. S_1 and S_3 are SiC MOSFETs and S_2 and S_4 are IGBTs. For cost considerations, different types of switching devices are used. As S_2 and S_4 are switched at HF around ZCR only and their current stress is much lower than that of S_1 and S_3 (because $L_g >> L_c$), IGBTs are used.

The average current mode control is implemented on a Texas Instruments TMS320F28379D. In this prototype, a notch-filter-based damping technique is used because the resonant frequency of LCL equivalence can be reduced to below $f_{\rm sw}/6$ [27]. The switching frequency is 20

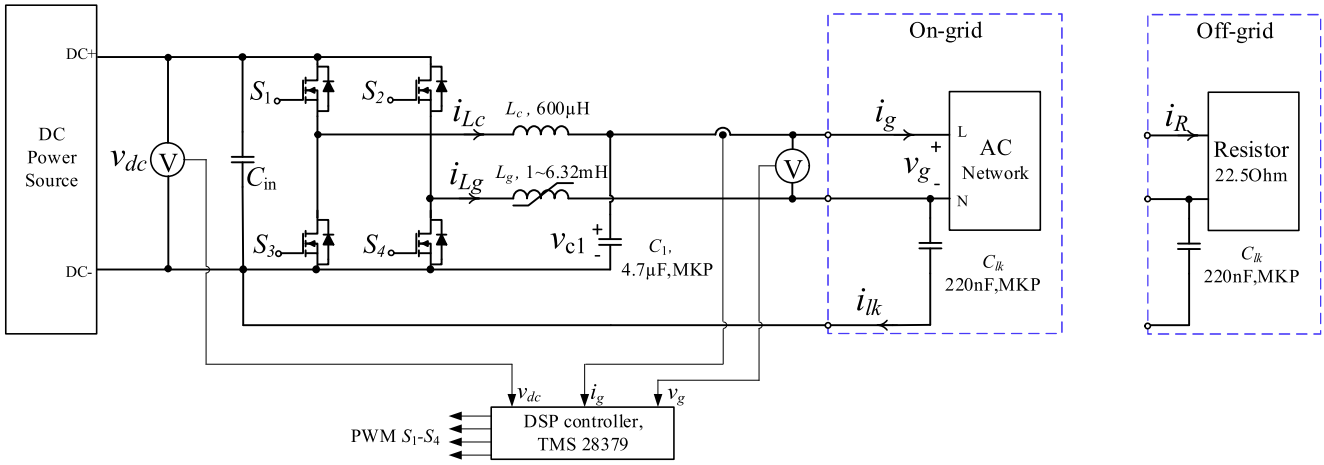

Fig. 18. Circuit diagram of the on-grid and off-grid experiment setup.

kHz. Fig. 18 shows the setup for testing the prototype. The ground leakage capacitance is emulated by connecting a 220 nF capacitor between the neutral terminal of the grid and the negative terminal of the dc source.

In order to illustrate the effectiveness of the proposed HPWM on eliminating oscillation caused by the abrupt change of the CM voltage in UPWM, a comparative study of HPWM and UPWM on the output to a resistive load in off-grid operation is first given. Then, the performance of the inverter in on-grid operation is provided.

A. Off-Grid Operation

For the sake of safety, the supply voltage is reduced to 60 V dc because the capacitor voltage could resonate up to a very large value. The output of the inverter is connected to a 22.5-Ω resistor bank and the inverter is in open-loop operation.

Fig. 19(a) shows the signals to S_3 and S_4, load current i_R, and the voltage across C_1, v_{C1}, when UPWM is applied. The peak value of v_{C1} is 120 V, which is twice the supply voltage, consistent with the predicted value in Fig. 9. The peak current through C_1 in the first resonance cycle is found to be 500 mA, which is also in close agreement with the value obtained by (24). i_R consists of current oscillation around zero crossings. Due to the damping effect of the resistive load, the amplitude of the oscillation attenuates in the subsequent cycles. More importantly, the current stress on S_1 and S_3 is 10 times larger the amplitude of the oscillating current in i_R. This can be explained by the equivalent circuit model in ZCRs (Section IV). The oscillation is caused by the abrupt change of $v_{\rm cm}$. As L_g is connected in parallel with L_c, the relationship between i_{Lg} and i_{Lc} can be derived from (16) that

$$|i_R| \approx |i_{Lg}| = \alpha\,|i_{Lc}|\,. \tag{44}$$

Fig. 19(b) shows the waveforms with HPWM. With $N_{\rm sw} = 40$, v_{C1} has SVTM around zero crossings. Both v_{C1} and i_R do not have oscillations, confirming the merits of the SVTM.

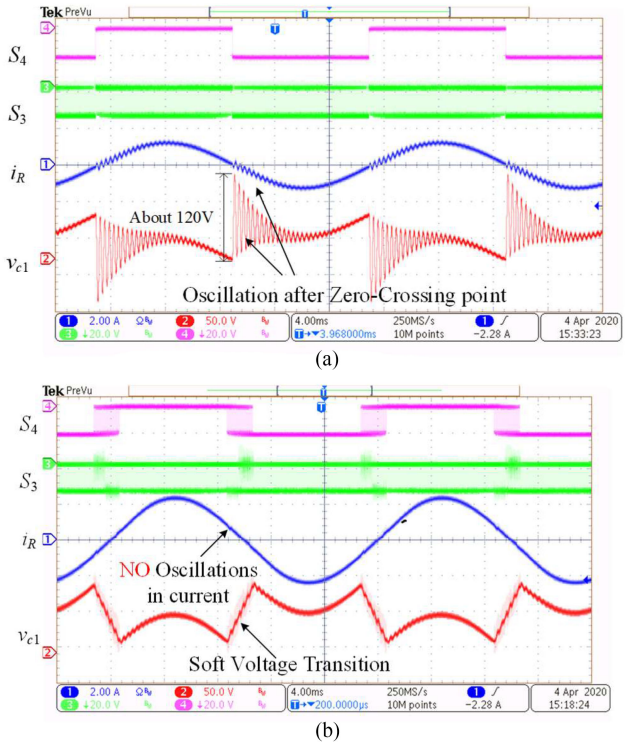

Fig. 19. Off-grid operation with UPWM and HPWM (Time base: 4 ms/div). (a) UPWM. (S_4: 20 V/div, S_3: 20 V/div, i_R: 2 A/div, v_{C1}: 50 V/div). (b) HPWM. (S_4: 20 V/div, S_3: 20 V/div, i_R: 2 A/div, v_{C1}: 50 V/div).

B. On-Grid Operation

With $N_{\rm sw} = 40$, Fig. 20(a)–(c) shows the steady-state waveforms when the output power is 140, 230, and 340 W, respectively. The measured leakage ground currents at the three output power levels are 98, 100, and 105 mA, respectively. The results are comparable with that reported in [10]. The differential mode (DM) current ripple is less than 0.5 A, which is comparable with that using the AVG technology in [10] and less than the CCT technology in [9]. In NZCRs, L_c acts as a converter-side

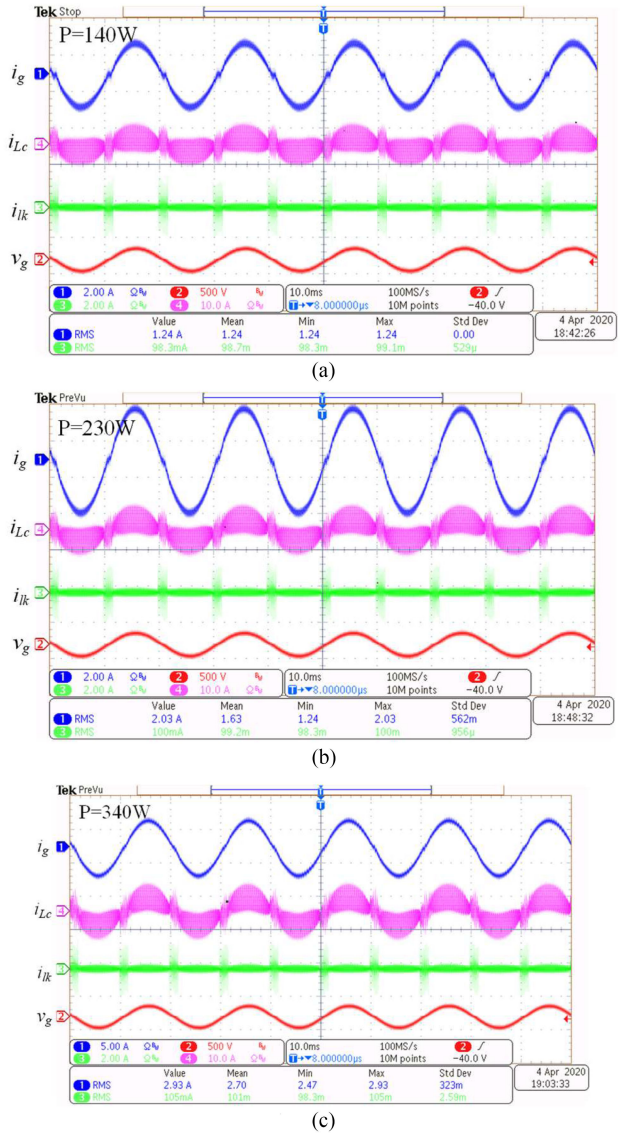

Fig. 20. Measured waveforms at different output powers (Time base: 10 ms/div). (a) Output power = 140 W (i_g: 2 A/div, i_{Lc}: 10 A/div, $i_{\rm lk}$: 2 A/div, v_g: 500 V/div). (b) Output power = 230 W (i_g: 2 A/div, i_{Lc}: 10 A/div, $i_{\rm lk}$: 2 A/div, v_g: 500 V/div). (c) Output power = 340 W (i_g: 5 A/div, i_{Lc}: 10 A/div, $i_{\rm lk}$: 2 A/div, v_g: 500 V/div).

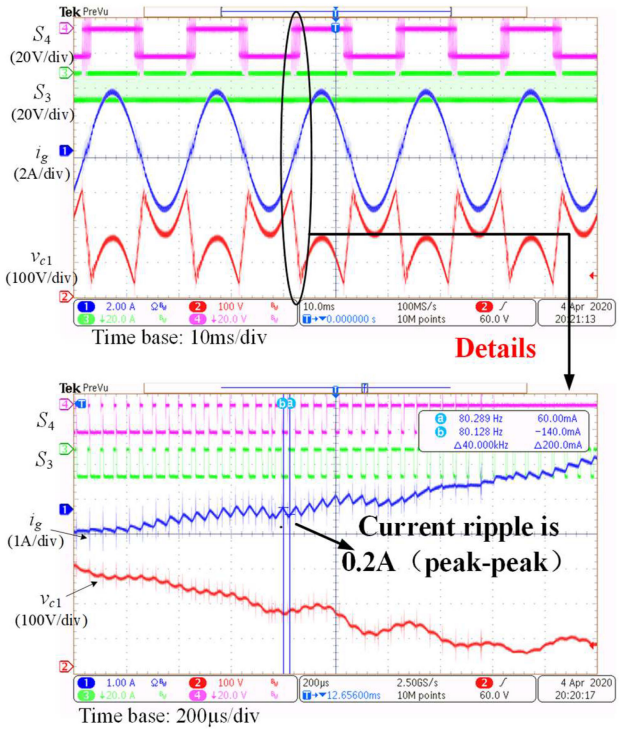

Fig. 21. Measured waveforms in ZCR.

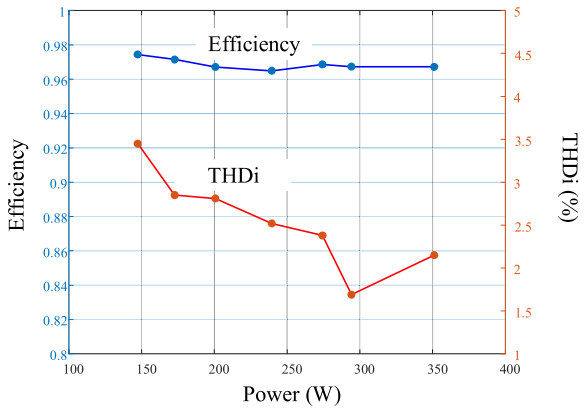

Fig. 22. Measured efficiency and THDi.

inductor which has larger current ripples while L_g acts like a grid-side inductor with smaller current ripples.

In ZCRs, the inductance of L_g is near $L_{g,\max}$. Based on (44), the current ripple in L_c is about 10 times the current ripple in L_g. Thus, the nonlinear inductor can provide large inductance in ZCRs to mitigate the current ripple in i_{Lg} as well asi_g.

Fig. 21 shows the measured waveforms over five line cycles and their details around the ZCR. Based on (28), $\lambda = 4.5$. All waveforms transit smoothly around the ZCR without abrupt changes or severe oscillation. The DM component of i_g is not affected by the introduced SVTM scheme, confirming the modulation technique given in Section IV. The maximum peak-to-peak value of the current ripple in i_g is found to be 200 mA.

Fig. 22 shows the measured efficiency and the THDi of i_g. The measured efficiency is around 97% over the operating range. Majority of the power loss is the switching loss of the FB. The THDi is below 3.5% over the operating range. The power loss can further be reduced if S_2 and S_4 are replaced by SiC MOSFETs.

Fig. 20(b) shows the leakage current waveform of the proposed inverter (green color) at 230 W. Fig. 23 shows the leakage current waveform around ZCR. The rms value of the leakage current is 100 mA, while the rms value of the leakage current over the ZCR is found to be 83.8 mA. As the duration of the soft voltage transition lasts one-fifth of the line cycle, the rms value of the leakage current over the NZCR is 103.7 mA. The difference of the rms value of the leakage between NZCR and ZCR is (103.7–83.8) mA = 19.9 mA, which can meet the requirements

TABLE IV
PERFORMANCE COMPARISON WITH THE AVG INVERTER IN [10]

	Power range	100W - 200W	200W - 300W	300W - 400W
THDi	AVG inverter in [10]	9% - 23%	8% - 10%	6% - 9%
	Proposed inverter	2.8% - 3.5%	1.7% - 2.7%	1.6% - 2.2%

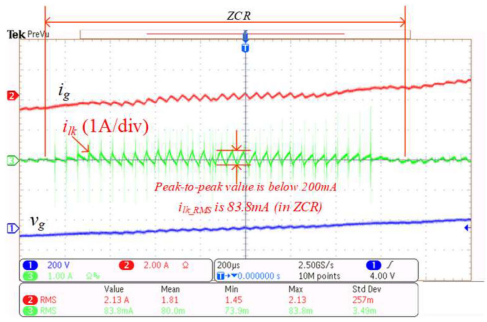

Fig. 23. Measured leakage current waveforms in ZCR at 230 W (Time base: 200 μs/div).

of some standards, such as DIN VDE V 0216-1-1 [21], [22]. First, the rms value of the leakage current is less than 300 mA and the change of the leakage current is less than 30 mA.

C. Comparison With Existing Technologies

1) Comparison With [10]: The output filter parameter and the switching frequency are similar between the setup of the AVG inverter in [10] and the proposed inverter prototype. The measured ground leakage current is similar. Although the maximum value of the nonlinear inductor is 6.72 mH, the physical size of the inductor used in the proposed inverter is equivalent to that used in [10]. However, the AVG inverter requires two additional switching devices on the output side. As the two-phase legs are switched at HF alternately, symmetrical inductors are needed. A comparison of the THDi between the AVG inverter in [10] and the proposed inverter operating at three power ranges is given Table IV.

2) Comparison With [11]: The circuit structure given in [11] is a typical FB inverter with symmetrical output filter. With two converter-side inductors of 2 mH each and a VG capacitor of 5 μF, the measured ground leakage current is 15 mA. The testing environment is slightly different from others. Apart from a smaller parasitic capacitance of 100 nF, a ground resistor of 10 Ω is introduced. As two bridge legs are switched at HF, the symmetrical LCL output filter requires six reactive elements. Compared with [11], the proposed inverter has a fewer number of output filter elements and its physical size is smaller. If the value of L_c in the proposed inverter is changed into 2 mH and the tested parasitic capacitance is changed into 100 nF (without the ground resistor), the rms value of the ground leakage current can be significantly reduced to 20 mA, giving a comparable leakage current as in [11].

3) Comparison With [12]: As stated in [12], the voltage on the stray PV capacitor is clamped to zero by adding a VG capacitor. This can reduce the common mode current to a low level. In addition, by using a switched-capacitor circuit to create a negative voltage level on the dc bus, UPWM scheme can be applied and unsymmetrical output filter is allowed. However, apart from increasing the number of switches, extra current stress is also reported, making it more suitable for low-power applications. Both inverters give similar level of THDi.

4) Comparison With [9]: The structure in [9] is a typical FB inverter with a VG formed by the center-tapped capacitors on the dc and ac sides. It has been compared in [10] theoretically and experimentally. As discussed in [10], with the same output filter, the inverter proposed in [9] has a higher DM ripple current than the AVG inverter in [10]. If the total value of the inductance in the proposed inverter is changed into 7.5 mH and the tested parasitic capacitance is changed into 10 nF, the simulated rms value of the ground leakage current can be significantly reduced to 1.2 mA, giving a comparable leakage current as in [9].

VIII. CONCLUSION

A single-phase transformerless FB PV grid-tie inverter has been presented. Its architecture has the following features:

1) *Simple Power Conversion Stage:* The entire circuit consists of an FB only without additional switching elements. The output filter consists of two inverter-side inductors and one VG capacitor only. It is simpler than the prior art with two symmetrical output filters.
2) *Use of UPWM Scheme With Passive VG Technique:* Typically, BPWM and DUPWM schemes are applied in inverters with VG technique. With the proposed SVTM scheme introduced in the zero crossings, UPWM can be applied and abrupt change of the low-frequency CM voltage around zero crossings can be eliminated. It exhibits low switching losses.
3) *Use of Nonlinear Inductor:* In order to maintain the ratio of the ripple current to the cycle average current, the value of the filter inductor should be large around zero crossings and can be small elsewhere. A nonlinear inductor is used so that the size and weight of the filter inductor can be reduced. Most previous work focused on preventing magnetic saturation of filter inductors [13]. In this article, the magnetic saturation of the filter inductor is used to mitigate current ripple in the predetermined operating region and reduce inductor size and loss.

Detailed analysis of the HPWM scheme and harmonic analysis of the output current due to the nonlinear inductor have been discussed. The proposed technology has been confirmed by applying it to a 340-W prototype.

Since the switching network is a typical FB, its soft-switching characteristics are expected to be the same as the typical FB structure and depend on the phase between the current and

voltage. Soft switching occurs when the equivalent current on the ac side is inductive. However, as there are two modulation schemes hybridized in driving the switches, further research is required to study the soft-switching properties over the line cycle.

Finally, further research will also be dedicated to studying the impact of the grid impedance on the performance of the inverter.

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