Interleaved Totem-Pole ZVS Converter Operating in CCM for Single-Stage Bidirectional AC–DC Conversion With High-Frequency Isolation

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***Abstract*—In this article, a new bidirectional single-stage interleaved totem-pole electrolytic capacitorless ac–dc converter with high-frequency isolation and low components count is proposed. The proposed converter is constructed using nonregulating two-phase interleaved totem-pole converter switched with a fixed 50% duty on the grid side and a full-bridge on the dc-side for active power and dc output regulation. This switching method results in a ripple-free grid current regardless of the magnitude of the input inductances. Consequently, a proper design of input inductance secures soft switching for all switches under wide voltage and load ranges without an auxiliary circuit or resonant tank. Hence, the proposed topology overcomes the reverse recovery issue, thereby enabling the use of Si devices in CCM. Moreover, the current spike around the ac main zero-crossing is avoided in the CCM operation due to small rectified voltage around zero-crossing. Furthermore, the instantaneous powers at the grid side and dc-side are identical since the proposed topology is electrolytic capacitorless with inherent second harmonic ripple current at the dc-side. PFC is inherently performed in the proposed converter without a current shaping control loop, and the phase-shift angle is the only control variable. Hence, the control system is simple and reliable. A 3.3 kW prototype of the proposed converter is built and tested in order to verify the performance and the theoretical claims.**

***Index Terms*—AC–DC converter, electrolytic capacitorless, high-frequency (HF) isolation, interleaved, single-stage, soft-switching, totem-pole bridgeless PFC.**

I. Introduction

AC–DC power converters with high-frequency (HF) isolation have been gaining special attention in recent years since they are widely used in many applications, including switch-mode power supplies [1], telecom power supplies [2], uninterrupted power supplies [3], energy storage systems, and EV battery chargers [4], [5]. Previous research on ac–dc power converter topologies aim at high power factor with good grid current quality, minimized EMI levels, high efficiency, reduced size of magnetics, and simple control [6]–[9].

The isolated ac–dc converter can be classified into two-stage and single-stage topologies. In the two-stage topology, an ac–dc conversion stage with a bulky dc-link capacitor is followed by an HF link dc–dc converter [10]–[12]. A wide voltage range and high power factor can be achieved using the two-stage structure. However, there are limitations in improving efficiency due to double power conversion and reducing cost due to high component count. Moreover, the dc-link electrolytic capacitor may reduce the system reliability because of its short lifetime in case of improper design or heat management failure. However, it is possible to control the internal temperature of electrolytic capacitors but at the expense of increased cost and size.

The single-stage ac–dc structure is an alternative solution to the two-stage since the power factor correction (PFC) circuit and isolated dc–dc converter are integrated to possibly achieve lower cost and higher efficiency [6]–[8], [13]–[30]. The downside of the single-stage ac–dc converter is inherent second harmonic ripple power since most of the topologies are electrolytic capacitorless. However, it was reported in [31] that low-frequency ripple currents do not have an obvious adverse effect on the efficiency and lifetime of the lithium-ion batteries. Several electrolytic capacitorless structures with sinusoidal charging have been proposed for the lithium-ion battery charger where low-frequency ripple is allowable at the output [6]–[8], [17], [20], [26]–[28].

Single-stage ac–dc converters with unfolding bridge have been proposed for different power levels [6], [13], [14], [18]–[20], [27], [29], [30]. The unfolding full-bridge rectifier converts a sinusoidal waveform into a double grid-frequency single-polarity dc voltage across a film capacitor. Then, the fluctuating dc voltage is converted into a pure dc-level within a specific range using isolated dc–dc converters such as isolated SEPIC [27], flyback or forward converters [13]. Due to their simple structures, these converters offer a cost-effective solution for low-power applications. However, they are not suitable for high power because of high voltage and current stresses on the switching devices as well as unidirectional core excitation.

Single-phase matrix-based ac–dc converters with HF isolation and zero-voltage switching (ZVS) were proposed in [16], [17], [22], and [23]. Despite the inherent bidirectional power flow capability provided by the converter, the use of back-to-back switches is a major challenge in the matrix converter since it increases the control complexity, conduction loss, and system cost [20]. A full-bridge based ac–dc topology or the so-called

Manuscript received December 9, 2019; revised April 30, 2020 and June 23, 2020; accepted July 30, 2020. Date of publication August 14, 2020; date of current version October 30, 2020. This work was supported by the National Research Foundation of Korea under Grant 2020R1A2C2006301 funded by the Korea government (MSIT). This paper was presented in part at the IEEE Energy Conversion Congress and Exposition, Portland OR, USA, 2018. Recommended for publication by Associate Editor A. Mertens. *(Corresponding author: Sewan Choi.)*

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Digital Object Identifier 10.1109/TPEL.2020.3016684

indirect matrix converter that avoids back-to-back switches is considered for high-power applications, such as high-voltage dc distribution systems and electric vehicles [18]–[20].

The indirect matrix ac–dc converter employing the conventional phase-shift modulation (PSM) exhibits soft-switching failure under wide voltage and load ranges since it achieves full-range ZVS only at a unity conversion ratio [32]. Therefore, improved modulation schemes with increased degrees of freedom are introduced to facilitate optimal ZVS operation of the dual active bridge (DAB) ac–dc converter [18]–[20]. The dual-phase shift (DPS) algorithm that adds an extra control parameter to accommodate the wide voltage range still loses the ZVS at light load [19], [20]. In [17], PSM and frequency modulation are combined to achieve ZVS over the whole ac mains voltage with minimum commutation current. Everts [19] further utilized the semiconductor switch output capacitance and charge to determine the ZVS boundary. In [20], primary DPS (PDPS) control and secondary DPS (SDPS) control were combined to maintain ZVS within the full voltage range and to realize a smooth transition between PDPS and SDPS. Despite various efforts of securing the ZVS through employing multiple phase shifts and frequency modulation, the aforementioned schemes are complicated to implement in practice, and the controllers are susceptible to instability because of the heavier calculations and numerous sensed parameters.

It is worthy to mention that the switching loss of the unfolding bridge is neglected in practice, but reducing the conduction loss by employing semiconductor devices with superior conduction characteristics increases the cost. Moreover, the unfolding bridge increases the weight and volume of the converter. Therefore, bridgeless ac–dc converters that eliminate the unfolding bridge are introduced. These topologies allow the current to flow through a minimum number of switching devices compared to the conventional PFC circuits. Accordingly, the converter conduction losses can be significantly reduced, and higher efficiency and lower cost can be obtained. In [25] and [26], a two-phase totem-pole configuration is integrated with the HF isolated dc–dc converter. The presented topology [26] was operated in continuous conduction mode (CCM) where a film capacitor is used to clamp voltage spikes caused by the leakage inductance of the transformer. Despite the improved efficiency with a simple control scheme, the topology suffers from limited ZVS range and current spikes at ac zero-crossing due to the large voltage across input inductors at ac main zero-crossing.

This article proposes a new bidirectional interleaved totem-pole converter for single-stage isolated ac–dc conversion. The converter has the following features.

1) Bridgeless totem-pole structure with reduced component count while providing interleaving effect for high-power applications.
2) Electrolytic capacitorless topology with HF isolation.
3) The two interleaving legs are switched with a fixed 50% duty to achieve full-range ZVS.
4) Ripple-free grid current regardless of the magnitude of the input inductances.
5) The reverse recovery of the body diodes of all switches is suppressed since ZVS turn-ON is achieved. Hence, the proposed topology can be operated in CCM to reduce conduction loss.
6) No zero-crossing current spike since the voltage across the clamping capacitor is equal to zero at ac main zero-crossing.

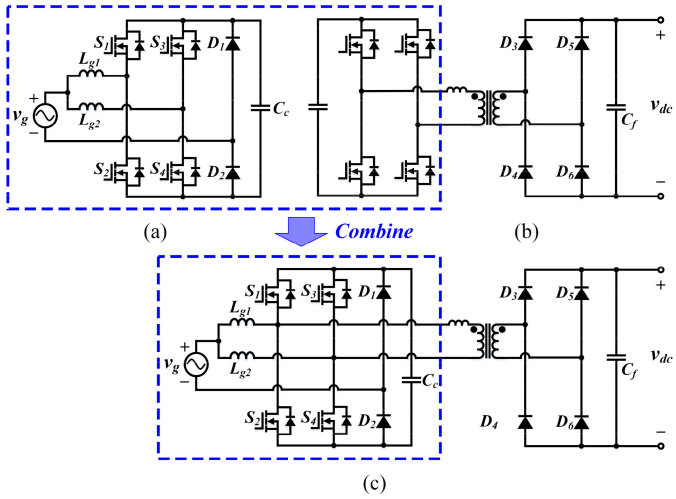


Fig. 1. Concept of topology derivation. (a) Nonisolated interleaved totem-pole ac–dc converter. (b) Isolated full-bridge dc–dc converter. (c) Unidirectional interleaved totem-pole isolated ac–dc converter [25], [26].

7) A simple phase controller is implemented to regulate the active power and dc voltage.

This article is organized as follows. Section II focuses on topology derivation and operating principles of the proposed ac–dc converter. The control strategy is discussed in detail in Section III. Section IV deals with the experimental implementation and the obtained experimental results of the proposed converter. Finally, Section V concludes this article.

II. Topology Derivation and Operating Principles of the Proposed Converter

A. Concept of Topology Derivation

This section provides a step-by-step explanation of the procedures to derive the proposed bidirectional single-stage isolated ac–dc converter. Fig. 2(a) shows the conventional nonisolated interleaved totem-pole ac–dc converter. During the positive (negative) half cycle of v_g, bottom shaded switches S_2 and S_4 (S_1 and S_3) that operate as boost switches cannot be turned ON with ZVS while top switches S_1 and S_3 (S_2 and S_4) that freewheel inductor currents are turned ON with ZVS. That is to say, ZVS turn-ON is achieved only for two switches at one instant. Integration of the nonisolated interleaved totem-pole ac–dc converter in Fig. 1(a) with an isolated full-bridge dc-dc converter in Fig. 1(b) gives the unidirectional interleaved ac–dc converter [26] shown in Fig. 1(c). This integration *partially* enables the ZVS for the bottom and the top switches during the grid positive and negative half-cycles, respectively. The partial ZVS is achieved using the energy stored in the leakage inductance of the HF transformer. A film capacitor is used to clamp voltage spikes caused by the leakage inductance of the transformer.

Fig. 2(a) and (b) shows the simplified equivalent circuits of the primary side of the unidirectional interleaved totem-pole ac–dc converter for the positive and negative half-cycles, respectively. Note that the equivalent primary-side circuit is nothing but *L*-type half-bridge converters with active clamping. The *L*-type half-bridge converters are modulated with asymmetric pulsewidth modulation (PWM) of a varying duty cycle for PFC, as plotted in Fig. 2(c). *An inherent issue* in the mentioned

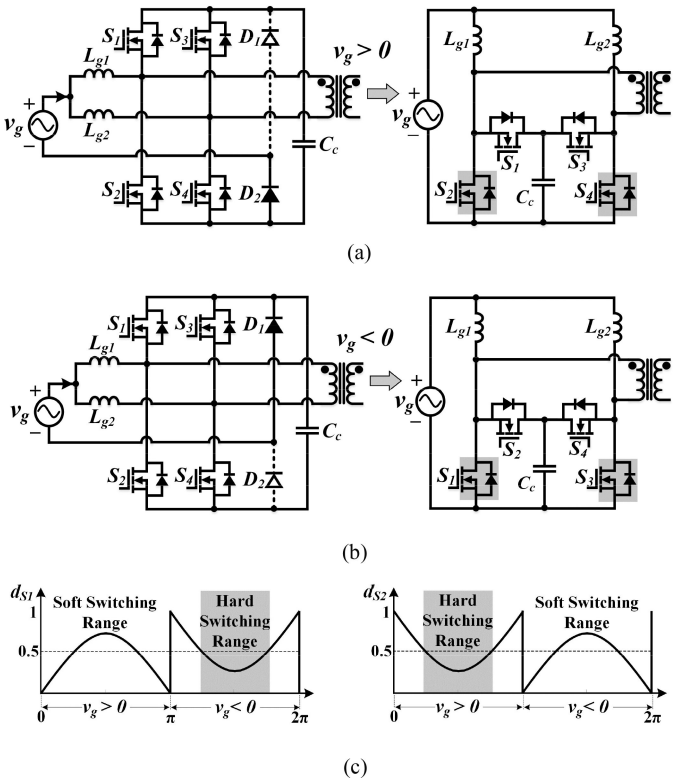


Fig. 2. Equivalent circuit of the unidirectional interleaved totem-pole isolated ac–dc converter. (a) Positive half-cycle. (b) Negative half-cycle. (c) Modulation of one commutation leg and its hard-switching range.

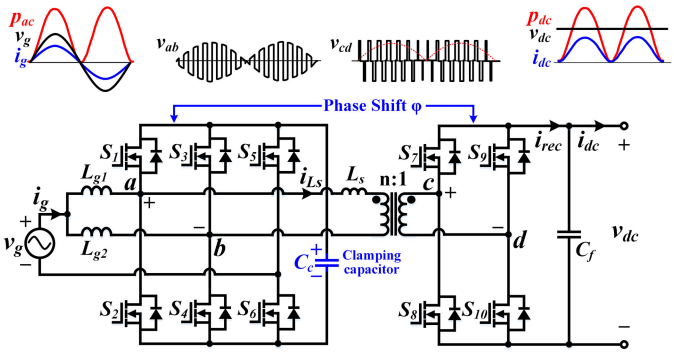


Fig. 3. Proposed bidirectional single-stage interleaved totem-pole ac–dc converter.

topology is that when the grid voltage is positive (negative), bottom switch S_2 (top switch S_1) always loses the ZVS at duty cycle smaller than 0.5, which is around the peak of v_g. The ZVS range was extended to a certain range in [26] by reducing the magnetizing inductance of the HF transformer, which leads to increased circulating current and turn OFF loss.

B. Proposed Converter and Its Operating Principle

Fig. 3 illustrates the proposed bidirectional interleaved totem-pole isolated ac–dc converter, which is derived by replacing the diodes of the unidirectional totem-pole isolated ac–dc converter in Fig. 2(c) with active switches. In the proposed topology, the two interleaving legs are switched with a fixed 50% duty, and the active power is controlled based on the phase shift φ between the primary and secondary and secondary bridges.

Due to the fixed 50% duty of the two interleaving legs, the grid current is ripple-free regardless of the magnitude of the input inductances L_{g1} and L_{g2}, and therefore, the ZVS turn-ON of switches $S_1 \sim S_4$ can always be achieved by proper design of inductances L_{g1} and L_{g2}.

An active full-bridge circuit at the dc-side is interfaced with the grid through an HF link (HFL). The HFL consists of a small HF transformer with a series inductor L_s, where L_s is a combination of a small discrete inductor and the leakage inductance of the transformer. Moreover, the interleaved totem-pole ac–dc converter operates in CCM with 180° phase-shift. Switches $S_1 \sim S_4$ commutate at high switching frequency, whereas S_5 and S_6 are switched at the grid frequency. For the grid positive half-cycle, S_6 is turned ON, whereas during the grid negative half-cycle, S_5 is turned ON.

As mentioned earlier, the bridge consisting of $S_1 \sim S_4$ is switched in a diagonal manner with 50% duty, as depicted in Fig. 4(a). The switching method implemented on the interleaved totem-pole ac–dc converter can be represented by switching function S_{ab} as follows:

$$S_{ab} = \begin{cases} 1, & \text{if } S_1 \text{ and } S_4 \text{ are ON} \\ -1, & \text{if } S_1 \text{ and } S_4 \text{ are OFF} \end{cases}$$

$$= \sum_{n=1,3,5..}^{\infty} \frac{4}{n\pi} \sin(n\omega_s t) \quad \text{for 50\% duty cycle.} \tag{1}$$

Regardless of power level, the voltage across the clamping capacitor is twice of the rectified grid voltage.

$$v_{Cc} = 2\,|v_g(t)| = 2V_{g,\text{peak}}\,|\sin(\omega_g t)|$$

$$= \frac{2}{\pi} - \frac{4}{\pi} \sum_{m=2,4,6,..}^{\infty} \frac{1}{(m^2-1)} \cos(m\omega_g t). \tag{2}$$

As shown in Fig. 4(a), the voltage v_{ab} across the ac side of the transformer is a multiplication of the low-frequency absolute sine wave and higher frequency switching function S_{ab} which are given in (1) and (2) respectively. Assuming ω_g is the grid angular frequency and ω_s is the switching angular frequency, the voltage v_{ab} follows the envelope of $v_{Cc}$with fundamental frequency as ω_s and harmonics $a_{\omega s,m}(\omega_s \pm m\omega_g)$appear as sidebands centered around the switching frequency ω_s and its odd multiples

$$v_{ab} = v_{Cc} \cdot S_{ab}$$

$$= \left[\sum_{n=1,3,5..}^{\infty} \frac{4}{n\pi} \sin(n\omega_s t) \right]$$

$$\times \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{m=2,4,6,..}^{\infty} \frac{1}{(m^2-1)} \cos(m\omega_g t) \right].$$

It is worth noting that the magnitude of the sidebands defined in (3) decreases rapidly and becomes insignificant with the

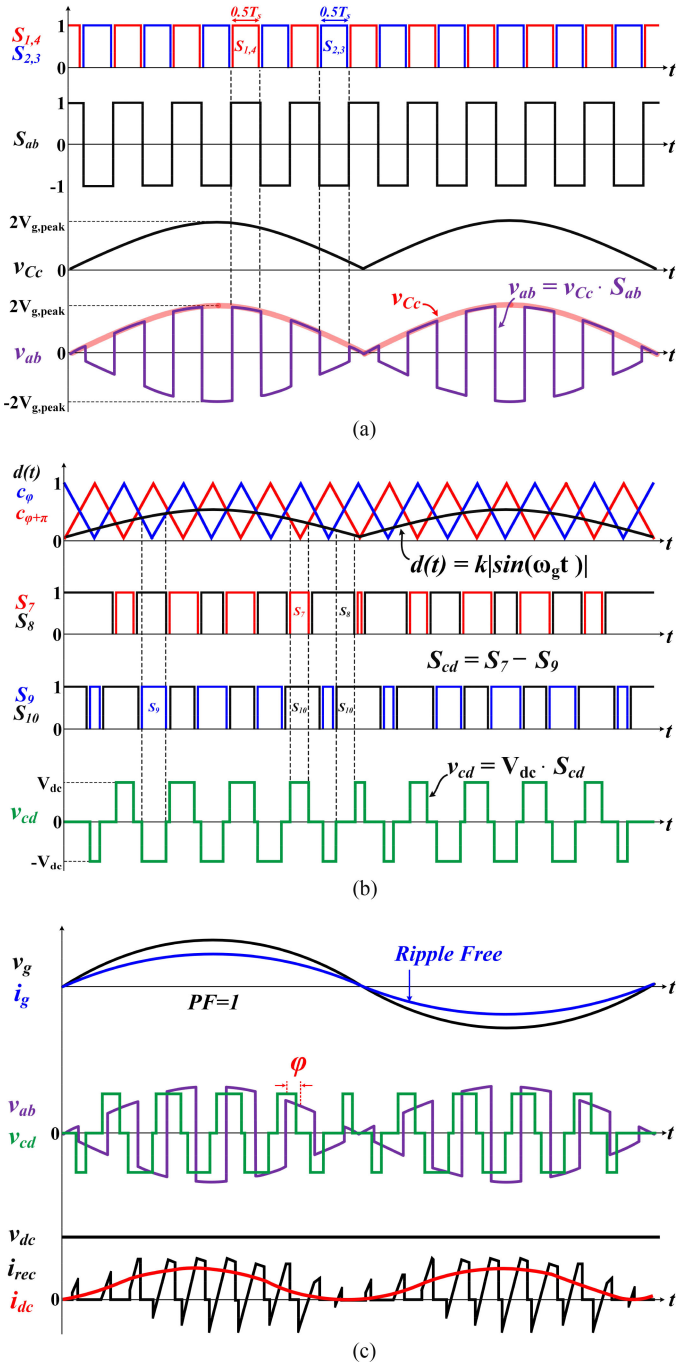


Fig. 4. Operating waveforms showing how to construct (a) voltage v_{ab}, (b) voltage v_{cd}, and (c) output current $i_{\rm dc}$.

increasing order of m

$$v_{ab} = 2V_{g,\text{peak}} \times \begin{bmatrix} 0.8\sin\omega_s t + a_{\omega_s,m}\sin\left(\{\omega_s \pm m\omega_g\}\cdot t\right) \\ +0.5\sin 3\omega_s t + a_{3\omega_s,m}\sin\left(\{3\omega_s \pm m\omega_g\}\cdot t\right) \\ +0.3\sin 5\omega_s t + a_{5\omega_s,m}\sin\left(\{5\omega_s \pm m\omega_g\}\cdot t\right) \\ \text{high-order terms} \end{bmatrix}. \tag{3}$$

The two legs of the full-bridge circuit at the dc-side are 180° phase-shifted and modulated using the signal d,

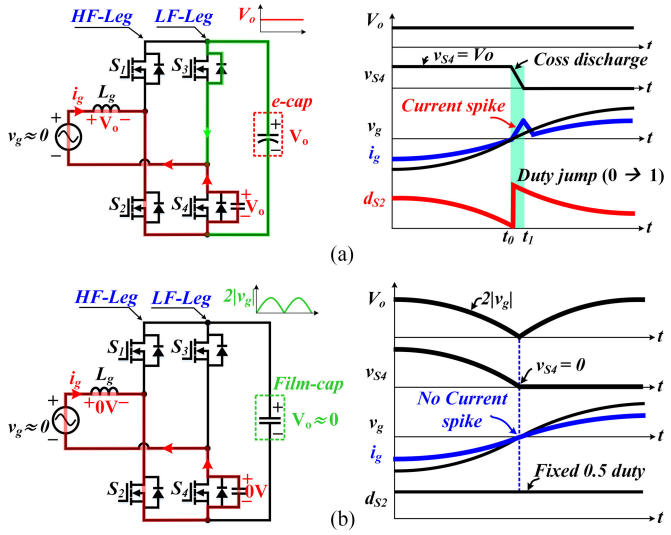


Fig. 5. Key figures showing the zero-crossing issue. (a) Using the conventional switching method. (b) Using the proposed switching method.

as illustrated in Fig. 4(b)

$$d(t) = k|\sin(\omega_g t)| \tag{4}$$

where $k \in]0, 0.5]$. Therefore, the voltage v_{cd} across the transformer secondary side is the product of the dc voltage $V_{\rm dc}$ and S_{cd}. The sine PWM switching function S_{cd} is the difference between the gate signal of the switch S_7 and the gate signal of the switch S_9

$$S_{cd} = S_7 - S_9.$$

Hence

$$v_{\rm cd} = V_{dc}\cdot S_{cd} = V_{dc}\sum_{q=1}^{q} F_{\rm PWM}(q_n, m_f, \beta, q) \tag{5}$$

where

$$F_{\rm PWM} = 16\sum_{n=1,2,3..}^{\infty} q_n \sin\left(n\beta + \frac{n\pi}{m_f}\right)\sin\left(\frac{n\pi}{m_f}\right) \times \cos^2\left(\frac{n\pi}{2}\right)\cos(n\omega_s t)$$

and $m_f = \dfrac{f_s}{f_g}$, $q = \dfrac{m_f}{4}$, $\beta = \dfrac{(2q-1)\pi}{m_f}$, $q_n = \dfrac{\sin(\frac{nd}{2})}{n\pi}$.

From the Fourier series expressions of v_{ab} and v_{cd} given in (3) and (5), voltages fed to the transformer do not include low-frequency components.

C. Zero-Crossing Issue in Bridgeless Totem-Pole AC–DC Converter

Another issue related to the conventional totem-pole ac–dc converter is the zero-crossing spike problem, which increases the total harmonic distortion (THD) and reduces the power factor. Fig. 5 shows the equivalent circuits at zero-crossing and operating waveforms of the totem-pole ac–dc converter with

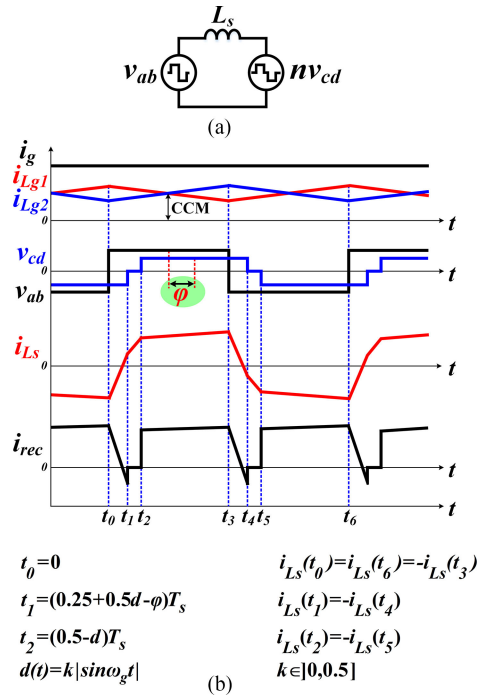


Fig. 6. Power flow of the proposed converter. (a) Simplified electrical model. (b) Theoretical waveforms.

the conventional and proposed switching methods, respectively. Ideally, if switch S_4 is turned ON instantly right after the grid voltage becomes positive, the inductor can build up the sinusoidal current without zero-crossing spike. However, in the conventional switching method, the output capacitor voltage of switch S_4 starts to *gradually* discharge due to the reverse recovery of the body diode of switch S_3. This causes a large current spike in L_g, as shown in Fig. 5(a), which continues to increase until the voltage of switch S_4 becomes zero due to the large duty of switch S_2. Therefore, in order to mitigate the zero-crossing spike in the conventional switching method, the switches in the line frequency leg (LF-Leg) should have good body diode characteristics and small output capacitance [33]. On the other hand, as shown in Fig. 5(b), the proposed method uses a fixed 50% duty for switches in the high-frequency leg (HF-Leg) so that the output voltage waveform becomes $2|v_g|$. Therefore, the voltage of switch S_4 around zero-crossing is almost zero, resulting in a negligible zero-crossing spike regardless of the body diode characteristics and output capacitance $C_{\rm oss}$ of the switch the switch in the LF-Leg.

D. Power Transfer

The proposed converter can be represented by two voltage sources v_{ab} and nv_{cd} connected across the series inductance L_s. Fig. 6(a) shows the simplified electrical model of the proposed converter. Fig. 6(b) presents the theoretical steady-state waveforms of the proposed converter during one switching period T_s for $v_g > 0$. Note that interleaving between the two inductors in CCM with 50% duty leads to a ripple-free grid current, as depicted in Fig. 6(b). As a result, more flexibility is provided for designing L_{g1} and L_{g2} without sacrificing grid current quality.

The voltage v_{ab} leads (lags) v_{cd} for the forward (reverse) mode. Current i_{Ls} through the series inductance is shaped according to the voltage difference between v_{ab} and nv_{cd}, and its slopes at each time interval are given as

$$\frac{di_{Ls}}{dt} = \begin{cases} \dfrac{2|v_g| - (-nV_{dc})}{L_s} = \dfrac{2|v_g| + nV_{dc}}{L_s}, & t_0 \le t < t_1 \\ \dfrac{2|v_g| - 0}{L_s} = \dfrac{2|v_g|}{L_s}, & t_1 \le t < t_2 \\ \dfrac{2|v_g| - (nV_{dc})}{L_s}, & t_2 \le t < t_3 \\ \dfrac{-2|v_g| - (nV_{dc})}{L_s} = -\left[\dfrac{2|v_g| + nV_{dc}}{L_s}\right], & t_3 \le t < t_4 \\ \dfrac{-2|v_g| - 0}{L_s} = \dfrac{-2|v_g|}{L_s}, & t_4 \le t < t_5 \\ \dfrac{-2|v_g| - (-nV_{dc})}{L_s} = \dfrac{-2|v_g| + nV_{dc}}{L_s}, & t_5 \le t < T_s. \end{cases}$$

The symmetrical voltages applied across the transformer leads to a symmetric current i_{Ls} with respect to the t-axis. Therefore, only the first half of the switching cycle is considered; and defining i_{Ls} at instants t_0, t_1, and t_2, as given in (6)–(8), is used to analyze power flow in the proposed converter.

$$i_{Ls}(t_0) = \frac{[-|v_g| + (0.5 - 2\varphi)nV_{\rm dc}]}{2L_s} \cdot T_s \tag{6}$$

$$i_{Ls}(t_1) = \frac{[(4\varphi + 2d - 2)|v_g| + dnV_{dc}]}{2L_s} \cdot T_s \tag{7}$$

$$i_{Ls}(t_2) = \frac{[(4\varphi - 2d)|v_g| + dnV_{\rm dc}]}{2L_s} \cdot T_s. \tag{8}$$

The determination of the power transferred is reduced to the determination of the average current $i_{\rm rec}(t)_{\rm avg}$

$$\begin{aligned} i_{\rm rec}(t)_{\rm avg} &= \frac{2n}{T_s}\int_{t_0}^{\frac{T_s}{2}} i_{Ls}(t)\,dt \\ &= \frac{2n}{T_s}\left[\int_0^{t_1} -i_{Ls}(t)\,dt + \int_{t_2}^{\frac{T_s}{2}} i_{Ls}(t)\,dt\right] \end{aligned} \tag{9}$$

where t_0, t_1, and t_2 are given in Fig. 6(b). Therefore, the instantaneous power is

$$\begin{aligned} p(t) &= V_{dc} \cdot i_{\rm rec}(t)_{\rm avg} \\ &= \frac{(4\varphi^2 - 2\varphi + d^2 - d + 0.25)nV_{dc}|v_g(t)|}{f_s L_s}. \end{aligned} \tag{10}$$

The power flow magnitude and direction can be adjusted with phase shift φ. The turn ratio and the series inductance need to be optimized for high efficiency while delivering the desired power.

E. Soft-Switching Conditions

Along with the adopted switching scheme, some design considerations need to be taken into account in order to maintain the ZVS turn-ON for switching devices $S_1 \sim S_4$. The soft commutation of switches in each interleaving leg depends on the relationship between the input inductor current (i_{Lg1}, i_{Lg2}) and current i_{Ls}.

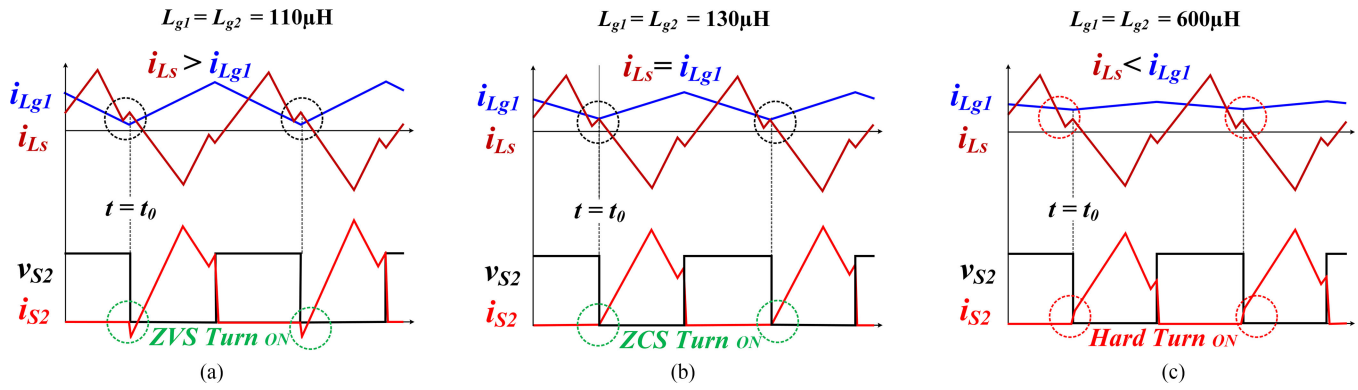


Fig. 7. Soft-switching condition. (a) $L_{g1} = L_{g2} = 110\ \mu$H. (b) $L_{g1} = L_{g2} = 130\ \mu$H. (c) $L_{g1} = L_{g2} = 600\ \mu$H.

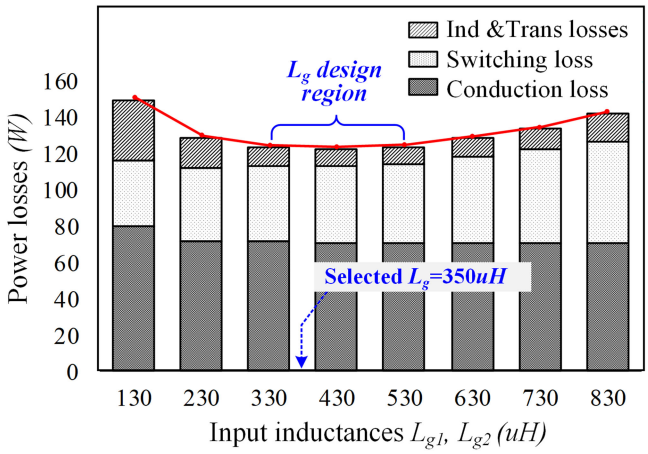


Fig. 8. Loss analysis of the proposed converter at full load.

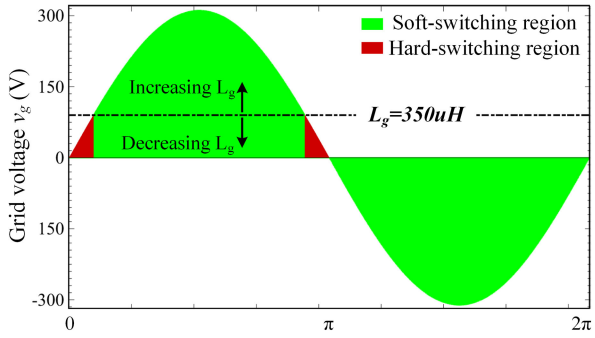


Fig. 9. Soft and hard switching regions of the main switch for $L_g = 350\ \mu$H.

In order to explain the ZVS condition, only switch S_2 that operates as a main (synchronous) switch during the grid positive (negative) half cycle is considered since the same condition can be said for other switches of the two interleaved legs. Switch S_2 turns ON at the instant t_0, as depicted in Fig. 7, and three different conditions are distinguished according to the value of the input inductance. Fig. 7(a) shows that ZVS turn-ON is always secured for $L_g < 130\ \mu$H if i_{Ls} is maintained greater than i_{Lg1} around 10% of the grid peak voltage $V_{\mathrm{g\_peak}}$. The boundary condition illustrated in Fig. 7(b) occurs for an input inductor $L_g = 130\ \mu$H that makes $i_{Ls} = i_{Lg1}$ at the instant t_0. In this case, S_2 is turned ON with ZCS. Fig. 7(c) shows the ZVS turn-ON failure around 10% of $V_{\mathrm{g\_peak}}$ for values of $L_g > 130\ \mu$H that make an input current i_{Lg1} greater than i_{Ls} at t_0. In other words, the ZVS condition of switches is determined based on the value of L_{g1} and L_{g2}. It is worthy to mention that considering very small input inductors extends the ZVS range, but the circulating current is increased. Therefore, L_{g1} and L_{g2} need to be designed properly considering the tradeoff between the switching loss and conduction loss.

In Fig. 8, the power losses of the proposed converter are calculated for different values of L_{g1} and L_{g2}, whereas the conduction and switching losses along with the losses attributed inductors and HF transformer are estimated according to the following specifications: $P_o = 3.3$ kW, $V_g = 220$ V, $V_{\mathrm{dc}} = 350$ V, $f_s = 100$ kHz, n:1 = 1.7:1, and $L_s = 45\ \mu$H. The switching losses of the line rectification switches S_5 and S_6 are assumed to be equal to zero. The minimum input filter inductance to operate the proposed converter in CCM is $L_{g1} = L_{g2} = 130\ \mu$H, where the largest power losses occur due to high circulating current and large inductor current ripple. At the minimum filter inductance of 130 μH, full-range ZVS is achieved for all switches. Despite the slight increase in the switching losses of $S_1 \sim S_4$ for larger inductances, the power losses keep decreasing because of the reduced core loss and lower circulating current. Note that for larger values than $L_{g1} = L_{g2} = 230\ \mu$H, no significant change is observed in the conduction loss as the circulating current becomes almost constant. The total power losses begin to increase due to the increase in switching and magnetic losses for values larger than $L_{g1} = L_{g2} = 530\ \mu$H. Hence, the interval highlighted in Fig. 8 characterizes the reasonable range to select L_{g1} and L_{g2}, and $L_{g1} = L_{g2} = 350\ \mu$H is selected for the given specifications.

Fig. 9 shows the soft- and hard-switching regions of the main switches in the case of $L_{g1} = L_{g2} = 350\ \mu$H. It is noted that decreasing the input inductances extends the soft-switching region. Despite the ZVS failure around the zero-crossing, the current level within this region is very low, and high efficiency can be maintained.

III. Control Strategy

Fig. 10 shows the control block diagram for the proposed converter. The active power and dc voltage are regulated based on the secondary side (dc-side) phase shifting with respect to the primary side. The control system consists of an outer-loop

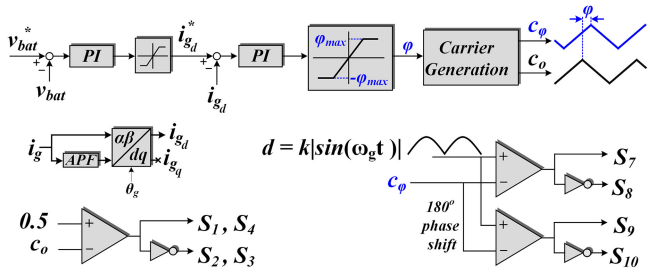


Fig. 10. Control block diagram.

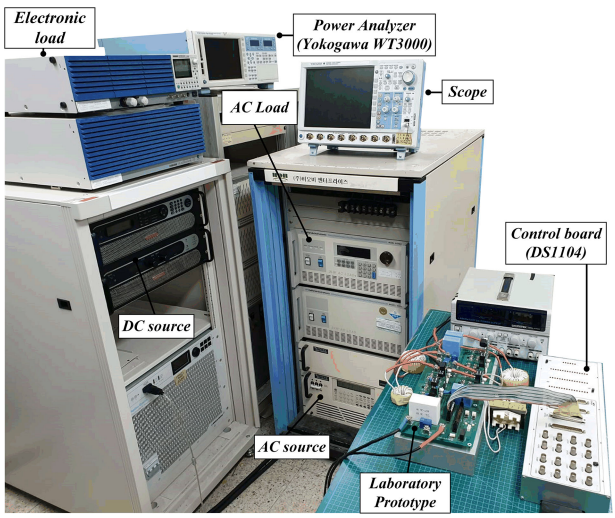


Fig. 11. Experimental setup.

dc voltage controller and inner-loop current controller. The first PI controller integrates the error between the pure dc feedback voltage and reference dc voltage to generate the corresponding reference grid current. The inner PI current regulator determines the phase angle of the shifted carrier with respect to a reference carrier signal. The dc-side full-bridge is modulated based on the shifted carrier signal.

The controller is simple and easily implemented since the ac-side circuit does not take part in the control; and the two interleaving legs are switched with a fixed 50% duty based on the reference carrier signal. All feedback and reference values are time invariant (pure dc). Hence, PI is a reliable controller to achieve zero steady-state error. As mentioned earlier, switching $S_1 \sim S_4$ with fixed 50% duty and employing small film clamping capacitor maintains $vc_c = 2|v_g|$; as a result, the average input current automatically tracks the sinusoidal shape of the input voltage. Hence, the proposed converter has an inherent PFC property.

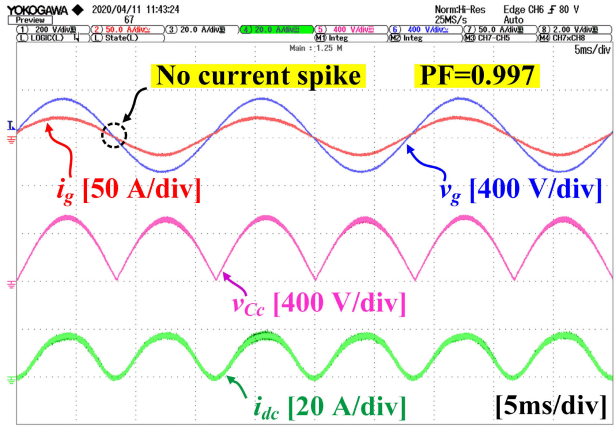
IV. Experimental Results and Discussions

In order to verify the performance and the theoretical claims of the proposed converter, a 3.3 kW laboratory prototype was built as shown in Fig. 11; and the presented experimental results are obtained according to following specification: $P_o = 3.3$ kW, $V_{g,\,\mathrm{rms}} = 220$ V, $f_g = 60$ Hz, $V_{\mathrm{dc}} = 320 \sim 400$ V, and $f_s = 100$ kHz. The system parameters of the proposed converter are listed in Table I. The minimum circulating current with minimum switch current rating is achieved at $k = 0.5$. Therefore, the parameter k in $d(t) = k|\sin(\omega_g t)|$ is kept constant in the experimental verifications of the proposed converter. The whole control system was implemented on a DS1104 DSPACE controller platform that processes the sensed values and generates the corresponding gate signals.

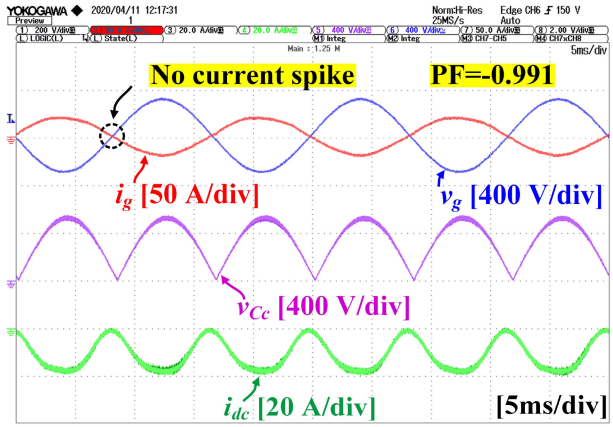
Fig. 12(a) and (b) shows the experimental waveforms of the proposed bidirectional ac–dc converter at full load for forward and reverse modes, respectively. A near unity power factor is inherently achieved for both power flow directions (0.997 for $P>0$ and -0.991 for $P<0$), as the voltage across the clamping

TABLE I
System Parameters of the Proposed Converter

Components	Symbols	Values
Input inductor	L_g	2 x 350 [μH]
Clamping capacitor	C_c	2.5 [μF]
Switch	$S_{1\sim10}$	IXYS: IXFN60N80P 800 V, 53 A
Series inductor	L_s	45 [μH]
HF Transformer	n	TDK: PQ78/39 1.7
DC-side filter capacitance	C_f	45 [μF]



(a)



(b)

Fig. 12. Experimental results. (a) Forward mode $P>0$. (b) Reverse mode $P<0$.

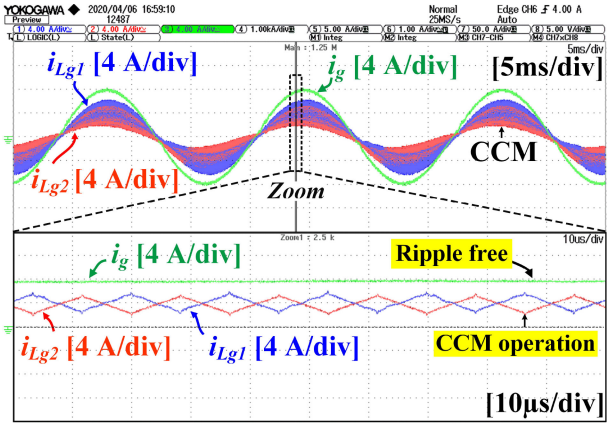
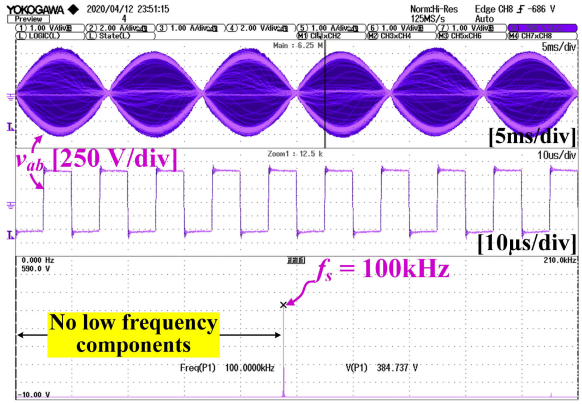
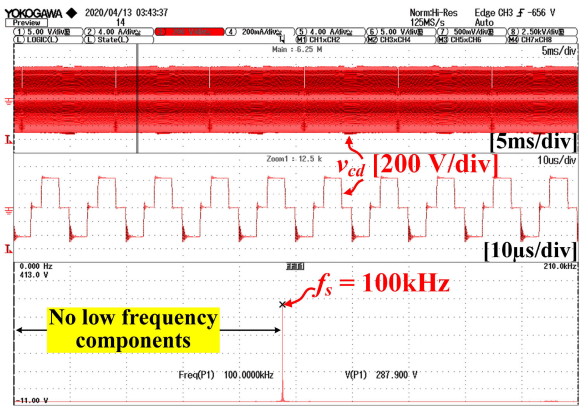


Fig. 13. Input inductors current and grid current.



(a)

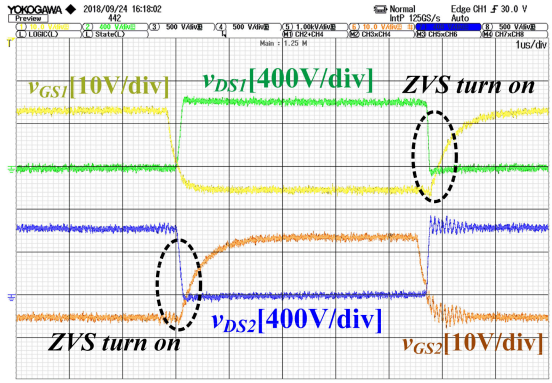


(b)

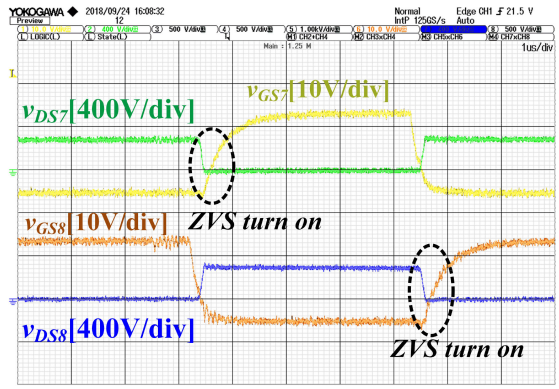
Fig. 14. Voltages across the HF transformer. (a) v_{ab} in the ac side. (b) v_{cd} in the dc-side.

capacitor C_c is inherently maintained $vc_c = 2|v_g|$ using a significantly small film capacitor. Hence, the average grid current automatically tracks the sinusoidal shape of the grid voltage.

As claimed in Section II-C, it is experimentally verified in Fig. 13 that the grid current changes the direction smoothly without a zero-crossing spike; that is because $vc_c = 2|v_g|$ is almost zero around the ac zero-crossing. As a result, low THD of the grid current is achieved at a wide load range.



(a)



(b)

Fig. 15. ZVS condition at 99% of $V_{\mathrm{g-peak}}$. (a) v_{ds} and v_{gs} of switches S_1 and S_2. (b) v_{ds} and v_{gs} of switches S_7 and S_8.

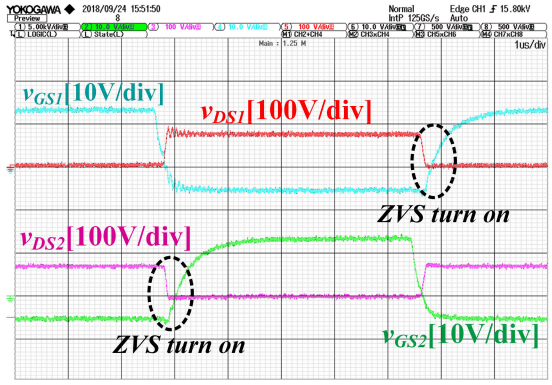
The dc current i_{dc} mainly includes dc and second harmonic components. As reported in [31], the second harmonic component in i_{dc} has no adverse effect in many ac–dc applications, including telecom power supplies, energy storage systems, and EV battery chargers.

The CCM operation of the proposed converter is presented more closely with the time-extended waveforms of the input inductor currents i_{Lg1} and i_{Lg2} in Fig. 13. It is seen that the switching frequency components in i_{Lg1} and i_{Lg2} are interleaved well with a 180° phase shift. As a result, the grid current is HF ripple-free regardless of input inductance since the two-phase interleaved boost converter is switched at a fixed 50% duty cycle.

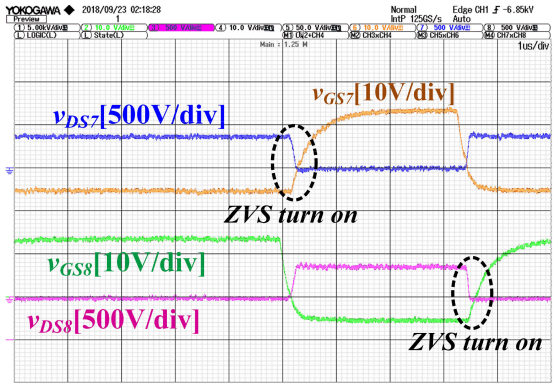
It is seen from Fig. 14 that the voltage across the transformer does not contain any low-frequency harmonics. Therefore, a lightweight HF transformer is used.

The switch current could not be accessed in the experiments; instead, the gating signal v_{gs} and drain–source voltage v_{ds} of the switches S_1, S_2, S_7, and S_8 are shown at 99% and 10% of $V_{\mathrm{g-peak}}$ for soft-switching verification. It is observed at the two mentioned points in Figs. 15 and 16 that the gate voltages begin to rise only after drain–source voltages decrease very close to zero. Hence, the ZVS turn-ON is maintained in almost the whole grid cycle without any auxiliary or resonant circuit.

The measured efficiencies of the proposed converter using Yokogawa WT3000 according to the load variation are shown in Fig. 17 for both forward and reverse modes. The peak efficiencies are 96.7% and 96.2% at 3.3 kW in the forward and reverse power flow, respectively. The appreciable efficiency of



(a)



(b)

Fig. 16. ZVS condition at 10% of V_{g_peak}. (a) v_{ds} and v_{gs} of switches S_1 and S_2. (b) v_{ds} and v_{gs} of switches S_7 and S_8.

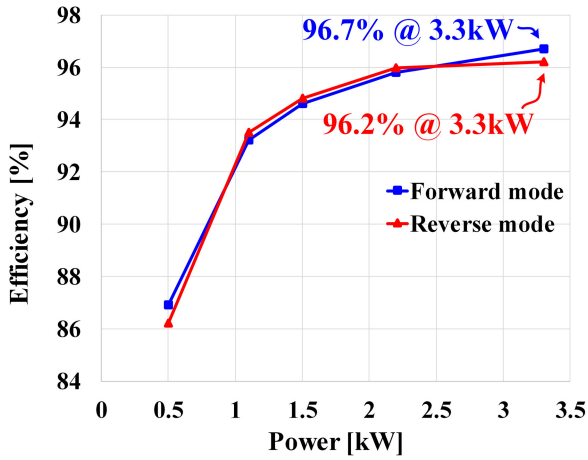


Fig. 17. Measured efficiency under tested load conditions.

the proposed converter is due to the achieved entire range ZVS and CCM operation that significantly reduces the circulating current and core loss in magnetic components.

The measured power factors are given in Fig. 18 for different load conditions. The maximum power factor is 0.997 at 3.3 kW.

Fig. 19 shows the measured THD of i_g under every tested load condition. A low THD of the grid current is achieved at a wide load range. The minimum point of the THD of the grid current is about 2.7% measured at full load.

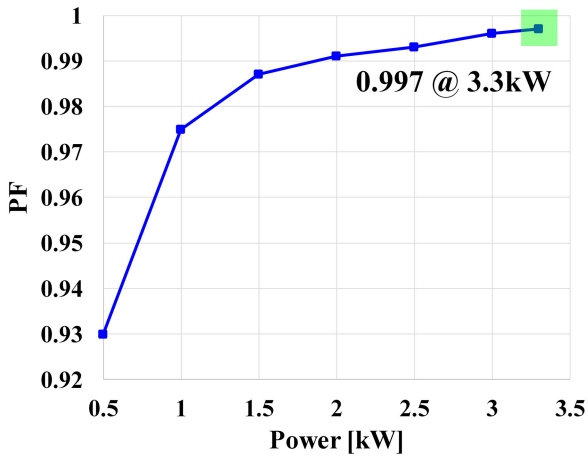


Fig. 18. Measured power factor under tested load conditions.

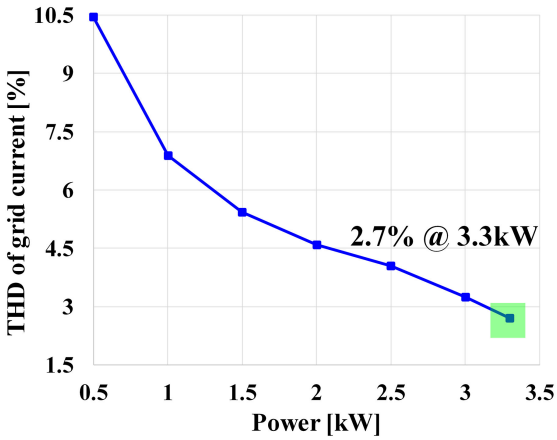


Fig. 19. Measured THD of grid current i_g under tested load conditions.

V. Conclusion

This article proposes a bidirectional isolated ac–dc converter with HF isolation. The key idea was to construct a single-stage structure by integrating the interleaved totem-pole ac–dc converter with the DAB. The proposed converter employs a simple phase-shift controller for power and dc output regulation, while the nonregulating ac side is switched with a fixed 50% duty. The grid current is switching frequency ripple-free with no zero-crossing spike regardless of the magnitude of the input inductance that can be adjusted to achieve full-range ZVS for all switches. Hence, the proposed converter using Si devices is operated in CCM without a reverse recovery issue. Furthermore, the introduced circuit offers high reliability due to reduced component count, high lifespan of the used film capacitors, and a simple controller. The operating principle of the converter has been addressed in detail, and the experimental results from a 3.3 kW prototype are provided to confirm the feasibility of the converter. The measured efficiency for both forward and reverse modes is almost identical with peak efficiencies of 96.7% and 96.2%, respectively.

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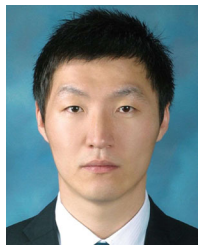

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