Enhanced Hybrid Active-Neutral-Point-Clamped Converter With Optimized Loss Distribution-Based Modulation Scheme

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***Abstract*—The active-neutral-point-clamped (ANPC) converter is a prominent topology for medium voltage applications. To realize a high-power-density three-level ANPC converter, silicon carbide (SiC) MOSFETs may be used but they also lead to an extremely high cost. Thus, it is important to properly utilize the SiC switches in order to achieve not only a highly efficient but also a low-cost system. In this article, a three-level enhanced hybrid ANPC (E-HANPC) structure is proposed, which optimally utilizes both Si insulated gate bipolar transistors (IGBTs) and SiC MOSFETs to achieve these objectives. A dedicated modulation scheme is also proposed that enables a reduction in the conduction and switching losses and, hence, higher efficiency is achieved. The presented method optimally distributes the losses amongst the converter switches that leads to enhanced power handling capability of the E-HANPC converter. Moreover, the proposed converter also achieves short-length commutation loops for the high-frequency SiC MOSFETs, which imparts fast-switching capability with reduced overvoltage stress on these switches. To validate the efficacy of the proposed converter and modulation scheme, extensive simulation and analytical studies are performed. A prototype of the single-phase leg of the E-HANPC converter is also developed to validate its feasibility, proposed principles, and reconfirm the simulation and analytical findings.**

***Index Terms*—Active-neutral-point-clamped (ANPC) converter, hybrid topology, loss distribution, modulation scheme, silicon (Si), silicon carbide (SiC) devices.**

I. Introduction

THE active-neutral-point-clamped (ANPC) converter is one of the most popular variants of the neutral-point-clamped (NPC) converter topology. Its major applications include electrical drives, power electronic interface for renewable energy sources, electric propulsion systems, and other medium-voltage applications [1]–[5]. The ANPC converter features more degrees of freedom in terms of balancing the dc-link voltages and having equal stress on the switching devices over the conventional NPC topology [1], [6].

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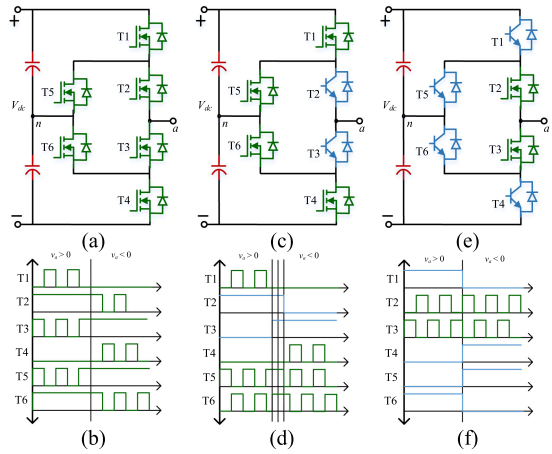

Fig. 1. Existing SiC-devices-based ANPC topologies with their PWM strategies. (a) All SiC-MOSFET-based ANPC (AANPC) [7]. (b) Its PWM scheme. (c) Four SiC-MOSFET-based hybrid ANPC (HANPC-1) [14]. (d) Its PWM scheme. (e) Two SiC-MOSFET-based hybrid ANPC (HANPC) [15]. (e) Its PWM scheme.

Recently, the silicon carbide (SiC) devices are proposed to be used for the ANPC converter applications [see Fig. 1(a)] to achieve high efficiency at high-power density by enabling high switching frequency with low switching losses [7]. It can be seen from its pulsewidth modulation (PWM) gate pulses, shown in Fig. 1(b), that all devices switch at the high frequency. However, this all-SiC devices-based (AANPC) topology requires six SiC MOSFETs per phase-leg leading to an increase in the cost. Presently, the SiC MOSFETs are more than four-times costlier than the similar rated Si insulated gate bipolar transistors (IGBTs) [8], [9]. Furthermore, it is expected that it may take much longer before the cost difference between the Si and SiC devices reduces significantly [10], [11]. It is also very unlikely that the SiC MOSFETs will be cheaper than the similar rated Si IGBTs in the near future [12], [13]. Therefore, for a successful adaption of this technology, the current feasible way can be through the development of hybrid devices-based converter topologies.

Fig. 1(c) shows one of such HANPC-1 topology consisting of four SiC MOSFETs and two Si IGBTs [14]. The four SiC MOSFETs operate at a higher frequency compared to the Si IGBTs, as can be seen from the PWM gate pulses shown in Fig. 1(d). The modulation scheme is designed to have an additional state during

the zero crossings of the output voltage that can be used to reduce the conduction losses [14]. However, the loss reduction is very small. Further reduction in the cost with only two SiC MOSFETs is presented in [15] with the circuit schematic shown in Fig. 1(e). This HANPC topology uses SiC MOSFETs in place of T2 and T3 switches and its PWM scheme is illustrated in Fig. 1(f). It can be seen from Fig. 1(f) that only SiC MOSFETs operate at a high switching frequency while the Si IGBTs are switched at the fundamental frequency.

In the aforementioned topologies, the SiC MOSFETs are utilized for reducing the switching losses. However, the effect on conduction losses is not taken into consideration. SiC MOSFETs being unipolar devices suffer from high conduction losses due to the high ohmic drop near to the rated current values [16]. Thus, it is very important to consider the effect of conduction loss on the net loss reduction in such SiC MOSFET-based topologies specifically at rated power. Furthermore, none of the aforediscussed PWM schemes balances the losses amongst all the converter switches resulting in high stress on the SiC switches at rated power operation. If the thermal management is not properly done, then the high stress on some selective switches in a given converter might lead to poor performance and degradation [17]. Furthermore, the maximum junction temperatures of the commercially available state of the art SiC devices are still limited due to the packaging restrictions [17], [18]. These facts are not considered in the aforediscussed SiC-based ANPC topologies while imposing the maximum stresses on the SiC devices. Thus, in most of these topologies, the SiC devices may actually restrict the converter operating limits.

Another issue with the SiC MOSFET-based ANPC topologies is the effect of commutation loop inductance on the converter operating limits. Since the SiC MOSFETs have extremely short switching ON and OFF timings the commutation loop inductance causes high overvoltage peak across the SiC MOSFET [19]. This overvoltage may also lead to device destruction [19]. Thus, it is important to reduce the loop inductance of the commutating path of the SiC MOSFETs to enhance the converter operating limits.

This article proposes an enhanced-HANPC (E-HANPC) converter topology, which aims to address the issues stated above with the existing topologies. The proposed topology using the novel modulation scheme achieves a reduction in both conduction and switching losses, which results in higher converter efficiency. For this, the proposed modulation scheme optimally utilizes the unipolar SiC MOSFETs to reduce the switching losses and bipolar Si IGBTs to reduce the conduction losses. Using this modulation scheme, most of the switching events are concentrated on the SiC MOSFETs, while Si IGBTs in the proposed E-HANPC topology are switched at either zero or at reduced currents. Moreover, the conduction losses are also reduced using the parallel conduction paths. The proposed modulation scheme also optimally balances the losses amongst the switches of the E-HANPC converter and, thus, avoids overstressing of the SiC switches. Furthermore, the proposed converter features small commutation loops for the SiC switches ensuring the reduced turn-OFF overvoltage peak across these switches without adding any external component in the circuit. Thus, the proposed modulation scheme not only reduces the device losses but also provides lower switching stress on the SiC switches in the E-HANPC converter. This results in an enhanced operating limit of the converter.

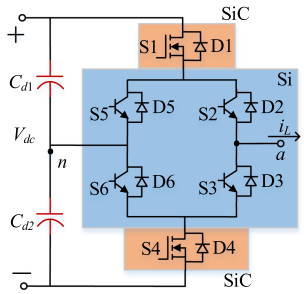

Fig. 2. Single-phase leg of the E-HANPC converter showing the selected locations of SiC switches.

II. Structure and Operation of E-HANPC Converter

In the SiC MOSFET-based ANPC topologies, the conduction loss becomes the dominant loss component specifically near to the rated power operation due to the unipolar nature of SiC MOSFET [16]. Hence, in order to achieve higher efficiency, the conduction loss component needs to be minimized. In Fig. 1(a) and (e), since the switches T2 and T3 conduct for most of the time, the SiC MOSFETs at these locations will experience high conduction losses. Furthermore, these switches commutate through a long commutation loop, which restricts the converter operating limit [19]. Thus, T2 and T3 may not be the best locations for the SiC MOSFETs. In the proposed topology, SiC MOSFETs are placed in the positions of the outer switches of an ANPC leg. These positions not only result in reduced conduction losses but also provide a balanced distribution of device losses using the proposed modulation scheme. Additionally, the shorter commutation loop is enabled for the SiC switches resulting in an enhanced operating limit.

This proposed structure of the E-HANPC converter and its working with the proposed modulation scheme is explained in the following sections.

A. Structure of E-HANPC Converter

The single-phase leg circuit schematic of the E-HANPC converter is shown in Fig. 2. This converter contains six active switches per phase-leg among which, as discussed earlier, S1 and S4 are the SiC MOSFETs with their body diodes D1 and D4, as shown in the figure. The switches S2, S3, S5, and S6 are Si IGBTs with their Si antiparallel diodes depicted as D2, D3, D5, and D6, respectively. It can be seen from Fig. 2 that the SiC MOSFETs in the E-HANPC topology have outer switch positions, which facilitate them to have low losses with the proposed modulation scheme. On the other hand, the Si IGBTs in the E-HANPC converter have positions of inner and clamping switches, which enables the use of the full-bridge Si IGBT module in the E-HANPC topology, unlike in the existing hybrid ANPC configurations [14], [15]. However, due to the outermost switch locations of the SiC MOSFETs, it is not possible to use a SiC MOSFET module in the proposed topology, and thus, the discrete SiC MOSFETs need to be utilized. Therefore, the maximum current rating of the proposed topology will be limited

TABLE I
SWITCHING STATES FOR THE E-HANPC CONVERTER

	S1	S2	S3	S4	S5	S6
P	1	1	0	0	0	1
O^{T1}	0	1	0	0	0	1
O^{p}	0	1	1	0	1	1
O^{n}	0	1	1	0	1	1
O^{T2}	0	0	1	0	1	0
N	0	0	1	1	1	0

up to 100 kW by the presently available discrete SiC MOSFETs [20]. Nonetheless, for applications requiring high current ratings, parallel-connected SiC MOSFETs can be used [21]. The E-HANPC converter operation with the proposed modulation scheme is explained next.

B. Operating Principles

The E-HANPC converter contains a combination of Si and SiC devices. In such hybrid configurations, the state-of-the-art modulation schemes use the redundant states of the converter to facilitate the distribution of switching events on the SiC devices resulting in reduced switching losses [14], [15]. On the other hand, in the E-HANPC converter, the proposed modulation scheme also minimizes the conduction losses in addition to the switching losses by reducing the duration of conduction of SiC MOSFETs and also by enabling the parallel conduction paths of Si IGBTs during zero states. Moreover, the proposed modulation scheme enables balanced loss distribution amongst the switches of the E-HANPC converter. Therefore, the SiC switches in the E-HANPC converter experience reduced switching stress, and the power handling capability of the converter can be enhanced. The proposed modulation scheme is explained next.

1) Proposed Modulation Scheme: The proposed modulation scheme for the E-HANPC converter is derived to handle two major tasks. The first is to avoid short-circuit occurrence while operating both Si and SiC switches as their switching timings are different [22], [23]. The second task of this modulation scheme is to optimally utilize the SiC MOSFETs to reduce the switching losses and enable parallel conduction paths using the Si IGBTs to reduce the conduction losses of the converter. To fulfill these objectives, six operating states are chosen, as listed in Table I (P, O^P, O^{T1}, O^{T2}, O^N, and N), where "1" and "0" indicate the ON and OFF states of the corresponding switch, respectively. The two consecutive operating states with a change in the state of a switch are shaded in Table I, depicting the switching transition of the respective switch. As can be seen, S1, S3, and S5 change their states in the positive half of the fundamental cycle, while S2, S4, and S6 have transitions in the negative half of the fundamental cycle. It can further be seen from Table I that in the null states (O^P and O^N), all Si IGBTs (S2, S3, S5, and S6) are turned-ON resulting in parallel conduction paths. This results in reduced conduction losses during the null states.

The gate pulse generation with the operating states from Table I using the proposed modulation scheme is illustrated in Fig. 3. The gate pulses are indicated as g1–g6 for the switches S1–S6, respectively.

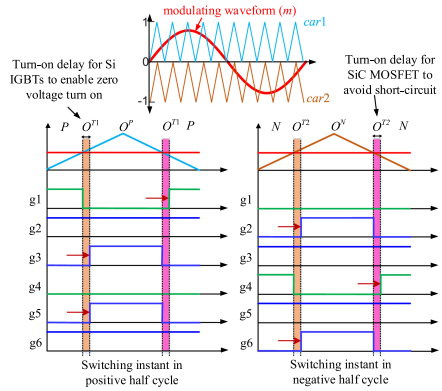

Fig. 3. Pictorial representation of the proposed modulation scheme switching pattern in detail for a switching cycle in the positive and negative half-cycle for the single-phase leg of the E-HANPC converter.

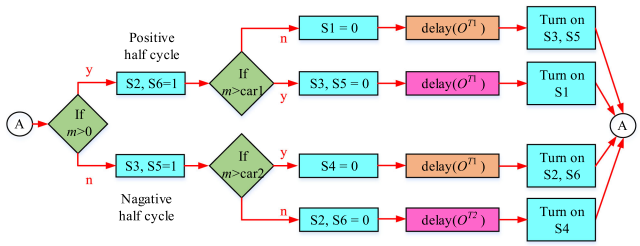

Fig. 4. Logic diagram for the generation of the gating pulses using the proposed modulation scheme for the E-HANPC converter.

Considering the switching events in the positive half of the fundamental cycle, during the transition from the P to O^P state, the delay-state O^{T1} is introduced first. This ensures the state change of only S1 from ON to OFF. Therefore, it now blocks the $V_{dc}/2$ voltage during this O^{T1} state, which results in zero voltage appearing across the Si IGBTs S3 and S5 during switching. In this way, zero voltage switching is achieved for the Si IGBTs leading to reduced switching losses. Furthermore, it can be seen from Fig. 3 that the delay-state O^{T1} is again introduced while transitioning from the O^P to P state. This ensures that the gating pulses are removed for S3 and S5 before turning ON the SiC MOSFET S1. Hence, this introduction of the O^{T1} operating state while transitioning from the O^P to P state provides a dead-time and avoids the short-circuit event. A similar operation is achieved using the delay-state O^{T2} during the negative half of the fundamental cycle. The overall converter operation is explained in further detail in the following section.

The logic for generating the gate pulses as per Fig. 3 is illustrated in Fig. 4. As can be seen, the SiC switches S1 and S4 are gated in only positive and negative halves of the fundamental cycles for $m > car1$ and $m > car2$, respectively. Furthermore, all the Si IGBTs are turned ON for $m<car1$ and $m<car2$ in the positive and negative halves of the fundamental cycles, respectively. It can also be seen from Fig. 4 that the turn-ON signals for all the switches are delayed using the delay blocks. These delay blocks represent the delay-states O^{T1} and

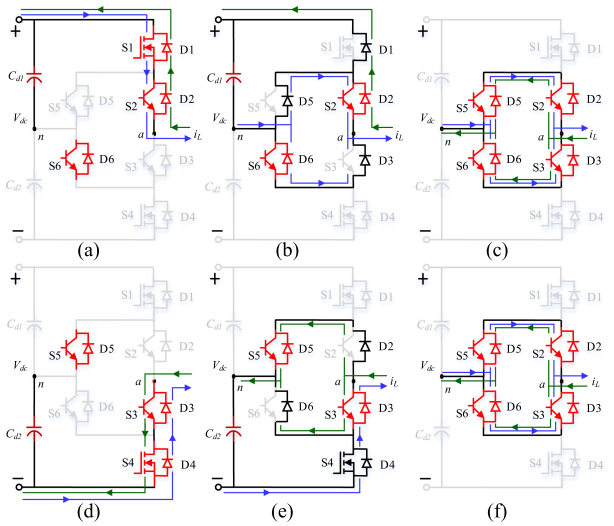

Fig. 5. Equivalent circuits of the E-HANPC converter operating in (a) P, (b) O^{T1}, (c) O^P, (d) N, (e) O^{T2}, and (f) O^N states using the proposed modulation scheme with the allowed conduction paths (blue for $i_L > 0$ and green for $i_L < 0$).

O^{T2} in the positive and negative half of the fundamental cycles, respectively, as explained above.

2) Converter Operation: Fig. 5(a)–(f) illustrates the equivalent circuits of the E-HANPC converter corresponding to its six operating states, as listed in Table I. As explained earlier using Table I and Fig. 3, in the positive half-cycle of the modulating waveform, there will be P-O^{T1}-O^P and O^P-O^{T1}-P state transitions. These state transitions are explained here in detail.

1) *P-O^{T1}-O^P transition:* The E-HANPC converter equivalent circuit for the P state is shown in Fig. 5(a) with the possible conduction paths. In this state, switches S1, S2, and S6 are turned-ON (see Table I). For load current (i_L) > 0, switches S1 and S2 conduct, while for $i_L < 0$, the current flows through the respective diodes D1 and D2. It is to be noted that S6 should be turned ON to guarantee equal voltage sharing between S3 and S4, as is also done in the ANPC topology for equal voltage sharing [1]. When the modulating signal (m) becomes lower than $car1$, as in Fig. 3, the converter operating state is changed from P to O^{T1} by applying the turn-OFF signal to S1 [see Fig. 5(b)]. This initiates the commutation of the current from S1 to the two parallel paths; D5-S2 and S6-D3 for $i_L > 0$. However, for $i_L < 0$ in the O^{T1} state, the current continues to flow through the D1–D2 path as S3 and S5 are still not turned ON, and hence, the converter output voltage will be $V_{\rm dc}/2$. It is clear from above that in this delay state (O^{T1}), the converter output voltage will be zero for $i_L > 0$ and $V_{\rm dc}/2$ for $i_L < 0$. It is also to be noted here that as S1 is turned OFF at the beginning of the O^{T1} state, for $i_L < 0$, the current majorly flows through the body diode D1 rather than through the channel of the SiC MOSFET S1. This causes an increased voltage drop due to a relatively higher ON-state drop of the body diode D1. Thus, the time duration for the operating state O^{T1} needs to be as small as possible for keeping the conduction loss in D1 limited for $i_L < 0$, and at the same time, it should be large enough to ensure turning OFF of S1 for avoiding the short-circuit occurrence, as discussed above.

Now, with the change of the converter operating state from O^{T1} to O^P, switches S5 and S3 are turned ON while the other switch states remain unchanged. This allows the parallel conduction paths through switches S5-S2 and S6-S3, as shown in Fig. 5(c). In this state, for $i_L > 0$, S5 and S3 achieve zero-voltage turn-ON as their corresponding antiparallel diodes (D5 and D3) were conducting in the O^{T1} operating state. On the other hand, for $i_L < 0$, the switches S5 and S3 do not achieve zero-voltage turn-ON. Nonetheless, they have to carry only half of the load current at their turn-ON instant in this state for $i_L < 0$ and, hence, incur lower switching losses. It is to be noted that the aforediscussed $i_L > 0$ and $i_L < 0$ conditions for the positive half of the fundamental cycle operation represent the unity power factor (upf) and non-upf loading conditions, respectively. Thus, it is clear from the discussion presented above that the Si IGBTs in the E-HANPC converter has nonzero switching losses at non-upf operation, while they have nearly zero losses for upf operation.

2) *O^P-O^{T1}-P transition*: In the O^P state, as stated above, there are two parallel conduction paths as S2, S3, S5, and S6 are all turned-ON. For the same reason as explained earlier, the delay-state O^{T1} is first introduced in the process of transitioning from the operating state O^P to P. Hence, the switches S5 and S3 are turned-OFF [see Fig. 5(b)]. In the same manner as explained above, the turning OFF of S5 and S3 occurs at zero voltage for $i_L > 0$ (as D5 and D3 were conducting in the O^P state). Similarly, for $i_L < 0$, S5 and S3 have to carry only half of the load current at their turn-OFF instant. Then, the converter transits to the P state by turning-ON S1 while keeping the other switch states unchanged. During this transition, for $i_L > 0$, the current commutates from the two parallel paths (D5-S2 and S6-D3) to S1. It is to be noted here that before S1 gets turned-ON, the Si diodes D3 and D5 were carrying current along with the Si IGBTs S2 and S6. In the process of current commutation from D3, D5 to S1, these Si diodes (D3, D5) undergo reverse-recovery. The reverse recovery current due to D5 flows through the path D5-$C_{\rm d1}$-S1, while that due to D3 flows through the path D3-D6-$C_{\rm d1}$-S1-S2. Thus, for $i_L > 0$, during its turn-ON event, the switch S1 carries the reverse recovery currents of diodes D3 and D5. This may lead to increased turn-ON losses of S1. However, in the proposed converter, the switch S1 being a SiC MOSFET, has substantially lower turn-ON time. Therefore, the voltage across S1 falls to zero almost instantaneously during the afore-mentioned transition from the O^{T1} to P state, and hence, the reverse recovery currents of D3 and D5 have a lesser effect on the turn-ON losses of S1. In contrast, for the cases where S1 is a Si switch, the reverse recovery currents due to D3 and D5 would have caused larger losses during the turn-ON event of S1. Furthermore, for $i_L < 0$, the current gets commutated from two parallel paths (D2-S5 and S3-D6) in the O^P state to D1 in the O^{T1} state. This is achieved by turning-OFF S3, S5 while the other switch

states remain unchanged, and hence, the current now flows through D1, D2. This change of the current path involves the current commutation from the Si diode D6. However, since the antiparallel body-diode D1 starts conducting that has almost negligible turn-ON losses, the reverse recovery effect due to D6 would be minimum in this case too.

In the fundamental negative half-cycle, the proposed converter operation can be similarly explained by considering the transitions N-O^{T2}-O^{N} and O^{N}-O^{T2}-N. The corresponding equivalent circuits illustrating the switching states and conduction paths are shown in Fig. 5(d)–(f).

This section has presented a new modulation scheme for the E-HANPC converter, which enables it to operate with lower losses by effectively utilizing both the Si and SiC switches.

In the following sections, the proposed converter is further analyzed in terms of the conduction and switching losses, optimized loss distribution amongst the converter switches, and the effect of the commutation path. For the comparative analysis, the existing HANPC topology [15] is considered as the base case as this topology, like the E-HANPC topology, also utilizes only two SiC MOSFETs per phase-leg in the ANPC structure.

III. Loss Analysis of the E-HANPC Topology

The proposed E-HANPC converter topology allows the optimized loss distribution among the converter switches with the objective of enhancing the converter power handling capability. This is accomplished by using the proposed modulation scheme discussed in the previous section, which optimizes both the conduction and switching losses for the converter switches. The effect of the proposed modulation scheme on the overall converter loss is evaluated by modeling the device losses in the following sections.

A. Modeling of Conduction Losses

As discussed earlier, the proposed modulation scheme enables the parallel conduction path during the null operating states to reduce the conduction losses of the converter. This results in enhanced efficiency and also helps in achieving higher power handling capability of the E-HANPC converter.

The conduction loss (P_c) of the E-HANPC converter can be calculated by evaluating losses of the devices in the conduction paths in each operating state, as per Fig. 5(a)–(f). Considering the positive half of the fundamental cycle, the conduction loss of the E-HANPC converter ($P_{c(E)}$) can be given, as in the following:

$$P_{c(E)} = P_{c(P\text{ state})} + P_{c(O^P\text{state})} \tag{1}$$

where

$$P_{c(P\text{ state})} = \underbrace{P_{c(S1)} + P_{c(S2)}}_{i_L>0} + \underbrace{P_{c(D1)} + P_{c(D2)}}_{i_L<0} \tag{2}$$

$$P_{c(O^P\text{ state})} = \underbrace{P_{c(S2)} + P_{c(D3)} + P_{c(D5)} + P_{c(S6)}}_{i_L>0} + \underbrace{P_{c(D2)} + P_{c(S3)} + P_{c(S5)} + P_{c(D6)}}_{i_L<0}. \tag{3}$$

In the abovementioned equations, the conduction losses (P_c) in SiC MOSFET (P_{c_mosfet}), Si IGBT (P_{c_igbt}), and Si antiparallel diode (P_{c_diode}) can be evaluated using (11)–(17), as expressed in the Appendix. Therefore, using (1)–(3) and the equations provided in Appendix, the conduction losses in the E-HANPC converter can be expressed as in the following:

$$P_{c(E)} = \left\{ \begin{array}{l} \left(\begin{array}{l} r_{\text{ds}} i_{sr}^2 + v_{ce0} i_{sa} + r_{ce} i_{sr}^2 + v_{ce0} \underline{i_{sa}} \\ + 0.5 r_{ce} \underline{i_{sr}^2} + v_{d0} \underline{i_{sa}} + 0.5 r_d \underline{i_{sr}^2} \end{array} \right)_{i_L>0} \\ + \left(\begin{array}{l} r_{\text{ds}} i_{sr}^2 + v_{d0} i_{sa} + r_d i_{sr}^2 + v_{ce0} \underline{i_{sa}} \\ + 0.5 r_{ce} \underline{i_{sr}^2} + v_{d0} \underline{i_{sa}} + 0.5 r_d \underline{i_{sr}^2} \end{array} \right)_{i_L<0} \end{array} \right\}. \tag{4}$$

As discussed earlier, for comparative evaluation, the HANPC topology [see Fig. 1(c)] is considered as the base case, and hence, its conduction loss is also evaluated for similar operating conditions. From [15] and Fig. 1(c), in the HANPC converter, the switching state of devices differs from that in the E-HANPC converter topology only in the null state. In the null state of E-HANPC topology, two Si diodes and two Si IGBTs conduct in the parallel conduction path for both $i_L > 0$ and $i_L < 0$, as discussed earlier. In contrast, in the null state of HANPC topology, one SiC body-diode and one Si IGBT conduct for $i_L > 0$, while one SiC MOSFET and one Si diode conduct for $i_L < 0$ in a given fundamental positive half-cycle. Thus, the HANPC converter conduction loss ($P_{c(H)}$) expression can be derived in a similar manner, as described above. The resulting expression of $P_{c(H)}$ is given in the following:

$$\mathrm{P}_{c(H)} = \left\{ \begin{array}{l} \left(\begin{array}{l} r_{\text{ds}} i_{sr}^2 + v_{ce0} i_{sa} + r_{ce} i_{sr}^2 \\ + v_{ce0} \underline{i_{sa}} + r_{ce} \underline{i_{sr}^2} + r_{\text{ds}} \underline{i_{sr}^2} \end{array} \right)_{i_L>0} \\ + \left(\begin{array}{l} v_{d0} i_{sa} + r_d i_{sr}^2 + r_{\text{ds}} i_{sr}^2 \\ + r_{\text{ds}} \underline{i_{sr}^2} + v_{d0} \underline{i_{sa}} + r_d \underline{i_{sr}^2} \end{array} \right)_{i_L<0} \end{array} \right\} \tag{5}$$

It is to be noted that the conduction paths in both the HANPC-1 and HANPC converters involve similar devices as can be observed from Fig. 1(c)–(f). Therefore, the conduction losses for the HANPC-1 converter ($P_{c(H\text{-}1)}$) can also be computed as in the following equation using (5):

$$P_{c(H-1)} = P_{c(H)}. \tag{6}$$

Furthermore, for the AANPC converter [see Fig. 1(a)], the conduction paths during an active state involve two SiC MOSFETs for $i_L > 0$, while two SiC diodes for $i_L < 0$. Similarly, for the null state, the conduction paths involve two parallel paths with one SiC diode and one SiC MOSFET in each of them. Therefore, the AANPC converter conduction loss ($P_{c(A)}$) expression can be derived in a similar manner, as explained above. The resulting expression of $P_{c(A)}$ is given in the following:

$$P_{c(A)} = \left\{ \begin{array}{l} \left(2 r_{\text{ds}} i_{sr}^2 + 0.5 r_{\text{ds}} \underline{i_{sr}^2} + 0.5 r_d \underline{i_{sr}^2} \right)_{i_L>0} \\ + \left(2 r_{\text{ds}} i_{sr}^2 + 0.5 r_{\text{ds}} \underline{i_{sr}^2} + 0.5 r_d \underline{i_{sr}^2} \right)_{i_L<0} \end{array} \right\}. \tag{7}$$

B. Modeling of Switching Losses

The converter switching losses involve turn-ON and turn-OFF losses of the SiC MOSFETs, Si IGBTs, and the reverse recovery

TABLE II
PARAMETERS FOR SIMULATION AND ANALYTICAL STUDY

Parameters	Value
DC-link voltage (V_{dc})	1500 V
AC output voltage (v_0)	450 V
Rated current (I_0)	25 A
Switching frequency (f_{sw})	40 kHz
Rated power ($P_{0\ \text{rated}}$)	11.25 kW
SiC MOSFET: C2M0080120D	1200V, 36A
Si IGBT: FGH15T120SMD	1200V, 30A

losses of the Si antiparallel diodes. The turn-ON and OFF losses of the active switches (P_{on} and P_{off}) and the reverse recovery losses of the Si antiparallel diodes (P_{rr}) can be modeled for the given rms load current $i_{L(\text{rms})}$ and the voltage across the switch or blocking voltage of the diode v_t at which the losses are already known as in the following equations, respectively [24], [25]:

$$P_{\text{on}} = \frac{0.5V_{\text{dc}}}{v_t T_s}\left(k_1 i^3_{L(\text{rms})} + k_2 i^2_{L(\text{rms})} + k_3 i_{L(\text{rms})}\right) \quad (8)$$

$$P_{\text{off}} = \frac{0.5V_{\text{dc}}}{v_t T_s}\left(k_4 i^3_{L(\text{rms})} + k_5 i^2_{L(\text{rms})} + k_6 i_{L(\text{rms})}\right) \quad (9)$$

$$P_{rr} = \frac{0.5V_{\text{dc}}}{v_t T_s}\left(k_7 i^3_{L(\text{rms})} + k_8 i^2_{L(\text{rms})} + k_9 i_{L(\text{rms})}\right) \quad (10)$$

where V_{dc} is the converter dc-link voltage and T_s is the switching time. The constants k_1, k_2, k_3, k_4, k_5, k_6, k_7, k_8, and k_9 are the curve fitting constants obtained by fitting the curve of the energy loss data available from the datasheet of the respective switching devices.

In this way, the device losses associated with the converter switches can be calculated. In the following section, the above-mentioned equations are used to compute the losses of the converter switches for further analysis.

IV. ANALYTICAL AND SIMULATION RESULTS

A. Results of Device Losses

In the E-HANPC converter, the proposed modulation technique enables a reduction in device losses. To analyze this, the conduction and switching losses of the E-HANPC converter are determined using (4) and (8)–(10), respectively, for the circuit parameters listed in Table II. Similarly, for the comparative analysis, the losses for the HANPC, HANPC-1, and AANPC converter topologies are also determined using (5)–(10). These losses are evaluated at the rated current for the four operating cases, where the combination of two different modulation indices (m_a) and load power factor (pf) values are considered, as shown in Fig. 6.

As can be observed from Fig. 6, the conduction losses in the E-HANPC converter are lower than those in the HANPC and HANPC-1 converters for all of the considered operating cases. As illustrated in Fig. 6(a), the switching losses in the E-HANPC converter are slightly higher than in the others due to the reverse recovery losses in the Si antiparallel diodes. However, the E-HANPC converter has the lowest conduction losses due to the optimal utilization of SiC MOSFETs and the implemented parallel conduction paths, as discussed before. As the conduction losses are the dominant component of total losses, the E-HANPC converter achieves the lowest losses for rated power operation [see Fig. 6(a)]. Moreover, for the lower m_a value, the duration for which the converter operates in the null state increases. As the parallel conduction paths get enabled in the null state operation of the E-HANPC converter, it achieves further reduced conduction losses for case-2 compared to case-1, as can be seen from Fig. 6(b).

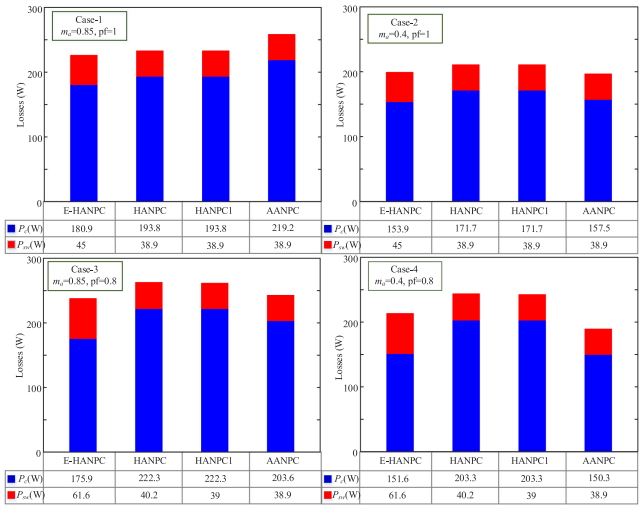

Fig. 6. Calculated values of the switching device losses for the E-HANPC, HANPC [15], HANPC-1 [14], and AANPC [7] converters operating at four conditions. (Parameters: $i_0 = 25$A, $f_{\text{sw}} = 40$ kHz, $T_{\text{amb}} = 25$ °C).

It can further be observed from Fig. 6(c) and (d) that the switching losses of the E-HANPC converter for non- upf operation are more than that for the upf operating conditions, while the switching losses in the HANPC and HANPC-1 converters remain nearly same. The increment in the switching losses in the E-HANPC converter for non-upf operation is due to the switching of Si IGBTs at finite values of voltage and currents for non-upf operation, as discussed earlier in Section II. Nonetheless, even for such cases (Cases 3 and 4), the total device losses in the E-HANPC converter are still lesser than in the HANPC and HANPC-1 [14] converters due to the significant reduction in the conduction losses of the E-HANPC converter, as can be observed from Fig. 6(c) and (d). Thus, the E-HANPC converter with the proposed modulation scheme achieves higher efficiency over the HANPC and HANPC-1 converters.

Furthermore, as can be observed from Fig. 6(a), the conduction losses in the AANPC converter are highest. This is due to the higher ON-state drop in the SiC MOSFETs compared to that in the Si IGBTs for rated power operation [16]. However, the AANPC converter achieves reduced conduction losses for lagging power factor operating conditions because of the parallel operation of SiC MOSFETs in the null state [7]. Moreover, as the Si IGBTs in the E-HANPC converter experience nonzero switching losses at non-upf operation, it has slightly higher losses than the AANPC converter [see Fig. 6(d)]. Therefore, compared to the AANPC converter, the proposed E-HANPC converter would be more suitable for the applications where the operating power

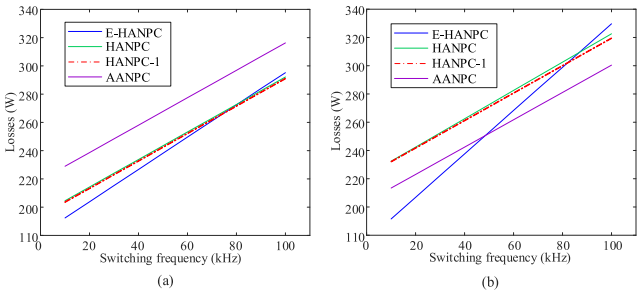

Fig. 7. Plots for the device loss values plotted for various values of switching frequencies of the E-HANPC, HANPC [15], HANPC-1 [14], and AANPC [7] converters operating at (a) upf and (b) 0.8 lagging pf loading conditions. (Parameters: $i_0 = 25$ A, $f_{\rm sw} = 40$ kHz, $T_{\rm amb} = 25$ °C).

factor values remain mostly close to unity. On the other hand, for non-upf conditions, compared to the AANPC converter, the E-HANPC converter can still achieve better performance up to the switching frequency value for which the increased switching losses dominate the reduced conduction losses. Therefore, to analyze the performance of the proposed converter for a wide range of switching frequencies, the losses in the aforediscussed converters are computed for varying switching frequency values, and the results are shown in Fig. 7(a) and (b) for unity and 0.8 lagging power factors, respectively. For this, the rated power operation as per Table II is considered and the converter losses are evaluated as per (4)–(10) with $m_a = 0.85$.

As can be observed from Fig. 7(a), the AANPC converter has relatively higher losses for upf operation compared to the other considered hybrid topologies for a wide range of switching frequency values. The AANPC topology has all switches as SiC MOSFETs, and hence, its conduction losses are higher compared to the hybrid topologies. Furthermore, among the hybrid configurations, the E-HANPC converter has the least losses up to 80-kHz switching frequency. However, as the reverse recovery losses in the E-HANPC converter increase with increase in the switching frequency, its losses become higher than the HANPC and HANPC-1 converters beyond 80 kHz. The HANPC and HANPC-1 converters have nearly the same losses as their conduction losses are equal and both have similar switching events for upf condition [see Fig. 1(c)–(f)]. On the other hand, for non-upf operation [see Fig. 7(b)], the HANPC-1 converter incurs slightly reduced losses than the HANPC converter due to the relatively reduced reverse recovery losses. However, the conduction losses in these converters increase significantly for non-upf condition, due to the relatively higher conduction losses in the diodes. Therefore, the E-HANPC converter still offers lower losses compared to HANPC and HANPC-1 converters for the switching frequencies below 85 kHz, as can be seen from Fig. 7(b). It is to be noted that the E-HANPC converter experiences nonzero switching losses for non-upf operation. Therefore, as can be seen in Fig. 7(a) and (b), the rate at which the losses increase is relatively higher for non-upf compared to upf operating conditions. Moreover, as the losses in the AANPC converter are also reduced for non-upf operation, as discussed before, the E-HANPC converter losses become higher than the AANPC converter losses beyond 50-kHz switching frequency.

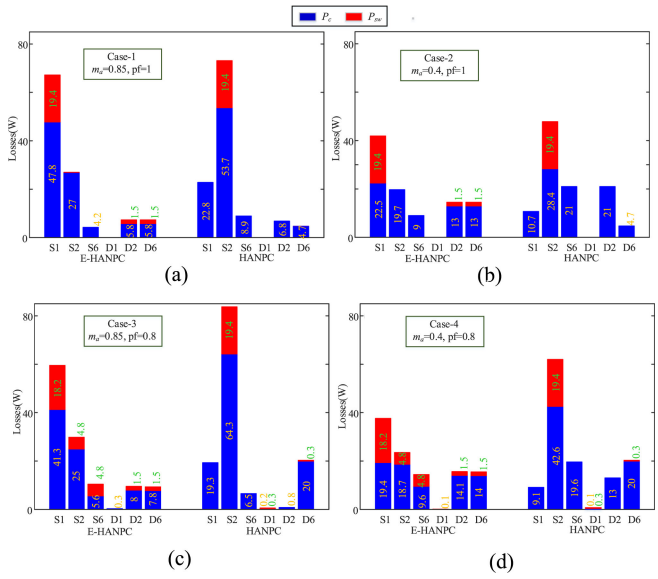

Fig. 8. Distribution of the losses among the switching devices of the E-HANPC and HANPC converters operating at four cases. (a) $m_a = 0.85$, pf $= 1$, (b) $m_a = 0.4$, pf $= 1$, (c) $m_a = 0.85$, pf $= 0.8$ lag, and (d) $m_a = 0.4$, pf $= 0.8$ lag. (Conditions: $i_0 = 25$ A, $f_{\rm sw} = 40$ kHz, $T_{\rm amb} = 25$ °C).

It can be concluded from the discussion presented above that the E-HANPC converter incurs relatively lower losses for a broader range of switching frequency values. This results in reduced converter size due to the reduced heat-sink volume requirement in the E-HANPC converter [26]. Therefore, considering the overall performance and the reduced cost, the E-HANPC converter can be preferred for wide operating conditions over the other existing aforediscussed converters. The effect of the proposed modulation scheme on the loss distribution among the converter switches is analyzed in the following section.

B. Loss Distribution in E-HANPC Converter Switches

The maximum power handling capability of the converter depends on the switch, which is highly stressed [1]. As discussed before (see Section II), using the proposed modulation scheme, the losses can be optimally distributed among the E-HANPC converter switches, which helps in enhancing the maximum power handling capability of the converter. The loss distribution in the proposed converter is analyzed by evaluating the losses in the converter switches over a fundamental cycle, and the results are plotted in Fig. 8. Furthermore, for comparative analysis, the device losses of the HANPC converter are also evaluated considering the similar SiC device count as that of the E-HANPC converter and are plotted in Fig. 8. In Fig. 8(a)–(d), the losses in three switches (S1, S2, and S6) and respective diodes (D1, D2, and D6) of the E-HANPC converter are illustrated for four different operating cases. The loss values of remaining switches: S3, S4, and S5 and their respective diodes can be similarly evaluated, which will be the same as that of S2, S1, and S5, respectively (see Fig. 3).

As can be seen from Fig. 8(a), for $m_a = 0.85$ at upf operation in the E-HANPC converter, S1 incurs the highest losses amongst

all the converter switches. It can also be seen that the conduction loss is the dominant loss component in S1. This is attributed to the higher ON state losses of SiC MOSFET compared to the Si IGBT for similar device ratings. On the other hand, for the HANPC converter, switch S2 (SiC MOSFET) is the most highly stressed switch. It can further be observed that the losses associated with S2 in the HANPC converter are higher than that in S1 of the E-HANPC converter [see Fig. 8(a)]. This is due to the fact that in the E-HANPC converter S1 conducts only in the positive half of the fundamental cycle (see Fig. 3), whereas the switch S2 in the HANPC converter conducts over the full fundamental cycle [see Fig. 1(f)].

For a lower value of $\mathrm{m_a}$ ($m_a = 0.4$) in Fig. 8(b), the losses in S1 of the E-HANPC topology further reduces. This is due to the smaller conduction period of S1, as the duration for which the converter operates in the active state (P) is reduced for lower values of m_a. Furthermore, for lower pf loading conditions, the switches S2 and S6 (Si IGBTs) of the E-HANPC topology experience finite switching losses, as can be seen in Fig. 8(c) and (d). These switching losses occur at half of the load current value because of the parallel conduction paths, as discussed before and, therefore, are having lower values. Although these losses are not observed in the HANPC converter [see Fig. 8(c) and (d)], the conduction loss reduction is a dominant factor that results in lower overall losses in the E-HANPC converter.

It can be observed from Fig. 8(a)–(d) that the maximum stressed switch in the E-HANPC converter has 8%, 12%, 29%, and 40%, respectively, lower losses than the losses occurring in the most stressed switch of the HANPC converter depending on the operating conditions. This difference in the losses causes the corresponding difference in the junction temperatures of the converter switches [21]. This results in the enhanced power handling capability for the proposed converter.

In addition to the optimal distribution of losses in the switching devices, the proposed converter also offers a short-length commutation loop for the commutation of fast switching SiC MOSFETs that results in lower peak values of the voltage overshoots. The following section discusses this effect of the commutation loop on the switching behavior of the SiC MOSFET in the proposed topology.

C. Effect of the Commutation Loop

In the SiC-MOSFET-based converters, the large commutation loop limits the switching speed due to high voltage stress on these switching devices [19]. As the SiC MOSFETs have very small switching times, it causes a high overvoltage spike during the turn-OFF event due to the parasitic inductance of its commutation path. This may lead to device degradation or even a failure. Thus, the effect of the commutation path needs to be analyzed for the considered converter in deciding its maximum switching speed and voltage blocking capability.

The possible commutation paths during the operation in positive half of the fundamental cycle for the HANPC and E-HANPC converters are shown in Fig. 9(a) and (b), respectively. The commutation event during the change of state from P to O^P is considered. In the HANPC converter, S2 is turned OFF while S3

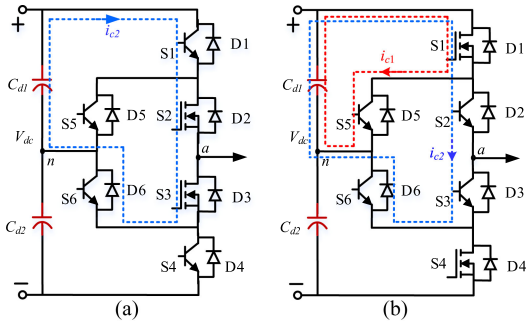

Fig. 9. Representation of the commutation paths in (a) HANPC and (b) E-HANPC topologies for the operation in the positive half of the fundamental cycle.

is turned ON with sufficient delay time. The commutation path for this transition is through S1, S2, S3, and D6, as shown in Fig. 9(a) [19]. On the other hand, for the E-HANPC converter, during this transition, S1 is given the turn-OFF signal, while S3 and S5 are turned-ON with the dead-time provided by the delay-state O^{T1} (Fig. 4), and thus, the current through S1 gets transferred to the available freewheeling paths. As S2 is gated, D5 gets forward biased and, thus, carries half of the current of S1, which is the first freewheeling path. Similarly, as S6 is also ON, D3 gets forward biased and allows the second freewheeling path. During this process, the current through S1 gets commutated to two different commutation paths, as indicated in Fig. 9(b). As can be seen from Fig. 9(b), for the first commutation path (c1), the commutation current (i_{c1}) flows through C_{d1}, S1, and S5. Similarly, for the second commutation path (c2), the commutation current (i_{c2}) flows through C_{d1}, S1, S2, S3, and D6. As also can be seen, the commutation path for i_{c1} is shorter than that for i_{c2}. The c1 being a shorter loop will have smaller inductance than that of c2. As both of the loops are in parallel, the resultant parasitic loop inductance is reduced in the E-HANPC topology. This leads to lower turn-OFF overvoltage peaks in the E-HANPC converter compared to that in the HANPC converter where only longer commutation loop is possible, as can be seen in Fig. 9(a).

The effect of commutation loop inductance on the switching event of SiC MOSFET in the E-HANPC converter is analyzed using the simulation studies with the parameters listed in Table II. For comparison, the HANPC converter model is also simulated. Since these models need the information of the loop inductances, an impedance analyzer is used to measure the loop inductances for the constructed prototypes (see Fig. 11) [27]. For this, the drain and source terminals of SiC MOSFETs, and collector and emitter terminals of the Si IGBTs are shorted using an external conductor with negligible resistance. The impedance analyzer is connected between the positive half of the dc-link by disconnecting the dc-link capacitors. The measured values of these loop inductances for c1 and c2 comes out to be 335 and 486 nH, respectively. As can be observed, these values are relatively higher as the developed converter prototype is not an optimized design. In a well-designed system, the commutation loop inductance values will be lower. Nonetheless, the loop inductance of the c1 path will always be smaller than that of the c2 path. Furthermore, it is to be noted that the HANPC

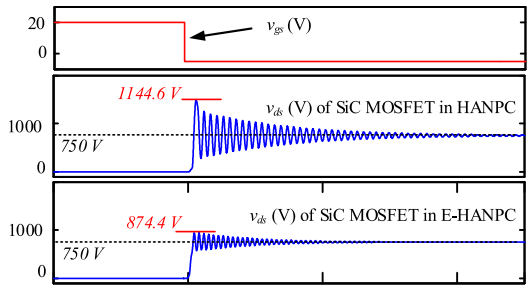

Fig. 10. Simulation results of the drain to source overvoltage peaks representing the turn-OFF events of the SiC MOSFET in the HANPC and E-HANPC converters for the parameters from Table II.

TABLE III
PARAMETERS FOR EXPERIMENTAL VALIDATION

Parameters	Value
DC-link voltage (V_{dc})	500 V
AC output voltage (V_{ac})	150 V
Rated current (I_{ac})	15 A
Switching frequency	20 kHz
Rated power	2.25 kW
SiC MOSFET: C2M0080120D	1200V, 36A
Si IGBT: FGH15T120SMD	1200V, 30A

converter only has a larger commutation loop for the SiC MOSFET S2 [see Fig. 9(a)] [19]. Since both converter prototypes are designed with identical PCB layouts and similar devices, the loop inductance value for the HANPC converter is the same as that of the c2 loop of the E-HANPC converter, as mentioned before.

Using the obtained loop inductance values, the turn-OFF switching transient equivalent models for the E-HANPC and HANPC converter are simulated and the voltage waveforms are shown in Fig. 10. As can be seen from the simulation results shown in Fig. 10 that the SiC MOSFET (S1) of the E-HANPC converter has the peak overvoltage value of only 874.4 V. On the other hand, the SiC MOSFET (S2) of the HANPC converter has the peak overvoltage value of 1144.6 V. This shows that the SiC MOSFET in the E-HANPC converter has around 24% less overvoltage peak than that in the HANPC converter. Therefore, the device stress in the E-HANPC converter is lower. Thus, the E-HANPC converter can be used with higher dc-link voltages than that in the HANPC converter.

V. EXPERIMENTAL RESULTS AND VALIDATION

To validate the principles presented above and also to reconfirm the analytical and simulation results obtained in the previous section, experimental studies are carried out with the parameters listed in Table III. The laboratory prototypes of one phase leg of the E-HANPC, HANPC, and HANPC-1 converters are constructed. It is to be noted that these developed prototypes are not the optimized designs, but they represent the simplified scaled-down setups to prove the operating principles discussed in the earlier sections. Furthermore, all the developed prototypes use identical PCB structures, dc-link bus bars, and passive components. Therefore, all of the observations presented below

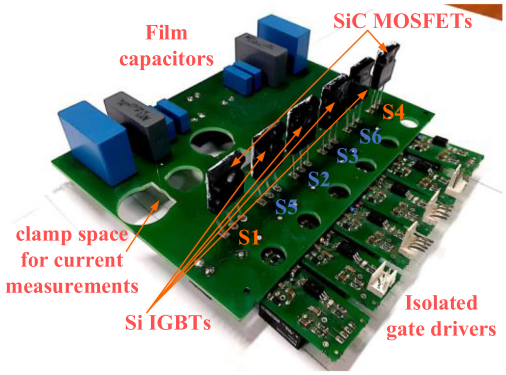

Fig. 11. Hardware prototype of the single-phase leg for the proposed E-HANPC converter showing the device arrangements with the isolated gate drivers.

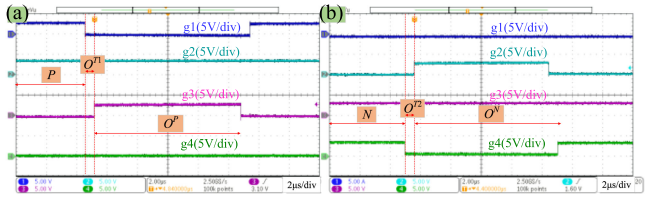

Fig. 12. Experimental waveforms of gating pulses obtained using the proposed modulation scheme showing the states of S1, S2, S3, and S4 switches in (a) positive and (b) negative halves of the fundamental cycle.

are obtained at similar operating conditions. Fig. 11 shows the experimental prototype of the E-HANPC converter, where S1 and S4 are the SiC MOSFETs, while S2, S3, S5, and S6 are the state-of-the-art Si IGBTs with negligible tail current values [28]. All of the switches of the converter use isolated gate drivers with the gate resistances of 15 and 30 Ω for SiC MOSFETs and Si IGBTs, respectively. All the experiments are carried out with the dc-link voltage of 500 V, which is obtained using the Keysight make N8949A dc power supply. Texas instrument's dual-core DSP TMS320F28379D is used to generate the gating pulses. Furthermore, Tektronix make MDO 3014 oscilloscope is used for the waveform measurements while the efficiency determination is done using the Yokogawa make DL850E scopecorder. The switch current waveforms are measured using the Yokogawa make high-bandwidth current probes for which the special clamping arrangement is made, as can be seen in Fig. 11.

Fig. 12(a) and (b) shows the gating pulses of S1, S2, S3, and S4 in the positive and negative halves of the fundamental cycle, respectively, using the proposed modulation scheme. As discussed earlier, the pulses for the remaining switches S5 and S6 will be similar to that of S3 and S2, respectively, (see Fig. 3). As can be observed from Fig. 12(a) and (b) that the delay-states O^{T1} and O^{T2} are applied during the transition from active to null states and vice versa. This enables safe switching of the combination of Si and SiC switches in the E-HANPC converter without the occurrence of a short circuit, as explained earlier. The experimental waveforms of the output voltage v_0, load current i_0, and dc-link voltage v_{dc} for the E-HANPC converter are shown

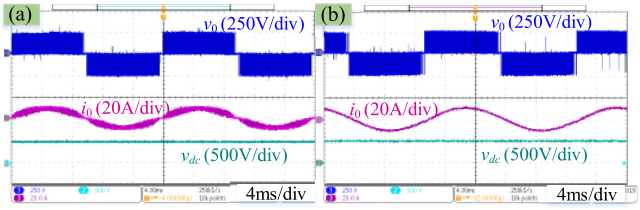

Fig. 13. Experimental waveforms for the output voltage (v_0), load current (i_0), and dc-link voltage (V_{dc}) of the proposed E-HANPC converter prototype operating at (a) upf load, and (b) non-upf load conditions.

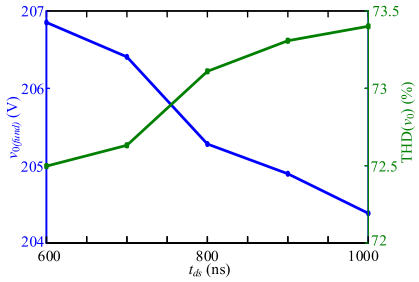

Fig. 14. Experimental results of the effect of variation in t_{ds} on the v_0(fund) and THD(v_0) in the proposed E-HANPC converter.

in Fig. 13(a) and (b) for upf and non-upf operation, respectively. It can be seen that the output phase voltage has three-levels as $+v_{dc}/2$, 0 and $-v_{dc}/2$. These waveforms show that the proposed converter can be effectively operated for different pf loading conditions using the proposed modulation scheme.

To analyze the effect of the delay-states on the output voltage of the proposed converter, experiments are performed to obtain the fundamental component of output voltage $v_{0\,(\mathrm{fund})}$ and its total harmonic distortion [THD(v_0)]. For this, the duration of the delay-states (t_{ds}) is varied and the output voltage waveform is recorded. The obtained values of $v_{0\,(\mathrm{fund})}$ and THD(v_0) are shown in Fig. 14. As can be seen from Fig. 14 that the THD(v_0) increases with t_{ds} due to the reduction in the $v_{0\,(\mathrm{fund})}$ component. This happens because, with the increase in the t_{ds} value, the duration of the active states reduces, which leads to lower $v_{0\,(\mathrm{fund})}$ values. Hence, in order to minimize the effect of the delay-states on the $v_{0\,(\mathrm{fund})}$ value, an optimum value of t_{ds} can be selected to enable safe operation of the Si and SiC switches with the least effect on the output voltage value.

Furthermore, for validating the effect of the loop inductance on the switching transition of the SiC MOSFET, experiments are performed to measure the switching voltage and current waveforms for the SiC MOSFETs in the E-HANPC and HANPC converters. To reverify the effect of loop inductance, the simulations are repeated with the same circuit parameters and at the same operating conditions as that of the experiments (see Table III). The obtained turn-OFF switching waveforms for the E-HANPC and HANPC converters are shown in Fig. 15(a)–(d) for both experimental and simulation results.

From the experimental results of the E-HANPC converter in Fig. 15(a), it can be observed that with the application of the turn-OFF signal, the drain to source voltage of S1 (SiC MOSFET)

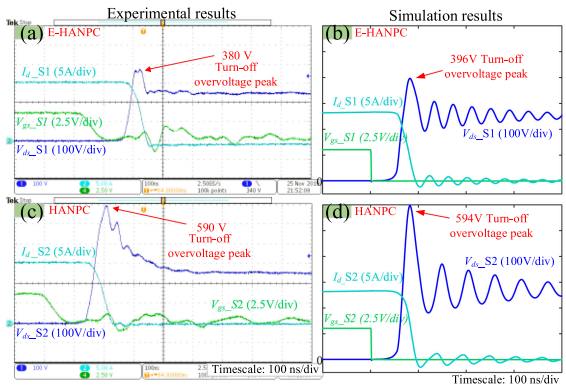

Fig. 15. Comparison of the switching waveforms during the turn-OFF switching event of the SiC MOSFET for (a) E-HANPC and (b) HANPC converters using the experimental prototypes and (c) E-HANPC and (d) HANPC converters using the simulation models for the circuit parameters as per Table III.

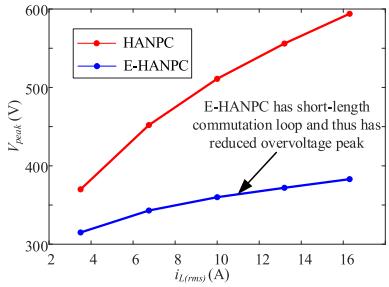

Fig. 16. Comparison of the turn-OFF overvoltage peak for the SiC MOSFET in the HANPC and E-HANPC topologies for variation in the load current.

increases and the device current falls. The observed peak of the drain to source voltage in the E-HANPC converter for S1 is 380 V. On the other hand, for the HANPC topology, the similar experiment results in 590 V as the peak value of the drain to source voltage for S2 (SiC MOSFET), as shown in Fig. 15(b). As can also be observed, the simulation results from Fig. 15(c) and (d) are in agreement with the respective experimental results. The slight difference in the turn-OFF overvoltage peak values between the simulated and experimental results is due to the difference in the measured and actual values of the loop inductances. Furthermore, the unaccounted resistance from the PCB path results in higher oscillations in the simulated waveforms. The aforediscussed results from Fig. 15(a)–(d) show that the overvoltage peak for the SiC MOSFET is around 35% lower for the E-HANPC converter compared to that for the HANPC converter. This clearly shows that the voltage stress across the SiC switch in the E-HANPC converter is lower compared to that in the HANPC converter. This is because of the availability of the short commutation loop in the proposed converter, as discussed earlier. The simulation results performed at two operating conditions [see Figs. 10 and 15(c)–(d)] and the aforediscussed experimental results confirm the efficacy of the proposed topology and modulation scheme.

Moreover, the turn-OFF overvoltage peak values are also measured for variation in the load current and are shown in Fig. 16 for the E-HANPC and HANPC converters. As can be observed

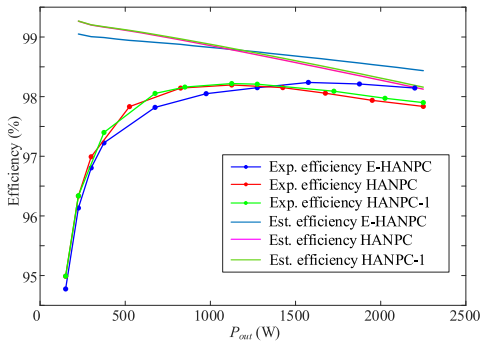

Fig. 17. Comparison of the efficiency values for the E-HANPC converter with the existing HANPC [15] and HANPC-1 [14] converters using the experimental and estimated results at upf loading condition.

from Fig. 16, the SiC MOSFET in the E-HANPC converter has relatively lower turn-OFF overvoltage peak (V_{peak}) values for all load current values. The rate of rise of overvoltage peak values with load current is higher for the HANPC converter due to the higher value of commutation loop inductance, as discussed before. These results show that the SiC MOSFETs in the E-HANPC topology have relatively lower switching stress compared to the HANPC converter.

In addition to the lesser overvoltage stresses, the proposed topology can also achieve lower device losses by using the proposed modulation scheme. The experimental validation for reduced converter losses is performed by determining the efficiency of the constructed prototypes. For this, the experiments are performed for different output power values (P_{out}) with the parameters listed in Table III. The measured efficiency values are plotted in Fig. 17 for the HANPC [15], HANPC-1 [14], and the proposed E-HANPC converters for upf loading conditions. Furthermore, the estimated efficiency values of these converters considering only the device losses are also shown. It is to be noted that the estimated efficiencies are higher than the experimentally measured efficiency values, which is mainly because of the losses in the passive components of the converter. Moreover, as can also be seen from Fig. 17, the natures of the estimated and experimental results are similar with a slight deviation in the crossover point.

Furthermore, as can be seen from both the estimated and experimental results in Fig. 17 that the E-HANPC converter has a relatively lower efficiency for lower output power values (P_{out}). This is attributed to the relatively higher ON-state voltage drop in the null state of the E-HANPC converter compared to that in the HANPC and HANPC-1 converters for lower output power values. In the E-HANPC converter, the Si antiparallel diode in the conduction path during the null state has a relatively higher ON-state drop for low current values compared to the SiC MOSFETs in the HANPC and HANPC-1 converters. However, the ohmic drop in the SiC MOSFETs of the HANPC and HANPC-1 converters increases more with the load current compared to that in the Si diodes of the E-HANPC converter. Also, as the conduction losses become the dominating loss component for the increased P_{out} values for the considered medium frequency operation, the loss reduction due to the parallel conduction paths in the E-HANPC converter dominates. Because of these reasons, the E-HANPC converter efficiency increases compared to the efficiencies of HANPC and HANPC-1 converters for the increased output power values. It is also observed that the efficiency values of the HANPC and HANPC-1 converters are nearly similar for the considered operating conditions, which is in agreement with the analytical results from Section IV-A. Thus, it can be concluded from the analytical, simulation, and experimental studies presented above that the proposed E-HANPC converter can be considered as a viable, efficient, and preferable solution for the medium-power medium-frequency applications.

VI. Conclusion

A three-level E-HANPC converter comprising Si and SiC switches is proposed in this article for medium voltage applications. A new modulation scheme is also proposed for operating the Si and SiC switches in a manner to achieve enhanced power handling capability with high converter efficiency. The analytical and simulation results highlight the efficacy of the E-HANPC converter with the proposed modulation scheme in terms of increased converter efficiency, optimal loss distribution amongst the converter switches, and minimized overvoltage peak values across the SiC MOSFETs. The high efficiency is obtained by reducing the conduction and switching losses of the converter switches. The reduction in the switching losses is achieved by enabling the reduced current switching of the Si IGBTs in the proposed topology, while the conduction losses are reduced by facilitating the parallel conduction paths during the zero states. The analytical modeling of the device losses is carried out, which shows optimally distributed device losses in the converter switches compared to the existing SiC-based HANPC topology. Furthermore, the simulated results show the reduced effect of commutation loop-inductance on the switching behavior of the SiC MOSFET in the proposed converter. This is due to the reduced loop-inductance of the commutation loop of the SiC MOSFETs in the proposed converter, which results in the lower drain to source overvoltage peak across these switches. Therefore, the proposed converter can be used with the higher dc-link voltages for the same device ratings.

A reduced-scale prototype of the proposed E-HANPC converter topology is developed to reconfirm the analytical and simulated results. The prototype is tested for different loading conditions. The experimental results are observed to be in alignment with the analytical and simulation results. Finally, the performance of the proposed converter is compared with the existing HANPC and HANPC-1 topologies using the efficiency values. The proposed E-HANPC converter has given high efficiency at rated output power.

Appendix

The conduction losses (P_c) in the SiC MOSFET ($P_{c\_\text{ mosfet}}$), Si IGBT (P_{c_igbt}), and Si antiparallel diode (P_{c_diode}) can be expressed as in the following equations, respectively [24]:

$$P_{c\_\text{mosfet}} = r_{\text{ds}} \times I^2_{\text{ds(rms)}} \tag{11}$$

$$P_{c\_\text{igbt}} = v_{ce0} \times I_{ce(\text{avg})} + r_{ce} \times I^2_{ce(\text{rms})} \tag{12}$$

$$P_{c\_\text{diode}} = v_{d0} \times I_{d(\text{avg})} + r_d I^2_{d(\text{rms})} \tag{13}$$

where $r_{\mathrm{ds},}$ r_{ce}, and r_d represent the resistances and $I_{\mathrm{ds(rms)}}$, $I_{ce(\mathrm{rms}),}$ and $I_{d(\mathrm{rms})}$ represent the rms currents of the MOSFET, IGBT, and diode, respectively. Furthermore, v_{ce0} and v_{d0} represent the voltage drop corresponding to zero current condition in IGBT and diode, respectively.

It is to be noted that the average and rms values of currents through the switches depend on the load current ($i_{L(t)}$) and the operating state (active or null). In the active state, the average and rms values of current (i_{sa} and i_{sr}) through the switch for the load current with a peak value of I_p can be expressed as in the following equations, respectively [7]:

$$i_{sa} = {}^{1}\!/_{2\pi} \int_0^{\pi} I_p \sin(\omega t - \phi) .m_a \sin(\omega t)\, dt \tag{14}$$

$$i_{sr}^2 = {}^{1}\!/_{2\pi} \int_0^{\pi} I_p^2 \sin^2(\omega t - \phi) .m_a \sin(\omega t)\, dt \tag{15}$$

where ω represents the fundamental frequency in rad/sec, ϕ is the power factor angle, and m_a is the modulation index.

In a similar way, the average and rms values of current through the conducting switch in the null state ($\underline{i_{sa}}$ and $\underline{i_{sr}}$) can be expressed as in the following equations, respectively [7]:

$$\underline{i_{sa}} = {}^{1}\!/_{2\pi} \int_0^{\pi} I_p \sin(\omega t - \phi) .(1 - m_a) \sin(\omega t)\, dt \tag{16}$$

$$\underline{i_{sr}^2} = {}^{1}\!/_{2\pi} \int_0^{\pi} I_p^2 \sin^2(\omega t - \phi) .(1 - m_a) \sin(\omega t)\, dt. \tag{17}$$

Using (12)–(15), the conduction losses in the respective switching devices can be calculated using (11)–(13).

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