

Analytical Derivation of Intersubmodule Active Power Disparity Limits in Modular Multilevel Converter-Based Battery Energy Storage Systems

Gaowen Liang ¹, Student Member, IEEE, Hossein Dehghani Tafti ², Member, IEEE, Glen G. Farivar ³, Senior Member, IEEE, Josep Pou ⁴, Fellow, IEEE, Christopher D. Townsend ⁵, Member, IEEE, Georgios Konstantinou ⁶, Senior Member, IEEE, and Salvador Ceballos

Abstract—Due to a dramatic increase in grid-connected renewable energy resources, energy storage systems are interesting and important for future power systems, among which the modular multilevel converter (MMC)-based battery energy storage systems (BESSs) are one of the most modular, efficient, and flexible topologies. Uneven active power distribution among submodules (SMs) in the arms of an MMC-based BESS is necessary for certain applications. The main contribution of this article is to present a general analysis of the inter-SM active power disparity problem which incorporates the inherent operational constraints of the MMC converter. An analytical method to derive inter-SM active power disparity limits is introduced. The proposed analysis can help facilitate the design of MMC-based BESS for applications such as recycled batteries and hybrid battery chemistries, which can both require significant inter-SM active power disparity. The analysis formulates a criteria vector and criterion value that describes whether an MMC-based BESS is capable of supplying demanded output powers while subject to inter-SM active power disparity. Simulation and experimental results are obtained on a single-phase system with varying numbers of SMs per arm, which verifies the feasibility and generality of the proposed analytical method.

Index Terms—Active power disparity, battery energy storage system (BESS), modular multilevel converter (MMC), operation limit.

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Gaowen Liang and Josep Pou are with the School of Electrical and Electronic Engineering, Nanyang Technological University Singapore 639798, Singapore (e-mail: gaowen001@e.ntu.edu.sg; josep.pou@ieee.org).

Hossein Dehghani Tafti and Georgios Konstantinou are with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW 2052, Australia (e-mail: hossein002@e.ntu.edu.sg; g.konstantinou@unsw.edu.au).

Glen G. Farivar is with the Energy Research Institute, Nanyang Technological University Singapore 639798, Singapore (e-mail: gh_farivar@hotmail.com).

Christopher D. Townsend is with the Department of Electrical, Electronic, and Computer Engineering, The University of Western Australia, Crawley, WA 6009, Australia (e-mail: townsend@ieee.org).

Salvador Ceballos is with Tecnalia, Basque Research and Technology Alliance (BRTA), 48160 Derio, Spain, and also with the Energy Research Institute at Nanyang Technological University Singapore 639798, Singapore (e-mail: salvador.cebillos@tecnalia.com).

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I. INTRODUCTION

DU E to the increase of renewable energy sources [1], energy storage systems (ESSs) are interesting and important for future power system infrastructure [2]. Battery energy storage systems (BESSs) are one of the most popular candidates among the ESS family. Power electronic converters are necessary for the integration of BESS to the grid. Compared to the conventional two-level converters, multilevel converters provide evident advantages, such as modularity, excellent harmonic performance, low switching frequency, etc., especially in medium/high-voltage applications [2]–[5]. Among the large family of multilevel converters, the modular multilevel converter (MMC) and cascaded H-bridge converter (CHB) are the best candidates for power conversion systems in BESSs [6]. The CHB converter has a slightly higher power conversion efficiency and a lower number of required components [5], [7], which makes it the natural choice for application with no common dc-link requirement [8], [9]. The MMC features a high voltage dc-link terminal and is used in applications like HVdc and medium-voltage electric drives [10], where a common dc link is needed. Furthermore, because of multiple circulating current paths, the MMC provides more flexibility to operate with significant interphase and interarm active power disparity [5]. Without giving preference, MMC-based BESS is studied in this research.

In operation of the MMC without integrated energy storage, strictly zero average active power from each submodule (SM) is required to maintain balanced capacitor voltages [11]. In the MMC-based BESS, uneven active power distribution among SMs, which is defined as inter-SM active power disparity in this article, is allowed and required in various conditions, as follows:

- 1) the state-of-charge (SoC) of batteries is unbalanced [12];
- 2) batteries of some specific SMs are faulty, meaning those SMs cannot provide/absorb active power [13], [14];
- 3) the integration of batteries is uneven, for example, batteries are integrated to some SMs only [15], [16];
- 4) hybrid combinations of multiple battery chemistries, or multiple energy storage technologies (batteries and supercapacitors for example), are utilized;
- 5) recycled batteries with different state-of-health (SoH) are utilized [17], etc.

When uneven active power distribution is required, it is necessary to determine the limits of inter-SM active power disparity to ensure that each SM can track its corresponding power reference. The interphase and interarm active power disparity in MMC-based BESS is investigated in [18]–[20], however, these references do not investigate the inter-SM active power disparity that can exist within any arm of an MMC-based BESS. Furthermore, despite a large number of available publications on the MMC-based BESS, only a few of them [13]–[16], [21] take the inter-SM active power disparity limits into consideration. Furthermore, the aforementioned papers do not investigate the general problem of inter-SM active power disparity. Instead, they focus on two specific cases of the general problem.

Case I: The target is to find the minimum percentage of SMs in one arm that can provide the total active power, with the remaining SMs merely providing reactive power [13]–[16]. A numerical solution is given in [13] by testing whether an MMC-based BESS can meet the active power requirement with various percentages of faulty SMs per arm. A numerical and an analytical algorithm for the calculation of inter-SM power disparity are proposed in [16]. The analytical method allows the sum of SM output voltages to be larger than the arm voltage reference, which simplifies the resulting analysis but also introduces significant errors, as is noted by the authors themselves. The numerical method is shown to be more accurate. However, numerical methods are computationally intensive, preclude real-time evaluation of active power disparity limits, and require significant effort in terms of their formulation within high-fidelity simulation packages.

A graphical method is also proposed in [14] to find the minimum percentage of SMs in one arm that can provide the total active power. This method assumes the output voltage of each SM is a superposition of a dc component and a fundamental ac component. However, in practice, the SM output voltage can contain ac components of any frequency. For example, to achieve the maximum average active power, one SM can output a square voltage waveform, which maximizes the fundamental frequency component of the SM output voltage. Another analytical method is proposed in [15], which assumes the SM output voltage as the average SM output voltage plus/minus a constant value, depending on the current direction and SM structure. In other words, an extra constraint is imposed on the output voltage of each SM. Both of the abovementioned assumptions in [14] and [15] unnecessarily limit the SM output voltages, which results in underestimation of the system's ability to deal with active power disparity.

Case II: The target is to determine the maximum difference between the active power of one SM and the average SM power [21]. Similar to the analysis in [14], the SM output voltage is assumed to be a superposition of a dc component and a fundamental ac component. Furthermore, the method does not consider the active power limits of multiple SMs. The active power limit of multiple SMs is typically not a multiple of the limit of one SM. For example, under some operational conditions, it is impossible that two SMs simultaneously supply the maximum power that could be supplied by one SM, which means the limit for two SMs is not equal to twice the limit for one SM. This will be illustrated in detail in this article.

To summarize, the abovementioned papers consider specific cases of inter-SM active power disparity, instead of analyzing the general problem. A general analysis is necessary, for instance, in an MMC-based BESS with recycled batteries, which can be one of the economical solutions in a future grid [22], where the batteries of different SMs may have different power ratings, SoC and SoH. In this case, either to make full use of battery power ratings or balance the SoC and SoH, an uneven set of power references is preferred, which for the purposes of design and control of the system requires knowledge of inter-SM power disparity limits to ensure the given references are viable.

To provide a general and accurate solution to the inter-SM active power disparity problem, this article proposes an analytical method to derive the inter-SM active power disparity limits without introducing any unnecessary constraints on the operation of the MMC-based BESS. Only the inherent operational constraints of the MMC (i.e., the arm voltage references and arm power references cannot be violated) are considered in the analysis. The proposed analysis does not make any assumption that limits the SM output voltages unnecessarily and hence provides a more accurate calculation of the ability of the system to deal with inter-SM active power disparity. The derived analysis is not restricted to the calculation of the power disparity limits of one SM. Instead, the proposed analytical derivation investigates the power disparity limits for any subset of SMs within the MMC arms. It is shown analytically that the limits of multiple SMs are not always an integer multiple of the limit of one SM. A criteria vector and a criterion value are proposed in this article to determine whether an uneven set of power references are allowed for the system under different operational conditions. Furthermore, the proposed analysis applies to the abovementioned Cases I and II. The minimum percentage of SMs in Case I can be calculated by the proposed analysis as it is the percentage of SMs whose maximum limit is equal to the total arm power. The maximum difference between the power of one SM and the average power values (Case II) can also be precisely computed as the difference between the maximum/minimum limit of one SM and the average value, in the proposed analysis.

The remainder of this article is organized as follows. Section II introduces the background of the MMC-based BESS. In Section III, an analytical method is proposed to derive the inter-SM active power disparity limits for a generalized MMC-based BESS. The criteria vector and criterion value are also proposed in this section to determine whether an uneven set of power references is viable. Section IV provides simulation results on a single-phase system with five SMs per arm. Section V provides experimental results on a single-phase system with two SMs per arm. Finally, Section VI concludes the article.

II. MMC-BASED BESS

This section reviews the topology of the MMC-based BESS and its operational principles, which establishes the background for the subsequent analysis.

A. System Topology

Fig. 1 depicts the circuit representation of a phase leg of an MMC-based BESS. Batteries can be integrated into SMs with

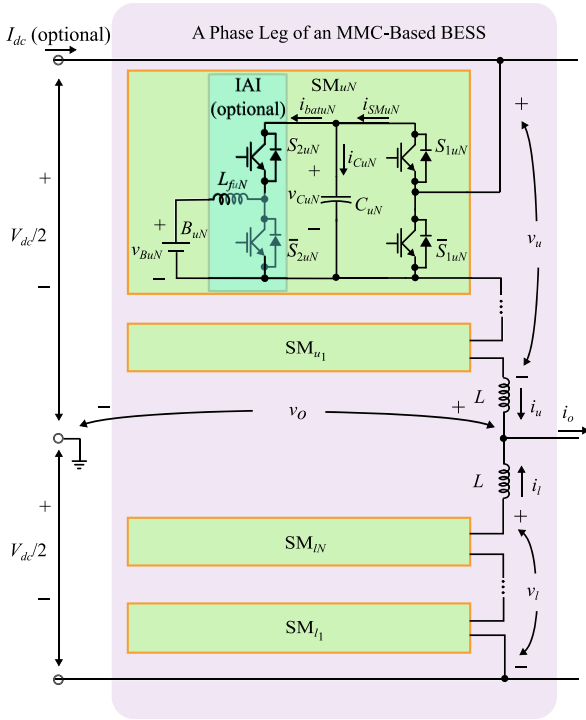


Fig. 1. Circuit diagram of a phase leg of an MMC-based BESS.

an indirect active interface (IAI) [10], which provides voltage boosting capability. In addition to using the IAI, batteries can also be integrated into each SM directly or with a passive interface (various filters [23]). The system is connected to a dc terminal, whose voltage and current are denoted as V_{dc} and I_{dc} , respectively. The variables v_{Cui} and v_{Cli} are the capacitor voltages of the i th SM in the upper and lower arms. Ideally, all the capacitor voltages are balanced and thus, the reference of v_{Cui} and v_{Cli} is

$$v_{Cui}^* = v_{Cli}^* = V_C = K \frac{V_{dc}}{N} \quad (1)$$

where V_C represents the average capacitor voltage and superscript “*” represents the reference value of quantities. K is a constant that indicates V_C may differ from $\frac{V_{dc}}{N}$. For example, when the sum of capacitor voltage of all SMs in one arm is higher than V_{dc} , K can be larger than 1.

B. Modeling and Analysis

By analyzing the equivalent common and differential mode circuits, the relationships among the main electrical variables of the MMC can be deduced [24]. Assuming that the voltage drops in the arm inductors are relatively small, the PWM steady-state voltages within the upper and lower arms are

$$v_u = \frac{V_{dc}}{2} - v_o; \quad v_l = \frac{V_{dc}}{2} + v_o \quad (2)$$

where v_o represents the output voltage of the MMC. In the case of a multiphase MMC system, a common-mode voltage can be superimposed on the arm voltages, to achieve desired functions such as arm energy balancing [11]. The currents flowing through

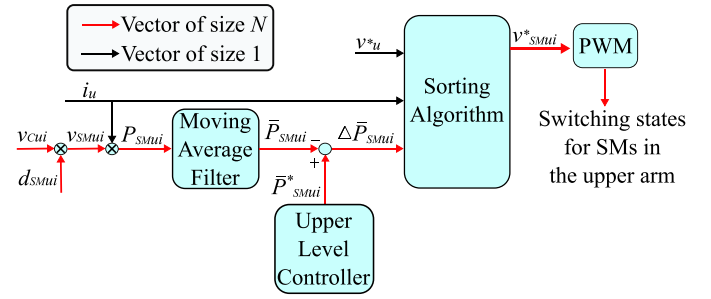


Fig. 2. Proposed sorting-based SM power control algorithm in the upper arm.

the upper and lower arm are

$$i_u = \frac{i_o}{2} + i_{circ}; \quad i_l = \frac{i_o}{2} - i_{circ} \quad (3)$$

where i_o and i_{circ} denote the converter output current and circulating current, respectively. i_{circ} circulates through the phase leg and hence, it does not affect the output current. The circulating current contains a dc component that exchanges energy between the dc side and the phase leg. Some ac components can also be included to achieve certain objectives such as arm energy balancing [24].

C. Control Scheme

Several circulating current injection methods and control algorithms for the MMC are discussed in [24]. The intercell voltage balancing methods for the conventional MMC are discussed in [25]–[28]. SoC and SoH balancing is discussed in [17] and [12]. In this article, a circulating current controller described in [24] is implemented. The capacitor voltage balancing algorithm is unnecessary if the capacitor voltage is regulated by the batteries. A control objective of the MMC-based BESS is to ensure that the active power of each SM tracks its reference. A sorting-based SM power control algorithm is proposed and implemented in this article, which is depicted in Fig. 2 for the upper arm, where d_{SMui} and v_{SMui} represent the duty cycle and output voltage of the i th SM in the upper arm. A similar controller is applied to the lower arm. In practice, there should be an upper level controller to decide the power references for SMs based on certain factors, such as the SoC and SoH of batteries per SM. However, the design and performance of this controller are beyond the scope of this article and hence, it is omitted in the implementation.

As is displayed in Fig. 2, the moving average filter (MAF) computes the average active power of each SM in a fundamental period, \bar{P}_{SMui} . Then the error ΔP_{SMui} is derived by comparing \bar{P}_{SMui} to the corresponding reference \bar{P}_{SMui}^*

$$\Delta P_{SMui} = \bar{P}_{SMui}^* - \bar{P}_{SMui}. \quad (4)$$

With the knowledge of upper arm voltage reference v_u^* , upper arm current i_u and power error $\Delta \bar{P}_{SMui}$ of each SM, the sorting algorithm decides the output voltage reference for each SM, v_{SMui}^* , in such a way that: 1) if the current is positive (with the potential to charge inserted SMs), v_u^* will be distributed among SMs with highest ΔP_{SMui} as much as possible; 2) if the current

is negative (with the potential to discharge inserted SMs), v_u^* will be distributed among SMs with lowest ΔP_{SMui} as much as possible. For example, if there are five SMs in the upper arm and $v_{Cui} = 3$ kV for all of them, when $v_u^* = 4$ kV and i_u is positive, v_{SMui}^* of the SM with highest ΔP_{SMui} will be 3 kV, v_{SMui}^* of the SM with second-highest ΔP_{SMui} will be 1 kV and others will be zero. In the steady state, ΔP_{SMui} of all SMs will approach zero, which means \bar{P}_{SMui} is equal to P_{SMui}^* .

III. INTER-SM ACTIVE POWER DISPARITY

This section introduces the analytical derivation of the inter-SM active power disparity limits for a general MMC-based BESS. Based on the derived limits, a method is proposed to determine whether a distribution of active power among SMs in one arm is viable for the system or not.

A. Derivation of Inter-SM Active Power Disparity Limits

Neglecting the typically small power conversion losses

$$\bar{P}_{dc} = \bar{P}_{armu} + \bar{P}_{arml} + \bar{P}_o \quad (5)$$

where \bar{P}_{dc} , \bar{P}_{armu} , \bar{P}_{arml} , and \bar{P}_o represent the average active power of the dc terminal, active power of the upper and lower arms, and ac side active power, respectively. Hereinafter, the analysis is focused on the upper arm of one phase, but a similar analysis can be applied to the lower arm and the arms in other phases. In a conventional MMC without embedded batteries, \bar{P}_{armu} is zero. In the case of the MMC-based BESS, \bar{P}_{armu} can be any value that is within the power limit of the inserted batteries. Because the main focus of this article is to analyze the inherent limits of the MMC converter, it is assumed that the batteries can meet arbitrary active power requirements.

The total upper arm power is

$$\bar{P}_{armu} = \sum_{i=1}^N \bar{P}_{SMui} \quad (6)$$

where \bar{P}_{SMui} refers to the average active power of the i th SM in the upper arm. \bar{P}_{SMui} has an upper limit and a lower limit, i.e., the maximum and minimum active power that one SM can absorb, which depend on the operation point. As (6) implies, to have a constant \bar{P}_{armu} , any change in \bar{P}_{SMui} must be compensated by a complementary change in the sum of other SMs' power. In other words, \bar{P}_{SMui} is not independent and it is a function of the power of other SMs. Similarly, the power summation of any combination of SMs is dependent on the power of the remaining SMs. Thus, apart from active power limits for one SM, there also exist maximum and minimum power limits for any combination/subset of n SMs, where $n \in [1, 2 \cdots N]$, which are represented hereinafter with \bar{P}_{max}^n and \bar{P}_{min}^n , respectively. The sum of any combination of n \bar{P}_{SMui} must lie between the corresponding \bar{P}_{max}^n and \bar{P}_{min}^n . The boundary cases for when the sum is equal to the maximum or minimum limit represent the most uneven active power distributions allowed for the system, i.e., the inter-SM active power disparity limits. The calculation of \bar{P}_{max}^n and \bar{P}_{min}^n is introduced in the following.

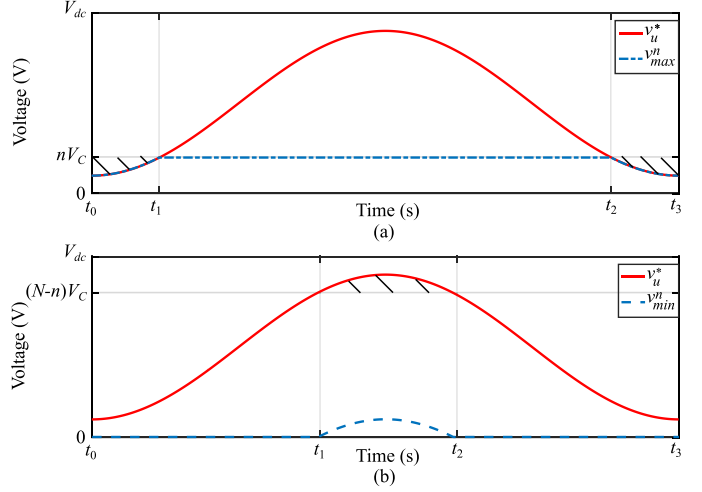


Fig. 3. Maximum and minimum output voltages of n SMs. (a) Maximum output voltage. (b) Minimum output voltage.

To achieve \bar{P}_{max}^n , the corresponding n SMs should operate with the maximum output voltage $v_{max}^n(t)$ when i_u is positive and operate with the minimum output voltage $v_{min}^n(t)$ when i_u is negative. Similarly, \bar{P}_{min}^n is achieved by operating the n SMs with $v_{max}^n(t)$ when i_u is negative and $v_{min}^n(t)$ when i_u is positive. Thus, considering T the fundamental period

$$\bar{P}_{max}^n = \frac{1}{T} \int_{t_0}^{t_0+T} v_{maxp}^n(t) i_u(t) dt$$

$$v_{maxp}^n(t) = \begin{cases} v_{max}^n(t) & \text{if } i_u(t) \geq 0 \\ v_{min}^n(t) & \text{if } i_u(t) < 0 \end{cases} \quad (7)$$

$$\bar{P}_{min}^n = \frac{1}{T} \int_{t_0}^{t_0+T} v_{minp}^n(t) i_u(t) dt$$

$$v_{minp}^n(t) = \begin{cases} v_{min}^n(t) & \text{if } i_u(t) \geq 0 \\ v_{max}^n(t) & \text{if } i_u(t) < 0. \end{cases} \quad (8)$$

The values of $v_{max}^n(t)$ and $v_{min}^n(t)$ are influenced by the SM topology, the value of n , and the operational condition of the system. Take the half-bridge SMs for example, which are not able to output negative voltages. The maximum output voltage of n SMs is $v_{max}^n(t) = \sum_{i=1}^n v_{Cui}(t) = nV_C$ and the minimum output voltage is $v_{min}^n = 0$. However, due to the arm voltage constraint, $v_{max}^n(t) = nV_C$ and $v_{min}^n(t) = 0$ are not always achievable as illustrated in Fig. 3, where v_u^* denotes the reference for the upper arm voltage.

Fig. 3(a) depicts the maximum output voltage of n SMs in a fundamental cycle. During the interval $[t_1, t_2]$, where $v_u^*(t) \geq nV_C$, $v_{max}^n(t)$ is equal to nV_C as desired. However, during the intervals $[t_0, t_1]$ and $[t_2, t_3]$ when $v_u^*(t) < nV_C$, the allowed maximum output voltage v_{max}^n is reduced to v_u^* in this condition, to avoid distorting the output voltage. Similarly, Fig. 3(b) depicts the minimum output voltage of n SMs in a fundamental period. During the intervals $[t_0, t_1]$ and $[t_2, t_3]$, where $v_u^*(t) \leq (N-n)V_C$, the rest of $N-n$ SMs have sufficient capacity to

generate v_u^* and thus, $v_{\min}^n(t)$ is equal to 0. However, during the interval $[t_1, t_2]$, where $v_u^*(t) > (N - n)V_C$, the allowed minimum output voltage is increased to $v_u^* - (N - n)V_C$ (instead of the desired value of 0 V) because the rest of $N - n$ SMs do not have the sufficient capacity to generate v_u^* (the maximum output voltage of the rest $N - n$ SMs is $(N - n)V_C$). Consequently, $v_{\max}^n(t)$ and $v_{\min}^n(t)$ of n half-bridge SMs are obtained as

$$v_{\max}^n(t) = \min [nV_C, v_u(t)] \quad (9)$$

$$v_{\min}^n(t) = \max [0, v_u(t) - (N - n)V_C]. \quad (10)$$

Hence, from (7) to (10), \bar{P}_{\max}^n and \bar{P}_{\min}^n of any number of SMs can be derived for one arm with the knowledge of the arm voltage, arm current, and SM capacitor voltage. Even if the arm voltages and currents are different for several arms, like when the upper and lower arms of one phase are providing different power, \bar{P}_{\max}^n and \bar{P}_{\min}^n can still be derived for each arm with the proposed analysis.

B. Active Power Distribution Viability Assessment Matrix

The computed power disparity limits from (7) and (8) determine whether a set of uneven active power references $[\bar{P}_{SMu1}^* \ \bar{P}_{SMu2}^* \ \cdots \ \bar{P}_{SMuN}^*]^T$ is viable. To simplify the evaluation, the power values are first sorted from the largest value to smallest in such a way that $\bar{P}_{uj}^* \geq \bar{P}_{uj+1}^*$, where \bar{P}_{uj}^* represents the j th maximum value among the SM power references. The given distribution is viable if and only if the following conditions are all met:

I) $\sum_{j=1}^N \bar{P}_{uj}^* = \bar{P}_{\text{armu}}$ [the sum of average active powers of all SMs is equal to the active power requirement of the upper arm, as (6) requests],

II) $\sum_{j=1}^n \bar{P}_{uj}^* \leq \bar{P}_{\max}^n$ for $1 \leq n \leq N - 1$ (thanks to the assumption that $\bar{P}_{uj}^* \geq \bar{P}_{uj+1}^*$, this inequality guarantees that the sum of average active power of any n SMs is not larger than \bar{P}_{\max}^n),

III) $\sum_{j=N-n+1}^N \bar{P}_{uj}^* \geq \bar{P}_{\min}^n$ for $1 \leq n \leq N - 1$ (similarly, this inequality guarantees that the sum of average active power of any n SMs is not less than \bar{P}_{\min}^n).

As shown in the following, conditions (II) and (III) are complementary. As (6) implies, the sum of active powers of all SMs is always equal to the total arm power. Hence, if n SMs are providing the maximum power (\bar{P}_{\max}^n), the remaining $N - n$ SMs must be providing the minimum power (\bar{P}_{\min}^{N-n}). Thus

$$\bar{P}_{\max}^n + \bar{P}_{\min}^{N-n} = \sum_{i=1}^N \bar{P}_{SMui} = \bar{P}_{\text{armu}}. \quad (11)$$

For an arbitrary system, if condition (II) is met ($\sum_{j=1}^n \bar{P}_{uj}^* \leq \bar{P}_{\max}^n$) for any n , by applying (11), it can be deduced that

$$\begin{aligned} \sum_{j=n+1}^N \bar{P}_{uj}^* &= \bar{P}_{\text{armu}} - \sum_{i=1}^n \bar{P}_{ui}^* \geq \bar{P}_{\text{armu}} - \bar{P}_{\max}^n \\ &= \bar{P}_{\min}^{N-n}. \end{aligned} \quad (12)$$

Therefore, condition (III) is also met for any n . Thus, to make the evaluation process compact, condition (III) can be omitted.

Condition (II) can be evaluated using the following criterion value:

$$\begin{aligned} \xi_{\min} = \min(\xi) &= \min \left(\begin{bmatrix} \xi_1 \\ \xi_2 \\ \vdots \\ \xi_{N-1} \end{bmatrix} \right) \\ &= \min \left\{ \begin{bmatrix} \bar{P}_{\max}^1 \\ \bar{P}_{\max}^2 \\ \vdots \\ \bar{P}_{\max}^{N-1} \end{bmatrix} - \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 1 & \ddots & \ddots & 0 \\ & 1 & \ddots & \ddots & 0 \\ 1 & \cdots & 1 & 1 \end{bmatrix} \begin{bmatrix} \bar{P}_{u1}^* \\ \bar{P}_{u2}^* \\ \vdots \\ \bar{P}_{uN-1}^* \end{bmatrix} \right\} \end{aligned} \quad (13)$$

where the n th row of the matrix is $\xi_n = \bar{P}_{\max}^n - \sum_{j=1}^n \bar{P}_{uj}^*$. If ξ_n is positive, then $\sum_{j=1}^n \bar{P}_{uj}^* \leq \bar{P}_{\max}^n$, which matches the expression of condition (II). $\xi = [\xi_1 \ \xi_2 \ \cdots \ \xi_{N-1}]^T$ is defined as the criteria vector and ξ_{\min} is the criterion value, which is the element with minimum value in ξ . A positive value of ξ_{\min} indicates a viable set of references, a zero value refers to the critical distribution (the boundary condition where at least one set of SMs has reached its maximum limit) and a negative value (at least one ξ_n is negative) indicates unviable references. Each element of ξ represents the active power margin for a certain combination of SMs. A positive ξ_n indicates that any value of power up to the maximum of ξ_n can still be added to $\sum_{j=1}^n \bar{P}_{uj}^*$ before it reaches the critical distribution, i.e., $\xi_n = 0$. A negative ξ_n indicates that, at least a minimum value of ξ_n should be subtracted from $\sum_{j=1}^n \bar{P}_{uj}^*$ before allowing this set of references. The entry ξ_N is omitted in the criteria vector because the condition (I) implies $\xi_N = 0$ as $\bar{P}_{\max}^N = \bar{P}_{\min}^N = \bar{P}_{\text{armu}}$.

It is worth to note that the above analysis considers the inherent operation constraints of the MMC only. In a practical system, there are hardware limitations for each SM. Such hardware limitations affect the power limit of individual SMs. However, they will not affect the proposed analysis in this article, which determines the power limits of multiple SMs based on the MMC operation constraints. Nevertheless, it is straightforward to consider these hardware limitations in the proposed analysis by saturating the derived limits on hardware limits.

IV. SIMULATION RESULTS

To verify the analysis in Section III, simulation results are obtained using a single-phase six-level MMC-based BESS, as depicted in Fig. 1. The batteries are directly connected in parallel with capacitors. Parameters of the simulation system are given in Table I.

The output voltage and current waveforms in the simulation are defined as

$$v_o = m_a \frac{V_{dc}}{2} \cos(\omega t); \quad i_o = \hat{I}_o \cos(\omega t + \varphi) \quad (14)$$

where variables m_a , \hat{I}_o , ω , and φ denote the modulation index, amplitude of the output current, angular frequency, and phase difference between the output current and voltage, respectively.

TABLE I
PARAMETERS OF THE STUDIED SYSTEM

Parameter	Value (Simulation)	Value (Experiment)
Number of SMs per arm, N	5	2
SM capacitance, C_{ui}/C_{li}	5 mF	5 mF
Battery voltage, V_{batui}/V_{batli}	3000 V	75 V
Arm inductance, L	2 mH	5 mH
Fundamental frequency, f	50 Hz	50 Hz

In the simulation, \hat{I}_o is 1200 A and the circulating current only contains a 600-A dc current that charges the batteries. Thus, the upper arm power is equal to the lower arm power

$$\bar{P}_{armu} = \bar{P}_{arml} = \frac{\bar{P}_{dc} - \bar{P}_o}{2} = \frac{V_{dc}I_{dc}}{2} - \frac{m_a V_{dc} \hat{I}_o}{8} \cos(\varphi). \quad (15)$$

All the power values in the following results are normalized based on $|\bar{P}_{armu}|$. For instance, a value of $P = 10\%$ represents 10% of $|\bar{P}_{armu}|$.

A. Derived Limits

The theoretical maximum active power limits for a varying percentage of SMs in one arm under various modulation indices and phase shift angles between voltage and current are displayed in Fig. 4. The minimum power limits are complementary to the maximum limits, as (11) implies. Results are displayed on the range $[0, \pi]$ for φ , which are symmetric for the range $[-\pi, 0]$. The results in Fig. 4 represent the maximum power limits for 20%, 40%, and 60% of SMs in one arm, respectively. In other words, the limits are derived and applicable for a general system regardless of the number of SMs per arm or the power rating. For example, in Fig. 4(a), the point $(m_a : 1, \varphi : 0, P : 50.23)$ denotes, when $m_a = 1$ and $\varphi = 0$, the maximum active power that 20% of SMs can absorb is 50.23% of the total arm power. In the case of the simulation system with five SMs per arm, these three figures correspond to one, two, and three SMs, respectively.

As one can see from Fig. 4(a), the value of P (the normalized maximum limits for 20% of SMs) decreases when φ increases from 0 to π . The change of P is decided by both the value of $\bar{P}_{max}^{N/5}$ (\bar{P}_{max}^1 in the simulation system) and \bar{P}_{armu} because $P = \bar{P}_{max}^{N/5} / \bar{P}_{armu} \times 100\%$. When $m_a \leq 0.6$ and φ increases, \bar{P}_{armu} increases while $\bar{P}_{max}^{N/5}$ remains constant, based on (15) and (7), hence P decreases. When $m_a > 0.6$ and φ increases, both \bar{P}_{armu} and $\bar{P}_{max}^{N/5}$ increase but \bar{P}_{armu} increases relatively faster, thus P decreases. The change of P is more complicated when m_a decreases from 1 to 0.2. When φ is between $[\pi/2, \pi]$, the value of P increases with the decrease of m_a . When φ is between $[0, \pi/2]$, with the decrease of m_a , the value of P will increase first and then decrease. Comparing Fig. 4(a)–(c), it is clearly indicated that the increase of power limit is not proportional to the increase of SMs. In other words, the maximum power limit of n SMs is not n times the power limit of one SM.

The simulation results of two specific cases are displayed in Figs. 5 and 6.

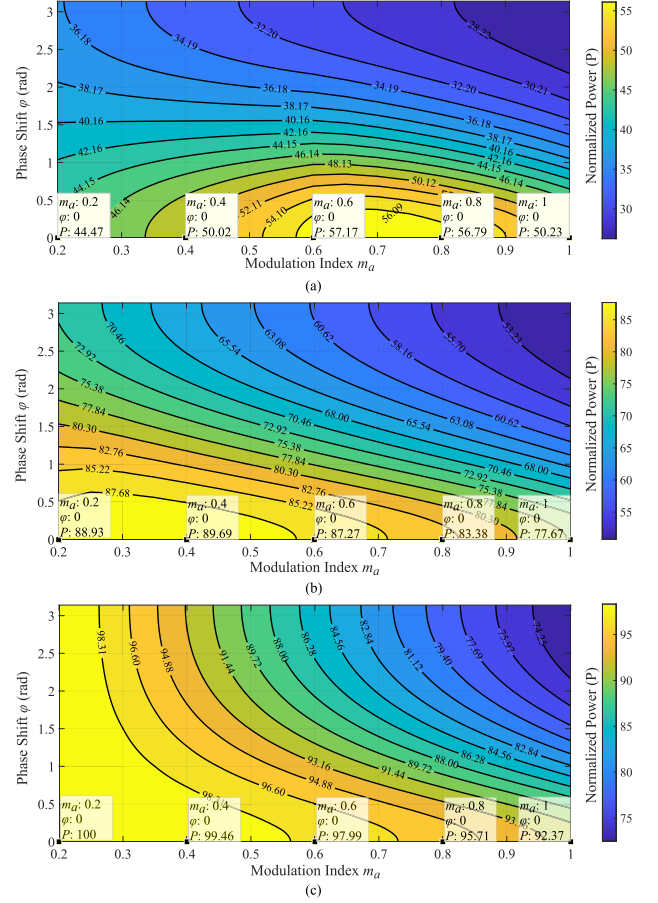


Fig. 4. Normalized maximum power limits under different operation points of a single-phase MMC-based BESS with half-bridge SMs. (a) 20% of SMs of the arm. (b) 40% of SMs of the arm. (c) 60% of SMs of the arm.

B. Case I

In this case, the system operates with the modulation index 0.8 and unity power factor. Initially, the active power references are evenly set for all SMs, which means $[\bar{P}_{SMu1}^* \ \bar{P}_{SMu2}^* \ \bar{P}_{SMu3}^* \ \bar{P}_{SMu4}^* \ \bar{P}_{SMu5}^*]^T = [20\% \ 20\% \ 20\% \ 20\% \ 20\%]^T$. Using (9), (9) and (10), $[\bar{P}_{max}^1 \ \bar{P}_{max}^2 \ \bar{P}_{max}^3 \ \bar{P}_{max}^4]^T = [56.79\% \ 83.38\% \ 95.71\% \ 99.73\%]^T$. Using (13), $\xi = [36.79\% \ 43.38\% \ 35.71\% \ 19.73\%]$ and thus $\xi_{min} = 19.73\%$, which indicates the references are viable and represents the available margins. As one can see from Fig. 5(a), the measured average active power of each SM remains at 20%. At 0.2 s, the references change unevenly. After this transition, $\xi_{min} = 3.38\%$ so the references are still viable. According to Fig. 5(a), after a short transient, the measured average active power of each SM tracks its corresponding reference.

At 0.6 s, the references become more uneven and accordingly, $\xi_{min} = -16.62\%$, indicating that the references are unviable. As one can see, none of the SMs are able to track the corresponding reference. In the steady state, \bar{P}_{SMu1} remains at \bar{P}_{max}^1 [56.79%, according to Fig. 4(a)] because its reference (70%) was beyond this maximum limit. Similarly, \bar{P}_{SMu5} remained at \bar{P}_{min}^1 [0.26%, according to (8)]. Even though \bar{P}_{SMu2}^* (30%) does not change, \bar{P}_{SMu2} cannot track this reference anymore because of the

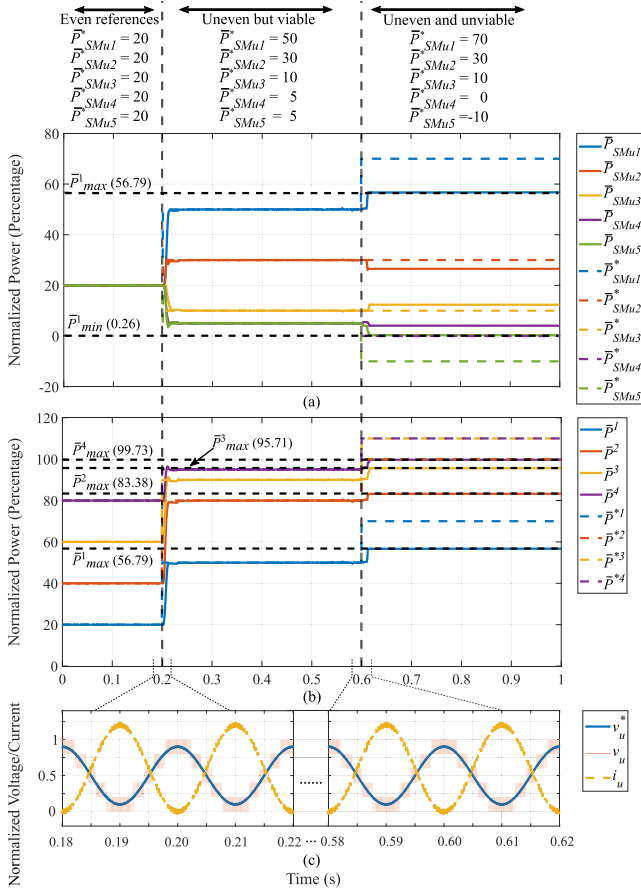


Fig. 5. *Case I*: Simulation results when $m_a = 0.8$ and $\varphi = 0$ (unity power factor). (a) Average active power waveforms of each SM and the corresponding reference. (b) Average active power waveforms of a different number of SMs and the corresponding reference. (c) Upper arm voltage and current of the converter.

limit of \bar{P}_{\max}^2 . Since $\bar{P}_{\max}^2 = 83.38\%$ and $\bar{P}_{SMu1} = 56.79\%$, \bar{P}_{SMu2} is forced to drop down to 26.59%. This process is displayed more clearly in Fig. 5(b), where $\bar{P}^n = \sum_{i=1}^n \bar{P}_{SMui}$ and $\bar{P}^{*n} = \sum_{i=1}^n \bar{P}_{SMui}^*$. As one can see, \bar{P}^2 , the sum of \bar{P}_{SMu1} and \bar{P}_{SMu2} , remains at \bar{P}_{\max}^2 [83.38%, according to Fig. 4(b)] in the steady state. Similar to the case of \bar{P}_{SMu2} , \bar{P}_{SMu4} cannot track its reference (0%) because of the limit of \bar{P}_{\max}^3 (95.71%). Since $\bar{P}_{SMu5} = 0.26\%$, \bar{P}_{SMu4} is forced to rise to 4.03% to ensure that the power of the remaining 3 SMs is no more than \bar{P}_{\max}^3 [95.71%, according to Fig. 4(a)]. As Fig. 5(b) displays, \bar{P}^3 remained at \bar{P}_{\max}^3 . Eventually, \bar{P}_{SMu3} is forced to rise to 12.33% to compensate for the total arm power.

Fig. 5(c) displays the upper arm voltage and current of the converter, where the voltage and current are normalized based on 15 kV and 1 kA, respectively. Since the proposed method always maintains the operational constraints of the converter, even when the active power distribution changes among SMs, the magnitudes of the converter are not distorted.

C. Case II

In this case, the system operates with the modulation index 0.8 and the power factor 0.5. The results are displayed in Fig. 6. The changes in power references and results of *Case II* are very

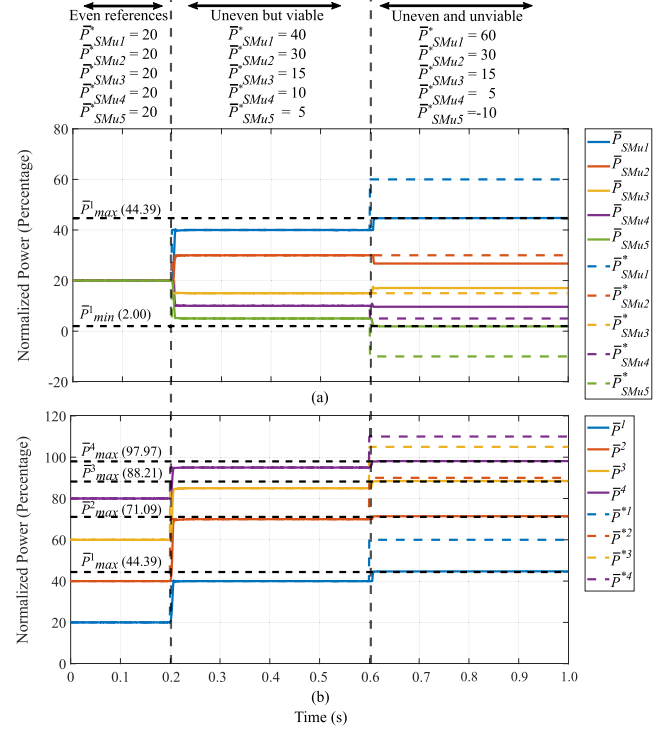


Fig. 6. *Case II*: Simulation results when $m_a = 0.8$ and $\varphi = 1.047$ (0.5 power factor). (a) Average active power waveforms of each SM and the corresponding reference. (b) Average active power waveforms of a different number of SMs and the corresponding reference.

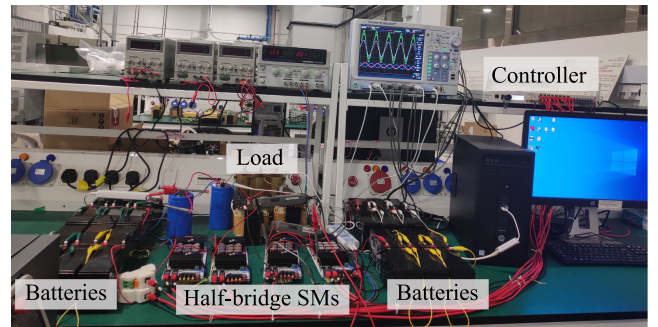


Fig. 7. Picture of the experimental system.

similar to those of *Case I*, hence a detailed analysis is omitted here. As is observed, the simulation results are aligned with the analyzed results in Fig. 4.

V. EXPERIMENTAL RESULTS

Experimental results are obtained using a single-phase three-level MMC-based BESS. No dc current is transferred from the dc terminal to the system and the circulating current is zero in the experiment. Batteries are directly connected in parallel with capacitors. In the experiments, the BESS works in discharging mode but, depending on the output power, it can also work in charging mode. Parameters of the experimental system are given in Table I, and a picture of the setup is provided as Fig. 7. The Imperix B-Box RCP control platform is used to implement the proposed control strategy in the experimental setup. The MMC is built by the series connection of Imperix

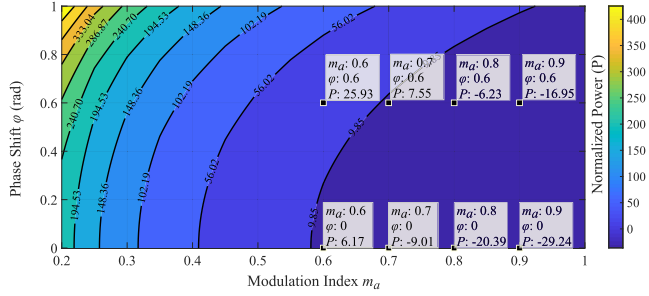


Fig. 8. Normalized maximum power limits for 50% of SMs of one arm of the single-phase MMC-based BESS, under different operating points.

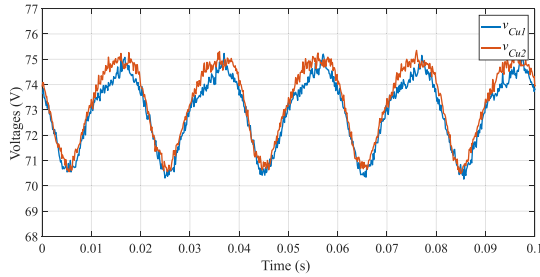


Fig. 9. Capacitor voltage waveforms of two SMs in the upper arm of the experimental setup.

PEH 2015 full-bridge power modules, which are configured as half-bridge converters. Six series-connected RS 537-5488 lead-acid batteries are connected to the dc-side of each SM, while resistors and inductors are connected to the output as a load.

A. Derived Limits

Fig. 8 displays the derived maximum active power limits for 50% of SMs of the upper arm under different operational conditions, which is one SM in this experimental system. Results are displayed in the range $[0, 1]$ for φ and $[0.2, 1]$ for m_a . Within this range, the upper arm is working at discharging mode thus \bar{P}_{armu} is negative. All the power values in the following results are normalized based on $|\bar{P}_{armu}|$. It is worth to note that the results in Fig. 8 are obtained with the assumption that the equivalent inner resistance of batteries are relatively low and thus, the capacitor voltage of each SM is equal to its battery voltage. However, in the experimental setup, six batteries are connected in series for each SM, which has a considerable equivalent inner resistance (represented with R_{in} , around 1.15Ω). Because of R_{in} and the corresponding voltage drop when current flows between the capacitor and batteries, the capacitor voltage is not equal to the battery voltage. As an example, the recorded capacitor voltage waveforms of two SMs in the upper arm is provided in Fig. 9 when the arm power is evenly distributed among them. This change in capacitor voltages will affect the maximum/minimum active power limits of SMs.

The voltage drop across R_{in} depends on the active power of the SM. To derive more accurate power limits, the average capacitor voltage of each SM can be approximated by assuming that this SM is providing a certain active power based on

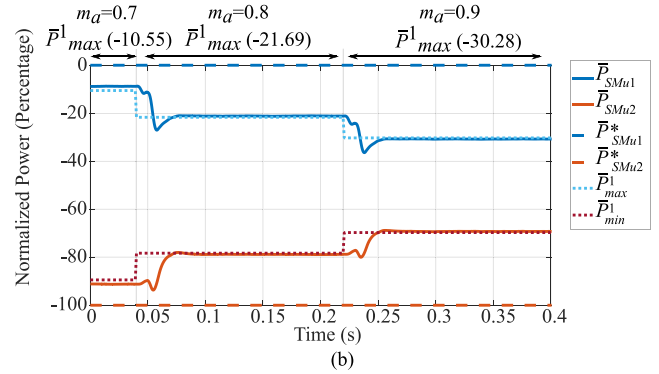
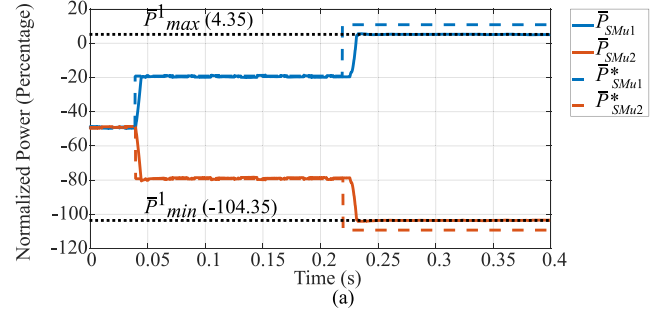


Fig. 10. Case I: Experiment waveforms of \bar{P}_{SMu1} and \bar{P}_{SMu2} under unity power factor. (a) Power references change with $m_a = 0.6$. (b) m_a changes with constant power references, set as 0 and 100% for two SMs, respectively.

Fig. 8. Then, with the approximated capacitor voltages, the maximum/minimum power limits can be updated with (7) and (8). For example, when $m_a = 0.8$ and $\varphi = 0.5$, if R_{in} is negligible, the maximum power of one SM is -20.39% of $|\bar{P}_{armu}|$. In the experimental setup, if one SM is providing -20.39% of $|\bar{P}_{armu}|$, the average capacitor voltage of this SM is estimated to be 74.20 V and the average capacitor voltage of the other SM in this arm is 71.8 V. Based on these two voltages, the maximum power of one SM in the experimental setup is calculated to be -21.69% of $|\bar{P}_{armu}|$ and the minimum power of one SM is -78.31% of $|\bar{P}_{armu}|$.

Experimental results are obtained for the following two cases, which are displayed in Figs. 10 and 11.

B. Case I

In this case, the system operates under unity power factor. Fig. 10(a) displays the results with a constant modulation index $m_a = 0.6$. Initially, the system is balanced, i.e., \bar{P}_{SMu1}^* and \bar{P}_{SMu2}^* are -50% . Because \bar{P}_{armu} is negative, the normalized \bar{P}_{SMu1}^* and \bar{P}_{SMu2}^* sum up to 100%. As one can see from the figure, in the period from 0 to 0.04 s, both \bar{P}_{SMu1} and \bar{P}_{SMu2} stay constant at -50% . At 0.04 s, \bar{P}_{SMu1}^* rises to -20% while \bar{P}_{SMu2}^* drops to -80% . \bar{P}_{max}^1 and \bar{P}_{min}^1 are 4.35% and -104.35% , respectively when $m_a = 0.6$. At this operating condition $\xi_{min} = 24.35\%$, which indicates the references are viable. Therefore, as can be observed, \bar{P}_{SMu1} and \bar{P}_{SMu2} are able to track the references. At 0.22 s, \bar{P}_{SMu1}^* rises to 10% while \bar{P}_{SMu2}^* drops to -110% . At this new operating condition $\xi_{min} = -5.65\%$, which indicates that the references are unviable. As can be seen, \bar{P}_{SMu1} and \bar{P}_{SMu2} are unable to follow these references and only can go as far as the calculated limits \bar{P}_{max}^1 and \bar{P}_{min}^1 , respectively.

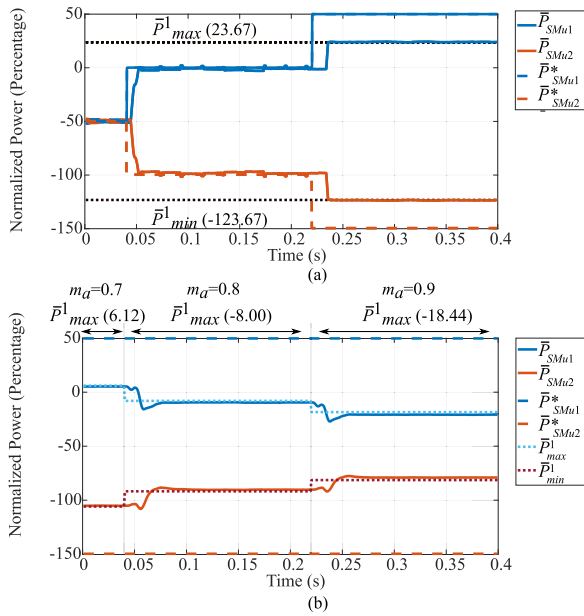


Fig. 11. Case II: Experiment waveforms of \bar{P}_{SMu1} and \bar{P}_{SMu2} under a power factor of 0.827. (a) Power references change with $m_a = 0.6$. (b) m_a changes with constant power references, set as -50% and 150% for two SMs, respectively.

Fig. 10(b) displays the results with different modulation indices at 0.7, 0.8, and 0.9. \bar{P}_{SMu1}^* and \bar{P}_{SMu2}^* are set constant at 0% and -100% , respectively, which are beyond the derived limits, based on Fig. 8. Thus, \bar{P}_{SMu1} and \bar{P}_{SMu2} should remain at the corresponding computed limits in the steady state. As one can see, when m_a changes, the derived \bar{P}_{max}^1 and \bar{P}_{min}^1 change. Accordingly, \bar{P}_{SMu1} and \bar{P}_{SMu2} also change, following the derived limits.

C. Case II

Similar experiments are repeated with a power factor of 0.827, which means $\varphi = 0.597$. The results are displayed in Fig. 11, which are similar to those in Fig. 10. It is evident that experimental results are aligned with the analysis under all operating conditions.

In the experimental results of Figs. 10 and 11, small discrepancies (less than 2%) between the measured and predicted power limits are observed. Apart from some inaccuracies in sensors measurement, the other factors that contribute to having this error include, voltage drop on semiconductors and capacitor voltage ripples. These small discrepancies demonstrate that the predicted active power disparity have low sensitivity to these factors.

VI. CONCLUSION

An analytical method to derive the inter-SM active power disparity limits for a generalized MMC-based BESS under arbitrary operational conditions has been proposed in this article. With this method, if the arm voltage, arm current, and capacitor voltages are known, the limits of this arm can be derived analytically. With

the derived limits, it is straightforward to determine whether an uneven set of power references are viable for the system under different operational conditions. If the sum of active power references of an arbitrary subset of SMs lies between the corresponding maximum and minimum limits, the references are viable. With the proposed analysis, it is also simple to determine how much the references can be modified to avoid violating the limits. A feasible and computationally efficient method is proposed for the determination process, with a criteria vector and a criterion value whose sign is able to tell whether an uneven set of references is viable. According to the analysis and provided analytical results, the system always has the ability to tolerate certain inter-SM active power disparity. The change of limits is not proportional to the change of the number of SMs, for example, the maximum limit for two SMS is not twice the maximum limit for one SM. Both simulation results and experimental results are obtained to verify the proposed method and criterion value, which indicate they are applicable for a general system under various operational points. The proposed method and analysis in this article facilitates the MMC-based BESS to make full use of the potential to operate with inter-SM active power disparity. Designing a BESS control strategy that uses the derived power limits as constraints to generate optimal SMs power references is a direction for future studies to complement this research.

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Gaowen Liang (Student Member, IEEE) received the B.Sc. degree in electrical engineering and automation from the South China University of Technology, Guangzhou, China, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with the Nanyang Technological University, Singapore.

His research interests include the grid-integration of energy storage systems with multilevel power converters in particular, modular multilevel converters, and cascaded H-bridge converters.



Hossein Dehghani Tafti (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering and power system engineering from the Amirkabir University of Technology, Tehran, Iran, in 2009 and 2011, respectively, and the Ph.D. degree in electrical engineering from Nanyang Technological University, Singapore, in 2018.

From February to August 2016, he was on a research exchange program with the University of New South Wales, Sydney, NSW, Australia, where he was working on the control of multilevel grid-connected converters. From August to October 2017, he was a Researcher with Aalborg University, Aalborg, Denmark, where he was working on the flexible power point tracking in photovoltaic power plants. From March 2018 to May 2020, he was a Research Fellow with Nanyang Technological University. Currently he is a Senior Research Associate with the University of New South Wales, Sydney, Australia. He was the Co-Editor of the book titled: *Advanced Multilevel Converters and Applications in Grid Integration* (John Wiley, 2018). His research interests include the grid-integration of renewable energy sources, in particular, photovoltaics and energy storage, and design and control of multilevel power converters.



Glen G. Farivar (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the Nooshirvani Institute of Technology, Babol, Iran, in 2008, the M.Sc. degree in power electronics from the University of Tehran, Tehran, Iran in 2011, and Ph.D. degree in electrical engineering from the University of NSW Australia, Sydney, Australia, in 2016.

He is currently working as a Postdoctoral Research Fellow with the Energy Research Institute, Nanyang Technological Institute (ERI@N), Singapore. His research interests include renewable energy systems, high power converters, energy storage, FACTS devices, and hybrid electric vehicles.



Josep Pou (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Technical University of Catalonia (UPC)-Barcelona Tech, Catalonia, Spain, in 1989, 1996, and 2002, respectively.

In 1990, he joined as an Assistant Professor with the Faculty of UPC, where he became an Associate Professor, in 1993. From February 2013 to August 2016, he was a Professor with the University of New South Wales (UNSW), Sydney, Australia. He is currently a Professor with the Nanyang Technological University (NTU), Singapore, where he is also a Program Director of power electronics at the Energy Research Institute at NTU (ERI@N) and Co-Director of the Rolls-Royce at NTU Corporate Lab. From February 2001 to January 2002, and February 2005 to January 2006, he was a Researcher with the Center for Power Electronics Systems, Virginia Tech, Blacksburg. From January 2012 to January 2013, he was a Visiting Professor with the Australian Energy Research Institute, UNSW, Sydney. He has authored more than 330 published technical papers and has been involved in several industrial projects and educational programs in the fields of power electronics and systems. His research interests include modulation and control of power converters, multilevel converters, renewable energy, energy storage, power quality, HVdc transmission systems, and more-electrical aircraft and vessels.

Dr. Pou was the recipient of the 2018 IEEE Bimal Bose Award for Industrial Electronics Applications in Energy Systems. He is the Co-Editor-in-Chief for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.



Christopher D. Townsend (Member, IEEE) received the B.E. and Ph.D. degrees in electrical engineering from the University of Newcastle, Australia, in 2009 and 2013, respectively.

From 2013 to 2016, he was with the ABB Corporate Research, Sweden, working on next-generation high-power converter technologies. Since then, he has held various Postdoctoral Research positions, including at the University of New South Wales, Australia, the University of Newcastle, Australia, and Nanyang Technological University, Singapore. In 2019, he joined the Department of Electrical, Electronic and Computer Engineering at the University of Western Australia, as a Senior Lecturer. He has authored more than 60 published technical papers and has been involved in several industrial projects and educational programs in the field of power electronics. His research interests include topologies and modulation strategies for multilevel converters applied in power systems, renewable energy integration, and electric vehicle applications.

Dr. Townsend is a member of the IEEE Power Electronics and IEEE Industrial Electronics Societies.

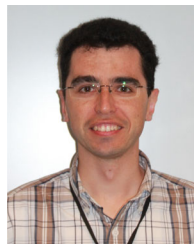


Georgios Konstantinou (Senior Member, IEEE) received the B.Eng. degree in electrical and computer engineering from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2007, and the Ph.D. degree in electrical engineering from The University of New South Wales, UNSW, Sydney, Australia, in 2012.

From 2012 to 2015, he was a Research Associate with UNSW. He is currently a Senior Lecturer with the School of Electrical Engineering and Telecommunications at UNSW Sydney. His main research

interests include multilevel converters, power electronics in HVdc, renewable energy, and energy storage applications.

Dr. Konstantinou is an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and IET POWER ELECTRONICS.



Salvador Ceballos received the M.S. degree in physics from the University of Cantabria, Santander, Spain, in 2001, and the M.S. and Ph.D. degrees in electronic engineering from the University of the Basque Country, Bilbao, Spain, in 2002 and 2008, respectively.

Since 2002, he has been with Tecnalia Research and Innovation in Derio, Spain, where he is currently a Principal Researcher with the Energy and Environment Division. From May 2008 to May 2009, he was a Postdoctoral Visiting Researcher with the Hydraulic and Maritime Research Centre, University College Cork (UCC), Cork, Ireland. From November 2014 to May 2015 he was a Visiting Researcher with the Australian Energy Research Institute, UNSW, Sydney, Australia. From January to August 2020, he joined the Energy Research Institute at Nanyang Technological University, Singapore, as a Principal Research Fellow. He has authored more than 140 published technical papers. His research interests include multilevel converters for high and medium voltage applications, fault-tolerant power electronic topologies, renewable energy systems, and power systems with high penetration of power converters.