# Advanced 650 V SiC Power MOSFETs With 10 V Gate Drive Compatible With Si Superjunction Devices

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***Abstract*—Advanced SiC planar-gate power MOSFETs have been successfully manufactured in a 6-inch commercial foundry with device structures optimized for operation with gate drive voltage of 10 V, compatible with gated drive voltage for Si superjunction products. The electrical characteristics of three advanced SiC MOSFET options are described in this article and compared with those of a state-of-the art Si superjunction MOSFET. The new advanced SiC power MOSFETs are demonstrated to exhibit superior ON-state and switching losses with significantly better body-diode reverse recovery performance. Their short-circuit withstand time is also found to be significantly longer than typical commercially available planar-gate SiC power MOSFETs. These improved characteristics make the advanced SiC power MOSFETs suitable replacements for Si superjunction transistors to enhance high frequency circuit performance.**

***Index Terms*—650 V, 4H-SiC, 10 V gate drive, gate-drain charge, gate oxide, high-frequency figures-of-merit, power MOSFETs, reverse-transfer capacitance, short-circuit withstand time, Si CoolMOS, specific ON-resistance, switching loss.**

## I. Introduction

SILICON carbide (SiC) power MOSFETs with 650 V rating have been commercialized for replacing Si insulated-gate bipolar transistors (IGBTs) in many applications, such as uninterruptible power supplies and solar photovoltaic (PV) inverters [1]. In addition, one of the promising opportunities for these SiC devices is in electric vehicle motor drives. In these and other applications, such as server and uninterruptible power supplies, SiC power MOSFETs will also have to compete with commercially available silicon superjunction devices.

Si superjunction products are designed to operate with a gate drive voltage of 10 V by the manufacturers [2], [3]. Their device output characteristics show no reduction of ON-resistance when the gate bias is increased beyond 10 V, and their ON-resistance and gate charge are provided in the datasheets using 10 V gate drive. Consequently, many applications for Si CoolMOS devices utilize a 10 V gate drive: uninterruptible power supply [4], photovoltaic boost converter [5], modular multilevel converter [6], and power factor correction boost converter [7].

In contrast, commercially available 650-V SiC power MOSFETs are designed to operate with a gate drive voltage of 15 V for planar-gate structures [8] and 18 V for trench-gate structures [9]. In fact, one of the manufacturers [9] specifically states a warning: *"Please be advised not to use SiC-MOSFETs with $V_{gs}$ below 13 V as doing so may cause thermal runaway"* in the datasheet. Consequently, a basic incompatibility exists in the gate drive voltage for SiC power MOSFET products and Si superjunction products. It is worth pointing out that many recent papers have evaluated and compared the performance of 650 V SiC power MOSFETs with Si superjunction devices and IGBTs [10]–[14]. In all of this previous work, a gate drive voltage between 15 and 20 V was used for the SiC power MOSFETs.

This article discusses the development of the first SiC planar-gate power MOSFETs with a blocking voltage rating of 650 V that are especially engineered to allow replacement of Si superjunction transistors without altering the 10 V gate drive voltage. The reduced gate drive voltage of 10 V is also desirable because it reduces the total gate charge and improves the short-circuit (SC) capability. Three advanced 650V SiC power MOSFET structures were therefore created to produce good performance with a gate drive voltage of 10 V. They were successfully manufactured in a 6-inch SiC commercial foundry, X-Fab, TX, with excellent parametric distributions and yield. Electrical characterization of the SiC power MOSFETs was performed for 60 devices of each type across a 6-inch wafer to generate wafer maps and statistical distributions. They demonstrated excellent manufacturability with high yield and good parametric distributions for all the devices. Data on typical devices for each of the three advanced power MOSFET structures are provided in this article. The wafer maps and statistical distributions are similar to those previous published for 1.2-kV devices [15]. The measured electrical performance of these SiC power MOSFETs are compared with those of a state-of-the-art commercially available Si superjunction transistor (Infineon COOLMOS 7$^{th}$ Gen product IPW65R190C7) in this article.

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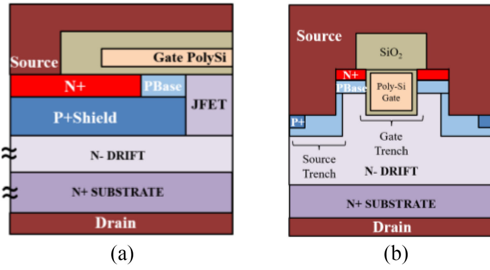


Fig. 1. Commercially available SiC power MOSFET cross-sections. (a) Planar-gate inversion-channel structure. (b) Rohm Trench-Gate inversion-channel structure.

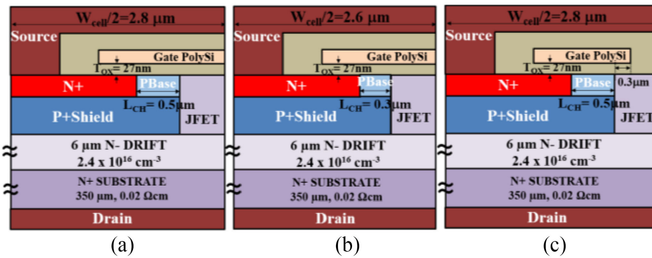


Fig. 2. Three Advanced SiC power MOSFET planar-gate structures with 27nm gate oxide thickness. (a) Inversion-channel structure with $L_{\rm CH} = 0.5$ $\mu$m. (b) Inversion-channel structure with $L_{\rm CH} = 0.3$ $\mu$m. (c) Inversion-channel SG structure with $L_{\rm CH} = 0.5$ $\mu$m.

## II. Commercial Device Structures

The cross-sections of commercially available 650-V SiC power MOSFET structures are shown in Fig. 1. SiC power MOSFETs must be engineered with a low ON-resistance to reduce conduction power losses during operation in power circuits. A smaller specific ON-resistance (ON-resistance for a device active area of 1 cm$^2$) allows fabricating smaller dies for a desired ON-resistance rating, bringing down the manufacturing cost. The specific ON-resistance of the planar-gate structure is determined by eight components [16] of which the channel, junction field effect transistor (JFET) region, and drift region resistances are dominant. This statement also holds true even for the Rohm trench-gate structure because a JFET component is introduced by the presence of the deep trench regions with P$^+$ doping that are required to shield the gate oxide. Both the planar-gate and trench-gate commercial devices utilize an inversion-mode electron channel formed on a P-base region for controlling the current flow. The channel is formed on the upper surface for the planar gate structure and along the vertical sidewall in the trench-gate structure. The JFET resistance for the planar SiC power MOSFET structure has been previously optimized by enhancing its doping concentration [17]. The drift region resistance is decided by its doping concentration and thickness chosen to support the required breakdown voltage [18].

For both structures, the specific channel resistance is given by [16]

$$R_{\rm CH,SP} = \frac{L_{\rm CH} W_{\rm Cell}}{2\mu_{\rm ni} C_{\rm OX} (V_{\rm gs} - V_{\rm TH})} \quad (1)$$

where $L_{\rm CH}$ is the channel length, $W_{\rm Cell}$ is the cell width, $\mu_{\rm ni}$ is the inversion-channel mobility at the ON-state gate bias, $C_{\rm OX}$ is the capacitance per cm$^2$ for the gate oxide, $V_{\rm gs}$ is the ON-state gate drive voltage, and $V_{\rm TH}$ is the threshold voltage. The $C_{\rm OX}$ is equal to the ratio of the dielectric constant for silicon dioxide to the gate oxide thickness ($T_{\rm OX}$). The planar-gate structure for the commercially available SiC power MOSFETs from CREE [8] has a channel length of 0.5 microns and a gate oxide thickness of 50 nm. The minimum channel length for the CREE devices has been published to be 0.5 microns [19]. The gate oxide thickness of 50 nm used in CREE devices has also been reported [19] with a statement that the gate oxide electric field is 3 MV/cm with a 15 V gate drive voltage, which implies an electric field of 4 MV/cm is acceptable for products [20] with a gate drive voltage of 20 V. Similar values are used for the trench-gate commercial MOSFETs [21]. The datasheets for these 650 V products utilize an ON-state gate drive voltage of 15 V. The channel resistance is inversely proportional to $(V_{\rm gs} - V_{\rm TH}) = (15 - 2) = 13$ V assuming a threshold voltage of 2 V. If the gate drive voltage is reduced to 10 V to achieve parity with the Si superjunction products, the channel resistance will be inversely proportional to $(V_{\rm gs} - V_{\rm TH}) = (10 - 2) = 8$ V producing an increase in its value by a factor of $(13/8) = 1.625$x. This substantial increase in channel resistance must be overcome to create a 650-V SiC power MOSFETs that can be driven with a gate voltage of 10 V compatible with Si superjunction products.

## III. Advanced Device Structures

The planar-gate device structure was improved in this article on the advanced SiC power MOSFETs (ASPMs) to counteract the increase in channel resistance discussed in the previous section. Three improved device structures, shown in Fig. 2, were proposed, analyzed, manufactured, and then characterized in this article. Their design methodology is discussed later.

First, the process for the ASPMs was altered to achieve a gate oxide thickness of 27 nm to increase the gate oxide capacitance ($C_{\rm OX}$) by a factor of 1.85x. This reduces the channel resistance contribution by a factor of 1.85x in the first device (ASPM-1) of this article, compensating for the reduced gate drive voltage. It is worth mentioning that the maximum gate voltage for these devices is reduced to −5 V/+20 V compared with –10 V/+30 V for previous devices with 50 nm gate oxide thickness. The gate leakage current for the 27 nm gate oxide devices at a gate bias of 10 V is similar to that for previous devices operated at a gate bias of 20 V and 50 nm gate oxide thickness because of the same magnitude (3–4 MV/cm) for the electric field. The reliability for the 27 nm gate oxide devices is also expected to be similar to that of previous devices operated at a gate bias of 20 V and 50 nm gate oxide thickness because of the same magnitude (3–4 MV/cm) for the electric field in the ON-state. The gate oxide electric field at 650 V in the blocking mode has been shown to be 3.2 MV/cm [22] which was well below the 4 MV/cm value required for reliable operation [23].

For the second device (ASPM-2) of this article, the same device structure as the ASPM-1 was used with the channel length ($L_{\rm CH}$) reduced from 0.5 to 0.3 $\mu$m. This additional change decreases the channel resistance by a factor of $(0.5/0.3) = 1.67$x. The smaller channel length produces a reduction in the cell width ($W_{\rm cell}$) as well. This decreases the specific channel resistance

TABLE I
DEVICE DISTINGUISHING PARAMETERS

| Parameter | NCSU SiC ASPM-1 | NCSU SiC ASPM-2 | NCSU SiC ASPM-3 |
|---|---|---|---|
| Channel Type | Inversion | Inversion | Inversion |
| Gate Oxide Thickness (nm) | 27 | 27 | 27 |
| Channel Length (μm) | 0.5 | 0.3 | 0.5 |
| Half-Cell Width (μm) | 2.8 | 2.6 | 2.8 |
| JFET Width (μm) | 0.7 | 0.7 | 0.7 |
| Gate Structure | Standard | Standard | Split-Gate |

by an additional factor of (2.8/2.6) = 1.1x for total reduction by a factor of 1.837x. The reduced channel length and cell pitch also produce an increase in the transconductance ($G_m$) of device ASPM-2 by a factor of 1.837x [16]. A larger transconductance shortens the transition times for the drain voltage and current during circuit operation, which reduces the switching losses [16].

For the third device (ASPM-3) of this article, the same device structure as the ASPM-1 was used with a change in the gate architecture to the split-gate (SG) form. The SG structure reduces the area of the overlap of the gate electrode with the drift region. This modification has been experimentally verified to reduce the gate-drain capacitance by a factor of 1.6x and the gate-drain charge by a factor of 1.5x [24]. A reduction of these parameters shrinks the transition time for the drain voltage in power circuits bringing down the switching losses.

The common features and differences between the structures for the three ASPMs are highlighted in Table I. The reduced gate oxide thickness and shorter channel length employed for the ASPMs in this article have not been used by commercial SiC power MOSFET manufacturers to our knowledge because the benefits have not been previously quantified. Experimental results are reported in this article to encourage adoption of these design improvements.

## IV. DEVICE FABRICATION

The proposed planar-gate ASPMs were manufactured at a commercial foundry, X-Fab, TX, on 6-inch $N^+$ substrates wafers with epitaxial layer parameters chosen to achieve a blocking voltage rating of 650 V. An epitaxial layer doping concentration of $2.4 \times 10^{16}$ $cm^{-3}$ and thickness of 6 $\mu$m was chosen based on numerical simulations of the device structure [22] and its hybrid-JTE edge termination [25]. The devices were manufactured using the NCSU engineered PRESiCE technology [26]. Details regarding the fabrication process can be found in this reference. All devices had P-base doping of $3 \times 10^{16}$ $cm^{-3}$, JFET doping of $5.4 \times 10^{16}$ $cm^{-3}$, $P^+$ shield doping of $1 \times 10^{18}$ $cm^{-3}$ and $N^+$ doping of $1 \times 10^{20}$ $cm^{-3}$. All three ASPMs had a die size of 3 mm $\times$ 3 mm and an active area of 0.045 $cm^2$.

## V. DEVICE CHARACTERIZATION

Extensive wafer-level measurements were first performed using a semiautomated signatone probe station with a Keysight B1505A curve tracer. A Kelvin-probe was used to minimize the influence of parasitic resistances. A total of 60 devices for each of the 3 ASPMs were characterized to obtain statistical data on the blocking voltage capability, ON-resistance, threshold voltage, transconductance, various capacitances, and the gate charge. All three types of device structures had an excellent parametric spread resulting in a high (>95%) yield. All measurements reported in this article were performed at room temperature and the data is reported for a typical device of each type.

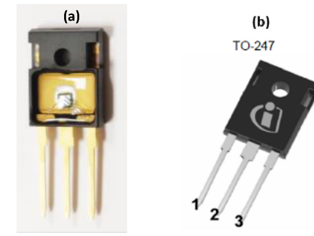


Fig. 3. (a) Photograph of the ASPM chip in an open-cavity TO-247 package. (b) TO-247 packaged infineon Si COOLMOS super-junction transistor.

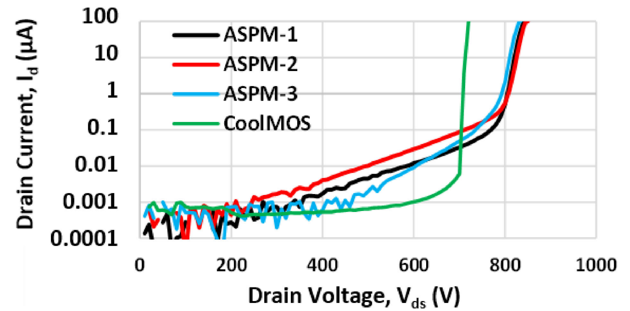


Fig. 4. Measured blocking characteristics for the three advanced SiC power MOSFETs and the CoolMOS IPW65R190C7 product at zero gate bias.

The wafers were diced to separate out individual devices. The dies were mounted in open-cavity TO-247 packages by using Sb/Sn solder. Multiple 10-mm diameter aluminum wire-bonds were attached to the source area to reduce the parasitic resistance. A single wire-bond was placed on the gate pad. An ASPM is shown in Fig. 3(a) in the open-cavity TO-247 package. A picture of the Infineon Si CooLMOS superjunction transistor in its TO-247 package is shown in Fig. 3(b) for comparison. It can be seen that the packaged ASPM devices are similar to commercially available CooLMOS devices allowing comparison of switching performance. Some of these packaged ASPMs were subjected to destructive SC tests to determine their SC withstand time. The similar packaging of the ASPM devices as the Si CoolMOS device allows achieving equivalent thermal resistance. The switching tests were performed with a low duty cycle to minimize self-heating. All data (except SC) reported in this article represents operation close to room temperature.

## VI. EXPERIMENTAL RESULTS

### A. Blocking Characteristics and Breakdown Voltage

The measured blocking characteristics of the three ASPMs are shown in Fig. 4 together with that measured for the Si Infineon CooLMOS 7th Gen product IPW65R190C7. These characteristics were obtained using zero gate bias. All three ASPMs

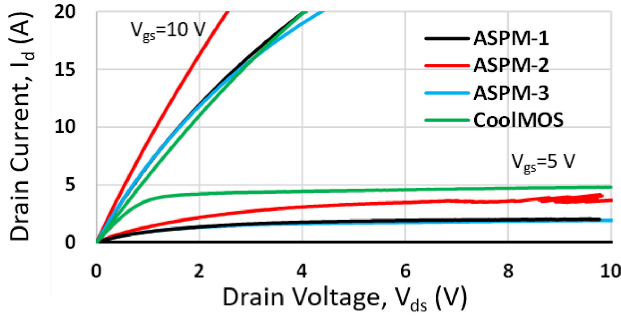


Fig. 5. Measured output characteristics for the 650 V ASPM-1, ASPM-2, ASPM-3, and CoolMOS IPW65R190C7 product with gate bias of 5 and 10 V.

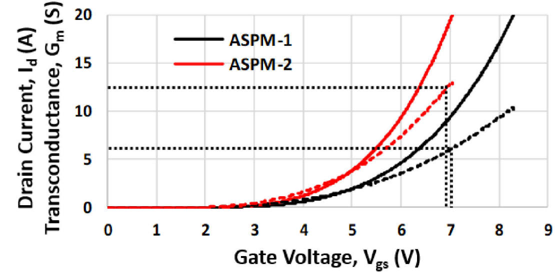


Fig. 6. Measured transfer characteristics for the ASPM-1 and ASPM-2 devices at drain bias of 20 V (solid line); and the extracted transconductance (dashed line).

exhibit a breakdown voltage of 850 V (at the typical leakage current of 100 $\mu$A used in datasheets), well above the rating of 650 V. The leakage currents are below 0.1 $\mu$A up to the rated blocking voltage of 650 V. All three re-engineered structures have excellent blocking characteristics with low leakage current and high breakdown voltage. In contrast, the CoolMOS product has a breakdown voltage of 710 V.

It was previously demonstrated via numerical simulations that the electric field in the gate oxide is <4 MV/cm for reduced gate oxide thickness of 27 nm [22]. This field is sufficiently low for reliable operation. In addition, it was shown in [27] that a channel length of 0.3 $\mu$m is sufficient to prevent reach-through induced degradation of the blocking voltage. The excellent blocking characteristics measured for the ASPM-2 in Fig. 4 demonstrates that this reduced channel length is practical.

### B. Output Characteristics and on-Resistance

The output characteristics for the three ASPMs were measured up to a gate bias of 10 V. The *i–v* characteristics for the ASPM-1, ASPM-2, and ASPM-3 can be compared using Fig. 5. The output characteristics for ASPM-1 and ASPM-3 are very similar and overlap because the devices have the same 0.5 $\mu$m channel length. It has been previously established that the SG structure does not alter the output characteristics [24]. The measured ON-resistance for both of these devices is 160 m$\Omega$ at a gate bias of 10 V and current density of 100 A/cm$^2$. This value is close to that of the CooLMOS product IPW65R190C7, allowing comparison of performance in the discussion section. The internal distributions of the ON-resistance obtained by analytical models [16] for ASPM-1 and ASPM-3 are 38% for the channel, 9% for the accumulation layer, 3% for the JFET region, 9% for the drift region, and 29% for the substrate.

From the output characteristics for the ASPM-2, also shown in Fig. 5, a smaller ON-resistance and larger transconductance is apparent due to its shorter 0.3 $\mu$m channel length. The ON-resistance for ASPM-2 is 115 m$\Omega$ at a gate bias of 10 V and current density of 100 A/cm$^2$, which is a factor of 1.39x smaller than the other two ASPMs. The reduction in total ON-resistance by a factor of 1.39x is smaller than the factor of 1.837x reduction of channel resistance mentioned in Section III because the channel constitutes only 38% of the total ON-resistance for ASPM-1. The internal distributions of the ON-resistance obtained by analytical models [16] for ASPM-2 are 26% for the channel, 10% for the accumulation layer, 3% for the JFET region, 11% for the drift region, and 36% for the substrate.

For completeness, the measured output characteristics for the CooLMOS product are included in Fig. 5. Its measured ON-resistance at $V_{\mathrm{gs}} = 10$ V is 180 m$\Omega$ (consistent with its datasheet value), which is close to that of ASPM-1 and ASPM-3.

### C. Transfer Characteristics and Transconductance

The transfer characteristics for ASPM-1 and ASPM-2, shown in Fig. 6, were obtained at a drain bias of 20 V up to a drain current of 20 A. The transfer characteristic for ASPM-2 lies above the ASPM-1 device due to its shorter 0.3 $\mu$m channel length. The transfer characteristics for ASPM-3 is not shown because it overlaps that for ASPM-1 due to the same 0.5 $\mu$m channel length and 2.8 $\mu$m cell pitch. The threshold voltage for all the devices was obtained similar to datasheets by incrementing the gate voltage until a drain current of 1 mA was observed. The measured threshold voltage for ASPM-2 was smaller (1.8 V) than ASPM-1 (1.9 V) due to drain induced barrier lower effects at shorter channel length [27]. The threshold voltage for ASPM-3 was the same as ASPM-1 because of the same P-base doping profile and gate oxide thickness.

The transconductance was computed from the transfer characteristics for the ASPMs and is plotted in Fig. 6. The $G_m$ is given by [16]

$$G_m = \frac{Z\mu_{\mathrm{ni}}C_{\mathrm{OX}}}{L_{\mathrm{CH}}}(V_{\mathrm{gs}} - V_{\mathrm{TH}}) \tag{2}$$

where $Z$ is the channel width, $\mu_{\mathrm{ni}}$ is the channel mobility, $C_{\mathrm{OX}}$ is the specific gate oxide capacitance, $L_{\mathrm{CH}}$ is the channel length, $V_{\mathrm{gs}}$ is the gate bias, and $V_{\mathrm{TH}}$ is the threshold voltage. The $G_m$ values are indicated by dotted lines in Fig. 6 at the same ($V_{\mathrm{G}}$-$V_{\mathrm{TH}}$) for ASPM-1 and ASPM-2. The $G_m$ for ASPM-2 is about 1.8x larger than ASPM-1 because its channel length is shorter by a ratio of 1.67x and its channel width is 1.08x larger. The $G_m$ for ASPM-3 is the same as that for ASPM-1 due to the same channel length and cell pitch.

### D. Input, Output, and Reverse-Transfer Capacitances

The input, output, and reverse-transfer capacitances were measured up to a drain bias of 400 V at a frequency of 100 kHz

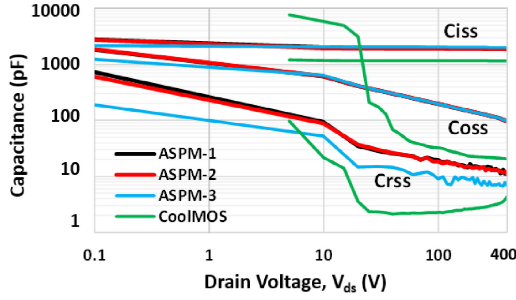


Fig. 7. Measured input, output, and reverse transfer capacitances for the three advanced SiC power MOSFETs and the CoolMOS IPW65R190C7 product.

for all three ASPMs. The dependence of these capacitances on the applied drain bias is shown in Fig. 7. As in the case of other power MOSFETs, the input capacitance ($C_{\rm iss}$) is a weak function of drain bias [16]. Its magnitude is approximately 2000 pF at a drain bias of 400 V for all three ASPMs. The measured input capacitance for the CoolMOS product is 1150 pF about half that of the ASPM devices.

The output capacitance ($C_{\rm oss}$) for the ASPMs is determined by the junction between the $P^+$ shielding region and the N- drift region [18]. Its value decreases with increasing drain bias due to the expansion of the depletion layer formed at the junction. The ASPM-1 and ASPM-3 have the same cell width and junction area as illustrated in Fig. 2. In both cases, the P–N junction area occupies $(2.1/2.8) = 0.73$ of the cell area. Consequently, they have identical output capacitance curves with a value of 97 pF at a drain bias of 400 V. The P–N junction for ASPM-2 occupies $(1.9/2.6) = 0.75$ of the cell area. This value is close to that for the other ASPMs and its measured output capacitance is close (95 pF) at a drain bias of 400 V. The $C_{\rm oss}$ for the CoolMOS product was measured for comparison with the ASPMs. It has a low value of 17 pF at 400 V but becomes extremely large (9000 pF) at a drain bias of 5 V. This large output capacitance is associated with the large area of the vertical P–N junctions within the CoolMOS structure to produce the desired charge-coupling effect needed to achieve a low ON-resistance [28]. The $C_{\rm oss}$ for the devices is determined by their active area and drift region depletion width at high drain bias voltages. The drift region and depletion width for the CoolMOS device is 35 microns compared to 5 microns for the SiC devices and their active areas are given in Table II. Using these values, the $C_{\rm oss}$ for the CoolMOS device is calculated to be a factor of 5.63x smaller than for the ASPMs which agrees with a measured ratio of 5.7x.

The reverse-transfer (or gate-drain) capacitance ($C_{\rm rss}$) for the ASPMs is created by the overlap of the gate electrode with the JFET region in the planar-gate structure [16]. The JFET region for all three of the ASPMs is identical with a width ($W_{\rm JFET}$) of 0.7 $\mu$m as shown in Fig. 2. However, this does not result in equal values for $C_{\rm rss}$ for all three structures as observed in Fig. 7. The $C_{\rm rss}$ for the ASPM-2 is larger than that observed for ASPM-1 because its smaller channel length shrinks the cell width ($W_{\rm cell}$) as shown in Fig. 2. This makes the percentage area of the JFET region in ASPM-2 larger than for ASPM-1. The magnitude of $C_{\rm rss}$ at a drain bias of 400 V for ASPM-2 is 11 pF while that for ASPM-1 is 10.8 pF.

TABLE II
COMPARISON OF STATIC CHARACTERISTICS FOR 650-V DEVICES

| Parameter | NCSU SiC ASPM-1 | NCSU SiC ASPM-2 | NCSU SiC ASPM-3 | Infineon Si COOLMOS |
|---|---|---|---|---|
| On-State Gate Bias $V_{gs}$ [V] | 10 | 10 | 10 | 10 |
| Breakdown Voltage (BV) [V] | 850 | 850 | 850 | 710 |
| On-State Resistance ($R_{on}$) [mΩ] | 160 | 115 | 160 | 180 |
| On-State Voltage Drop $V_{on}$ @ 10 A [V] | 1.8 | 1.3 | 1.8 | 1.9 |
| Threshold Voltage $V_{th}$ [V] | 1.9 | 1.8 | 2.0 | 3.5 |
| Tranconductance $G_m$ @ $V_d$=20V [S] | 7.0 | 13 | 7.0 | 20 |
| Input Capacitance $C_{iss}$ @ 400V [pF] | 1930 | 1860 | 2000 | 1150 |
| Output Capacitance $C_{oss}$ @ 400V [pF] | 97 | 95 | 97 | 17 |
| Output Capacitance $C_{oss}$ @ 1 V [pF] | 620 | 600 | 620 | 13,000 |
| Reverse-Transfer Capacitance $C_{rss}$ @ 400V [pF] | 10.8 | 11 | 6.8 | 4 |
| Reverse-Transfer Capacitance $C_{rss}$ @ 1 V [pF] | 90 | 80 | 60 | 900 |
| Active Area [$cm^2$] | 0.045 | 0.045 | 0.045 | 0.056 |
| $R_{on,sp}$ [mΩ-$cm^2$] | 7.2 | 5.18 | 7.2 | 10 |

The reverse transfer capacitance for ASPM-3 is substantially smaller than for ASPM-1 and ASPM-2. This difference is deliberately produced by the employment of the SG design in ASPM-3 [24]. The measured magnitude of $C_{\rm rss}$ for ASPM-3 was 6.8 pF at a drain bias of 400 V, which is near the noise limit for the wafer probe measurements. The measured magnitude of $C_{\rm rss}$ for ASPM-3 was 60 pF at a drain bias of 10 V compared with 90 pF for the other devices.

The reverse transfer capacitance for the CoolMOS product is 4.0 pF at a drain bias of 400 V which is smaller than that of the ASPMs. However, it becomes very large at small drain bias voltages. A value of 900 pF was measured at a drain bias of 1 V. This increases the gate-drain charge as discussed later.

*E. Gate-Drain Charge:* The gate-drain charge ($Q_{\rm gd}$) is an important parameter for power MOSFETs because it determines the duration of the drain voltage transient and hence the switching losses [16]. The gate-charge characteristics for the three ASPMs, measured using a drain voltage of 300 V and a drain current of 10 A, are shown in Fig. 8. The gate plateau voltage for ASPM-2 (6.8 V) is smaller than ASPM-1 (7.2 V) due its larger $G_m$. The larger $G_m$ for ASPM-2 also makes its measured total gate charge ($Q_g$) slightly smaller than for ASPM-1. The gate-source charge ($Q_{\rm gs}$) is equal for ASPM-1 and ASPM-3 because they have the same plateau voltage ($V_{\rm GP}$). (The plateau in the gate voltage for ASPM-3 is less distinct due to the SG form.) The plateau voltage is determined by the drain current, $G_m$, and $V_{\rm TH}$ [16], which are identical for these structures as

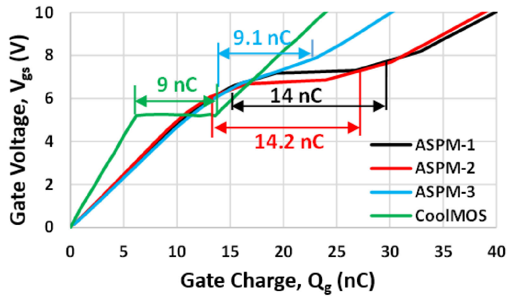


Fig. 8. Measured gate charge for the three Advanced SiC power MOSFETs using a drain bias of 300 V and drain current of 10 A and CoolMOS IPW65R190C7 at drain bias of 400 V and drain current of 5.7 A.

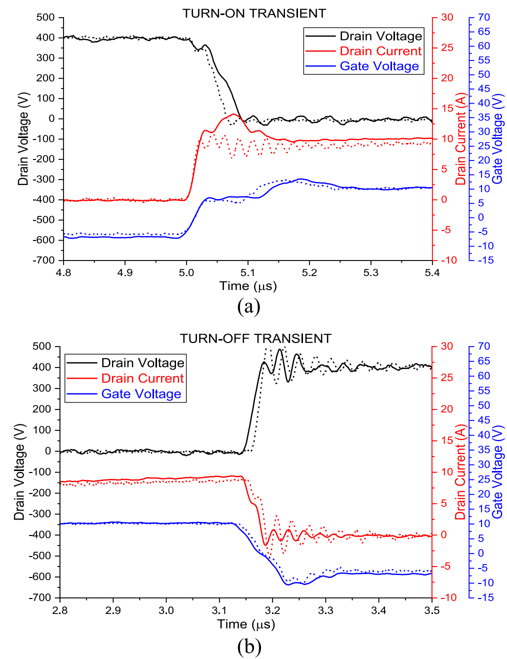


Fig. 9. Measured drain voltage (black) and current (red) waveforms for ASPM-1 (solid) and ASPM-2 (dotted) measured using $R_g = 2.5\Omega$. (a) Turn-ON transients. (b) Turn-OFF transients. Gate voltage transients ranging from $-5$ to $+10$ V are also shown in blue.

reported in previous sections. The $Q_{\rm gs}$ for ASPM-2 is slightly smaller because its plateau is reduced by a larger $G_m$ for the structure due to its shorter channel length.

The gate-drain charge ($Q_{\rm gd}$) is different for the three ASPM structures for the same reasons discussed in the previous part on the reverse transfer capacitance. The measured value for $Q_{\rm gd}$ for ASPM-2 is larger than for ASPM-1 due to its smaller cell width and equal JFET width, which increases the JFET density. The measured value for $Q_{\rm gd}$ for ASPM-3 is much smaller than for ASPM-1 due to the SG design, which reduces the area of overlap between the gate electrode and the drift region [24]. The measured values of $Q_{\rm gd}$ are 14, 14.2, and 9.1 nC for ASPM-1, ASPM-2, and ASPM-3, respectively.

The gate charge characteristics for the CoolMOS product is also shown in Fig. 8. The $Q_{\rm gd}$ for this device is 9 nC which is close to that of ASPM-3.

### F. Switching Power Losses

The total power loss incurred within a power MOSFET in applications is the sum of the conduction loss related to its ON-resistance and the switching losses due to drain voltage and current transients during both turn-ON and turn-OFF. The switching losses were obtained by using the typical double-pulse method with the Cree evaluation board KIT8020-CRD-8FF1217P-1. The same values of drain bias of 400 V, drain current of 10 A, gate drive voltage of 10 V, and gate drive resistance of 2.5 Ω were used for all three devices. A low gate drive resistance of 2.5 Ω is often used in commercial SiC power MOSFET datasheets to minimize the switching losses [8], [9]. The same type of power MOSFET (e.g. ASPM-1) with its gate-source shorted was placed at the high-side (across the inductor) and same type of power MOSFET (e.g. ASPM-1) was placed on the low-side locations in the double-pulse circuit to measure the impact of the body diode reverse recovery.

The measured switching transients for the drain voltage and drain current are shown in Fig. 9 for the case of ASPM-1 and ASPM-2. Faster voltage transients during turn-ON and turn-OFF are observed for ASPM-2 which reduces the switching losses. A turn-ON energy loss of 210 $\mu$J and turn-OFF energy loss of 25 $\mu$J was extracted for ASPM-1 from the switching transients leading to a total switching energy loss of 235 $\mu$J. A turn-ON energy loss of 124 $\mu$J and turn-OFF energy loss of 24 $\mu$J was extracted for ASPM-2 from the switching transients leading to a total switching energy loss of 148 $\mu$J. The reduced switching losses measured for ASPM-2 compared with ASPM-1 are produced by its larger $G_m$ due to a shorter channel length. A larger $G_m$ for ASPM-2 shortens its current rise-time. More significantly, it reduces the plateau voltage for ASPM-2 leading to a faster drain fall time [16] as observed in Fig. 9(a).

### G. SC Capability

It is well documented [29], [30] that the SC capability of commercially available 1.2-kV SiC power MOSFETs is only about 3.5 $\mu$s when testing at a drain bias of 800 V and gate bias of 20 V, which is well below the 10 $\mu$s value for commercially available Si IGBT products. An improvement in the SC capability for 1.2-kV SiC power MOSFETs by reduction of the gate oxide thickness was previously reported [31]. This improved performance should also occur for the ASPMs fabricated in this study with a reduced gate oxide thickness of 27 nm but required verification.

Short-circuit characterization was conducted by turning-on the ASPM-1 using 10 V gate pulses with a dc drain voltage of 400 V without any load. The width of the gate pulse was incremented for the same device until destructive failure was observed. The measured SC waveforms for the drain current are shown in Fig. 10 for ASPM-1 with gate pulse width incremented up to 8.4 $\mu$s beyond which the device failed. A peak drain current of 110 A is observed at 2.5 $\mu$s followed by decline to 60 A due to temperature rise. An increase in gate leakage current after even short pulses without failure have been reported for 1.2-kV

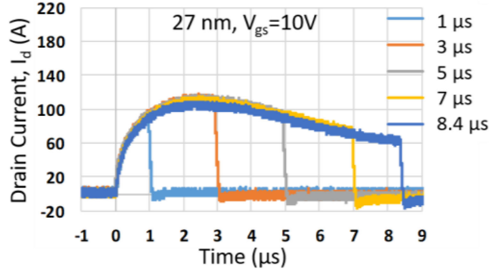


Fig. 10. Short circuit waveforms for a single ASPM-1 device at $V_{\rm ds} = 400$ V and $V_{\rm gs} = 10$ V with increasing pulse width.

SiC power MOSFETs [32]. This behavior was not obvious during the testing of the ASPM-1 device even with the reduced 27 nm gate oxide thickness. The slight reduction of the peak current for the last pulse may indicate a degradation of the gate oxide, but the device failed during this test. The SC test confirms that a significantly (2.4x) longer SC time can be obtained using the ASPM-1 structure with 27 nm gate oxide thickness and gate drive voltage of 10 V than typically reported for commercially available 1.2-kV SiC power MOSFETs.

The peak SC current for the ASPM-2 can be expected to be 1.67x larger than for ASPM-1 due the shorter channel length producing a larger $G_m$ as shown in the previous section. It has been established that the SC time is inversely proportional to the SC drain current both from a theoretical [16] and experimental basis [33]. Consequently, the SC capability for ASPM-2 is projected to be 5.0 $\mu$s. The ASPM-3 has the same channel length and gate oxide thickness as ASPM-1 resulting in the same magnitude for the $G_m$ as shown in previous sections. Consequently, its peak SC current is the same as for ASPM-1, which results in an SC capability of 8.4 $\mu$s for this device.

## VII. Discussion

The measured electrical performance of the 650-V advanced SiC power MOSFETs with three improved device structures has been described in the previous section. It is appropriate to compare their relative performance and quantify the difference between these devices. In addition, it is important to compare them with the commercially available 650-V state-of-the art Si superjunction transistors they are intended to replace.

### *A. Static Characteristics*

The measured static characteristics for the three types of ASPMs are given in Table II based up on the data shown in the previous section. The values from the datasheet for the state-of-the-art Si superjunction MOSFET manufactured by Infineon (COOLMOS 7th Gen product IPW65R190C7) are included in the fourth column for comparison. These values were verified by performing the same type of tests used for the ASPM devices. The ASPM-1 and ASPM-3 have an ON-resistance of 160 m$\Omega$ at a gate bias of 10 V, which is close to the 180 m$\Omega$ value for the chosen Si superjunction product. The ON-resistance value for the ASPM-2 is 115 m$\Omega$ at a gate bias of 10 V, which is smaller than that of the chosen Si superjunction product. Its conduction losses are consequently much lower than that for the other ASPMs and the Si superjunction device.

The threshold voltage for the ASPMs is about 1.9 V compared with a value of 3.5 V for the COOLMOS device. This lower value is still sufficient for noise immunity during switching in power circuits because the gate voltage spikes remain below 0 V when a typical gate drive of $-5$ V is used to turn-OFF the devices in half-bridge topologies [34].

The measured transconductance ($G_m$) for the ASPM-1 and ASPM-3 have the same value of 7.0 S as discussed earlier. The ASPM-2 has a $G_m$ of 13 S due to its shorter channel length. The $G_m$ for all the ASPMs is much smaller than reported for the COOLMOS device because the inversion-channel mobility in Si is an order of magnitude larger than in SiC devices.

The measured input capacitance ($C_{\rm iss}$) for the three ASPMs are approximately equal and 1.65x larger than for the COOLMOS device. The larger input capacitance observed for the SiC MOSFETs is attributed to the thin gate oxide of 27 nm required for operation at a gate bias of 10 V. The calculated ratio of the input capacitance is 1.61x if the Si CoolMOS oxide thickness is twice that for the ASPM devices and active area (given in Table II) ratio of 1.24x is taken into account.

The measured output capacitance ($C_{\rm oss}$) for the three ASPMs are equal and 5.5x larger than for the COOLMOS device at a drain bias of 400 V. The charge-coupled structure in the Si superjunction structure is designed to completely deplete at a drain bias of about 25 V. This makes the $C_{\rm oss}$ of this device decrease drastically above a drain bias of 25 V at seen in the device datasheet and Fig. 7. In contrast, the $C_{\rm oss}$ of the SiC power MOSFETs decreases more gradually with increasing drain bias.

A different picture emerges in the case of small drain bias voltages. For a reduced drain bias of 1 V, the $C_{\rm oss}$ of the COOLMOS device becomes very high with a value of 13,000 pF in the device datasheet and 9000 pF at 5 V from the measured data in Fig. 7. In the case of the three ASPMs, the $C_{\rm oss}$ increases to only 600 pF at 1 V, which is a factor of 22x smaller. During switching, the MOSFET drain bias varies from its ON-state value of about 1.6 V to the power supply value of 400 V. Consequently, a larger output capacitance must be charged and discharged in the Si superjunction device slowing down its switching transients when compared with the ASPMs.

The measured reverse-transfer capacitance ($C_{\rm rss}$) for the ASPM-1 and ASPM-2 are close as discussed earlier. The measured $C_{\rm rss}$ value is only 11 pF at a drain bias of 400 V but 2.8x larger than for the COOLMOS device. The value for ASPM-3 is only 1.7x larger than for the COOLMOS device. The $C_{\rm rss}$ increases drastically for the COOLMOS device when the drain bias is reduced below 25 V as observed in the datasheet and the measured data in Fig. 7. At a reduced drain bias of 1 V, the $C_{\rm rss}$ of the COOLMOS device becomes 900 pF. In the case of the three ASPMs, the $C_{\rm rss}$ increases to only 60–90 pF, which is a factor of 10–15x smaller. The MOSFET drain bias varies during switching from its ON-state value of about 1.6 V to the power supply value of 400 V. Consequently, a larger reverse-transfer capacitance must be charged and discharged in the Si superjunction devices compared with the ASPMs. This produces a smaller turn-OFF

TABLE III
COMPARISON OF DEVICE SWITCHING CHARACTERISTICS

| Parameter | NCSU SiC ASPM-1 | NCSU SiC ASPM-2 | NCSU SiC ASPM-3 | Infineon Si COOLMOS |
|---|---|---|---|---|
| Total Gate Charge $Q_g$ [nC] | 40 | 39 | 30 | 23 |
| Gate-Source Charge $Q_{gs}$ [nC] | 15.2 | 13.1 | 14 | 8.5 |
| Gate-Drain Charge $Q_{gd}$ [nC] | 14 | 14.2 | 9.1 | 9 |
| Reverse Recovery Time $t_{rr}$ [ns] | 120 @ dI/dt of 650A/µs | 100 @ dI/dt of 650A/µs | 120 @ dI/dt of 650A/µs | 830 @ dI/dt of 55A/µs |
| Reverse Recovery Charge $Q_{rr}$ [nC] | 235 | 60 | 235 | 6500 |
| (Peak $I_{rr}$)/$I_d$ @ dI/dt=650A/µs [A] | 0.4 | 0.12 | 0.4 | > 5 |
| Turn-on Switching Energy $E_{on}$ [µJ] | 210 $R_g$=2.5Ω | 124 $R_g$=2.5Ω | 180 $R_g$=2.5Ω | 2650 $R_g$=100Ω |
| Turn-off Switching Energy $E_{off}$ [µJ] | 25 $R_g$=2.5Ω | 24 $R_g$=2.5Ω | 12 $R_g$=2.5Ω | 55 $R_g$=100Ω |
| Total Switching Energy $E_{total}$ [µJ] | 235 $R_g$=2.5Ω | 148 $R_g$=2.5Ω | 192 $R_g$=2.5Ω | 2705 $R_g$=100Ω |

energy loss for the ASPMs as found in the measured data reported in the previous section.

### *B. Dynamic Characteristics*

The measured dynamic characterization data for the three ASPMs can be compared with each other and the Si COOLMOS product using Table III.

The total gate charge ($Q_g$) for ASPM-1 and ASPM-2 is the same. It is smaller for the ASPM-3 due to its reduced $Q_{\rm gd}$. The $Q_g$ for the Si superjunction device is much smaller. The gate-source charge ($Q_{\rm gs}$) for the three ASPMs is similar and larger than for the Si COOLMOS product. This is due to the smaller $G_m$ for these devices because of the low channel mobility in SiC power devices.

The gate-drain charge ($Q_{\rm gd}$) for ASPM-1 and ASPM-2 are equal and larger than that of the Si COOLMOS product. It is much smaller for ASPM-3 due to the SG implementation, with a value equal to the Si COOLMOS device.

The switching tests based on the double-pulse method allows obtaining not only the power MOSFET switching losses, but also the reverse recovery behavior of the MOSFET internal body diode. For this purpose, it is necessary to use the same type of MOSFET on the high-side across the inductor as on the low side during the switching tests. The drain current turn-ON transients obtained with ASPM-1 and ASPM-2 are shown in Fig. 11 for the case of a drain supply voltage of 400 V, ON-state drain current of 10 A, and a gate drive resistance of 2.5 Ω. The observed small overshoot in the drain current during turn-ON represents the body diode reverse recovery current. The peak reverse recovery current is about 4 A for ASPM-1 giving a ratio ($I_{\rm rr}/I_d$) of 0.4 given in Table III with the *dI/dt* of 650 A/$\mu$s during this test. The peak reverse recovery current for ASPM-2 is only 1.2 A under the same *dI/dt* conditions.

The reverse recovery information in the datasheet for the Si COOLMOS product is provided at a much smaller *dI/dt* of 55 A/$\mu$s. Turn-ON transient test were performed on the Si COOLMOS product in this study for comparison with the ASPMs. It was found that the Si devices failed when turned-ON with a *dI/dt* of 650 A/$\mu$s due to a very large peak reverse recovery current. The results obtained with turn-ON performed using a *dI/dt* of 65 A/$\mu$s obtained by using a $R_G = 100\ \Omega$ for the Si COOLMOS product are shown in Fig. 11 with a reduced ON-state current of only 5.7 A per its datasheet. A large peak reverse recovery current of about 20 A is observed in this case. The ratio ($I_{\rm rr}/I_d$) for the Si COOLMOS product given in Table III is consequently $>5$ for the larger *dI/dt* of 650 A/$\mu$s.

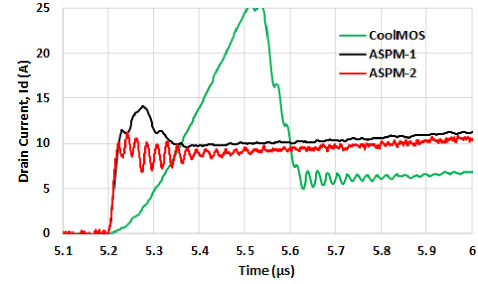


Fig. 11. Measured turn-on drain current transient at $V_{\rm ds} = 400$ V for an ON-state current 10 A for ASPM-1 and ASPM-2 with $R_g = 2.5\ \Omega$ and for the COOLMOS product at an ON-state drain current of 5.7 A with a much larger $R_g = 100\ \Omega$.

A reverse recovery time ($t_{\rm rr}$) of 120 ns and 100 is observed from the turn-ON transient for ASPM-1 and ASPM-2 at a *dI/dt* of 650 A/$\mu$s. A reverse recovery charge ($Q_{\rm rr}$) of 235 nC was extracted from the turn-ON transient for the ASPM-1 and 60 nC for ASPM-2. The values for $t_{\rm rr}$ and $Q_{\rm rr}$ for ASPM-3 are equal to those for ASPM-1 due to identical cell size and junction area.

The reverse recovery time and charge for the Si COOLMOS product are given in Table III as reported in its datasheet at a *dI/dt* of 55 A/$\mu$s. The $Q_{\rm rr}$ is a measure of power losses in circuits due to the body diode reverse recovery phenomenon. The ASPMs have $Q_{\rm rr}$ values that a factor of 27-times smaller than the Si COOLMOS product. The large reverse recovery switching power loss associated with the Si COOLMOS product can be mitigated by connecting a SiC JBS diode across the device.

Previous studies have been published comparing the performance of SiC power MOSFETs with Si CoolMOS devices. One example [35] is a comparison between a 1200-V SiC power MOSFET and a 600-V Si CoolMOS device. No reduction of ON-resistance was observed for the CoolMOS device with gate bias above 10 V. A low-voltage Si Schottky diode was used in series with the Si CoolMOS device to prevent body diode conduction. In addition, an anti-parallel SiC Schottky diode was used. Another example [36] is a comparison between 900 V SiC power MOSFETs and 900 V Si CoolMOS devices. A very large reverse recovery current was observed for the body diode necessitating increasing the gate resistance as observed in our tests. It was pointed out that a low-voltage Si Schottky diode must be connected in series with the CoolMOS device to prevent body diode conduction leading to significant increase in converter complexity. The approach and its complexity has been reported in other papers as well [37], [38]. In summary, the solution to

TABLE IV
COMPARISON OF SC CAPABILITY

| Parameter | NCSU SiC ASPM-1 | NCSU SiC ASPM-2 | NCSU SiC ASPM-3 | Infineon Si COOLMOS |
|---|---|---|---|---|
| Short-Circuit Time [μs] | 8.4 | 5.0 | 8.4 | 19 |
| SC Energy Density [J/cm$^2$] | 6.0 | 6.0 | 6.0 | 6.7 |

TABLE V
COMPARISON OF DEVICES

| Parameter | NCSU SiC ASPM-1 | NCSU SiC ASPM-2 | NCSU SiC ASPM-3 | Infineon Si COOLMOS |
|---|---|---|---|---|
| High-Frequency Figure of Merit HF-FOM($R_{on}$*$Q_{gd}$) [mΩ-nC] | 2,240 | 1,633 | 1,456 | 1,620 |
| Figure-of-Merit FOM ($C_{iss}$/$C_{rss}$) | 179 | 169 | 294 | 288 |
| Figure-of-Merit FOM($R_{on}$*$Q_{rr}$) [mΩ-nC] | 37,600 | 6,900 | 37,600 | 1,170,000 |
| Figure-of-Merit FOM($V_{on}$*$E_{Total}$) [V- μJ] | 423 | 207 | 346 | 5140 |

the reverse recovery problem increases ON-state voltage drop with larger conduction power losses for the Si CoolMOS device, and adds extra cost and additional packaged components to the power electronics.

The measured switching energy loss during turn-ON and turn-OFF are given in Table III for ASPM-1 and ASPM-2 for the case of a gate drive resistance of 2.5 Ω and a gate drive voltage of 10 V. The ASPM-2, with shorter channel length, has much smaller turn-ON switching loss than ASPM-1 due to its larger transconductance. The switching losses for the Si COOLMOS product given in Table III were obtained using the data taken from the test shown in Fig. 11 and scaling the losses to 10 A. The turn-ON switching losses for the ASPM-1 and ASPM-2 are a factor of 12.6x and 21.2x smaller than for the Si COOLMOS product. The ASPM-3 structure could not be packaged and tested in time for inclusion in this article. The switching losses for the ASPM-3 were therefore obtaining using the data for ASPM-1 and accounting for a reduced $Q_{\rm gd}$ by a factor of 1.26x. The smaller $Q_{\rm gd}$ proportionally reduces the drain voltage fall time leading to smaller power loss [16]. Its switching loss falls in between that for ASPM-1 and ASPM-2.

The SC withstand capability of SiC power MOSFETs is of interest in motor control applications. The values of the SC time for the ASPMs are given in Table IV for the case of a drain supply voltage of 400 V and gate drive voltage of 10 V. The SC capability of the Si COOLMOS product is not provided in the datasheet. Measurement of this device were conducted using the same conditions as the SiC MOSFETs. It was found that these devices had excellent SC time of 19 $\mu$s. The specific ON-resistance of 650-V Si COOLMOS devices has been reported as 10 mΩ-cm$^2$ [39], [40]. An active area of 0.056 cm$^2$ in Table II was calculated for the 180 mΩ CoolMOS device by using this value. The active area for the Si COOLMOS device is 1.24x

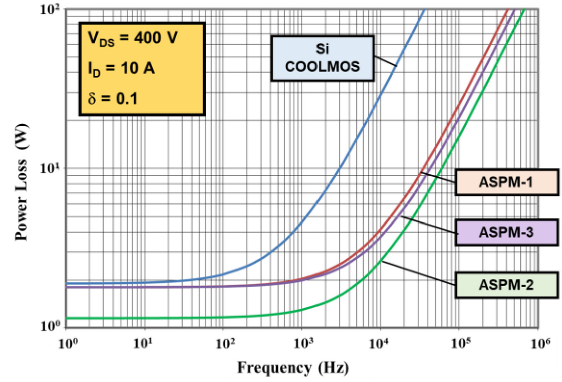


Fig. 12. Calculated power loss as a function of operating frequency for the advanced SiC power MOSFETs and the Si COOLMOS product.

larger and its depletion region is 6x larger than the ASPMs, extending its short circuit time, which is determined by the semiconductor volume being heated during the short circuit event [16]. The SC energy density calculated for the devices is listed in the table.

## VIII. CONCLUSION

This article has reported the manufacturing of Advanced SiC power MOSFETs with a blocking voltage rating of 650 V and gate drive voltage of 10 V for compatibility with Si superjunction products. Several figures-of-merit (FOM) have been defined to allow comparison of power MOSFETs built using various technologies [16]. The values for these FOM are given in Table V for the ASPMs manufactured for this article.

The high frequency figure-of-merit [HF-FOM($R_{\rm on}*Q_{\rm gd}$)] for the ASPM-1 is 2240, a factor of 1.4x larger than that for the Si COOLMOS product. This would imply lower switching losses for the Si superjunction device. However, this HF-FOM does not account for the large turn-ON switching loss observed in the Si COOLMOS product due to huge reverse recovery current from its body diode. The HF-FOM($R_{\rm on}*Q_{\rm gd}$) for ASPM-2 is 1633, which is equal to the Si COOLMOS product. The HF-FOM for ASPM-3 is 1456, about 1.11x smaller than that for the Si COOLMOS product.

The figure-of-merit ($C_{\rm iss}/C_{\rm rss}$) is a useful measure of shoot-through immunity for power MOSFETs operating in high frequency circuits with large *dV/dt* excursions. The calculated value for the ASPMs is given in Table V with that for the Si COOLMOS product. It is lower (worse) than for the Si superjunction device because of the very low $C_{\rm rss}$ in this structure at large drain bias voltages. The magnitude of this FOM is however adequate for all the devices to provide good immunity against shoot-through issues.

The figure-of merit ($R_{\rm on}*Q_{\rm rr}$) calculated for the ASPMs is given in Table V together with that for the Si COOLMOS product. The large reverse recovery charge for the Si superjunction device makes its FOM about 60x worse than for the SiC MOSFET manufactured for this article.

Another figure-of-merit that can be used to assess the overall power losses in a power transistor is the product of the ON-state

voltage drop and the total switching loss. This FOM($V_{\text{on}} * E_{\text{Total}}$) can be used to compare MOSFETs with IGBTs, which have a knee in the ON-state characteristics. The calculated value for this FOM, given in Table V for the ASPMs, is about 12–25x better (smaller) than for the Si COOLMOS product.

The power loss incurred in the transistors can be computed by summing the conduction loss and the switching loss, which is a function of the frequency. The conduction loss can be obtained as the product of the ON-state voltage drop, the drain current level, and the operating duty cycle. The switching loss can be obtained as the product of the total switching loss and the frequency. The case of a dc supply voltage of 400 V and a drain current of 10 A, with a duty cycle of 0.1, was modeled for the three ASPMs and the Si COOLMOS product using the ON-state voltage drop from Table II and total energy loss per cycle from Table III. The plots in Fig. 12 show that all three ASPMs have superior (lower) power loss at all frequencies than the Si COOLMOS product. The lowest power loss is observed for the ASPM-2 due to its low ON-resistance and switching loss. Its power loss is only 16 W (0.4%) at 100 kHz versus 272 W (6.8%) for the Si COOLMOS device, a factor of 17x smaller. The reverse recovery power loss in the Si CoolMOS device can be reduced by adding a series Si Schottky diode to prevent body diode conduction and an antiparallel SiC diode. This will however increase the ON-state power loss and converter complexity.

In conclusion, the advanced SiC power MOSFETs manufactured for this article provide a significant improvement in power circuit operation as replacements for Si superjunction devices with a compatible 10 V gate drive. The experimental results reported in this article should encourage manufacturers of SiC power MOSFETs to consider reducing the gate oxide thickness and the channel length; and utilize the SG architecture to produce superior devices.

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