Adaptive Gate Delay-Time Control of Si/SiC Hybrid Switch for Efficiency Improvement in Inverters

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***Abstract*—Varying gate delay time of the Si insulated-gate bipolar transistor/SiC MOSFET hybrid switch is the key to achieving high efficiency of Si/SiC-hybrid-switch-based power converters because of time-varying characteristics of its junction temperature and operation current. Based on the swarm intelligent algorithm, a novel adaptive delay-time control method of the Si/SiC hybrid switch in an inverter is proposed to achieve higher efficiency than the traditional fixed delay time. In addition, by evaluating the fitness values, the proposed method can easily achieve this goal without establishing the physics-based analytical model of device loss and additional hardware support. The platform of the Si/SiC-hybrid-switch-based single-phase inverter is established and tested, and the particle swarm optimization algorithm is taken as example. Experimental results demonstrate that the proposed technique yields 6.2% reduction in the total loss of the single-phase inverter compared to a fixed delay time.**

***Index Terms*—Adaptive control, modeling, optimization methods, power semiconductor switches.**

I. Introduction

A Si/SiC hybrid switch comprising a small-capacity silicon carbide (SiC) MOSFET and a large-capacity silicon (Si) insulated-gate bipolar transistor (IGBT) in parallel not only demonstrates its advantages in the cost and performance, but also possesses high redundancy. Therefore, it is perceived as the key enabler of high reliability, high efficiency, and low cost in the application of power converters [1]–[3]. Generally, the internal SiC MOSFET should be turned ON earlier and turned OFF later than the internal Si IGBT to achieve the zero-voltage turn-OFF of the IGBT and low switching loss of the Si/SiC hybrid switch [4]–[6]. It means that the optimal gate delay time between the SiC MOSFET and the Si IGBT is required for the efficiency improvement of the Si/SiC-hybrid-switch-based power converters.

Most previous research works mainly focused on studying the optimal fixed delay time to achieve the power loss reduction of the Si/SiC-hybrid-switch-based power converters [7]–[13]. In [7]–[11], the relationship between the power loss of the Si/SiC hybrid switch and its internal delay time can be established through the double-pulse test (DPT) and single-pulse test experiments. Then, the optimal fixed delay time can be obtained and applied to power converters. In [12] and [13], power losses of inverters at different delay times are compared, and the optimal fixed delay time is recommended with the smallest power loss. However, the junction temperature and the operation current of the Si/SiC hybrid switch in inverters are time varying, resulting in large change in the conduction and switching conditions of the Si/SiC hybrid switch [2], [14]. It means that the minimum conduction loss and switching loss of the Si/SiC hybrid switch at various current levels cannot be simultaneously achieved by the fixed delay time, leading to nonoptimized efficiency improvement of the Si/SiC hybrid switch.

In order to further improve the efficiency of the Si/SiC-hybrid-switch-based inverters, the delay time need to be time varying with different operation conditions of inverters, and an accurate loss model of the Si/SiC hybrid switch is needed to obtain the delay time. In [15] and [16], the corresponding loss model was established by analyzing the conduction and switching characteristics of the Si/SiC hybrid switch. The conduction loss model can be established by the I–V characteristics curve of the Si/SiC hybrid switch, and the switching loss model can be established by testing the Si/SiC-hybrid-switch-based double pulse clamped inductive load circuit. Therefore, the optimal time-varying delay time can be obtained by these loss models. However, the establishment of the Si/SiC hybrid switch's loss model is based on a single operation state, and the different operation states of the power electronics system are not considered. It means that the proposed methods in these papers are only suitable for the dc–dc converter, where both the current and the device junction temperature are almost constant. In fact, in the application of the Si/SiC-hybrid-switch-based inverters, few researchers have attempted to further improve the efficiency of these inverters by obtaining the optimal time-varying delay time. And, the traditional method for obtaining the optimal time-varying delay time by solving the device loss model will face significant challenges, i.e., acquiring the complex physics-based analytical model of

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device loss and the additional hardware burden. Therefore, a simple and effective method has yet to be explored.

In this article, a novel adaptive delay-time control method adopting the swarm intelligent algorithm is proposed to solve these problems. It does not require the physics-based analytical model of device loss and the additional hardware support, but only needs to evaluate the fitness values to easily achieve the efficiency improvement of the Si/SiC-hybrid-switch-based inverter. The classical particle swarm optimization (PSO) algorithm in the swarm intelligent algorithm and the single-phase inverter are taken as example, and the main contributions of this article are listed as follows.

1) The swarm intelligent algorithm is first applied to the Si/SiC-hybrid-switch-based inverter with significantly improved efficiency by optimizing the time-varying delay time.
2) The optimization idea of the proposed method is simple, and its adaptive optimization process is only guided by a simple fitness function. Therefore, it can effectively overcome the challenges faced by the traditional method.
3) The PSO algorithm does not require high computational costs and real-time performance, so it has little influence on the real-time computation of the DSP, and there is enough room in the DSP to implement other functions.

The rest of this article is organized as follows. In Section II, the topology of the Si/SiC-hybrid-switch-based single-phase inverter is presented at first. Then, the device loss model of the Si/SiC hybrid switch is analyzed. In Section III, the principle of the adaptive gate delay-time control method is given. Experiments are presented in Section IV. Finally, Section V concludes this article.

II. Major Challenges of Obtaining Time-Varying Delay Time

In this section, the topology and power loss distribution of the Si/SiC-hybrid-switch-based single-phase inverter is presented. Then, the major challenges of obtaining the optimal time-varying delay time by solving the device loss model of the Si/SiC hybrid switch are also analyzed. Details are shown as follows.

A. Topology of Si/SiC-Hybrid-Switch-Based Single-Phase Inverter

The topology and power loss distribution of the Si/SiC-hybrid-switch-based single-phase inverter are shown in Fig. 1. As can be seen from Fig. 1, $U_{\rm dc}$, $I_{\rm dc}$, I_o, U_o, L_n ($n = 1, 2$), C, and R represent the dc voltage, dc current, output current, output voltage, filter inductance, filter capacitance, and load, respectively. S_n (n=1, 2, 3, 4) represents the Si/SiC hybrid switch. And $V_{\rm GS\_MOSFET}$ and $V_{\rm GE\_IGBT}$ represent the gate drive signals of the SiC MOSFET and the Si IGBT, respectively. In general, the SiC MOSFET should be turned ON earlier and turned OFF later, which means there is internal delay time in the Si/SiC hybrid switch. And $t_{\rm on\_delay}$ and $t_{\rm off\_delay}$ represent the turn-ON delay time and turn-OFF delay time, respectively.

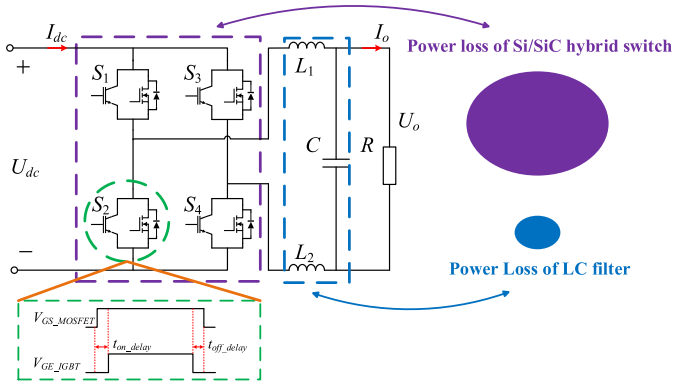

Fig. 1. Topology and power loss distribution of the Si/SiC-hybrid-switch-based single-phase inverter.

B. Device Loss Model of Si/SiC Hybrid Switch

As shown in Fig. 1, the power loss of the LC filter possesses a small part in the total loss of the single-phase inverter [17], [18]. The power losses of the Si/SiC hybrid switches possess a large proportion in the total loss of the single-phase inverter, and they can be easily changed by adjusting their internal delay time. In this article, $t_{\rm on\_delay}$ can be set as 0 μs to facilitate analysis and experiments. When the unipolar sinusoidal pulsewidth modulation (SPWM) strategy is adopted [18]–[20], and S_4 is taken as example, the total power loss of the Si/SiC hybrid switch is calculated as

$$P_l(t_{\rm off\_delay}) = P_s(t_{\rm off\_delay}) + P_c(t_{\rm off\_delay}) \tag{1}$$

where P_s and P_c represent the total switching loss and the total conduction loss of the Si/SiC hybrid switch, respectively. Details about the device loss model are presented in the following.

1) *Switching loss model of Si/SiC hybrid switch:* The total switching loss model is calculated as [14]

$$P_s(t_{\rm off\_delay}) = E_{\rm off\_IGBT}(t_{\rm off\_delay}) + E_{\rm on\_MOS} + E_{\rm off\_MOS} \tag{2}$$

where

$$\begin{cases} E_{\rm off\_IGBT}(t_{\rm off\_delay}) = f_s\left[e^{-\tau\times t_{\rm off\_delay}}\left(\dfrac{a_{pi}I_{oh}^2}{4} + \dfrac{b_{pi}I_{oh}}{\pi} + \dfrac{c_{pi}-E_{sr}}{2}\right) + \dfrac{E_{sr}}{2}\right] \\ E_{\rm on\_MOS} + E_{\rm off\_MOS} = f_s\left[\dfrac{a_{pm}}{4}I_{oh}^2 + \dfrac{b_{pm}I_{oh}}{\pi} + \dfrac{c_{pm}}{2}\right]. \end{cases} \tag{3}$$

In (2) and (3), $E_{\rm off\_IGBT}$, $E_{\rm on\_MOS}$, and $E_{\rm off\_MOS}$ represent the turn-OFF loss of the Si IGBT, turn-ON loss of the SiC MOSFET, and turn-OFF loss of the SiC MOSFET, respectively. f_s, τ, I_{oh}, and E_{sr} represent the switching frequency, exponent related to the turn-OFF delay time, current ON-state current amplitude of the Si/SiC hybrid switch, and residual switching loss of the Si IGBT, respectively. $a_{pi}, b_{pi}, c_{pi}, a_{pm}, b_{pm}$, and c_{pm} are the fitting parameters, which can be obtained by the DPT experiment [14], [21].

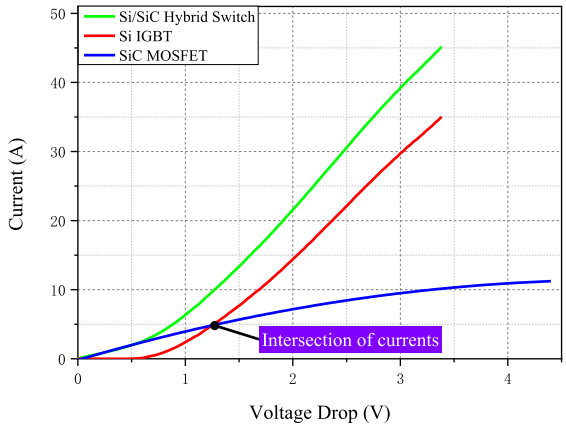

Fig. 2. I–V curve of Si/SiC hybrid switch at $T_j = 150\,^{\circ}\mathrm{C}$, where T_j represents the junction temperature.

2) *Conduction loss model of Si/SiC hybrid switch:* The total conduction loss model is calculated as [14]

$$\begin{cases} P_c(t_{\text{off\_delay}}) = P_{c\_\text{IGBT}}(t_{\text{off\_delay}}) + P_{c\_\text{MOS}}(t_{\text{off\_delay}}) \\ P_{c\_\text{IGBT}} = \dfrac{1}{2\pi}\displaystyle\int_{\sigma}^{\pi-\sigma} R_{c\_\text{IGBT}} i_{oc\_\text{IGBT}}^2 D_{d\_\text{IGBT}} d\theta \\ P_{c\_\text{MOS}} = \dfrac{1}{2\pi}\displaystyle\int_{\sigma}^{\pi-\sigma} R_{c\_\text{MOS}} i_{oc\_\text{MOS}}^2 D_{d\_\text{MOS}} d\theta \\ \qquad + \dfrac{1}{2\pi}\displaystyle\int_{\sigma}^{\pi-\sigma} U_d i_{oc} D_{d\_\text{offdelay}} d\theta \\ \qquad + \dfrac{1}{\pi}\displaystyle\int_{0}^{\sigma} U_d i_{oc} (D_{d\_\text{IGBT}} + D_{d\_\text{offdelay}}) d\theta \end{cases} \tag{4}$$

where P_{c_IGBT}, i_{oc_IGBT}, and D_{d_IGBT} represent the conduction loss, ON-state current, and duty cycle of the Si IGBT, respectively. P_{c_MOS}, i_{oc_MOS}, and D_{d_MOS} represent the conduction loss, ON-state current, and duty cycle of the SiC MOSFET, respectively. R_{c_MOS} and R_{c_IGBT} represent the ON-state equivalent resistance of the SiC MOSFET and ON-state equivalent resistance of the Si IGBT, respectively. In (4), the ON-state equivalent resistances are the key to calculating the total conduction loss of the Si/SiC hybrid switch. And with the increase in the junction temperature, the value of the ON-state equivalent resistance will be increased [22], [23].

The I–V curve of the Si/SiC hybrid switch at $T_j = 150\,^{\circ}\mathrm{C}$ is shown in Fig. 2. According to (1)–(4) and Fig. 2, the fixed $t_{\text{off\_delay}}$ can reduce the switching loss of the Si/SiC hybrid switch and the conduction loss of the Si IGBT while increasing the conduction loss of the SiC MOSFET. In fact, the ON-state equivalent resistances and ON-state current of the Si/SiC hybrid switch are time varying in the single-phase inverter, so the fixed $t_{\text{off\_delay}}$ cannot guarantee the lower power loss of the Si/SiC hybrid switch at any current level, leading to that the higher efficiency of the single-phase inverter cannot be achieved.

C. Technology Challenges of the Traditional Method

In order to solve this problem, $t_{\text{off\_delay}}$ should be time varying during each fundamental cycle. However, the traditional method to obtain the optimal time-varying $t_{\text{off\_delay}}$ by solving the device loss model will face the challenges, i.e., establishing the physics-based analytical model of device loss and the additional hardware burden. Details are presented in the following.

1) *Establishment of device loss model is time-consuming:* The premise of establishing an accurate switching loss model is to obtain the corresponding fitting parameters and the residual switching loss of the Si IGBT by the DPT experiment. And the device information of the Si/SiC hybrid switch in the conduction loss model should be obtained by the datasheets of the Si IGBT and the SiC MOSFET. Therefore, these processes are time-consuming.
2) *Establishment of an accurate device loss model is difficult:* Because the accurate junction temperature of each device inside the Si/SiC hybrid switch is very difficult to be obtained [24]–[29], which means that the accurate ON-state equivalent resistance cannot be easily acquired, it is difficult to build an accurate conduction loss model. Meanwhile, the residual switching loss of the Si IGBT and fitting parameters obtained by the DPT experiment will cause errors in the switching loss model, which means that the establishment of the accurate switching loss model is also difficult.
3) *Power density reduction and cost increase of single-phase inverter:* In order to establish the accurate device loss model, the case temperature and the ON-state current of each device inside the Si/SiC hybrid switch need to be obtained online, so the additional sampling circuits are required, resulting in the power density reduction and cost increase of the single-phase inverter.

In conclusion, it is difficult to obtain the optimal time-varying $t_{\text{off\_delay}}$ by this traditional method, resulting in that the efficiency improvement of the Si/SiC-hybrid-switch-based single-phase inverter cannot be easily achieved.

III. Principle of Adaptive Delay-Time Control Method

In order to overcome these problems, a novel adaptive delay-time control method adopting the PSO algorithm is proposed. The principle of the PSO algorithm, particle coding, fitness function, implementation of the online optimization, and computational cost are presented in the following.

A. Principle of PSO Algorithm

The PSO algorithm is a classical swarm intelligence algorithm, which was introduced by Kennedy and Eberhart in 1995 [30]. There are several characteristics of the PSO algorithm [30]–[32], which is shown in Fig. 3. As shown in Fig. 3, we have the following.

1) All particles search the optimal area in the D-dimensional space.
2) Each particle is given a memory ability, so the history optimal position can be remembered.
3) Each particle continually adjusts its own current position based on its own historical information and the historical information of other particles.

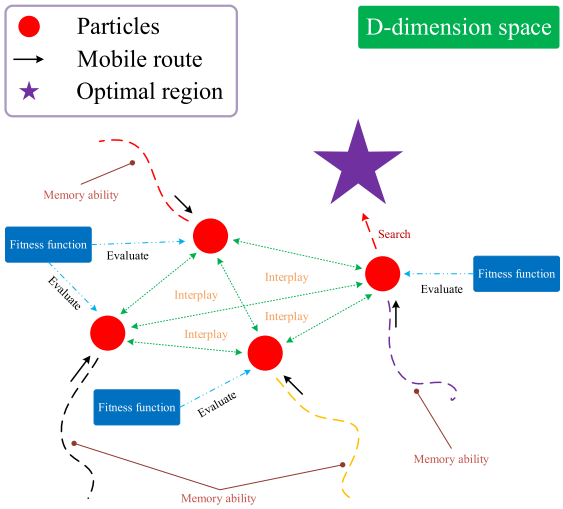

Fig. 3. Principle of the PSO algorithm.

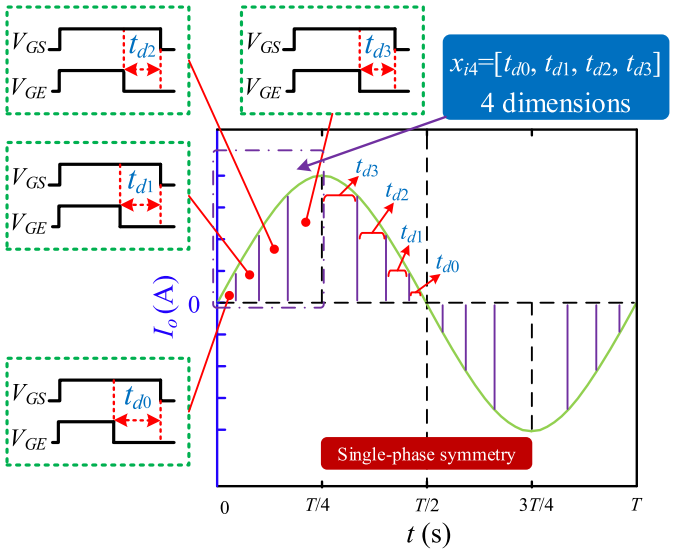

Fig. 4. Particle coding of the PSO algorithm: four-dimensional coding is taken as example. Turn-OFF delay time is changed four times in a quarter of a fundamental cycle, which means that there are four dimensions for each particle.

4) With the help of the fitness function, which can directly reflect the optimization performance, each particle can evaluate the effeteness of its current position.

Combining with the above four characteristics, the optimal region can be quickly and adaptively found by the PSO algorithm.

Because of its simple concept, fast search speed, and no requirement of an exact model, the PSO algorithm has been widely adopted in many fields, such as microgrids, renewable energy resources, performance improvement of the inverters, big data, cloud computing, and network security [33]–[38]. In this article, the PSO algorithm can be used to optimize the time-varying $t_{\text{off\_delay}}$, which can achieve the efficiency improvement of the Si/SiC-hybrid-switch-based single-phase inverter without obtaining the physics-based analytical model of device loss.

The update equation of the PSO algorithm is defined as [30]–[32]

$$\begin{cases} v_{ij}(iter+1) = \omega v_{ij}(iter) + c_1 r_1 (pbest_{ij}(iter) \\ \qquad\qquad -x_{ij}(iter)) + c_2 r_2 (gbest_{ij}(iter) - x_{ij}(iter)) \\ x_{ij}(iter+1) = x_{ij}(iter) + v_{ij}(iter+1) \end{cases} \tag{5}$$

where $iter$, ω, and j are the number of current iterations, inertia weight, and dimension of the particles, respectively. c_1 and c_2 are the acceleration factors, and r_1 and r_2 are, respectively the random numbers of [0,1]. $x_{ij} = (x_{i1}, x_{i2}, x_{i3}, \ldots\ldots, x_{in})$ is the current position of the particle, which represents the turn-OFF delay time. $v_{ij} = (v_{i1}, v_{i2}, v_{i3}, \ldots\ldots, v_{in})$ is the current velocity of the particle, which represents the update step size of the turn-OFF delay time. $pbest_{ij}(iter)$ represents the local best of the personal particle, and $gbest_{ij}(iter)$ represents the global best of all particles. In (5), the inertia weight (ω) is the time-varying parameter, which is written as [32]

$$\omega = \omega_{\max} - (\omega_{\max} - \omega_{\min}) \frac{iter}{T_{\max}} \tag{6}$$

where $\omega_{\max}$, $\omega_{\min}$, and $T_{\max}$ are the maximum inertia weight, minimum inertia weight, and number of maximum iterations, respectively.

B. Particle Coding

Particle coding is the key to obtaining the dimension information of each particle in the PSO algorithm, which is shown in Fig. 4. As shown in Fig. 4, the four-dimensional coding is taken as example. The turn-OFF delay time is changed four times in a quarter of a fundamental cycle, which means that there are four dimensions for each particle. In fact, it is only necessary to optimize the turn-OFF delay time in a quarter of a fundamental cycle, and the rest is repeated according to the principle of the single-phase symmetry.

C. Fitness Function

The fitness function is the only index to evaluate the optimization performance of the PSO algorithm. In general, the smaller the fitness value obtained from this function, the better the optimization effect [39]. Because the purpose of reducing the power losses of the Si/SiC hybrid switches is to further improve the efficiency of a single-phase inverter, the average total loss of the Si/SiC-hybrid-switch-based single-phase inverter can be set as the fitness function. Referring to [40], its formula is written as

$$\begin{aligned} F_v &= P_{adc} - P_{aac} \\ &= \frac{1}{t_o} \int_0^{t_o} [U_{\text{dc}}(t) \times I_{\text{dc}}(t)] dt \\ &\quad - \frac{1}{2t_o} \int_0^{t_o} [U_{o\alpha}(t) I_{o\alpha}(t) + U_{o\beta}(t) I_{o\beta}(t)] dt \end{aligned} \tag{7}$$

TABLE I
COMPUTATIONAL COSTS OF INTERRUPT AND PSO ALGORITHM

	Interrupt	PSO algorithm (4-dimension)	PSO algorithm (16-dimension)
Execution time of interrupt and PSO algorithm			
$t_{io1} + t_{io2}$	×	0.15ms	0.64ms
$t_{ui1} + t_{ui2} + t_{ui3}$	×	0.46ms	1.68ms
$30 \times t_o$	×	30s	30s
t_f	0.55μs	×	×
t_p	4.19μs	×	×
t_{ad}	2.12μs	×	×
Resources (Number of used units in the RAM of the DSP)			
RAM (.switch)	32 (0.11%)	0 (0%)	0 (0%)
RAM (.text)	2077 (7.24%)	1024 (3.57%)	1024 (3.57%)
RAM (.cinit)	8 (<0.10%)	277 (0.97%)	277 (0.97%)
RAM (.ebss)	0 (0%)	1268 (4.42%)	4648 (16.21%)

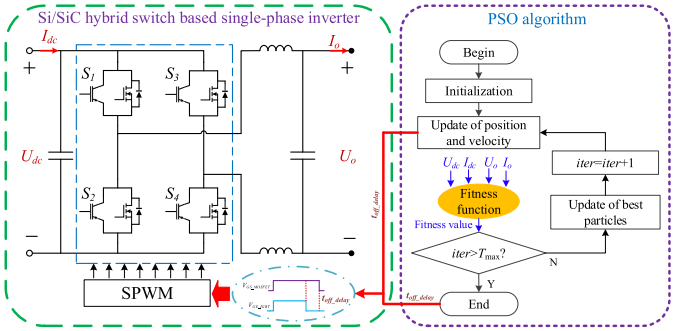

Fig. 5. Optimization principle of an adaptive delay-time control method.

where P_{adc} and P_{aac} represent the average input power and the average output power, respectively. $U_{o\alpha}$ and $U_{o\beta}$ represent the output voltages at the stationary coordinate. $I_{o\alpha}$ and $I_{o\beta}$ represent the output currents at the stationary coordinate. t_o represents the operating time of the single-phase inverter required to obtain the fitness value in the optimization process of the PSO algorithm, and the larger value of t_o, the more stable value of the average power. In fact, its value needs to consider the actual application and hardware conditions. In conclusion, the establishment of the fitness function does not need to obtain the case temperature and the ON-state current of each device inside the Si/SiC hybrid switch, so additional sampling circuits are not required.

D. Implementation of Online Optimization and Computational Cost

Based on the PSO algorithm, fitness function, and Si/SiC-hybrid-switch-based single-phase inverter, the optimization principle of the adaptive delay-time control method is shown in Fig. 5. The implementation of online optimization in the DSP is shown in Fig. 6, and different computation time is highlighted by different colors. Meanwhile, computational costs of the interrupt and PSO algorithm are shown in Table I. As can be seen from Fig. 6, the number of particles is 30, F_{vi} $(i = 1, 2, 3, \ldots, 30)$ represents the fitness value of each particle, and there is $f_s = 1/t_s = 40\,\text{kHz}$. Except for the calculation process of the fitness value, the optimization processes of the PSO algorithm in the proposed method are not carried out in the interrupt, but they are working in the main function. And the purpose of adopting the PSO algorithm is to further reduce the average power loss of the Si/SiC-hybrid-switch-based single-phase inverter, so it does not require high real-time performance. According to Figs. 5 and 6, the online optimization process of the proposed method comprises three phases, and details are presented in the following.

Phase 0: Optimization initialization.

Step 1: The position and velocity of the particles are initialized, which means that $t_{\text{off\_delay}}$ and its update step size are initialized. The execution time of this process is t_{io1}. Meanwhile, $iter$ is set as 0. Then, the local best of the personal particle and the global best of all particles are also initialized, and the execution time of this process is t_{io2}. Finally, the optimization moves to the next phase.

As can be seen from Table I, when the particle dimension is 4, the overall computation time (t_{total}) of "Step 1" is calculated as

$$t_{\text{total}} = t_{io1} + t_{io2} = 0.15\,\text{ms}. \tag{8}$$

When the particle dimension is 16, the overall execution time (t_{total1}) of "Step 1" is calculated as

$$t_{\text{total1}} = t_{io1} + t_{io2} = 0.64\,\text{ms}. \tag{9}$$

Phase 1: Optimization iteration.

Step 2: The position and velocity of the particles are updated by (5) and (6), and the execution time of this process is t_{ui1}. Then, the new $t_{\text{off\_delay}}$ is sent to the interrupt to obtain new voltage and current signals from the Si/SiC-hybrid-switch-based single-phase inverter.

Step 3: According to (7), the fitness function obtains these voltage and current signals to calculate the new fitness values of all particles, and the execution time of this process is $30t_o$. Finally, these new fitness values will be sent to the PSO algorithm.

In "Step 3," the fitness value of each particle is obtained by running the interrupt of k times, so there is $t_o = kt_s$. As can be seen from Table I, the overall execution time (t_{total2}) of the SPWM strategy, calculation of the fitness value, and the analog-to-digital (AD) converter in each interrupt is calculated as

$$t_{\text{total2}} = t_p + t_f + t_{ad} = 6.86\,\mu\text{s} < t_s = 25\,\mu s \tag{10}$$

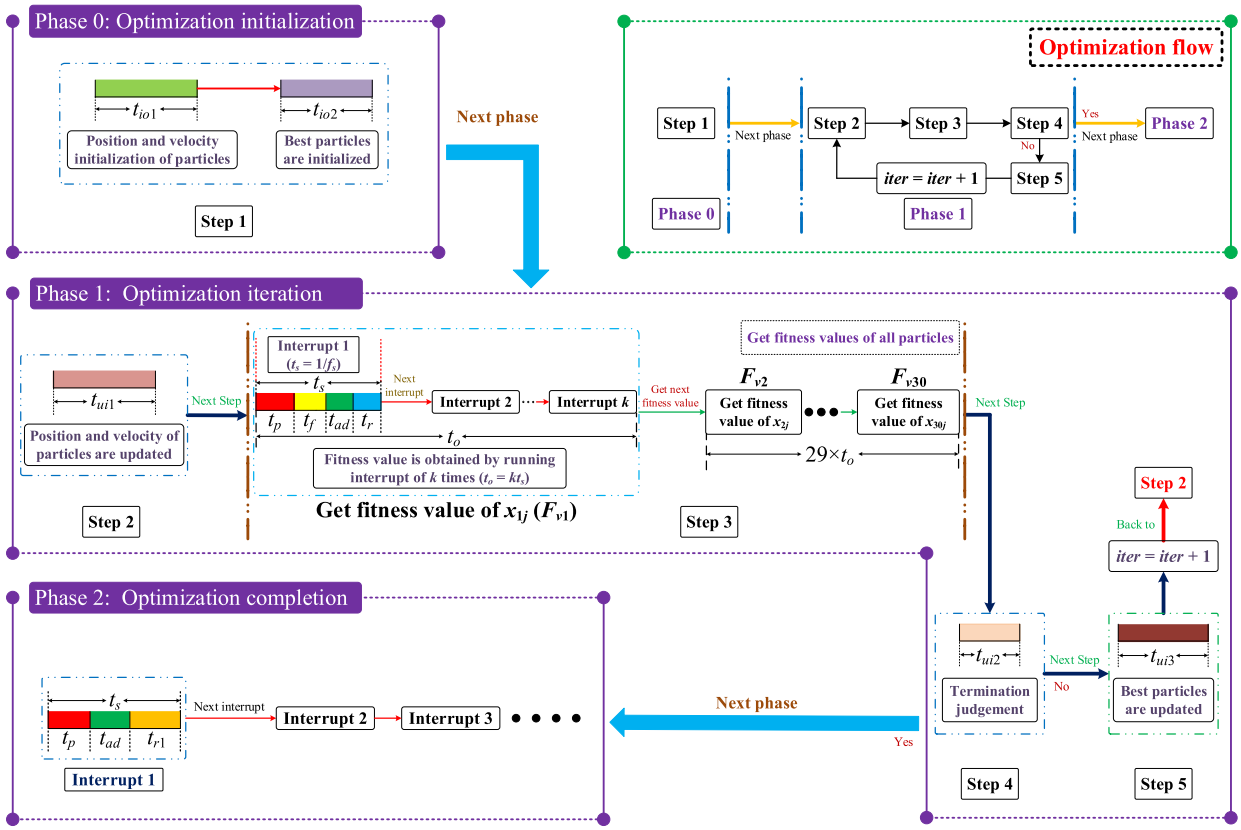

Fig. 6. Implementation of online optimization in the DSP: Except for the calculation process of the fitness value, the optimization processes of the PSO algorithm in the proposed method are not carried out in the interrupt, but they are working in the main function. And the purpose of adopting the PSO algorithm is to further reduce the average power loss of the Si/SiC-hybrid-switch-based single-phase inverter, so it does not require high real-time performance.

where t_p, t_f, and t_{ad} represent the execution time of the SPWM strategy, execution time of calculating the fitness value, and execution time of the AD converter, respectively. t_r and t_{r1} in Fig. 6 present the rest time of the interrupt.

Step 4: The optimal termination condition is determined, and the execution time of this process is t_{ui2}. If there is $iter > T_{\max}$, the optimization moves to the next phase. Otherwise, the optimization is continued to "Step 5."

Step 5: The local best of the personal particle and the global best of all particles are updated by evaluating the corresponding fitness values, and there is $iter = iter + 1$. The execution time of this process step is t_{ui3}. Then, go back to "Step 2."

As can be seen from Table I, the execution time of "Step 3" is 30 s. When the particle dimension is 4, the overall execution time (t_{total3}) of Steps 2, 4, and 5 is calculated as

$$t_{\text{total3}} = t_{ui1} + t_{ui2} + t_{ui3} = 0.46\,\text{ms}. \tag{11}$$

When the particle dimension is 16, the overall execution time (t_{total4}) of Steps 2, 4, and 5 is calculated as

$$t_{\text{total4}} = t_{ui1} + t_{ui2} + t_{ui3} = 1.68\,\text{ms}. \tag{12}$$

Phase 2: Optimization completion.

In this phase, the optimization is finished, and only the SPWM strategy and the AD converter are working in each interrupt. Meanwhile, the time-varying $t_{\text{off\_delay}}$ with the minimum fitness value is taken as the final parameter for the Si/SiC-hybrid-switch-based single-phase inverter.

In conclusion, the PSO algorithm has a low requirement on the real-time performance. And even if the calculation of the fitness value, SPWM strategy, and AD converter are working in the interrupt, their overall execution time is 28% smaller than the interrupt time.

As can be seen from Table I, when the dimension of the particle is 16, the total number of used units of the PSO algorithm in the RAM of the DSP is 21% smaller than the total units of the RAM. It means that the PSO algorithm does not require too many hardware resources of the DSP. And with the decrease in the particle dimension, the hardware resources occupied by the PSO algorithm will also be decreased. Meanwhile, the total number of used units of each interrupt in the RAM is 7.5% smaller than the total units of the RAM. Therefore, the proposed method has little influence on the real-time computation of the DSP, and there is enough room in the DSP to implement other functions.

IV. Experimental Verifications

In order to verify the effectiveness of the proposed method, the corresponding experimental platform is established, which is shown in Fig. 7. As can be seen from Fig. 7, the experimental platform comprises the dc source, power analyzer, personal

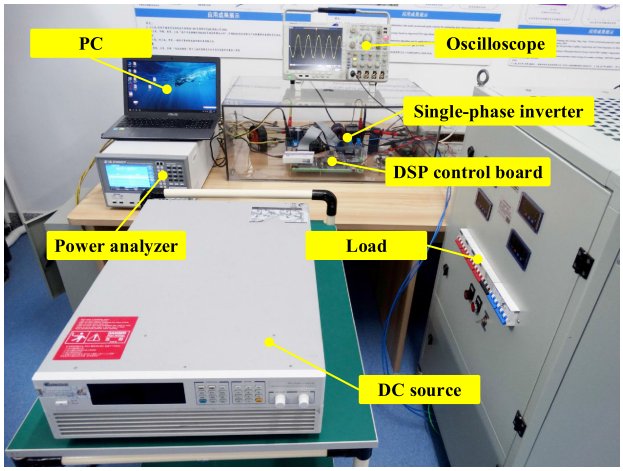

Fig. 7. Experimental platform.

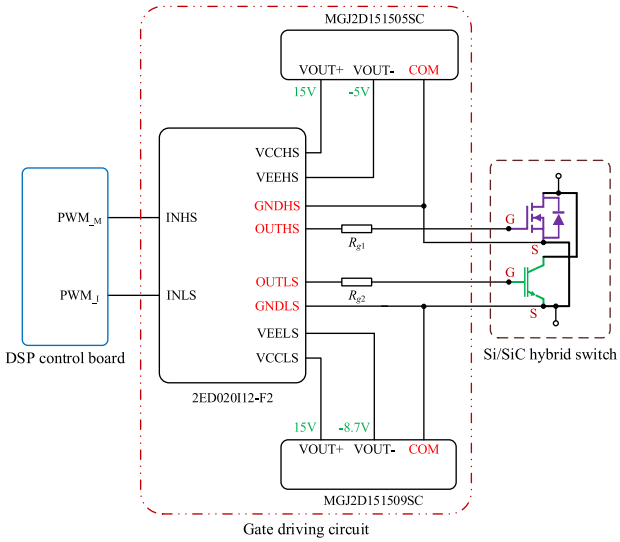

Fig. 8. Gate driving circuit structure of Si/SiC hybrid switch.

TABLE II
EXPERIMENTAL PARAMETERS

Parameters	values
DC voltage (U_{dc})	400V
Filter inductance (L_1 and L_2)	0.308mH
Filter capacitor (C)	24μF
Switching frequency (f_1)	40kHz
Modulation ratio (m)	0.778
Number of particles	30
Optimization interval of t_{off_delay}	[0, 3](μs)
Maximum iteration ($T_{\max}$)	50
Operating time of single-phase inverter (t_o)	1s
Si IGBT (IGW25N120H3)	1200V/25A
SiC MOSFET (C2M0160120D)	1200V/12.5A

computer (PC), DSP control board, single-phase inverter, load, and oscilloscope. Partial experimental parameters are described in Table II. According to [16], when the load current is smaller than 25 A (root mean square) and $t_{\text{off\_delay}}$ reaches to 3 μs, the Si/SiC hybrid switch still can work stably. Therefore, the optimization interval of $t_{\text{off\_delay}}$ can be set as $[0, 3]$ μs. When t_o is set as 1 s, the power fluctuation of the average power is already very small. Meanwhile, according to experiments at various power levels, when the number of optimization iterations approaches to 30, the average power loss is almost unchanged, which means that the optimization has reached the optimal region. Therefore, $T_{\max}$ can be set as 50 in the following experiments. The selection of the Si IGBT (IGW25N120H3, 1200 V/25 A [41]) and the SiC MOSFET (C2M0160120D, 1200 V/12.5 A [42]) inside the Si/SiC hybrid switch is only an example. In fact, the device loss models of different types of Si/SiC hybrid switches can be established by (1)–(4), and the relationship between $t_{\text{off\_delay}}$ and the device loss model of different Si/SiC hybrid switches will not be changed. It means that the proposed method is suitable for any type of Si/SiC hybrid switch.

A. Propagation Delay Analysis of Gate Driving Circuit

Based on [41], the structure of the gate driving circuit is shown in Fig. 8. As can be seen from Fig. 8, R_{g1} and R_{g2} represent the gate driving resistance of the SiC MOSFET and the gate driving resistance of the Si IGBT, respectively. The gate driving circuit of the Si/SiC hybrid switch comprises gate driving resistances, a dual-channel isolated driver (2ED020I12-F2), and isolated power supplies (MGJ2D151505SC and MGJ2D151509SC). The isolated power supplies can provide the turn-ON and turn-OFF voltages to the SiC MOSFET and the Si IGBT. In addition, with the help of the dual-channel isolated driver, the pulsewidth modulation (PWM) signals from the DSP can drive the Si IGBT and the SiC MOSFET.

In fact, the propagation delay exists in the gate driving circuits. However, the propagation delay errors between the gate driving signals of the Si IGBT and the SiC MOSFET (Turn-ON and turn-OFF) are smaller than 3 ns, which means that the propagation delay errors are too small to affect the power losses of the Si/SiC hybrid switches. Therefore, the influence of the propagation delay of the gate driving circuit on the proposed method can be neglected.

B. Obtaining of Optimal Parameters in the PSO Algorithm

Different parameters in the PSO algorithm may change its own optimization performance, so obtaining of optimal parameters for the PSO algorithm is necessary.

When different parameters in the PSO algorithm are adopted, the average total loss of the single-phase inverter with 30 independent optimizations (average total loss), minimum total loss in 30 independent optimizations (minimum total loss), and maximum total loss in 30 independent optimizations (maximum total loss) are shown in Table III. As can be seen from Table III, different parameters are denoted as Sets 1–10. When c_1 and c_2 are set as 2 and there is $\omega = 0.9$–0.4 (Set 1), the average total loss is 184.1 W, which is smaller than that of Sets 2–6. The minimum total loss adopting Set 1 is 181.9 W, which is smaller than that of Sets 2–6. And, the maximum total loss adopting Set 1 is smaller than that of Sets 1–3, 5, and 6. Therefore, the optimal c_1 and c_2 are set as 2.

TABLE III
COMPARISON OF DIFFERENT PSO PARAMETERS

Groups	Parameters in PSO algorithm	Average total loss (W)	Minimum total loss (W)	Maximum total loss (W)
	Different acceleration factors (c_1 and c_2)			
Set 1	$c_1, c_2 = 2, 2$	184.1	181.9	187.5
Set 2	$c_1, c_2 = 2, 3$	189.6	183.9	195.8
Set 3	$c_1, c_2 = 1, 3$	187.7	184.1	192.9
Set 4	$c_1, c_2 = 3, 2$	184.9	182.8	186.8
Set 5	$c_1, c_2 = 3, 1$	186.4	184.3	189.2
Set 6	$c_1, c_2 = 1, 1$	187.5	184.5	191.9
	Different inertia weight (ω)			
Set 7	$\omega = 0.9 \sim 0.4$	184.1	181.9	187.5
Set 8	$\omega = 1.3 \sim 0.4$	185.2	181.9	189.2
Set 9	$\omega = 1.6 \sim 0.4$	187.3	184.5	192.6
Set 10	$\omega = 0.9 \sim 0.2$	190.2	185.9	196.1

TABLE IV
COMPARISON OF DIFFERENT METHODS (LOAD POWER IS SET AS 4 kW)

	Average total loss (W)	Minimum total loss (W)	Maximum total loss (W)
Fixed t_{off_delay}(1.25μs)	197.1	Same	Same
PSO time-varying t_{off_delay} (Particle dimension of 4)	184.1	181.9	187.5
PSO time-varying t_{off_delay} (Particle dimension of 8)	183.0	180.0	185.1
PSO time-varying t_{off_delay} (Particle dimension of 16)	182.8	179.6	186.0

TABLE V
COMPARISON OF DIFFERENT METHODS (LOAD POWER IS SET AS 5 kW)

	Average total loss (W)	Minimum total loss (W)	Maximum total loss (W)
Fixed t_{off_delay} (1.25μs)	289.9	Same	Same
PSO time-varying t_{off_delay} (Particle dimension of 4)	270.9	268.6	272.8
PSO time-varying t_{off_delay} (Particle dimension of 8)	268.8	266.1	271.5
PSO time-varying t_{off_delay} (Particle dimension of 16)	268.4	265.5	272.4

Based on the optimal acceleration factors $(c_1, c_2 = 2, 2)$, when the inertia weight (ω) is set as 0.9–0.4 (Set 7), the average total loss is smaller than that of Sets 8–10. Meanwhile, the minimum total loss and the maximum total loss adopting Set 7 are also smaller than those of Sets 8–10. Therefore, the optimal ω can be set as 0.9–0.4.

C. Comparison Experiments at Different Power Levels

When the load power is set as 4 and 5 kW, comparison results of the optimal fixed $t_{\text{off\_delay}}$ and the time-varying $t_{\text{off\_delay}}$ optimized by the PSO algorithm are presented in Tables IV and V. Experimental waveforms adopting the PSO algorithm are shown in Figs. 9 and 10. And the power loss distributions adopting the fixed $t_{\text{off\_delay}}$ and the time-varying $t_{\text{off\_delay}}$ optimized by the PSO algorithm (16-dimensional optimization) are shown in Fig. 11. Detailed analysis is shown as follows.

1) *Load power is set as 4 kW:* As shown in Table IV, when the load power is set as 4 kW and the optimal fixed $t_{\text{off\_delay}}$ is $1.25\,\mu$s, the total loss of the Si/SiC-hybrid-switch-based single-phase inverter adopting this fixed $t_{\text{off\_delay}}$ is 197.1 W. When the particle dimension is 4, the average total loss adopting the PSO algorithm is 184.1 W, which is 13.0 W smaller than that of the fixed $t_{\text{off\_delay}}$. The minimum total loss adopting the PSO algorithm is 181.9 W, which is 15.2 W smaller than that of the fixed $t_{\text{off\_delay}}$. And the maximum total loss adopting the PSO algorithm is smaller than that of the fixed $t_{\text{off\_delay}}$. Therefore, the time-varying $t_{\text{off\_delay}}$ optimized by the PSO algorithm can further reduce the total loss of the Si/SiC-hybrid-switch-based single-phase inverter at this power level. The experimental waveforms of a set of time-varying $t_{\text{off\_delay}}$ in 30 independent optimizations (four-dimensional optimization) are shown in Fig. 9(a). When the particle dimension is 8, the average total loss is 183.0 W, which is 1.1 W smaller than that of the four-dimensional optimization (particle dimension of 4). Meanwhile, the minimum total loss and the maximum total loss are also smaller than those of the four-dimensional optimization. It means that with the increase in the dimension, the adjustment accuracy of the power loss in a fundamental cycle will be increased, so the optimization effect will be improved. The experimental waveforms of a set of time-varying $t_{\text{off\_delay}}$ in 30 independent optimizations (eight-dimensional optimization) are shown in Fig. 9(b). The average total loss of the 16-dimensional optimization is 182.8 W, which is 0.2 W smaller than that of the eight-dimensional optimization. Therefore, the optimization effect will not be significantly improved when the

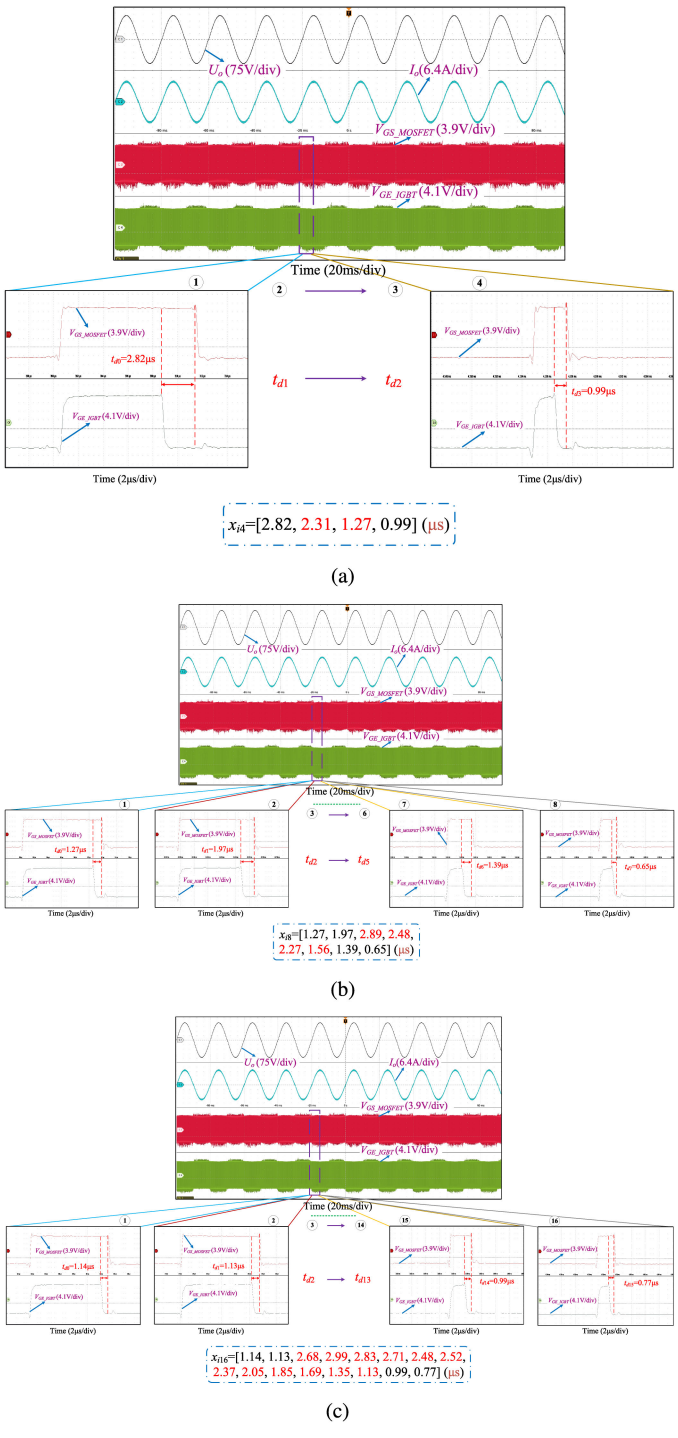

Fig. 9. Experimental waveforms adopting PSO algorithm (load power is set as 4 kW): $t_{\text{off\_delay}}$ near the peak-current region is smaller than that of the zero-crossing region, which means that the power loss of the Si/SiC hybrid switch at the low current level is mainly reduced by decreasing the switching loss. And, the reduction of power loss at the high current level mainly depends on the reduction of the conduction loss of the SiC MOSFET. (a) Four-dimensional optimization. (b) Eight-dimensional optimization. (c) Sixteen-dimensional optimization.

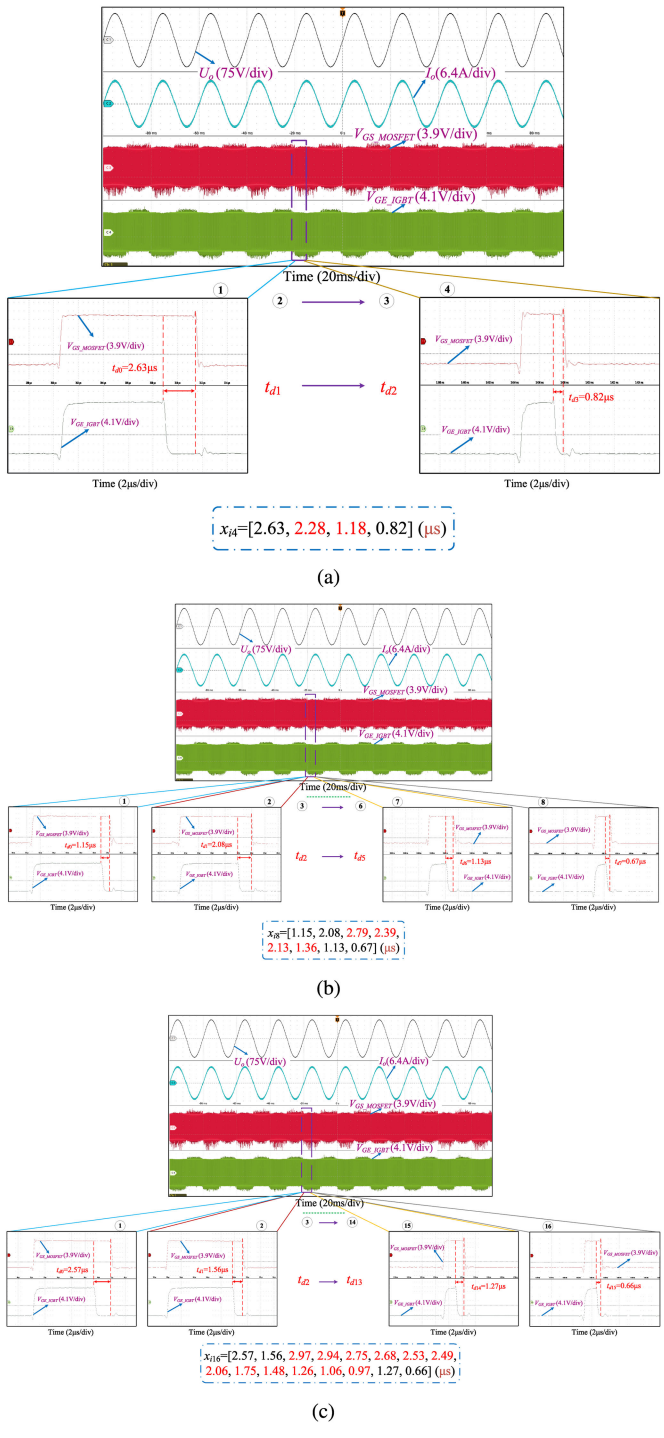

Fig. 10. Experimental waveforms adopting PSO algorithm (load power is set as 5 kW). (a) Four-dimensional optimization. (b) Eight-dimensional optimization. (c) Sixteen-dimensional optimization.

dimensions of the particle are more than eight. The experimental waveforms of a set of time-varying $t_{\text{off\_delay}}$ in 30 independent optimizations (16-dimension optimization) are shown in Fig. 9(c), and the power loss distribution adopting this time-varying $t_{\text{off\_delay}}$ is shown in Fig. 11(b).

As can be seen from Fig. 11(a), the total conduction loss of all Si/SiC hybrid switches adopting this time-varying $t_{\text{off\_delay}}$ is 63.19 W, which is 4.60 W smaller than that of the fixed $t_{\text{off\_delay}}$. And the total switching loss of all Si/SiC hybrid switches adopting this time-varying $t_{\text{off\_delay}}$ is 76.81 W, which is 7.30 W smaller than that of the fixed $t_{\text{off\_delay}}$.

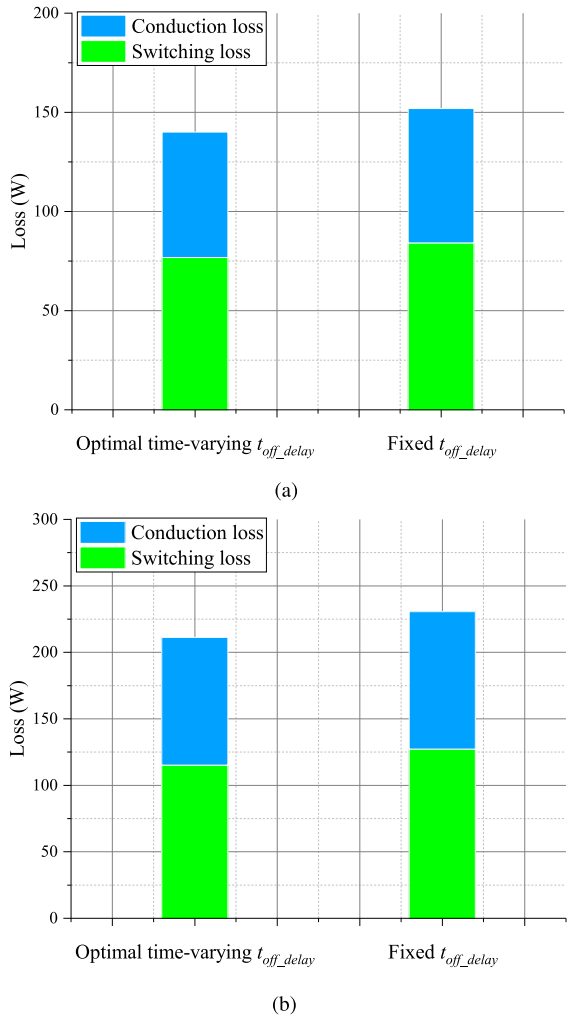

Fig. 11. Power loss distributions adopting fixed $t_{\text{off\_delay}}$ and time-varying $t_{\text{off\_delay}}$ optimized by the PSO algorithm (16-dimensional optimization): only considering the switching losses and conduction losses of all Si/SiC hybrid switches. Both the total conduction loss and total switching loss of all Si/SiC hybrid switches can be reduced by optimizing the time-varying $t_{\text{off\_delay}}$, so the power loss reduction of the single-phase inverter can be achieved. (a) Power load is set as 4 kW. (b) Power load is set as 5 kW.

According to Figs. 9 and 11(a), $t_{\text{off\_delay}}$ near the peak-current region is smaller than that of the zero-crossing region, which means that the power loss of the Si/SiC hybrid switch at the low current level is mainly reduced by decreasing the switching loss. And the reduction of power loss at the high current level mainly depends on the reduction of the conduction loss of the SiC MOSFET. Therefore, both the total conduction loss and the total switching loss of all Si/SiC hybrid switches can be reduced by optimizing the time-varying $t_{\text{off\_delay}}$, which means that the power loss reduction of the single-phase inverter can be achieved.

2) *Load power is set as 5 kW:* As shown in Table V, when the load power is set as 5 kW, the average total loss of the four-dimensional optimization is 270.9 W, which is 19.0 W smaller than that of the fixed $t_{\text{off\_delay}}$ $(1.25\,\mu\text{s})$. The minimum total loss of the four-dimensional optimization is 268.6 W, which is 21.3 W smaller than that of the fixed $t_{\text{off\_delay}}$. And the maximum total loss of the four-dimensional optimization is smaller than that of the fixed $t_{\text{off\_delay}}$. Therefore, the PSO algorithm can also achieve the lower loss of the single-phase inverter at this power level. The experimental waveforms of a set of time-varying $t_{\text{off\_delay}}$ in 30 independent optimizations (four-dimension optimization) are shown in Fig. 10(a).

The average total loss of the eight-dimensional optimization is 268.8 W, which is 2.1 W smaller than that of the four-dimensional optimization. Meanwhile, the minimum total loss and the maximum total loss of the eight-dimensional optimization are smaller than those of the four-dimensional optimization. It means that the optimization effect can be further improved at the eight-dimensional optimization. The experimental waveforms of a set of time-varying $t_{\text{off\_delay}}$ in 30 independent optimizations (eight-dimensional optimization) are shown in Fig. 10(b).

The average total loss of the 16-dimensional optimization is 268.4 W, which is 0.4 W smaller than that of the eight-dimensional optimization. It means that the improvement of the optimization effect will also not be obvious with the further increase in the particle dimension. The experimental waveforms of a set of time-varying $t_{\text{off\_delay}}$ in 30 independent optimizations (16-dimensional optimization) is shown in Fig. 10(c), and the power loss distribution adopting this time-varying $t_{\text{off\_delay}}$ is shown in Fig. 11(b). As can be seen from Fig. 11(b), the total conduction loss adopting this time-varying $t_{\text{off\_delay}}$ is 96.07 W, which is 7.35 W smaller than that of the fixed $t_{\text{off\_delay}}$. And the total switching loss adopting this time-varying $t_{\text{off\_delay}}$ is 115.23 W, which is 12.01 W smaller than that of the fixed $t_{\text{off\_delay}}$.

According to Figs. 10 and 11(b), the value of $t_{\text{off\_delay}}$ near the peak-current region is also smaller than that of $t_{\text{off\_delay}}$ near the zero-crossing region. Therefore, the power loss of the single-phase inverter can be effectively reduced by decreasing the total conduction loss and total switching loss of all Si/SiC hybrid switches.

D. Comparison Experiments at Different Switching Frequencies

When the load power is set as 5 kW and the switching frequency is changed, the comparison experiments of different methods are presented in Table VI.

1) *Switching frequency is decreased:* As can be seen from Table VI, when the switching frequency is changed from 40 to 20 kHz, the average total loss of the four-dimensional optimization is 243.12 W, which is 16.68 W smaller than that of the fixed $t_{\text{off\_delay}}$. Meanwhile, the minimum total loss and maximum total loss of the four-dimensional optimization are smaller than those of the fixed $t_{\text{off\_delay}}$. Therefore, the proposed method can achieve the lower power loss of the single-phase inverter when the switching frequency is reduced.
2) *Switching frequency is increased:* As can be seen from Table VI, when the switching frequency is changed from 40 to 60 kHz, the average total loss of the four-dimensional

TABLE VI
COMPARISONS OF DIFFERENT METHODS AT VARIOUS SWITCHING FREQUENCIES

	Average total loss (W)	Minimum total loss (W)	Maximum total loss (W)
Switching frequency is changed from 40kHz to 20kHz			
Fixed t_{off_delay} (1.25μs)	259.80	Same	Same
PSO variable t_{off_delay} (Particle dimension of 4)	243.12	242.01	246.05
Switching frequency is changed from 40kHz to 60kHz			
Fixed t_{off_delay} (1.25μs)	325.74	Same	Same
PSO variable t_{off_delay} (Particle dimension of 4)	305.51	303.12	308.74

optimization is 305.51 W, which is 20.23 W smaller than that of the fixed $t_{\text{off\_delay}}$. Meanwhile, the minimum total loss and maximum total loss of the four-dimensional optimization are smaller than those of the fixed $t_{\text{off\_delay}}$. Therefore, the proposed method can also achieve the loss reduction of the single-phase inverter when the switching frequency is increased.

V. CONCLUSION

In this article, a novel adaptive delay-time control method adopting the PSO algorithm is proposed for the Si/SiC-hybrid-switch-based single-phase inverter, and there are several advantages for the proposed method.

1) The optimization process of the proposed method is convenient and simple. The adaptive adjustment of the time-varying delay time is only guided by a simple fitness function, which means that the additional sampling circuits, DPT experiment platform, and device information of the Si/SiC hybrid switch are not required.
2) The optimization objective of the proposed method can be achieved. Only by evaluating the fitness values, the PSO algorithm can further improve the efficiency of the Si/SiC-hybrid-switch-based single-phase inverter under different operating states.

An experimental platform of the Si/SiC-hybrid-switch-based single-phase inverter is set up and tested. Compared to the fixed delay time, the power loss reduction of the single-phase inverter at different operating states can be achieved by adaptively adjusting the time-varying delay time. With the increase in the dimension of particles, the optimization effect of the PSO algorithm will be improved at first, and then, its improvement will not be obvious, which means that further increase in the particle's dimension is unnecessary. Meanwhile, the real-time computation of the DSP is slightly affected by the proposed method, and there is enough room in the DSP to implement other functions. In fact, these goals can be easily implemented by other swarm intelligence algorithms. In the future, the swarm intelligence algorithms with the better performance will be studied.

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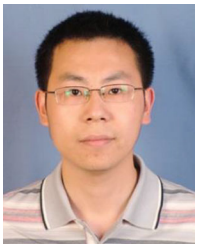

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