Active Bridge Rectifier With DM EMI Reduction Based on Linear Reverse Operation of MOSFETs

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***Abstract*—A new linear control scheme for operating power MOSFETs in the third quadrant (i.e., synchronous rectifier (SR) operation) is proposed and applied to electromagnetic interference (EMI) mitigation of switching converters. MOSFETs operating in the third quadrant exhibit electrical characteristics equivalent to a voltage-controlled voltage source between the gate-source and the drain-source voltages. Such operation is an alternative to typical SR mode, allowing fast control of the ac drain-source voltage. It is applied to active bridge rectifiers (ABRs) that can produce the necessary high-frequency voltage compensation signal to reduce differential-mode EMI. The ABR can then play the role of ac line rectification and EMI reduction at the same time. Its characteristics are modeled, and experimental verifications are carried out on a boost-type power factor corrector (PFC). The EMI performance of the PFC is improved with the proposed technique. The proposed technique facilitates the reduction of passive filter size and gives the potential of integrating active filtering function into the ABR as a solid-state front-end module. The idea can, thus, help increase the power density of power converters.**

***Index Terms*—Active filters, electromagnetic interference, power MOSFET, rectifiers.**

I. Introduction

In THE power electronic industry, diode bridge rectifier is an essential part of ac–dc converters. One persistent drawback of silicon power diode is the high dropout voltage, around 1 V, resulting in significant conduction loss. Active bridge rectifier (ABR) is proposed in [1] by replacing rectifier diodes with MOSFETs and reproducing the line-frequency commutation operation with a very low dropout voltage. The idea is extended from the widespread usage of power MOSFET which substitutes the freewheeling diode, taking advantage of the low ON resistance of MOSFETs [2], [3]. The MOSFETs in freewheeling applications are controlled in synchronous with the main switch and are, thus, referred to as synchronous rectifier (SR). The MOSFETs for the ac line rectification are controlled to synchronize with the line voltage polarity instead. ABR can achieve significantly lower conduction loss than a diode bridge.

Power line filter is another critical part of switching converters. It is used to suppress electromagnetic interference (EMI) from entering the power grid. The EMI is generated by the switching converters due to fast and repetitive switching actions. A typical power line filter is made up of a multistage passive *LC* circuit. One of the major concerns of passive EMI filters is their bulkiness [4], [5]. The active EMI filter concept is first introduced in [6]. The basic classification and implementation of active filters are introduced in [7] and [8]. Later, they become the classic references for subsequent work. For active differential-mode (DM) EMI/ripple filters, Farkas and Schlecht [9] first show the feasibility of applying active EMI filtering in utility grid applications. Hamill [10] and Chow and Perreault [11] employ an inductor-enhancing topology and a capacitor-enhancing topology [7], [8], respectively, with output feedback and input feedforward control scheme. Zhu *et al*. [12] and Chen *et al*. [13] utilize capacitor-enhancing topologies with a feedforward control and a feedback control, respectively, to achieve DM or CM noise suppression. Chen *et al*. [14] propose a more precise classification by comparing the insertion loss of various topologies. Recently, Xu and Lee [15] have employed an inductor-enhancing type active circuit for both CM and DM noise suppression. Goswami and Wang [16] have utilized a capacitor-enhancing topology for DM noise suppression with comprehensive modeling and stability analysis. In those works, active circuits are utilized to inject noise compensating signal to the power circuit. All active EMI filters are dominant of hybrid type, composing of both solid-state devices for filtering function and passive elements for filtering, sensing, and output coupling. To further reduce the physical size of passive elements and facilitate integration of filter into a solid-state power conversion system, MOSFET is employed as the input filtering device in [17]–[20]. In these works, the MOSFET (or any power transistor) is a series-pass, linear operated device, which regulates the total input current of the converter through feedback control, as shown in Fig. 1(a). The technique is extended to ac–dc converters [21], [22], as shown in Fig. 1(b) to serve more general applications. The main challenge of those transistor-based filters is to reduce the power loss due to the dropout voltage such as a linear regulator. Especially, as discussed in the beginning, the input diode bridge rectifier adds even more conduction loss.

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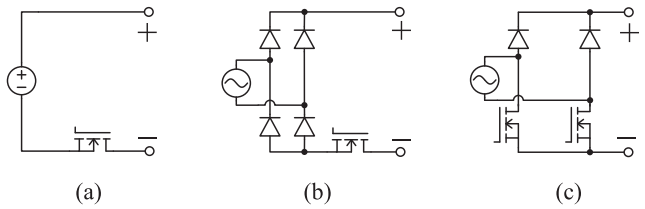

Fig. 1. Configurations of transistor-based filters. (a) In dc–dc converter. (b) In ac–dc converter, named power semiconductor filter. (c) In an ABR using SR FETs. High-side diodes are kept [1] or may also be replaced by SR FETs.

To reduce the dropout loss, an attempt of merging the filtering device into the rectifier is proposed in this article. While the MOSFETs are used to replace diodes and facilitate active filtering function, the rectification function is also preserved. The arrangement is using an ABR [1] as illustrated in Fig. 1(c). One immediate concern is during SR conduction, it is supposed to be like "ideal diode" without filtering function. In prior-art [23] and [24], inventors have proposed techniques in varying the channel resistance of the secondary-side SR FETs slowly to achieve output voltage regulation. It is proved in this work with experiments that in reverse conduction region (the third quadrant), fast linear active control can be performed on the MOSFETs under investigation. Critical assessments have been carried out and have shown that MOSFETs can act as a linear voltage-controlled voltage source (VCVS) with limited output swing. The property is utilized to achieve active EMI mitigation function of a bridge rectifier with an analog controller. By integrating the active filtering device into the bridge rectifier, the hybrid filter design can be made more compact. The loss in configuration Fig. 1(b) is, thus, reduced by reducing component count and lower rectifier dropout voltage than diodes.

A small-signal model of the hybrid filter circuit is built and proceeded with the stability analysis. A controller design procedure is provided. The proposed ABR prototype is tested on a power factor corrector (PFC).

II. Proposed Active Rectifier

The proposed hybrid filtering technique is illustrated in Fig. 2. Semi-full bridge structure is used, as in Fig. 1(c). A small series inductor L_{s1}, which is used as a sensing element [17], is connected between the ABR and the input capacitor C_{sh}. A controller with a fast response is assigned to amplify the inductor voltage feedback v_L which derives the driving signal v_{GS} shown at the right-hand side of Fig. 2. Due to the VCVS property, which is presented in the next section, $\tilde{v}_{DS}$ is proportional to $\tilde{v}_{GS}$ and gives an amplified $\tilde{v}_L$ waveform that compensates for the ripple voltage on C_{sh}, caused by the input current ripple $\tilde{i}_P$ of the switching converter. With adequately high controller gain, $\tilde{v}_{DS} \simeq \tilde{v}_C$ can be achieved so that the ripple at the input port $\tilde{v}_{\text{in}}$ vanishes. The input DM noise is, thus, suppressed. The ABR is an inductor-enhancing active filtering device, as depicted in [7], that can overperform the passive inductor L_{s1} significantly. The $\tilde{i}_P$ is forced to circulate between the converter and C_{sh}. The ripple size of $\tilde{v}_{DS}$ or $\tilde{v}_C$ is 0.4 Vp-p in the experimental prototype. On the contrary, typical diode bridges are transparent to high frequency ripple. The waveforms over a line cycle are

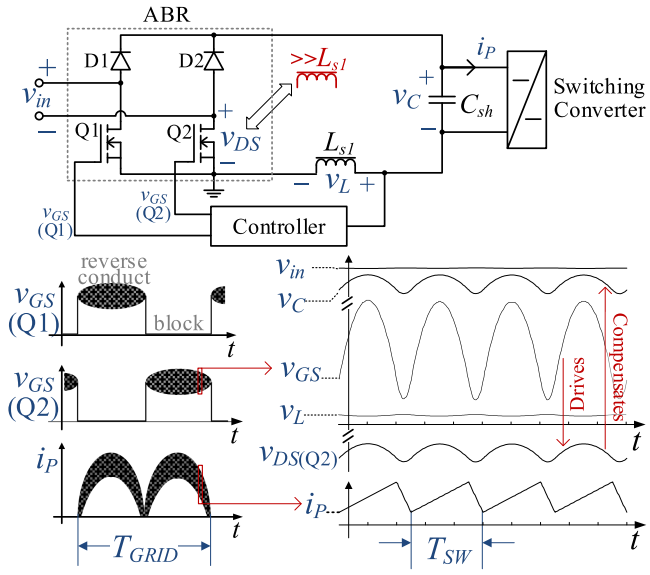

Fig. 2. Key structure and waveforms illustrating the proposed active rectifier, during conduction phase of D1 and Q2.

shown on the left-hand side of Fig. 2. The ABR commutates like a typical diode bridge. The gate signals to the MOSFETs switch between reverse-blocking and reverse-conduction modes at the line frequency. It should be noted that the proposed reverse conduction is not "standard" SR conduction (i.e., driving the SR deep into the ohmic region). Instead, the voltage across the SR is actively controlled by the v_{GS}.

III. Linear Reverse Conduction Operation

The basis of this article is the linear VCVS property of a MOSFET operating in the reverse conduction region. This section starts by showing the VCVS property. An ac model is formulated and verified experimentally.

An *n*-channel MOSFET in reverse operation conducts current from its source to drain. Consider two phases during the conducting state of a standard SR: 1) with zero V_{GS}, the MOSFET exhibits its body diode property, the dropout voltage $|V_{DS}|$ is virtually constant around -0.7 V; 2) with V_{GS} pulled up to the maximum of the driver, V_{DS} approaches zero. The two extreme cases indicate that there can be intermediate V_{DS} value tunable by V_{GS} within -1 to 0 V range. A static *V–I* characteristic graph in Fig. 3 shows such intermediate traces in the third quadrant operation, such as that in [2]. It is measured from a sample of the MOSFET IPP60R060P7. With higher V_{GS}, V_{DS} values tend to be higher (less negative); there exists a positive correlation. By rearranging the curve-tracing data into Fig. 4, there shows a linear portion at the middle of the V_{DS}–V_{GS} traces for each current bias. V_{DS} saturates on the two ends. The linear portion is recognized as the VCVS region to implement the proposed active control. It can be represented by the expressions

$$\Delta V_{DS}|_{\Delta I_{DS}=0} = A_{M0}\Delta V_{GS} \tag{1}$$

or

$$\frac{\partial V_{DS}}{\partial V_{GS}} = A_{M0} \tag{2}$$

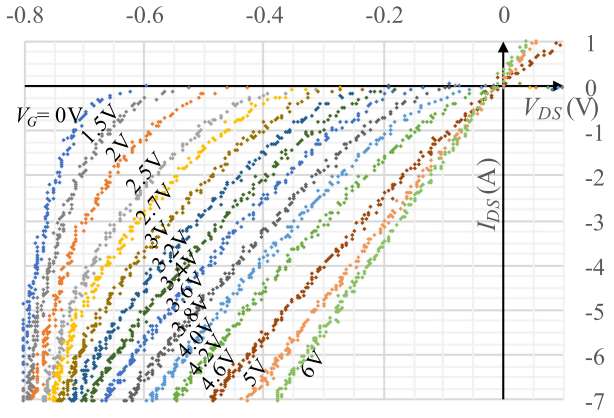

Fig. 3. MOSFET third quadrant dc *V–I* characteristics.

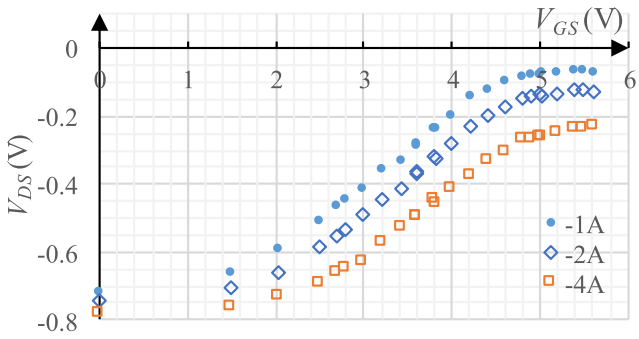

Fig. 4. Measured V_{DS}-V_{GS} relationship of IPP60R060P7 with. The slope in VCVS region stays unchanged with I_{DS} at -1, -2, and -4 A.

where A_{M0} is defined as the dc voltage gain of the MOSFET. The value is around 0.2. The assumption $\Delta I_{DS} = 0$ is to match the ideal filtering outcome wherein the ac ripple is eliminated. A second observation in Fig. 3 is that the slope of the *V–I* curves is nearly constant within the VCVS region. The slope of a single trace is expressed as

$$\frac{\partial V_{DS}}{\partial I_{DS}} = R_{SD0} \tag{3}$$

which is referred to the Thevenin equivalent drain-source resistance of the MOSFET. The value of R_{SD0} is close to the claimed $R_{DS(ON)}$ of the MOSFET.

It is attempted to prove (2) theoretically according to [2], which is based on Meyer's model. In [2], an *n*- MOSFET in third quadrant with strong inversion near the drain area but no inversion near the source is referred as in "reverse saturation" mode, which has a current expression in [2] and [25] as

$$\begin{aligned} I_{DS} = {} & K \exp\left(qV_{GS}/mkT\right)\left[1 - \exp\left(-qV'_{d,t}/\eta kT\right)\right] \\ & + \beta\left\{-\tfrac{2}{3}\gamma\left[\left(2\left|\phi_p\right| + V'_d\right)^{1.5} - \left(2\left|\phi_p\right| + V'_{d,t}\right)^{1.5}\right]\right. \\ & + \left[V_{GS} - V'_{d,t} - V_{FB} - 2\left|\phi_p\right| - \tfrac{1}{2}(V'_d - V'_{d,t})\right] \\ & \left. \cdot (V'_d - V'_{d,t})\right\} \end{aligned} \tag{4}$$

where the potential of the conceptual pinch-off point between the inversion and noninversion sides is defined as [2]

$$V'_{d,t} = V_{GS} - V_{FB} - 2\left|\phi_p\right| + \tfrac{1}{2}\gamma^2 - \gamma\sqrt{V_{GS} - V_{FB} + \tfrac{1}{4}\gamma^2} \tag{5}$$

which is higher in potential than V'_d but lower than 0. V'_d is the channel-determined drain-source potential, with the total resistive dropout excluded. That is

$$V'_d = V_{DS} - I_{DS}R_{SD0}. \tag{6}$$

K, β, m, η, γ, V_{FB}, and $|\phi_p|$ are structural and material constants. The exponential term in (4) is neglected due to its insignificant absolute value. To find (2), perform partial differentiation of (4) and (6) with respect to V_{GS}. This partial derivative in (2) is defined with constant I_{DS}, therefore $\partial I_{DS} = 0$. By deformation and substitution of (5), it yields

$$A_{M0} = \frac{\partial V_{DS}}{\partial V_{GS}} = \frac{\partial V'_d}{\partial V_{GS}} = \frac{1}{1 + \gamma\frac{1}{\sqrt{V'_{d,t}+2|\phi_p|}+\sqrt{V'_d+2|\phi_p|}}}. \tag{7}$$

To further simplify the equation, approximation techniques are applied. $V'_{d,t}$ is neglected because typically $|V'_{d,t}| \ll 2|\phi_p|$. Apply Taylor series to linearize the remaining equation at point $V'_d = \alpha$

$$\begin{aligned} \frac{\partial V_{DS}}{\partial V_{GS}} \approx {} & MV'_d - \alpha M \\ & - \gamma\left(\gamma + \sqrt{2\left|\phi_p\right|} + \sqrt{2\left|\phi_p\right| + \alpha}\right)^{-1} + 1 \end{aligned} \tag{8}$$

where

$$M = \frac{\gamma}{2\sqrt{2\left|\phi_p\right| + \alpha}\left(\gamma + \sqrt{2\left|\phi_p\right|} + \sqrt{2\left|\phi_p\right| + \alpha}\right)^2}. \tag{9}$$

Considering that body diode voltage is ~0.7 V, the biasing point of V'_d should be around -0.35 V ($=-0.7$ V/2) in proper linear reverse operation. Then $\alpha = -0.35$V is set for a good approximation. The body effect factor γ is determined by silicon permittivity ε_{Si}, doping concentration N_a, oxide permittivity ε_{ox}, and thickness d_{ox}. However, those parameters are seldom included in datasheet. Alternatively, γ can be estimated by its relationship with a threshold voltage

$$V_{\text{TH}} = V_{\text{FB}} + 2\left|\phi_p\right| + \gamma\sqrt{2\left|\phi_p\right|} \tag{10}$$

where V_{FB} is the flat-band voltage whose value is around -0.6 V [2]. The value of $|\phi_p|$, i.e., the potential difference between doped Fermi level and intrinsic Fermi level, is assumed to be 0.4 V [2].

The IPP60R060P7 is taken as an example for validation. From the datasheet, V_{TH} is typically 3.5 V, then by (10), γ is 3.69. Using (9), M is evaluated as 0.099 V^{-1}, which indicates that A_{M0} value is almost constant as V'_d varies. Using (8), with $V'_d = -0.35$V, A_{M0} is found to be about 0.3 V. V'_d of -0.2 and -0.6 V yields A_{M0} of 0.31 and 0.27, respectively. This is considered a close result to the measured value of 0.21 noting that the physical model employed is highly simplified and many parameters are estimated.

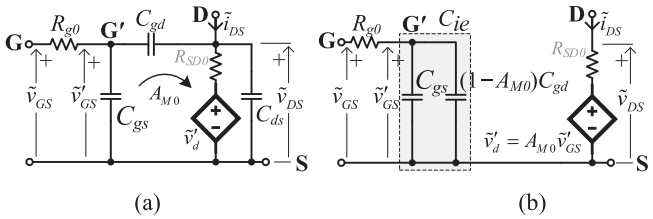

Fig. 5. (a) AC model of the MOSFET in linear reverse operation. (b) Equivalent and simplified version of (a).

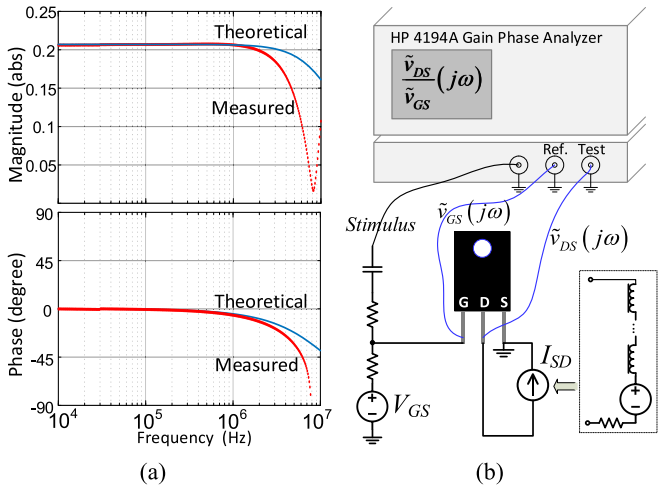

Fig. 6. AC characterization of MOSFETs in linear reverse operation. (a) $A_{M,\mathrm{open}}(f)$ plot. (b) Measurement configuration.

An ac small-signal circuit model is proposed as shown in Fig. 5(a), based on the well-known hybrid-pi model, but a Thevenin equivalent version. The dependent source with gain A_{M0} corresponds to the V'_d in (4)–(7). The small Thevenin resistor is R_{SD0} in (3). There are four parasitic elements R_{g0}, C_{gs}, C_{gd}, and C_{ds}. The model is converted into Fig. 5(b) as a first-order approximation. The reverse transfer capacitor C_{gd} is lumped to the input side with value $(1 - A_{M0})C_{gd}$. C_{ds} is neglected for simplification. Ideally, the ripple on i_{DS} is strongly suppressed by the active filtering mechanism while $\tilde{v}_{DS}$ is considerably large for compensating the ripple voltage across C_{sh}. Since the value of R_{SD0} is small, there is $\tilde{i}_{DS}R_{SD0} \ll \tilde{v}_{DS}$ and it can be assumed that $\tilde{v}_{DS} = \tilde{v}'_d$. R_{SD0} is, thus, neglected in the analysis. Therefore, the gain of the open-load drain-to-gate small signal gain $A_{M,\mathrm{open}}(j\omega)$ is

$$A_{M,\mathrm{open}}(j\omega) = \frac{\tilde{v}_{DS}}{\tilde{v}_{GS}}(j\omega) = A_{M0}\frac{1}{1 + sR_{g0}C_{ie}} \tag{11}$$

where $C_{ie} = C_{gs} + (1 - A_{M0})C_{gd}$.

A_{M0} and R_{SD0} can be determined by dc measurement as in Fig. 3. The parasitic element values can be retrieved from the MOSFET datasheet or measured with an impedance analyzer. With the parameters used in the model, the theoretical open-load gain/phase is plotted as in Fig. 6(a). An experiment is designed to verify (11) with a gain-phase analyzer HP 4194A. The configuration is shown in Fig. 6(b). The MOSFET is fed with a constant current I_{SD} flowing through source to drain. The constant current source is implemented by a series circuit

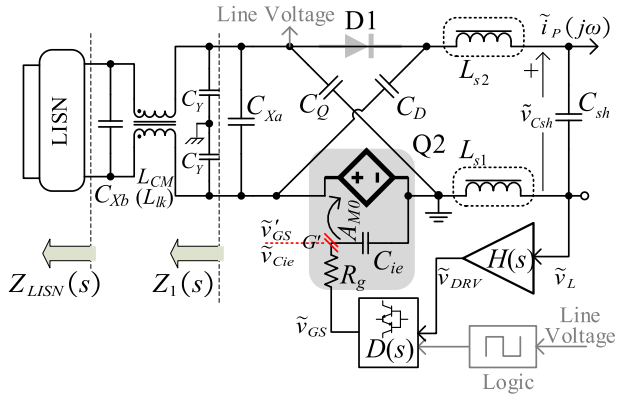

Fig. 7. Model of the hybrid filter with proposed ABR, connected to the LISN as in conducted EMI tests.

of a voltage supply and an RL impedance module in order to hold the MOSFET current nearly constant. A constant gate bias voltage V_{GS} is applied to define the dc load line. Then, the ac stimulus $\tilde{v}_{GS}$ is generated by the analyzer coupled to the gate through dc-blocking capacitor. The "reference" channel measures $\tilde{v}_{GS}$. The "test" channel measures $\tilde{v}_{DS}$. The reference ground is attached to the source of the MOSFET. The measured $A_{M,\mathrm{open}}(f)$ curve is shown in Fig. 6(a), which matches well with the modeled frequency response below 5 MHz. The measured A_{M0} agrees with the dc measurement.

The above ac model has its limitations on linearity. In Fig. 3, it can be seen that the minima of v_{DS} is bounded by the body diode, and the maxima is bounded by the channel resistance in ohmic mode. The operational area between the two bounds shrinks gradually with the increase in the source-drain current. The nonlinearity is also reflected in Fig. 4 as the saturation. Therefore, the linear property is defined only within certain *V*–*I* range to avoid distortion, to be discussed in Section V. The peak–peak swing of $\tilde{v}_{DS}$ is around 0.4 V and the dropout V_{DS} is around −0.35 V for the MOSFETs that authors have measured.

IV. Control Principle

The ac model of Fig. 2 circuit in positive half line cycle is shown in Fig. 7. For clarity, all parasitic elements are not shown. During the conduction phase of D1 and Q2, D2 and Q1 are reverse biased and considered junction capacitors C_D and C_Q, respectively. There is a passive DM filter part $C_{Xb} - L_{\mathrm{lk}} - C_{Xa}$ and a common mode (CM) filter part $L_{\mathrm{CM}} - 2C_Y$, where L_{lk} is the leakage inductance of the CM choke. The ABR forms a second DM filter stage together with C_{Xa}, $L_{s1,2}$, and C_{sh}.

The VCVS property facilitates the implementation of an active inductor or inductor enhancing device [7] as illustrated in Fig. 8. In the ideal case, the controlled VCVS amplifies v_L by the gain *K*. The VCVS is, thus, very sensitive and fully compensating the C_{sh} ripple voltage. This is equivalent to magnifying L_s to a much higher inductance, which virtually diverts all the ripple current from the converter toward C_{sh}. Consequently, the Line Impedance Stabilization Network (LISN) side receives virtually no disturbance from the converter.

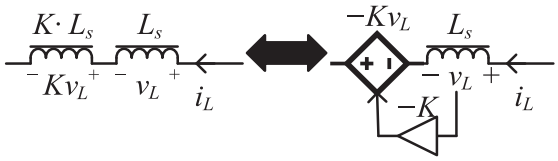

Fig. 8. Inductor enhancing principle. MOSFET is modeled as a VCVS being equivalent to a much larger inductor. Suppose K>>1.

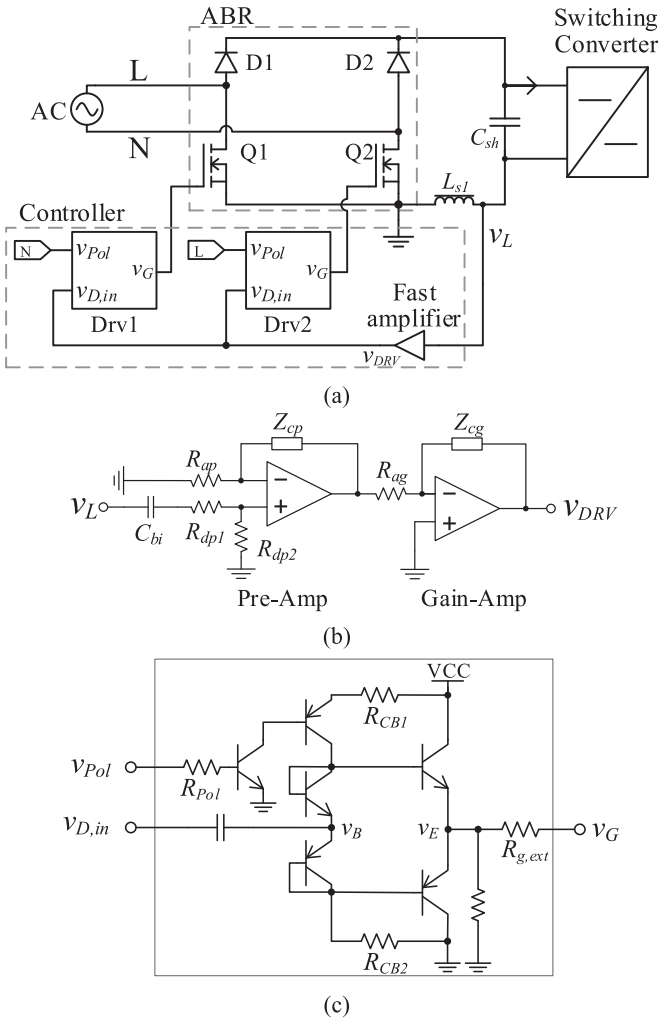

Fig. 9. Key circuit diagram. (a) System architecture. (b) Circuit schematic of the "fast amplifier" in (a). (c) Circuit schematic of the driver modules "Drv1" and "Drv2" in (a), based on a class-AB power amplifier.

The circuit implementation is shown in Fig. 9. There are two parts in the controller shown in Fig. 9(a). The first part is the inductor voltage amplifier $H(s)$, a fast controller with high gain. It is implemented by two cascaded operational amplifiers, as shown in Fig. 9(b). The controller generates a continuous ripple voltage in a fashion that cancels out the noisy converter voltage while the MOSFET is the actuator. The second part is the driving modules depicted in Fig. 9(c). In each module, there is a logic branch that determines the MOSFET commutation at line frequency, by detecting the drain voltage of the other MOSFET, i.e., an interlocking technique, to prevent shoot-through. If the NPN transistor is triggered on by line voltage at v_{Pol} above a threshold, the class-AB amplifier becomes properly biased and generates a signal at $v_{D,\mathrm{in}}$. Otherwise, the driver is inhibited. Tunable blanking time is implemented by adjusting the resistor R_{Pol}. The output of a fast amplifier signal is shared by the two drivers alternatively. The class-AB amplifier is used to mitigate the loading effect for the Gain-amp in Fig. 9(b), because of the high input capacitance of the power MOSFETs (>1000 pF). MOSFET gate bias level is preset by R_{CB1} and R_{CB2}.

The system open-loop gain, referring to Figs. 5(b) and 7, at node G′ for a $\tilde{v}'_{GS}$ and a $\tilde{v}_{Cie}$ is investigated. To simplify the analysis,

1) the switching converter is regarded as a current source within the frequency of interest;
2) the parasitic elements including C_Q and C_D are neglected;
3) the loading effect at v_L and v_{DRV} nodes are neglected.

Assume $L_{s1} = L_{s2} = L_s$. R_g is the summation of R_{g0} and external gate resistance $R_{g,\mathrm{ext}}$. The gain of the power stage, i.e., the gain of $\tilde{v}'_{GS}$ through the hybrid filter network is

$$\frac{\tilde{v}_L}{\tilde{v}'_{GS}}(j\omega) = A_{M0}\frac{j\omega L_s}{Z_1||(j\omega C_{Xa})^{-1} + 2j\omega L_s + (j\omega C_{sh})^{-1}} \tag{12}$$

where $Z_1(j\omega) = [Z_{LISN}(j\omega)||(j\omega C_{Xb})^{-1} + 2j\omega L_{\mathrm{lk}}]$, as in Fig. 7.

Then the open-loop gain for the hybrid filter system is

$$A_{\mathrm{OPL}}(j\omega) = \frac{\tilde{v}_L}{\tilde{v}'_{GS}}(j\omega)\cdot\frac{\tilde{v}_{Cie}}{\tilde{v}_L}(j\omega)$$
$$= \frac{A_{M0}\cdot j\omega L_s}{Z_1||(j\omega C_{Xa})^{-1} + 2j\omega L_s + (j\omega C_{sh})^{-1}}\cdot\frac{H(j\omega)\,D(j\omega)}{1 + j\omega R_g C_{ie}}. \tag{13}$$

To find the controller gain, the small-signal model of Fig. 7 is transformed into Fig. 10 [16]. The most significant loading is the MOSFET gate, which is interfaced by the driver. Hence,

$$H(j\omega) = A_P(j\omega)\cdot A_G(j\omega) \tag{14}$$

$$A_P(j\omega) = \frac{(R_{ap} + Z_{cp})\,A_{OL1}(j\omega)}{R_{ap}A_{OL1}(j\omega) + Z_{OA1} + R_{ap} + Z_{cp}} \cdot \frac{R_{dp2}}{1/j\omega C_{bi} + R_{dp1} + R_{dp2}} \tag{15}$$

$$A_G(j\omega) = \frac{-Z_{cg}A_{OL2}(j\omega) + Z_{OA2}}{R_{ag}A_{OL2}(j\omega) + Z_{OA2} + R_{ag} + Z_{cg}}. \tag{16}$$

The class-AB amplifier model in Fig. 10 is a parallel equivalent circuit of two common-collector BJT models. In Fig. 10, the transconductance g_{me} is the sum of g_m of the two BJTs. R_{oe}, $R_{\pi e}$, $C_{\pi e}$, and $C_{\mu e}$ are parallel equivalent values of the corresponding parasitic elements within the two transistor models. $R_{CBe} = R_{CB1} \parallel R_{CB2}$. A simplified base-voltage-to-emitter-voltage transfer function is (17), where the driver parasitic

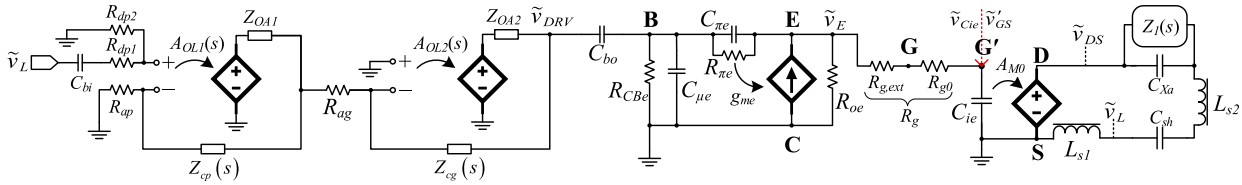

Fig. 10. Small signal model for the open-loop gain, including the hybrid filter network and the controller.

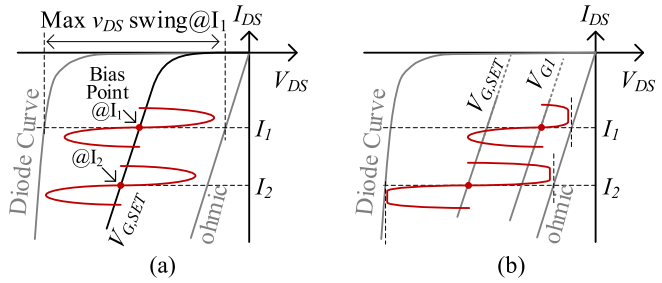

Fig. 11. Illustration for the biasing scheme of the proposed linear application of MOSFET in third quadrant. Bias point is defined by gate voltage level and D–S current level. $\tilde{v}_{DS}$ fluctuation is depicted. (a) Proper bias, no clipping. (b) Improper bias (at V_{G1}), and ac overdriving both results in clipping of the v_{DS}. If V_G is set too high, the MOSFET will conduct like standard SR, inside ohmic region.

elements are neglected

$$D(j\omega) = \frac{\tilde{v}_E}{\tilde{v}_B}(j\omega) \approx \left[1 + \frac{1}{g_{me}}\left(\frac{1}{R_g + (j\omega C_{ie})^{-1}} + \frac{1}{R_{oe}}\right)\right]^{-1}. \quad (17)$$

V. Circuit Design

The design for a practical power line filter circuit requires comprehensive consideration, analysis, and fine tuning. In this part, the most basic design procedures are provided with an explanation of the purpose of design.

A. MOSFET Selection

The most important parameters in selecting proper devices are enough current and *D-S* voltage rating, low $R_{DS(\mathrm{ON})}$, low reverse conduction voltage, and wide bandwidth in VCVS operation. Among the devices of adequate ratings, those with minimal $R_{DS(\mathrm{ON})}$ are preferred because the ohmic characteristic confines the voltage swing of the small-signal $\tilde{v}_{DS}$ as shown in Fig. 11. Higher swing means the capability to compensate stronger ripple noise. If $R_{DS(\mathrm{ON})}$ of a MOSFET is too large, the ohmic region approximates the diode curve, the VCVS property tends to vanish. An equation for estimating the needed $R_{DS(\mathrm{ON})}$ is

$$R_{DS(\mathrm{ON})} < (0.7 - |v_{DS,\mathrm{pk-pk}}|)/|I_{DS}| \quad (18)$$

which puts a relatively low ceiling for the $R_{DS(\mathrm{ON})}$. $|v_{DS,\mathrm{pk-pk}}|$ is the swing of the $\tilde{v}_{DS}$, around 0.2–0.4 V.

However, devices of low $R_{DS(\mathrm{ON})}$ usually have large parasitic capacitances that hinder the bandwidth of the device. Finally, the device should be able to achieve lower reverse conduction voltage than a diode of similar voltage and current ratings. Nevertheless, the above design factors are sometimes mutually contradictory. In particular, the $R_{DS(\mathrm{ON})}$ and parasitic capacitances of high-voltage devices are also high in nowadays technologies. It will limit the performance of the filter. The most acceptable MOSFETs are of superjunction type because they generally have low $R_{DS(\mathrm{ON})}$ among high-voltage MOSFETs. The key parameters A_{M0}, R_{SD0}, and $|v_{DS,\mathrm{pk-pk}}|$ can be measured by inexpensive instruments.

B. Passive Component Selection

The DM passive componentsC_{sh}, $L_{s1,s2}$, and C_{Xa} are critical in the hybrid filter design. First, the converter input capacitor C_{sh} should be sufficiently large due to the limited ripple compensation capability of the MOSFET. In the ideal case of EMI elimination, $\tilde{v}_{DS}$ fully compensates the $\tilde{v}_{Csh}$. C_{sh} can be estimated by

$$C_{sh} > |i_{P,\mathrm{pk-pk}}|/2\pi \mathrm{f}\,|v_{DS,\mathrm{pk-pk}}| \quad (19)$$

which is based on the single-tone approximation for the ripple. Good estimation can be done using the converter's switching frequency for the variable f in (19). Large capacitance value benefits filtering performance, but it is practically limited by the size, cost, and power factor (PF) requirements. Considering the size and cost, dc-rated film capacitors are preferable than the ac-rated products, especially those safety certified. Therefore, C_{sh} is chosen a dc-rated type. However, since C_{Xa} must be an X-cap, its value is selected to be much smaller, e.g., 1/10 of C_{sh}. Finally, the $L_{s1,s2} - C_{Xa}$ combination should ensure sufficient attenuation of the switching frequency. A simple equation for selecting total inductance value is

$$\mathrm{f}_{\mathrm{res},\,LC} = \frac{1}{2\pi\sqrt{L_{s1,s2}C_{Xa}}} < \frac{1}{2}\mathrm{f}_{\mathrm{sw}}. \quad (20)$$

L_{s1} and L_{s2} are two identical inductors separated onto both lines, like in Fig. 7, for better CM EMI reduction. f_{sw} is switching frequency of the converter.

C. Controller Design

First, during the conduction phase, the MOSFET gate dc voltage level V_G is hardware-preset. Therefore, the dc *load line* of the MOSFET is simply the *V–I* trace set by the V_G, as shown in Fig. 11. I_{DS} is determined solely by the power converter; its variation

makes the V_{DS} moving along the dc load line. The importance of selecting the proper load line as well as the V_{DS} bias is to keep the fluctuation of $\tilde{v}_{DS}$ within the linear VCVS area. Fig. 3 shows that all *V–I* traces droop naturally along I_{DS} and are bounded by the sloped diode and ohmic regions. Therefore, having preset value of V_G is the simplest design to keep $v_{\rm DS}$ range within the bounds throughout I_{DS} variation, as illustrated in Fig. 11(a). To determine a proper V_G level, one may examine the *V–I* graph for the curve(s) allowing maximum $\tilde{v}_{\rm DS}$ swing throughout the specified input current range of the converter. If V_G is incorrectly set, like the V_{G1} trace in Fig. 11(b), $v_{\rm DS}$ is clipped near the boundaries and the VCVS behavior becomes nonlinear. Even if the load line is properly defined, overdriving of the ac gate voltage could also result in clipping shown in the same figure. The configuration is shown in Fig. 6(b) is used to find the optimized gate bias voltage more precisely. A total of 3.5 V is chosen for the IPP60R060P7 MOSFET.

Second, a preliminary controller design of the two cascaded high-speed amplifiers is introduced. Stability must be ensured while higher gain is preferred. In Section V-B, the passive components are designed as 1) C_{sh} value is sufficiently large; 2) the resonant pole of $L_{s1,s2} - C_{Xa}$ is sufficiently low so that within the concerned frequency range, both capacitors C_{sh} and C_{Xa} can be considered as a short circuit. Then, the filter network in Fig. 10 can be simplified as a series circuit of MOSFET, L_{s1} and L_{s2}. Thus, the gain of the filter network (12) can be simplified as

$$\frac{\tilde{v}_L}{\tilde{v}'_{GS}}(j\omega) \approx \frac{1}{2}A_{M0}. \tag{21}$$

Its value is around -20 dB with zero phase. To simplify the design procedure, the phase lag due to the pre-amp is neglected, and the pre-amp is considered as a constant gain A_{P0}. The total phase lag only counts on the combination of the gain amplifier and the MOSFET. The open-loop transfer function of the gain-amp is written as [26]

$$A_{OL2}(j\omega) = A_{OLG}\frac{1}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2}}\right)}. \tag{22}$$

Substitute (22) into (16). The amplifier's small output impedance Z_{OA2} is neglected for simplicity. Then the closed-loop transfer function of the gain-amp can be rewritten as

$$A_G(j\omega) \approx -\frac{Z_{cg}}{R_{ag}}\left[1+\frac{R_{ag}+Z_{cg}}{R_{ag}A_{OLG}}\left(1+\frac{j\omega}{\omega_{p1}}\right)\left(1+\frac{j\omega}{\omega_{p2}}\right)\right]^{-1}. \tag{23}$$

Assume that the driver is an ideal buffer. The overall open-loop gain, i.e., simplified expression of (13), is given as

$$A_{\rm OPL}(j\omega) \approx -\frac{1}{2}A_{M0}\cdot A_{P0}\cdot A_G(j\omega)\cdot\frac{1}{1+j\omega R_g C_{iss}}. \tag{24}$$

For (24), it is preferable to set the gain-amp with a much higher bandwidth than the MOSFET, while adding no external gate resistor. Because in this way $A_G(j\omega)$ exhibits a flat gain, and the open-loop gain $A_{\rm OPL}(j\omega)$ only exhibits RC response defined by the MOSFET input impedance, which ensures a $+90$ degree phase margin. However, this scheme requires a very high-GBW amplifier. If a less extreme amplifier is used, the gain-amp pole might be closer to the MOSFET input pole, which leads to -40 dB/decade roll-off. Then the phase margin can hardly be adequate. A compensation circuit to the gain amplifier is then added, and a Type-II compensator as shown in Fig. 12 is used to pull down the loop gain at a lower frequency than the MOSFET input pole and boost the phase near the crossover frequency. The pole created by the compensator can be estimated by

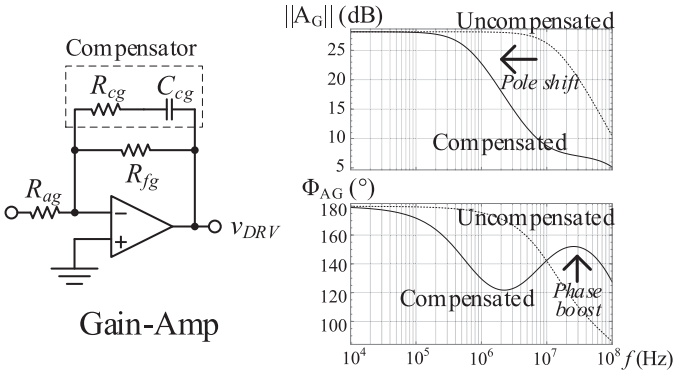

Fig. 12. Type-II compensator circuit and its effect.

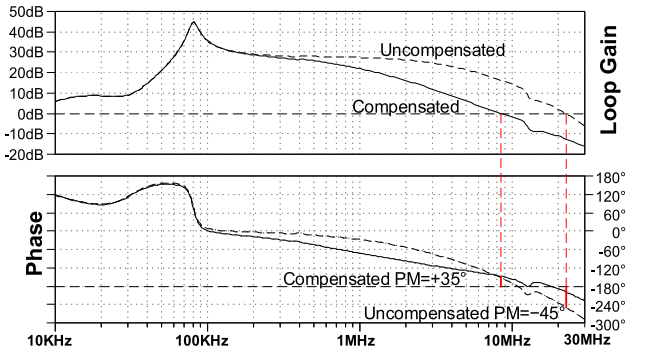

Fig. 13. Overall open-loop gain simulated with LTspice. The compensation technique based on the simplified model is verified by this model. Phase margin is improved by 80°.

$$\omega_{p,\rm comp} \approx \frac{1}{R_{fg}C_{cg}}. \tag{25}$$

The zero created by the compensator can be estimated by

$$\omega_{z,\rm comp} \approx \frac{1}{R_{cg}C_{cg}}. \tag{26}$$

The simulated loop gain is shown in Fig. 13. After the compensation, the original bandwidth is reduced to compromise with the phase margin.

The key circuit design parameters with component selection are shown in Table I.

VI. Experimental Verification

A hybrid filter prototype with the proposed ABR is built. It is tested with the converter part using a boost PFC evaluation

TABLE I
KEY PARAMETERS AND COMPONENTS

Item	Value	Item	Value
C_{sh}	2.2μF, DC film cap	Gain-amp	LMH6654
L_{s1}, L_{s2}	10μH each, (IHLP3232DZER100M01)	R_{ag}, R_{fg}	390Ω, 10kΩ
C_{Xa}	0.22μF, X2 film cap	R_{cg}, C_{cg}	1kΩ, 22pF
L_{CM}, L_{lk}	560μH@200kHz, 4.1μH leakage (KEMET SCF-05-350)	ω_{p1}, ω_{p2}	23kHz, 500MHz
		A_{OLG}	15000
C_Y	2.2nF each, Y2 ceramic	Pre-amp	AD8038
C_{Xb}	-	R_{dp1}, R_{dp2}	100Ω,1kΩ
MOSFET	IPP60R060P7	R_{ap}, Z_{cp}	100Ω, 1kΩ
A_{M0}, R_{SD0}	0.21, 0.07Ω	Class AB amplifier	MMBT3904, MMBT3906
R_{g0}, $R_{g,ext}$	2.8Ω, 5Ω		
C_{iss}, C_{ie}	5nF, 4.6nF	R_{CB1}, R_{CB2}	3kΩ, 2.5kΩ

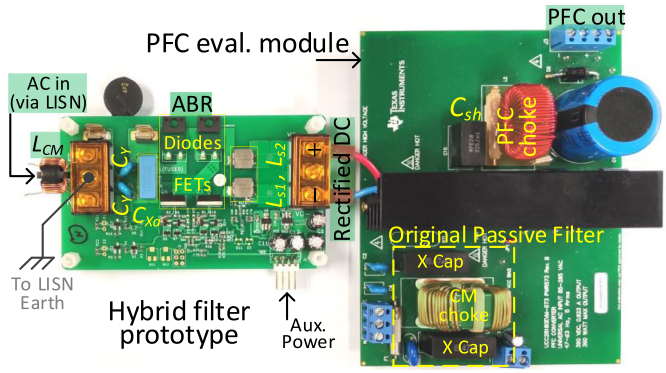

Fig. 14. Test configuration. The hybrid filter prototype including the proposed ABR is connected to a PFC.

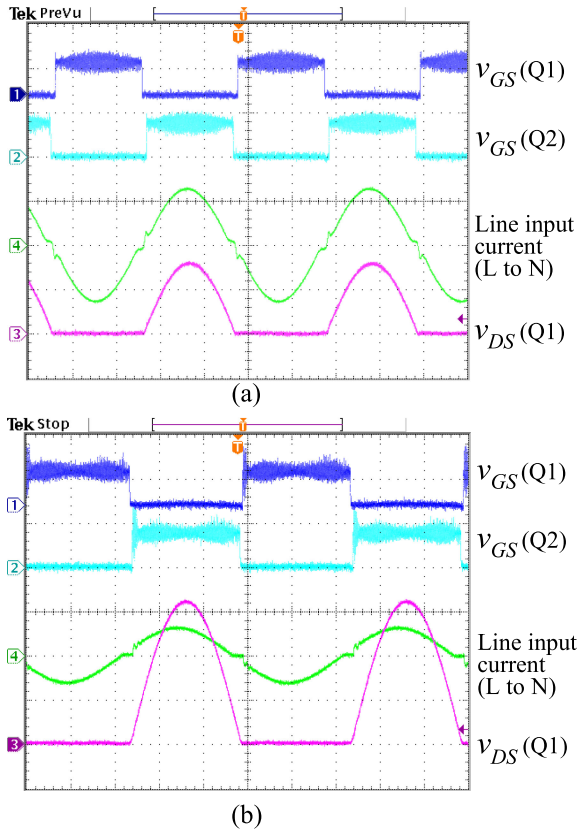

Fig. 15. Key waveforms of the PFC with hybrid filter, with (a) 115 V 60 Hz input and (b) 230 V 50 Hz input. CH1, CH2: 5 V/div, CH3: 100 V/div, CH4: 2 A/div. Timescale: 4 ms/div.

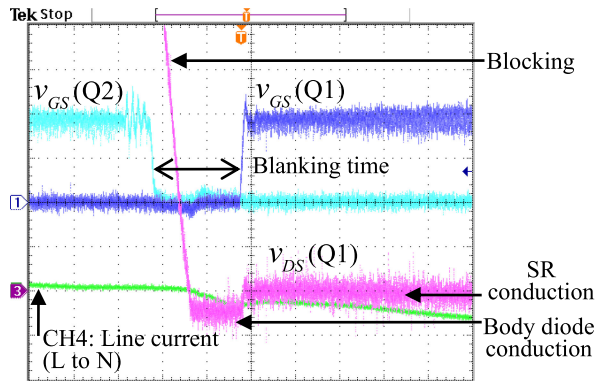

Fig. 16. Transients during the MOSFETs' commutation. CH1, CH2: 2 V/div, CH3: 1 V/div, CH4: 2 A/div. Timescale: 200 μs/div.

module, Texas Instrument UCC28180EVM-573, which runs in CCM with average current mode control. The original onboard passive filter (*C-L-C* filter, two 0.47 μF X-cap, and a 5 mH CM choke) and rectifier are disconnected from the circuit, replaced by the filter prototype. The input capacitor C_{sh} is changed from 0.33 to 2.2 μF. The switching frequency of the PFC is adjusted to 200 kHz. The other parts of the PFC remain unchanged. The circuit configuration under test is shown in Fig. 14. The input voltage is 115 V 60 Hz and 230 V 50 Hz. The output voltage of the PFC is 390 V. The load is an 800-Ω wire-wound resistor. The power source is Kikusui PCR500LA. The LISN is EMCO 3180/2.

The key operation waveforms of the proposed ABR are shown in Fig. 15. The MOSFET gates commutate regarding to the line voltage to implement rectification. During the conduction state of a MOSFET, its driver output is pulled up to the preset level with fast control signal superimposed, exhibiting an envelope shape. The line input current is solely shaped by the PFC. The drain-source waveform reflects the blocking and conduction states of the MOSFET.

A closer view shows a commutation transient in Fig. 16. As the line current crosses zero, Q1 voltage drops rapidly. Q2 is turned OFF before Q1 is turned ON. The blanking time is around 400 μs. The blanking time is adjustable through changing the value of R_{Pol} in Fig. 9(c). By using a smaller R_{Pol}, lower grid voltage can trigger the transistor, therefore the trigger point is closer to zero-crossing point and the blanking time can be reduced. Since the blanking time is utilized by the interlocking mechanism to avoid shoot through, too short blanking time might reduce the safety margin. Moreover, the gate-source voltages applying to the MOSFETs might bounce around zero crossings of the grid voltage due to low triggering voltage.

As shown also in Fig. 16, the ABR behaves like a typical diode bridge rectifier during the blanking period. The conduction

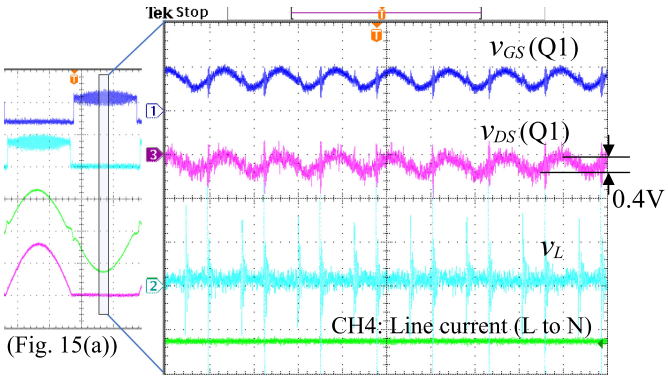

Fig. 17. Active filtering operation of a MOSFET in the ABR. CH1: 5 V/div, CH2, CH3: 1 V/div, CH4: 2 A/div. Timescale: 4 μs/div.

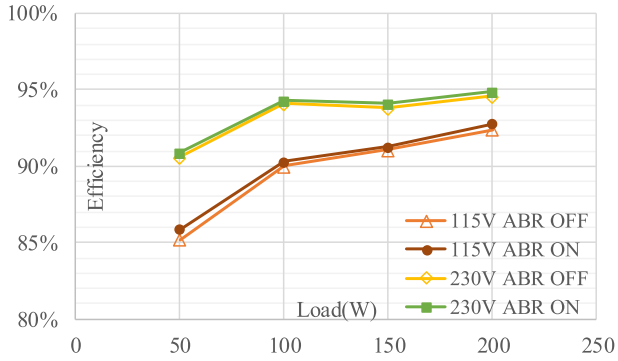

Fig. 18. Efficiency under various conditions versus load power.

voltage difference of body diode and SR is observable as a minor step at the bottom of the drain voltage. Thus, long blanking time might increase the power loss and EMI, but not significant, because the input current magnitude and its associated current ripple are small around zero crossing.

A closer view of the active filtering operation is shown in Fig. 17. The waveforms match the illustration in Fig. 2. The inductor voltage v_L is a weak ac ripple. It is amplified as the v_{GS} to drive the MOSFET. The $\tilde{v}_{DS}$ has a similar shape as $\tilde{v}_{GS}$ with the scale factor of 1:5, which reflects $A_{M0} \approx 0.2$ in the MOSFET VCVS model. The ripple in v_{DS} is 0.4 Vp-p. The dc bias in $v_{\rm DS}$ can be observed as the slightly negative voltage in CH3. The spikes appear in Fig. 17 is due to the switching action of the PFC connected to the output of the ABR. Moreover, oscilloscope probes can also pick up such high-frequency spikes. The frequency of the spikes is found to be 200 kHz, which is the same as the switching frequency of the PFC. Because high-voltage differential probe is used, there is noticeable offset error as well as noise in $v_{\rm DS}$ waveform.

The efficiency versus loading power is shown in Fig. 18. The power quality measurements are shown in Table II. They are measured with a power analyzer Voltech PM6000. The efficiency is obtained by measuring the input and output power of the setup in Fig. 14. First, the setup was measured with the ABR controller disabled. The ABR module was effectively a diode bridge rectifier. The measurement was taken after operating the PFC for 5 min. Then, the setup was measured with the ABR

TABLE II
POWER QUALITY MEASUREMENTS WITH 200-W LOAD

Test Condition	115V, 60Hz		230V, 50Hz	
Status of the ABR	Enabled	Disabled	Enabled	Disabled
PF	0.996	0.996	0.976	0.976
THDi (%)	5.44	5.58	6.46	6.61
Efficiency (%)	92.8	92.4	94.9	94.6

TABLE III
SINGLE-DEVICE POWER LOSS MEASUREMENTS

Test Conditions (*SR-MOSFET using IPP60R060P7)	115V, 60Hz	230V, 50Hz
Diode, in original rectifier GBU8J-BP	1.16W	0.49W
Body diode operation, V_{GS}=0V	1.18W	0.63W
Standard SR operation, V_{GS}=6.7V	0.26W	0.13W
Proposed ABR operation, V_{GS}=3.5V	0.65W	0.31W

controller enabled. The measurement was taken after operating the PFC for 5 min. The results show that the ABR has no impact on the PF and the total harmonic distortion of the input current (THDi). Efficiency is improved as expected with the ABR due to the lowered dropout voltage of the SR MOSFETs.

From the perspective of power loss, when the input is 115 V, 60 Hz, the loss is reduced from 200/0.928 $\times$ (1–0.928) $=$ 15.52W to /0.924 $\times$ (1–0.924) $=$ 16.45 W with the ABR enabled, showing a reduction of (16.45–15.52)/15.52 $=$ 5.65%. Similarly, when the input is 230 V, 50 Hz, with the ABR enabled, the reduction is 5.87%.

The conduction losses of various devices are measured and are shown in Table III. The device power loss was obtained by using calibrated oscilloscope and probes to measure the voltage and current waveforms associated with the device. After multiplying the voltage and current waveforms over the conduction period with the MATH function, the average value is used to determine the average device power loss. The off-state power loss has not been taken into account, as the leakage current is extremely small. Especially, the loss of the MOSFET in standard SR operation, i.e., reverse fully turn-ON, is also measured. The data show that the proposed active rectifier device consumes significantly less power than a diode.

Although the proposed active driving technique requires a higher dropout voltage than standard SR driving, it gains the capability in noise reduction. The ABR control circuit consumption is about 160 mW.

The transient responses of the PFC under different operating conditions have been tested and are given in Fig. 19. CH1 and CH2 show the measured waveforms of the drain-source voltage of the two MOSFETs in the ABR. CH3 is the input current of the PFC. CH4 is the gate-source voltage of one of the MOSFETs in the ABR. Fig. 19(a) shows the start-up transients of the PFC when the input voltage is 115 V, 60 Hz, and the output power is 200 W. Due to initial charging of the output capacitor, the input current has a high inrush current. Such inrush current is limited by a thermistor in the PFC evaluation module. Afterward, the input current becomes sinusoidal. Fig. 19(b) shows the load transients when the output power is changed from 100 to 200 W. The input current can remain sinusoidal over the transient

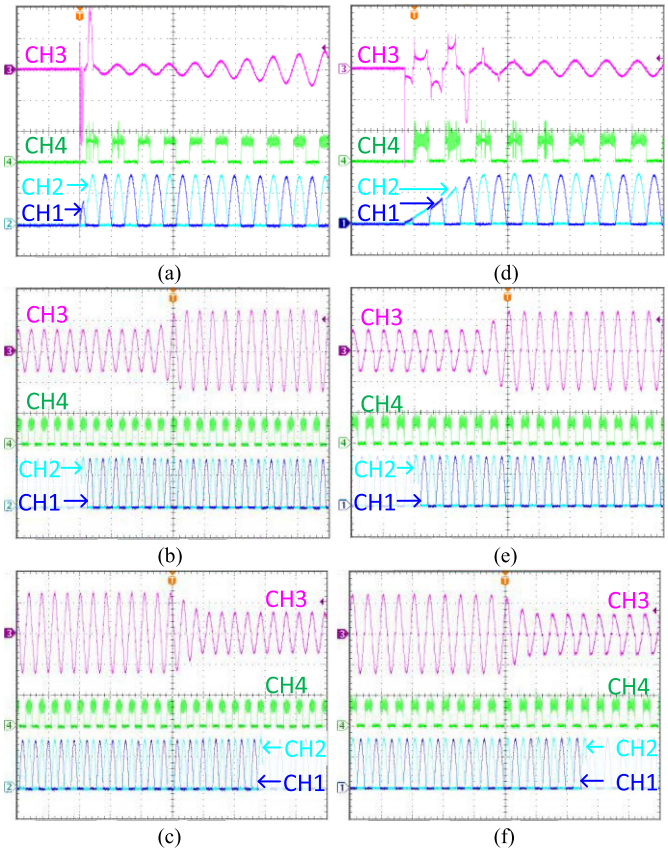

Fig. 19. PFC power transient waveforms. (a)–(c) 115-V 60-Hz input. CH1, CH2: 100 V/div. CH4: 5 V/div. (a) CH3: 5 A/div. Timebase: 20 ms/div. (b), (c) CH3: 2 A/div. Timebase: 40 ms/div.(d)–(f) 230 V 50 Hz input. CH1, CH2: 200 V/div. CH4: 5 V/div. (d) CH3: 5 A/div. Timebase: 20 ms/div. (e), (f) CH3: 1 A/div. Timebase: 40 ms/div.

period. Fig. 19(c) shows the load transients when the output power is changed from 200 to 100 W. The input current remains sinusoidal over the transient period.

Fig. 19(d)–(f) shows the corresponding start-up transients with the input voltage of 230 V, 50 Hz, and the output power of 200 W. The performance is similar to that with the input voltage of 115 V, 60 Hz.

Apart from lowering power loss, reduction of EMI of the power converter is also a key consideration in the proposed research work. Conducted EMI is measured by the Rohde & Schwarz ESCI7 receiver via a coaxial cable connected to the LISN signal output. The receiver frequency step is set to be 4 kHz, RBW 9 kHz, and measurement time 20 ms with a peak detector. In Fig. 20, the EMI scan results of three configurations are compared. They are

1) original evaluation board configuration with bulky passive filter;
2) hybrid filter, with the proposed active rectifier enabled;
3) hybrid filter with the active rectifier disabled, i.e. acting as diode bridge.

Under both ac input conditions, the PFC with ABR enabled exhibits lowest EMI emission; −20-dB reduction is achieved comparing to the original passive filter configuration at 200 kHz. It confirms the filtering function of the ABR.

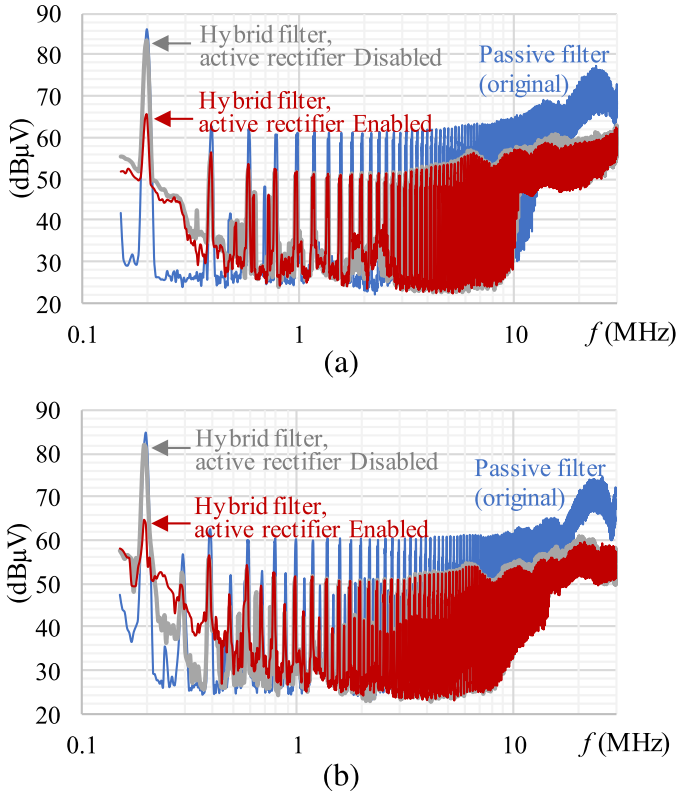

Fig. 20. EMI scan results from Rohde & Schwarz ESCI7 receiver. The ABR control is turned OFF resulting in the bold gray curves, for which the filtering is determined merely by the passive components within the hybrid filter. Input conditions: (a) 115 V 60 Hz. (b) 230 V 50 Hz.

TABLE IV
PASSIVE COMPONENT SIZE MEASUREMENTS

Part	Hybrid filter (mm^3)	Original filter (mm^3)
C_{sh}	17.5×15.5×10	17.5×9.5×17.5
C_{Xa}	18×7×12.5	25×8.5×18.5
L_{CM}	16×12×16	37×20.5×38
C_{Xb}	-	25×8.5×18.5
L_{s1}, L_{s2}	8.2×8.6×4, 2pcs.	-
C_Y	9×5×11, 2pcs.	9×5×11, 2pcs. (2.2nF each)
Total	8914	40585

Finally, the volume of the passive components from the hybrid filter is compared with the original passive filter, in Table IV. The total volume of the passive components is reduced by 78%. There is no C_{Xb} added in the hybrid filter.

VII. DISCUSSION

The proposed ABR benefits the volume reduction of the EMI filter. In the experiment, the original passive filter of the evaluation board has no dedicated DM inductor; the CM choke contributes its leakage inductance as DM inductance. However, to achieve an adequately large leakage inductance for DM filtering, the CM choke might be large. The active rectifier relaxes the requirement of DM filtering inductance, thus contributes to the total size reduction of the filter. In the prototype ABR,

four discrete TO-220 package devices are used, the total size is 3000 mm^3. The size of the original diode bridge module in the evaluation board is around 1700 mm^3. The size of the ABR is not much larger than the integrated diode rectifier. Package integration of the discrete power devices may eliminate the size penalty on using the MOSFETs. Moreover, the loss reduction due to the proposed technique could require less material and space for heat dissipation. The proposed analog controller and driver can be easily integrated without high voltage process. Therefore, the size penalty on the control part could also be minimized.

The limitations of the proposed technique are the relatively small $\tilde{v}_{\rm DS}$ swing, limited bandwidth and high cost. First, the limited MOSFET voltage swing restricts the noise amplitude to be compensated. The limitation can hardly be removed due to the body diode property ($\sim$0.7 V) and the demand for low dropout (lower than diode). As an example, SiC MOSFETs allow larger voltage swing in third-quadrant operation because of its high body diode threshold voltage [3], [27]; however, for correct load line, the dropout voltage has to be increased accordingly, which leads to higher loss than diodes. Second, the limited bandwidth mainly due to the MOSFET frequency response. Fortunately, the DM filtering do not require very high bandwidth. The proper design of fast controller is of higher importance. Finally, the cost for a usable MOSFET plus the high-speed amplifier for this application is much higher than a diode currently. Technically speaking, wide bandgap devices can offer better performance. However, due to their high cost, they are currently not the best candidate. This is expected to be settled through the evolution of semiconductor technology, which may improve the dynamic characteristics and power handling capability of even Silicon MOSFETs.

VIII. Conclusion

The MOSFETs in the proposed ABR are not operated in the first quadrant ohmic or saturation region. Instead, they are operated in the third quadrant saturation region. In the first quadrant ohmic region, the ON-state resistance of MOSFETs can be adjusted by changing the magnitude of the gate-source voltage. In the saturation region, the channel is pinched off. The drain current is in linear relationship with gate-source voltage.

It has been shown experimentally that the gate-source voltage is in a linear relationship with the drain-source voltage in the third quadrant saturation region, behaving differently from the characteristics in the first quadrant. In addition, the required bias in the gate-source voltage, operating range, and frequency response are different from that in the first quadrant operation.

This article reveals the linear dependent voltage source property of an *n*-MOSFET in reverse operation in both dc and ac. It is attempted to provide a proof with semiconductor physics equations. The property is also verified by experiments. A linearly driven ABR is built based on this property, exhibiting an EMI reduction function. It is considered as an inductor-enhancing device in a hybrid filter. Small signal model of the hybrid filter is provided. The design consideration is shown. The proposed active rectifier plays two roles, i.e., rectification and filtering, and facilitates reduction in power loss and filter size. It is expected that an integrated circuit can be fabricated for the entire ABR module, such as the one in [28]. Both the cost and physical size can, thus, be reduced. It is considered to be a novel idea of function integration for future high-power-density converters.

Further research will be dedicated to extending the technology to common-mode noise suppression.

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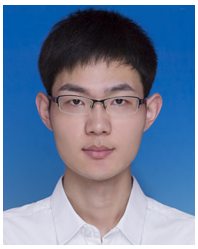

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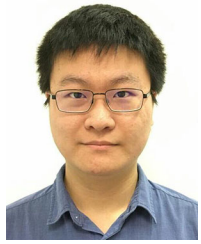

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