Letters

A Low-Loss Compact Reflected Wave Canceller for SiC Motor Drives

Yu Zhang, *Student Member, IEEE*, Hui Li, *Fellow, IEEE*, and Fang Z. Peng, *Fellow, IEEE*

***Abstract*—The overvoltage caused by reflected wave phenomenon in motor drives becomes worse with the application of SiC devices due to the significantly higher dv/dt compared with that of Si devices. This letter presents a low-loss and compact active reflected wave canceller (ARWC) to suppress the overvoltage at the motor terminal. The proposed ARWC circuit uses low current devices to break the rising and falling edges of the pulsewidth modulation voltage waveforms to two steps, whereas the second step cancels the first step reflection. In addition, the ARWC circuit does not require an additional dc power supply that allows the ARWC self-sustained. The experimental results on one phase 6 kVA application with and without proposed ARWC are provided and compared to verify the validity of proposed method.**

***Index Terms*—Motor drives, reflection, silicon carbide (SiC), surge voltage.**

I. Introduction

OVERVOLTAGE at motor terminals due to reflected wave phenomenon (RWP) is recognized as a main source of premature winding insulation failures in drive systems. This issue becomes more serious with the application of SiC devices that has significantly higher dv/dt compared with that of Si devices [1]. The high dv/dt leads to the RWP happens in a motor drive at shorter cable length. In [2], it is reported the overvoltage ratio at the motor terminal increased from 20% to 100% when pulsewidth modulation (PWM) voltage rise time decreased from 200 to 25 ns with 20 ft cable length.

Passive dv/dt filters are usually adopted to suppress the overvoltage caused by the RWP [2], [3]. However, passive dv/dt filters are bulky and generate high power loss, especially for high-frequency motor drive applications. Recently, an optimized passive dv/dt filter for a 75-kW SiC inverter drive is presented in [2]. The total weight of this optimally designed dv/dt filter is 2.8 kg and the power loss of the damping resistor is 191 W per phase.

In order to overcome the bulky size and high power loss of traditional passive dv/dt filters, several active dv/dt filters have been developed. In [4], an active control with *LC* circuit is proposed to reduce the overvoltage by shaping the rising/falling edge of the inverter output voltage. With the active control, the filter inductance can be designed to be notably smaller than the one in a conventional dv/dt filter, resulting in smaller filter size. Since a single-charge pulse is required at each rising/falling edge, the switching loss will increase, especially in SiC inverters which usually operate at much higher switching frequency compared with Si-inverters.

An active motor terminal dv/dt filter to achieve low-loss is presented in [5] and [6]. The filter is not only designed to clamp the maximum motor terminal voltage, but also can alter the rising/falling edge to improve the interturn voltage distributions in the motor. The power loss is extremely low with the synchronous modulation, which help recover the energy gained from the overvoltage suppression. However, the passive components *R*, *L*, and *C* are still required in this method as well as additional active devices, voltage sensors, and microcontroller to perform the synchronous modulation, which increases the cost and size of this active filter.

In addition to above methods, the cancellation concept has been proposed in [7]–[10] to reduce the overvoltage at the motor terminal with low power loss. The *T*-type topology is adopted in [7] and the middle voltage level $V_{\rm dc}/2$ is utilized to break the inverter output voltage into two steps. Optimal cancellation can be achieved when the duration of the middle voltage level $V_{\rm dc}/2$ is equal to twice of the transmission time. The cost for this method is that it needs six active switches for three-phase motor drive that has the same current rating with the motor drive switches and the switching loss is also increased. A similar idea but using an external H-bridge for each phase is applied in [10] to generate a nanosecond voltage pulse to break the rising/falling edge into two steps for reflected voltage cancellation. The device current rating of the canceller is much smaller than the one in [7]–[9]. However, 12 active devices are required for three-phase application and the need of an external dc voltage supply may limit its application.

A low-cost solution to modify the PWM pulse pattern is also proposed to reduce the overvoltage [11], [12]. The PWM pulse pattern is modified with dwell time and polarity reversal time to prevent double pulsing phenomenon that occurs when a new switching signal arrives but the previous voltage oscillation is not fully decayed. This method can only reduce the overvoltage caused by double pulsing. Furthermore, for SiC inverters with

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The authors are with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL 32310 USA (e-mail: yz16@my.fsu.edu; hli@caps.fsu.edu; peng@caps.fsu.edu).

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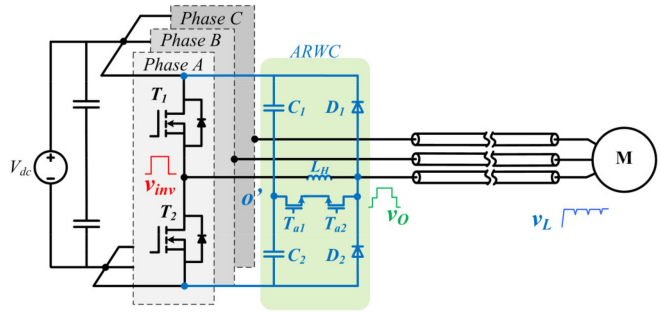

Fig. 1. Motor drive system with proposed ARWC to cancel overvoltage caused by reflective wave phenomenon.

high switching frequencies, large dwell time will become a significant portion of the PWM period, therefore, this method may result in voltage distortion for SiC motor drive.

This letter proposes a low-loss low-cost active reflected wave canceller (ARWC) for SiC motor drive based on the cancellation concept. The ARWC utilizes low current rating devices and reduces active device number to two per phase. In addition, the canceller does not need a separate dc power supply. The operation principle of the ARWC is described in Section II. The experimental verification of ARWC for one phase 6 kVA application is provided in Section III. Finally, the conclusion is presented in Section IV.

II. Operation Principle

The proposed ARWC in a motor drive system is presented in Fig. 1. It is located between the output terminal of the inverter and the input terminal of the cable. It consists of two active devices T_{a1}, T_{a2}, two diodes D_1, D_2, and one small inductor L_H for each phase. The two capacitors C_1 and C_2 provide a middle voltage level of V_{dc}. At each rising/falling edge of the PWM voltage waveforms, T_{a1} and T_{a2} are turned ON, clamping v_O to ½ $V_{\rm dc}$. After a nanosecond time interval, T_{a1} and T_{a2} turn OFF and D_1/D_2 turns ON, which operates in freewheeling mode where v_O equals to the output voltage of the inverter. Therefore, the rising/falling edge is broken into two steps that have a nanosecond time delay between these two steps. The reflected voltage at motor terminal of each step can be cancelled by accurately controlling this time delay.

According to the transmission line theory, this time delay can be calculated theoretically to cancel the reflected voltage of each step. The voltage at the motor terminal, v_L, can be expressed as

$$v_L\ (l,s) = \frac{(1+\Gamma_L)\cdot e^{-t_t\cdot s}}{1-\Gamma_L\Gamma_S\cdot e^{-2\cdot t_t\cdot s}}\ V_{\rm dc}\,(s) \tag{1}$$

where Γ_L is the reflection coefficient at the motor terminal; Γ_S is the reflection coefficient at the inverter side; t_t is the transmission time for the voltage travelling in the cable, which is defined by $t_t = l_{\rm cable}/v$; $l_{\rm cable}$ is the cable length; and v is the velocity of the voltage travelling in the cable, which is approximately half of the speed of light [10].

The reflection coefficient value Γ_L and Γ_S is defined as follows:

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}\ \text{ and }\ \Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2}$$

where Z_L is the motor impedance, Z_0 is the cable characteristic impedance, and Z_S is the source impedance. Typically, Γ_L is close to 1 and Γ_S is close to –1, because $Z_L \gg Z_0$ and $Z_S \approx 0$.

With the proposed ARWC, the rising/falling edge of v_O becomes a two-step waveform of which the amplitude is ½ $V_{\rm dc}$ the motor terminal voltage is, therefore, given as follows:

$$v_{L\_\rm ARWC}\ (l,s) = \frac{(1+\Gamma_L)\cdot e^{-t_t\cdot s}}{1-\Gamma_L\Gamma_S\cdot e^{-2\cdot t_t\cdot s}}\ \left(1+e^{-t_d\cdot s}\right)\frac{V_{\rm dc}\,(s)}{2} \tag{3}$$

where $t_{\rm d}$ is the time delay between these two steps which need to be designed.

Letting $t_d = 2t_t$ in (3) yields

$$\begin{aligned} v_{L\_\rm ARWC}\,(l,s) &= \frac{(1+\Gamma_L)\cdot e^{-t_t\cdot s}}{1-\Gamma_L\Gamma_S\cdot e^{-2\cdot t_t\cdot s}}\ \left(1+e^{-2\cdot t_t\cdot s}\right)\frac{V_{\rm dc}\,(s)}{2} \\ &= \frac{\left(1+e^{-2\cdot t_t\cdot s}\right)\cdot e^{-t_t\cdot s}}{1-\Gamma_L\Gamma_S\cdot e^{-2\cdot t_t\cdot s}}\ (1+\Gamma_L)\frac{V_{\rm dc}\,(s)}{2}. \end{aligned} \tag{4}$$

Since $\Gamma_L\Gamma_S$ is close to –1, and Γ_L is close to 1, (4) becomes (5) which shows that the motor terminal voltage is close to the input voltage

$$v_{L\_\rm ARWC}\,(l,\ s) \approx V_{\rm dc}\,(s)\cdot e^{-t_t\cdot s}. \tag{5}$$

The key waveforms with the proposed ARWC are presented in Fig. 2, where only the rising edge scenario is presented, since the waveforms at the falling edge is symmetrical to the ones at the rising edge. In Fig. 2, $v_{\rm inv}$ is the PWM output voltage of the inverter with high dv/dt. v_O is the input voltage of the cable (refer to Fig. 1), which is broken into two steps v_{O1} and v_{O2}. Each step voltage will be transmitted to the motor terminal after the transmission time t_t. v_{L1} refers to all the reflected voltages of v_{O1} while v_{L2} is the reflected voltage of v_{O2}. The amplitude of v_{L1} and v_{L2} is twice of v_{O1} and v_{O2}, respectively, due to the RWP. v_L is the motor terminal voltage, which is the sum of v_{L1} and v_{L2}. It can be found that if the time delay between v_{O1} and v_{O2} is $2t_t$, the motor terminal will not see overvoltage because of the cancellation effect of v_{L1} and v_{L2}. The motor terminal voltage without the ARWC is also presented in Fig. 2 as shown by the red dotted curve at the bottom of which the amplitude is twice of the dc-link voltage.

Consider the similar operation of ARWC for each phase, the commutation of ARWC is illustrated on one phase. The equivalent circuit of one phase with ARWC is shown in Fig. 3, where mode (a)–(c) describes the commutation at the rising edge, the commutation at the falling edge is presented from mode (d) to (f). The corresponding waveforms from (a) to (f) is shown in Fig. 4. Each operation mode is described as follows.

Mode (a) [t_0, t_1]: T_1 turns ON at t_0. The rising edge appears at $v_{\rm inv}$. Since T_{a1}/T_{a2} are OFF, D_2 is freewheeling until i_{D2} decreases to zero and T_{a1}/T_{a2} is still in OFF state. The voltage

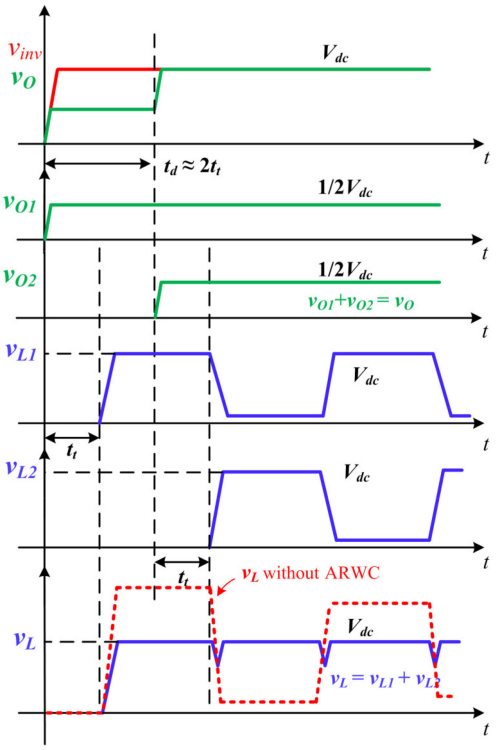

Fig. 2. Key waveforms of proposed ARWC.

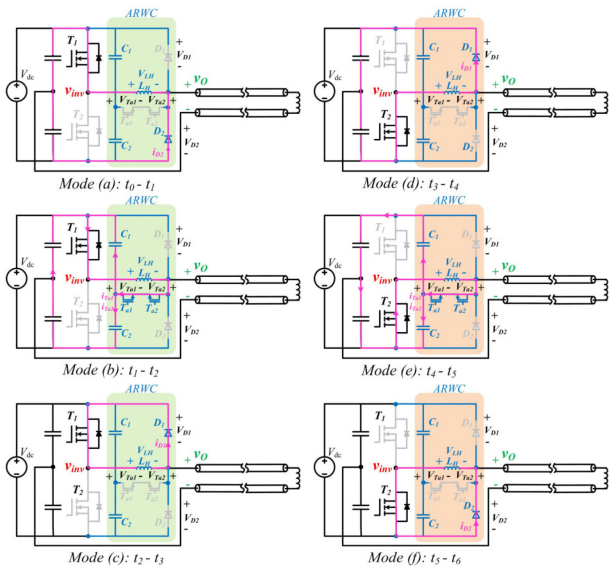

Fig. 3. Operation modes during commutation. (a)–(c) are operation modes at rising edge. (d)–(f) are operation modes at falling edge.

across L_H equals to $V_{\rm dc}$. Since L_H << load inductance, i_{D2} can be calculated as follows:

$$i_{D2}(t) \approx i_{D2}(t_0) - \frac{V_{\rm dc}}{L_H}(t - t_0). \tag{6}$$

It should be noted that in some switching cycles, i_{D2} already decreases to zero in mode (*f*), then D_2 keeps in OFF state.

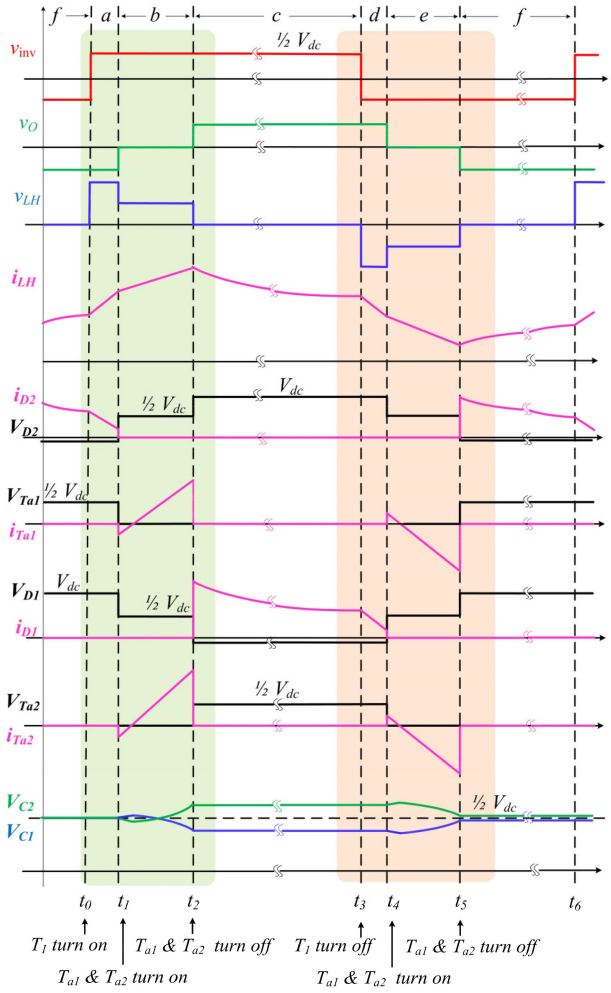

Fig. 4. Commutation waveforms during operation modes (a)–(f).

Mode (b) [t_1, t_2]: T_{a1} and T_{a2} turn ON. v_O is clamped to the middle level of $V_{\rm dc}$. During this time, $v_{LH} = 1/2\,V_{\rm dc}$. i_{Ta1}/i_{Ta2} start increasing and can be calculated as follows:

$$i_{Ta1}(t) \approx -i_{Ta1}(t_1) + \frac{V_{\rm dc}}{2L_H}(t - t_1). \tag{7}$$

It is important to mention that $t_2 - t_1$ equal to twice of transmission time t_t (refer to Fig. 2) to achieve the cancellation effect.

Mode (c) [t_2, t_3]: T_{a1} and T_{a2} turn OFF. D_1 operates in the freewheeling mode. i_{D1} starts decreasing, the decreasing slope depends on L_H and load current

$$i_{D1}(t) \approx i_{D1}(t_2) - \left(\frac{V_{D1}}{L_H} + \frac{1/2V_{\rm dc} + V_{D1}}{L_{\rm Load}}\right) \cdot (t - t_2) \tag{8}$$

where V_{D1} is the voltage drops of D_1.

Mode (d) [t_3, t_4]: T_1 turns OFF and T_2 turns ON at t_3, the falling edge appears at $v_{\rm inv}$. T_{a1} and T_{a2} are OFF. D_1 is freewheeling until i_{D1} decreases to zero.

Mode (e) [t_4, t_5]: T_{a1} and T_{a2} turn ON. v_O is clamped to the middle level of $V_{\rm dc}$. During this time, $v_{\rm LH}$ = ½ $V_{\rm dc}$ and i_{Ta1}/i_{Ta2} starts increasing.

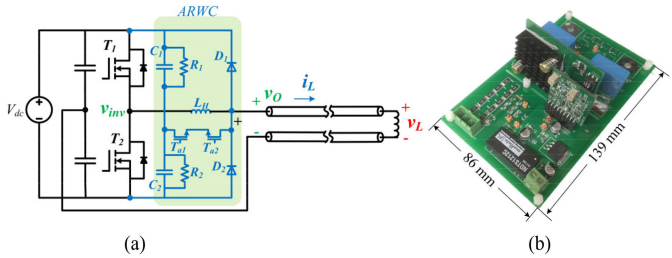

Fig. 5. Test setup to verify the proposed ARWC. (a) Testbed circuit diagram. (b) ARWC prototype photo.

Mode (f) [t_5, t_6]: T_{a1} and T_{a2} turn OFF. D_2 operates in the freewheeling mode. i_{D2} starts decreasing. It can be found that mode *(a)–(c)* is symmetrical to mode *(d)–(f)*.

According to the above analysis, T_{a1} and T_{a2} turn ON only in modes *(b)* and *(e)* of which the time period is twice of the transmission time t_t (typically hundreds of nanosecond), load current does not flow into T_{a1} and T_{a2}, therefore, T_{a1} and T_{a2} can be designed with relatively small current rating. In mode *(b)* and *(e)*, i_{Ta1} flows into the neural point of C_1 and C_2 charging/discharging C_1 and C_2. Due to duty cycle variation of the PWM waveforms, i_{Ta1} differs at each switching cycle, which will cause the voltage of the neural point fluctuating. C_1 and C_2 are designed to reduce the voltage variation of the neutral point. It is important to mention that due to the short charge/discharge durations in mode *(b)* and *(e)*, the size and rms current of C_1 and C_2 are small. $L_{\rm H}$ sizing is a tradeoff design. Large inductance will result in a small current rating of T_{a1} and T_{a2}. However, large inductance will also increase the size and power loss. The design principle of $L_{\rm H}$ is similar to [10] and will not be repeated here. It should be noted that in [10], the load current may flow into the canceller to increase the device current stress but will not happen in proposed ARWC. In addition, the canceller circuit of [10] requires a separate dc power supply, which need to be carefully designed to suppress common-mode noise, especially for SiC motor drive application. The ARWC in this letter does not have this issue due to removal of this power supply, resulting in a simple, low-cost, and enhanced immunity to common mode noise design.

III. Experimental Verification

A single-phase test bed is developed in the laboratory to verify the proposed ARWC, since the operation principle of ARWC is same for each phase. An air core inductor is utilized as the load. The dc input voltage is 400 V and the load rms current is 40 A to emulate a motor drive which one phase is rated as 6 kW. T_1 and T_2 are 1200 V SiC MOSFETs with ~17 V/ns dv/dt. The output fundamental frequency is 400 Hz while the switching frequency is 20 kHz. The schematic of the test bed and ARWC prototype is shown in Fig. 5(a) and (b), respectively. The key parameters of this test bed and ARWC prototype are presented in Table I. The 10 μF value is selected for C_1 and C_2 so that the middle-point voltage variation can be restricted within 5% of ½ $V_{\rm dc}$, the calculated rms current of C_1 and C_2 is less than 1 A based on Table I parameters, which implies again that the capacitors are very small in size, just like snubber capacitors filtering short switching transients.

TABLE I
Parameters of the Test Bed and ARWC Prototype

Parameters	Specs
V_{dc}	400 V
i_L	40A (RMS)
L_H	18 µH
T_{a1}/T_{a2}	600 V GaN LMG3410R150
C_1/C_2	10 µF Film capacitor
D_1/D_2	SiC Schottky Diode IDH06G65C5
T_1/T_2	1200V SiC MOSFET
l_{cable}	134 ft
Output frequency	400 Hz
Switching frequency	20 kHz
t_t	320 ns

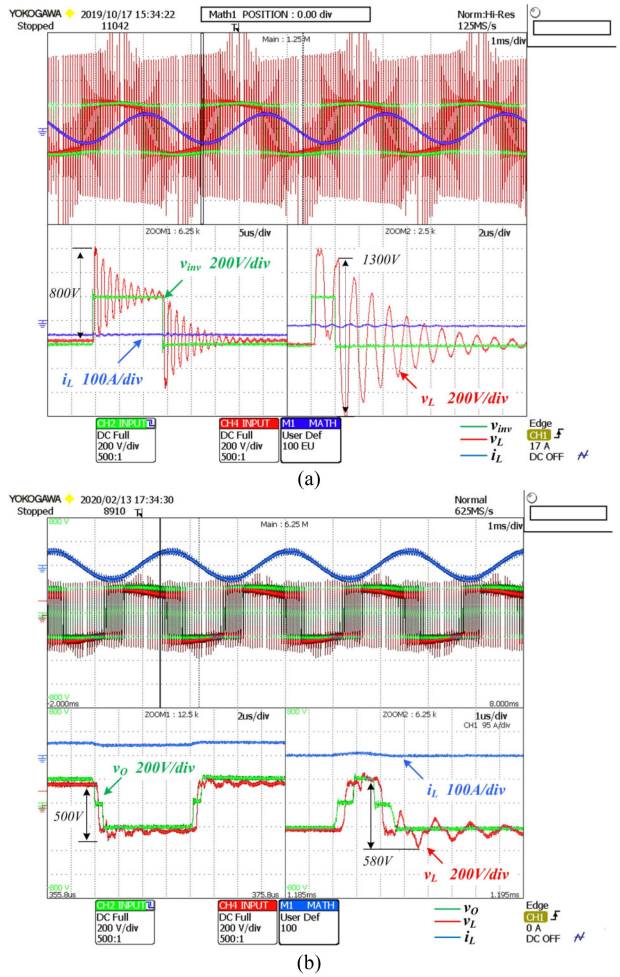

Fig. 6. Experimental results. (a) Inverter voltage, load voltage and load current w/o proposed ARWC. (b) Inverter voltage, load voltage and load current w/ proposed ARWC.

The load voltage, v_L, with and without the designed ARWC is presented in Fig. 6. Fig. 6(a) shows that when there is no ARWC, the peak to peak value of v_L is 800 V in most cases which is 200% of $V_{\rm dc}$. The ARWC is able to provide 75% reduction, suppressing the peak to peak value of v_L from 800 V (200% of $V_{\rm dc}$) to 500 V

(125% of $V_{\rm dc}$). It should be noted that in some switching cycles without ARWC, the peak to peak value of v_L is 1300 V as shown in Fig. 6(a), which is more than twice of $V_{\rm dc}$. This is caused by double pulsing phenomenon, i.e., when the rising and falling edge are very close to each other, the reflected voltage of the rising edge coupled with that of the falling edge, resulting in much higher load voltage than other switching cycles. With proposed ARWC, the peak to peak value of v_L in this case is suppressed from 1300 V (325% of $V_{\rm dc}$) to 580 V (145% of $V_{\rm dc}$), which is 180% reduction.

The measured total power loss of ARWC is 21.62 W at 6 kVA operation. The power loss breakdown is analyzed by calculating the switching loss (0.86 W), conduction loss (0.76 W), inductor loss (4.82 W), and diode and resistive loss in freewheeling modes (15.18 W) based on the experimental waveforms. It should be noted that the diode and resistive loss, which is the power loss during the freewheeling mode, account for 70% of total power loss. The resistive loss refers to the power loss dissipated on the resistance in the freewheeling loop, such as the MOSFET $R_{\rm dson}$ and the wire resistance. The reason of freewheeling mode loss becoming dominant is multifold. First, ARWC is operated at freewheeling mode most of time which increases this power loss. Second, the forward voltage drop of SiC Schottky diode applied in ARWC prototype is 1.5 V, which also increases the diode loss. Diode with lower forward voltage drop and low reverse recovery charge is, therefore, preferred in ARWC to reduce the power loss.

The experimental results and measured loss are based on inductive load. It is important to mention that with *RL* load, the cancelation performance will remain same, since mode *(b)* and *(e)* is not affected by load current, the loss in freewheeling modes will be different considering that load current can change the slope of diode current during freewheeling modes. The maximum power loss in freewheeling modes can be calculated as $1/2 \cdot V_{\rm dc\cdot Ipeak} \cdot t_d \cdot f_s$ by assuming diode current decrease to zero at each rising edge/falling edge of PWM waveforms. In our experiment, $I_{\rm peak}$ is 12 A, t_d is 640 ns, f_s is 20 kHz, the maximum power loss during freewheeling modes will be 30.72 W. Since the diode current does not decrease to zero in every switching cycle, the power loss during freewheeling mode with *RL* load will be smaller than 30.72 W.

When proposed ARWC is scaled up for high power SiC motor drive application, the current/voltage ratings of the device and capacitor sizing is directly affected by higher $V_{\rm dc}$ while L_H is directly affected by higher load current, since load current does not flow into ARWC devices but through L_H. On the other hand, the design of L_H affects the device current rating and capacitor rms current, therefore, there is a tradeoff design between the device/capacitor and L_H, where L_H can be optimized to minimize the ARWC loss and achieve smaller size and weight.

V. Conclusion

This letter has presented a low-loss ARWC based on cancellation concept for SiC motor drives. Compared to other active methods, especially those adopting similar concepts, the proposed ARWC has the advantages of low device numbers with low current ratings, simple control, and no need of an extra dc power supply that leads to low loss, low cost, and compact features. The operation principle of ARWC has been verified on a SiC based one-phase application. The experiment results have been provided to demonstrate the effectiveness of the proposed method. The proposed ARWC can achieve 75% reduction in most cases. The measured power loss is 21.62 W at 6 kVA with inductive load, which is an order of magnitude smaller than that of a passive filter.

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