A Dynamic Resonant Period Control Technique for Fast and Zero Voltage Switching in GaN-Based Active Clamp Flyback Converters

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***Abstract*—Compared to Si FETs, when the main GaN FET is in full zero voltage switching condition, maximum switching loss reduction can be achieved. Therefore, in this article, an active clamp flyback converter with GaN devices that implements fast ZVS by using the proposed dynamic resonant period control (DRPC) technique can reduce large transformer leakage inductance energy loss on the active resonant circuit. As the loading changes, the DRPC technique can dynamically adjust the ON-time in auxiliary switch to prevent large voltage stress on the components in the primary side. In full load condition, the leakage energy loss can be reduced, thereby transferring more energy to the secondary side with maximum efficiency up to 94%.**

***Index Terms*—Active clamp flyback (ACF), active resonant circuit (ARC), dynamic resonant period control (DRPC) technique, zero voltage switching (ZVS).**

I. Introduction

FLYBACK converters are often used in low power applications due to their simple circuit structure and reduced external component usage. The quasi-resonant (QR) flyback converter in [1] uses QR valley detection to reduce switching loss, but does not implement a full zero voltage switching (ZVS). Therefore, conventional active clamp flyback (ACF) converter uses the energy of the transformer leakage inductance to achieve full ZVS, thereby achieving high efficiency [2], [3]. However, due to the parasitic resistance on the active clamp circuit, the leakage inductance energy is wasted and leads to the performance of the ZVS effect compromised. That is, conduction loss will be larger than the reduction of switching loss. In [4], it uses an auxiliary switch in the active clamp circuit to delay conduction and to improve efficiency. However, since the on-time of the auxiliary switch is fixed, the voltage stress on the primary-side component becomes too large and ZVS fails when the primary-side current is too large or the auxiliary switch's conduction time is too short.

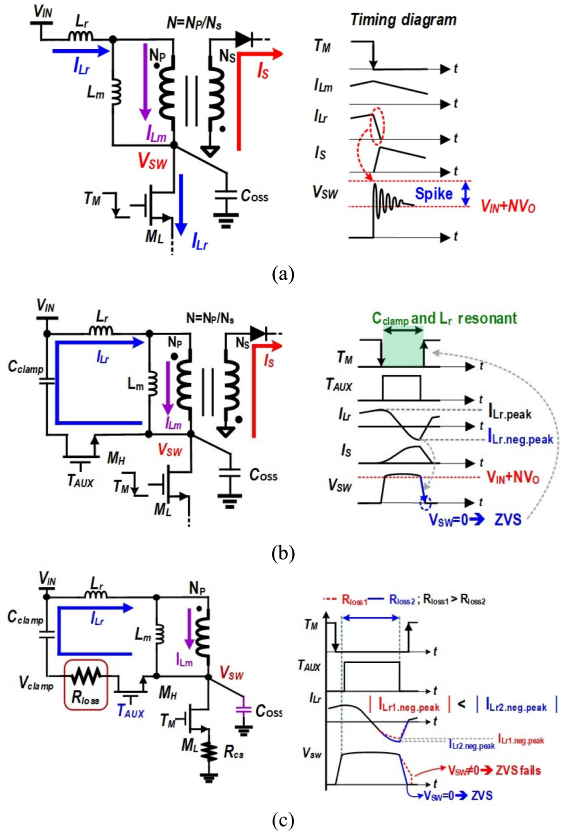

Fig. 1. (a) Conventional flyback converter. (b) Active clamp flyback converter. (c) $R_{\rm loss}$ critical to full ZVS.

In Fig. 1(a), the input voltage ($V_{\rm IN}$) of the conventional flyback converter stores energy to the primary side magnetizing inductance (L_m) and the leakage inductance (L_r) when the low-side switch M_L is turned ON. The current mode control determines when the M_L is turned OFF once L_m has sufficient energy. After that, L_m starts to transfer energy from the primary side to the

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secondary side output. Meanwhile, L_r releases the stored energy to resonate with the capacitance $C_{\rm OSS}$ at the switching node $V_{\rm SW}$. But, the released energy will cause large voltage spikes at the $V_{\rm SW}$ and result in high voltage stress on the switch M_L. Thus, Fig. 1(b) shows an active resonant circuit (ARC) composed of a clamp capacitor $C_{\rm clamp}$ and an auxiliary high-side switch M_H can resonate with the leakage inductor L_r. When M_L is OFF and M_H is ON, the energy in L_r resonates with $C_{\rm clamp}$ to effectively suppress the voltage spike at the $V_{\rm SW}$. At the same time, the resonance effect also causes the energy stored in the $C_{\rm clamp}$ to charge L_r in a counterclockwise direction. That is, negative current $I_{\rm Lr.neg}$ will discharge $C_{\rm OSS}$ to pull low $V_{\rm SW}$ to zero and to achieve full ZVS on the M_L when M_H turns OFF. Using the ARC to recycle the energy in L_r, the voltage spike of $V_{\rm SW}$ can be suppressed to achieve full ZVS for reducing switching loss of M_L.

In Fig. 1(c), switching power loss is basically from two parts: one is due to charging and discharging the output capacitance $C_{\rm OSS}$ in (1) and the other is due to the conduction loss of resonant current I_{Lr} on the parasitic resistances $R_{\rm loss}$ and $R_{\rm ON}$ of M_H in (2). $C_{\rm OSS}$ is the output capacitance of the power device, $V_{\rm ds}$ is the M_L's drain–source voltage, and $f_{\rm SW}$ is switching frequency [5]

$$P_{\rm loss\_SW} = C_{\rm OSS} V_{\rm ds}^2 f_{\rm SW} \tag{1}$$

$$P_{\rm loss\_Lr} = I_{Lr}^2 \cdot (R_{\rm loss} + R_{\rm ON}). \tag{2}$$

As a result of small $C_{\rm OSS}$ in GaN-based device, the full ZVS requires less resonant energy, which can significantly reduce switching loss [6]–[9]. Both rising and falling edges of $V_{\rm SW}$ also depend on the voltage variations across $C_{\rm OSS}$. In addition to the advantage of less switching loss, small $C_{\rm OSS}$ in GaN switches has lower $I_{\rm Lr(rms)}$, which also indicates that GaN switch can have less power loss at the point where the converter operates in full ZVS condition. The ACF technique in [4] uses the resonant energy to ensure full ZVS on GaN devices. However, owing to continuous energy resonating between the inductance and capacitance, larger leakage inductance L_r and more resonant current I_{Lr} are required to ensure full ZVS. In contrast, the proposed DRPC technique uses discontinuous resonant inductance current to improve efficiency.

On the ARC current path, parasitic resistances $R_{\rm loss}$ and $R_{\rm ON}$ of the M_H will cause the increase of $P_{\rm loss\_Lr}$ in 2). Large $P_{\rm loss\_Lr}$ will need more energy stored in L_r and insufficient energy stored in the L_r will cause the failure of full ZVS. Thus, to solve this problem, it is necessary to increase the value of L_r in conventional designs to store sufficient energy and ensure complete discharge of the $C_{\rm OSS}$ [11]–[17]. However, this incurs the increased cost and transformer volume. More seriously, overall efficiency also decreases due to the increase of L_r value.

In this article, the proposed GaN-based ACF with the dynamic resonant period control (DRPC) technique can use a small L_r to effectively achieve full ZVS for high efficiency, which is described in Section II. The circuit implementations are illustrated in Section III. Experimental results are shown in Section IV. Finally, Section V concludes this article.

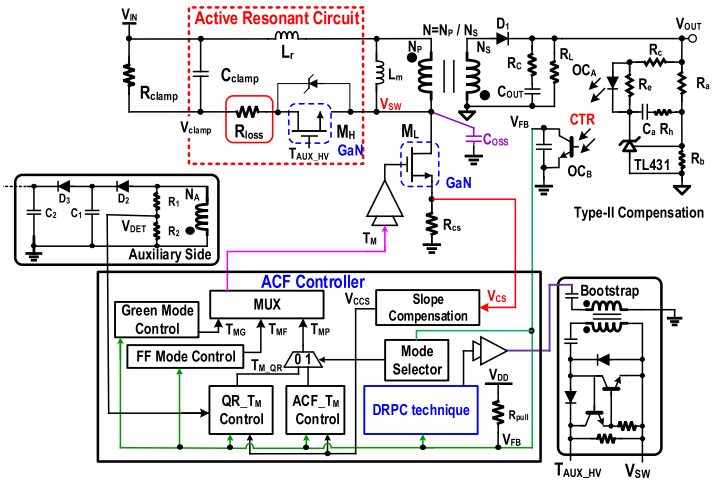


Fig. 2. Proposed DRPC technique in the GaN-based ACF converter.

II. Proposed ACF Converter With the Dynamic Resonant Priod Control Technique

Fig. 2 shows the proposed ACF converter which includes ACF mode, QR mode, frequency fold-back (FF) mode, and green mode. The switching frequency can vary according to load current for improving efficiency.

A. Proposed DRPC Technique

To mitigate energy loss caused by $R_{\rm loss}$ and $R_{\rm ON}$, the ACF converter with the proposed DRPC technique in Fig. 2 can reduce the current flowing through $R_{\rm loss}$ and $R_{\rm ON}$. The proposed DRPC technique is similar to the concept of transition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The converter can regulate the output in CCM operation. However, if the inductor current approaches zero, the turn-OFF of low side switch can avoid the resonant energy loss and thus raise the efficiency. Similarly, the proposed DRPC technique can avoid the resonant power loss and accurately control the resonant energy to raise efficiency.

In the ACF operational waveforms of Fig. 3(a), there exists dead time when M_L is turned OFF first and M_H is turned ON later. I_{Lr} flows through the Schottky diode and the parasitic resistance on the ARC path. I_{Lr} causes the power loss of L_r until it decreases to zero. When I_{Lr} is equal to zero, the Schottky diode can prevent I_{Lr} from flowing in the opposite direction and reduce power loss. When M_H is turned ON, the I_{Lr} flows through the M_H in the opposite direction to achieve ZVS on the M_L, where the absolute value of $I_{\rm Lr.neg.peak}$ is critical to determine whether full ZVS can be achieved or not.

In a conventional ACF design, the resonant period formed by L_r and $C_{\rm clamp}$ determines when ZVS occurs. Fig. 3(b) shows that once the resonance period of time is not long enough, $I_{\rm Lr.neg}$ will be too small to ensure ZVS. To solve this problem, the value of $C_{\rm clamp}$ can be increased to extend the resonance period at the cost of extra PCB area. In contrast to prior design, the proposed DRPC technique can dynamically adjust the ON-time $T_{\rm AUX}$ of high-side switch M_H to save energy and achieve ZVS.

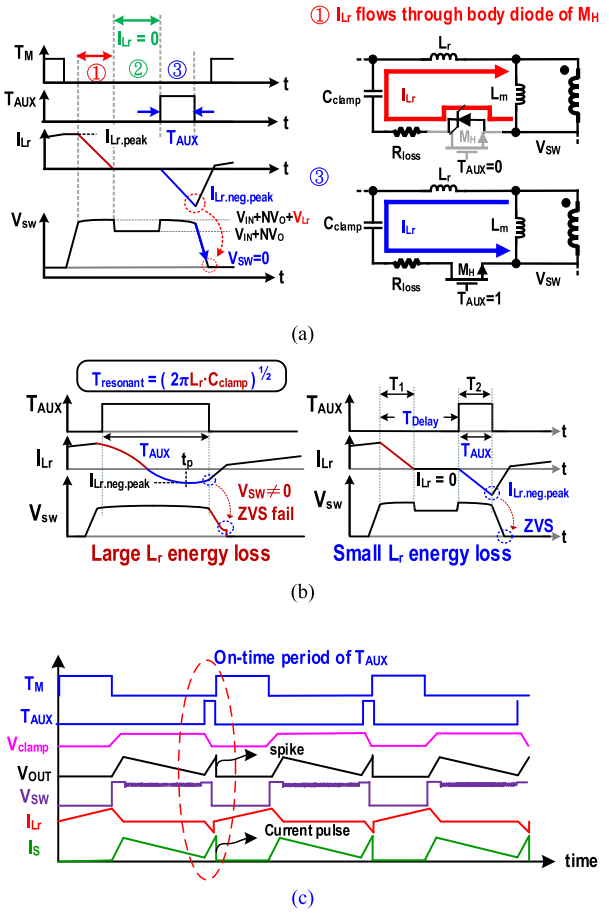


Fig. 3. (a) DRPC operation. (b) Comparison between conventional ACF and the ACF with the DRPC. (c) Disturbance voltage spike caused by a pulse in secondary side before ZVS.

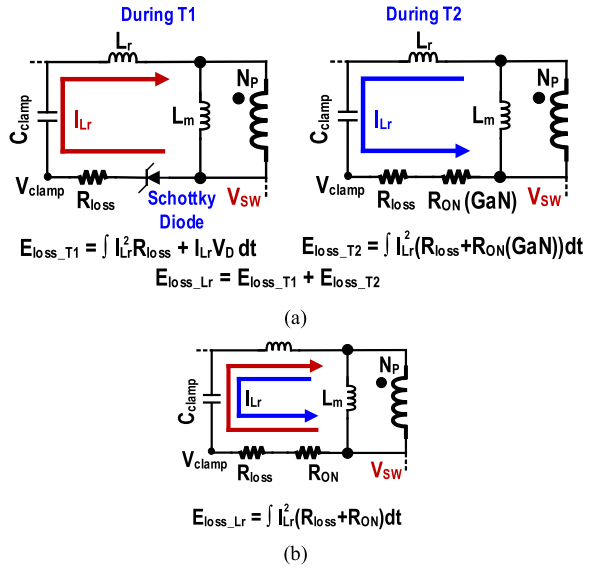


Fig. 4. (a) Loss calculation of ACF with the DRPC. (b) Loss calculation of conventional ACF.

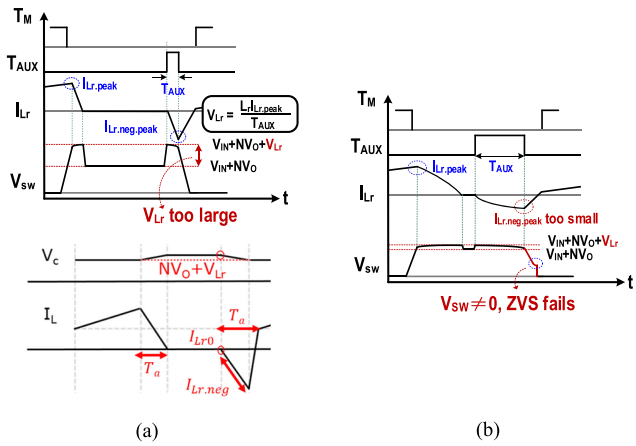


Fig. 5. (a) V_{SW} has a high voltage stress when T_{AUX} is too short. (b) ZVS fails when T_{AUX} is too long.

The proposed AFC with the DRPC technique does not require to increase the value of C_{clamp} and L_r. Compared to the technique in the work of Zhang in [4], in this article, the auxiliary switch is dynamically controlled by T_{AUX} to save more power loss with a fixed switching frequency. Although, in Fig. 3(c), before ZVS conduction is reached, a current pulse I_S will be delivered to the secondary side during the ON-time of T_{AUX}, the ripple at the output V_{OUT} is sufficiently small and the regulation is still kept.

In Fig. 4(a), when the DRPC is applied, energy loss $E_{\text{loss\_}T1}$ during T_1 is caused by the Schottky diode and R_{loss}. On the other hand, energy loss $E_{\text{loss\_}T2}$ during T_2 is caused by R_{ON} of GaN and R_{loss}. Then, total energy loss $E_{\text{loss\_}Lr}$ can be obtained by summing $E_{\text{loss\_}T1}$ and $E_{\text{loss\_}T2}$. Owing to the zero I_{Lr} as shown in Fig. 4(b), the energy loss $E_{\text{loss\_}T2}$ can be minimized.

Therefore, the control of T_{AUX} becomes very important to improve the overall efficiency. Fig. 5 shows the conditions when T_{AUX} is too long or too short. If T_{AUX} is too short in Fig. 5(a), the charge in $C_{\text{clamp}p}$ stored by L_r will not be discharged during each switching cycle. V_{clamp} will rise slowly, resulting in high voltage at V_{Lr} and V_{SW}. This condition causes high pressure stresses on the primary side components, which is detrimental to the full ZVS operation. Conversely, if T_{AUX} is too long in Fig. 5(b), the energy stored in L_r is not enough to constitute a full ZVS.

To derive the the relationship between L_r and T_{AUX}, Fig. 6(a) shows the resonant effect among R_{loss}, C_{clamp}, and L_r with the timing diagram in Fig. 6(b).

According to the simplified circuit in Fig. 6(a), (3) can be derived by KVL, where $v_C(t)$ can be assumed as (4), in which C_1 and C_2 are initial paramaters

$$\frac{d^2 v_C(t)}{dt^2} + \frac{R_{\text{loss}}}{L_r}\frac{dv_C(t)}{dt} + \frac{v_C(t)}{L_r C_{\text{clamp}}} = 0 \tag{3}$$

$$v_C(t) = C_1 e^{S_1 t} + C_2 e^{S_2 t}. \tag{4}$$

The initial condition is $v_C(0)$ is also expressed in (5). Thus, v_C(t) can be modified as (6). Correspondingly, I_{Lr}(t) can be

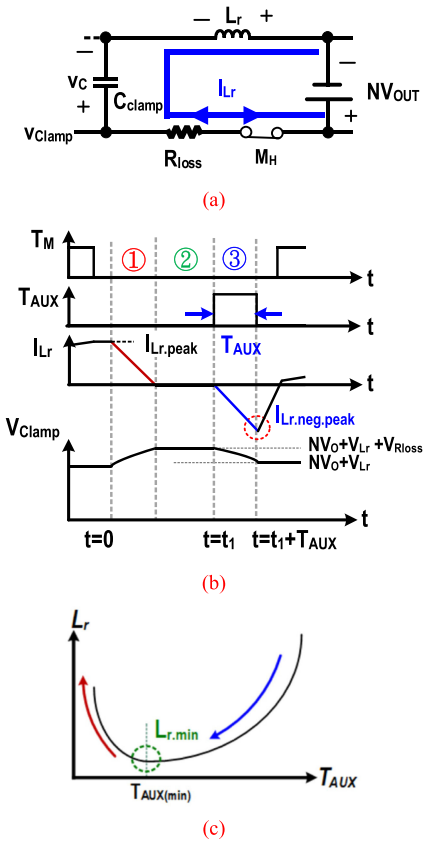


Fig. 6. (a) Modeling of resonant circuit. (b) Timing diagram to describe the resonant effect. (c) Determination of optimum on time of M_H.

derived as (7)

$$v_C(0) = C_1 + C_2 = V_{\text{Clamp}}(0) - NV_{\text{OUT}}$$
$$\Rightarrow C_2 = V_{\text{Clamp}}(0) - NV_{\text{OUT}} - C_1 \tag{5}$$
$$v_C(t) = C_1 e^{S_1 t} + (V_{\text{Clamp}}(0) - NV_{\text{OUT}} - C_1) e^{S_2 t} \tag{6}$$
$$I_{Lr}(t) = C_{\text{Clamp}} \frac{dv_C(t)}{dt}$$
$$= C_{\text{Clamp}} \left[C_1 s_1 e^{S_1 t} + s_2 (V_{\text{Clamp}}(0) - NV_{\text{OUT}} - C_1) e^{s_2 t} \right]. \tag{7}$$

The initial condition $I_{Lr}(0)$ is $I_{\text{Lr(peak)}}$ and the initial parameter C_1 can be derived in

$$I_{Lr}(0) = I_{\text{Lr(peak)}} = C_{\text{clamp}} \left[C_1 (s_1 - s_2) + s_2 (V_{\text{Clamp}}(0) - NV_{\text{OUT}}) \right]$$
$$\Rightarrow C_1 = \frac{\frac{I_{\text{Lr(peak)}}}{C_{\text{Clamp}}} - s_2 (V_{\text{Clamp}}(0) - NV_{\text{OUT}})}{s_1 - s_2}. \tag{8}$$

Consequently, I_{Lr}(t) and v_C(t) can be expressed as (9) and (10), respectively. The parameters s_1 and s_2 can be shown in (11). Let $I_{Lr}(t_1) = 0$ and $V_{\text{Clamp}}(t_1) = V_{Lr} + \text{NV}_{\text{OUT}} + V_{R\text{loss}}$. After the T_{AUX}, I_{Lr} approaches $I_{Lr}(t_1 + T_{\text{AUX}})$ with a maximum value of $I_{\text{Lr.neg.peak}}$ to achieve ZVS. The inequality of (12) needs

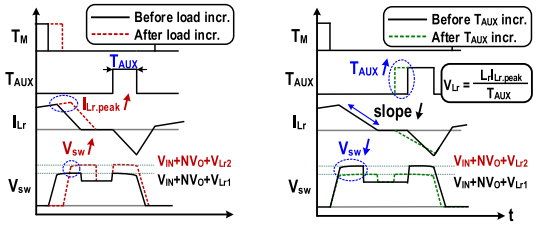


Fig. 7. (a) V_{SW} is impacted by $I_{\text{Lr.peak}}$. (b) Control of T_{AUX} can reduce the V_{SW}.

to be confirmed to ensure ZVS.

$$I_{Lr}(t) = \frac{(V_{\text{Clamp}}(0) - NV_{\text{OUT}})}{L_r(s_2 - s_1)}(e^{s_1 t} - e^{s_2 t}) - \frac{I_{\text{Lr(peak)}}}{s_2 - s_1}(s_1 e^{s_1 t} - s_2 e^{s_2 t}) \tag{9}$$
$$v_C(t) = \frac{(V_{\text{Clamp}}(0) - NV_{\text{OUT}})}{(s_2 - s_1)}(s_2 e^{s_1 t} - s_1 e^{s_2 t}) - \frac{I_{\text{Lr(peak)}}}{C_{\text{Clamp}}\,(s_2 - s_1)}(e^{s_1 t} - e^{s_2 t}) \tag{10}$$
$$s_1 = -\frac{R_{\text{loss}}}{2L_r} + \sqrt{\left(\frac{R_{\text{loss}}}{2L_r}\right)^2 - \frac{1}{L_r C_{\text{Clamp}}}} \text{ and}$$
$$s_2 = -\frac{R_{\text{loss}}}{2L_r} - \sqrt{\left(\frac{R_{\text{loss}}}{2L_r}\right)^2 - \frac{1}{L_r C_{\text{Clamp}}}}$$
$$\text{If } R_{\text{loss}} < \sqrt{\frac{L_r}{C_{\text{Clamp}}}} \Rightarrow \text{Under} - \text{damping} \tag{11}$$
$$\frac{1}{2} L_r I_{Lr} (t_1 + T_{\text{AUX}})^2 \geq \frac{1}{2} C_{\text{OSS}} (V_{\text{IN}} + NV_{\text{OUT}} + V_{Lr}(t_1 + T_{\text{AUX}}))^2. \tag{12}$$

Then, the minimum value of L_r can be derived as

$$L_r \geq \frac{C_{\text{OSS}} (V_{\text{IN}} + NV_{\text{OUT}} + V_{Lr}(t_1 + T_{\text{AUX}}))^2}{I_{Lr}(t_1 + T_{\text{AUX}})^2}. \tag{13}$$

Here, differentiate $L_{r(\text{ZVS})}(t)$ in (14) by time and set it to zero. The minimum value can be derived as $L_{r(\min)}$ in (15) when $t = t_1 + T_{\text{AUX}}$ and I_{Lr} reaches $I_{\text{Lr.neg.peak}}$

$$L_{r(\text{ZVS})}(t) = \frac{C_{\text{OSS}} (V_{\text{IN}} + NV_{\text{OUT}} + V_{Lr}(t))^2}{I_{Lr}(t)^2} \tag{14}$$
$$L_{r,\min} = \frac{C_{\text{OSS}} (V_{\text{IN}} + NV_{\text{OUT}} + V_{Lr})^2}{I_{\text{Lr.neg.peak}}^2}. \tag{15}$$

As the load rises, the ON-time T_M of the M_L extends to deliver more energy to the output for system stabilization. The increase of T_M induces the $I_{\text{Lr.peak}}$ increment in Fig. 7(a). Meanwhile, during the resonance time, L_r stores more charge on C_{clamp} and results in high voltage stress on V_{clamp} and V_{SW}, and thus full ZVS cannot be guaranteed. That is, if L_r has sufficient energy to achieve full ZVS, a well controlled and adaptive T_{AUX} in

Fig. 7(b) is necessary for C_{clamp} discharge to avoid storing too much charge when $I_{\text{Lr.peak}}$ increases.

The required energy stored in L_r to achieve full ZVS at the GaN switch can be minimized. Correspondingy, the smaller value of L_r can be used for higher efficiency. Moreover, when the load changes, the feedback signal V_{FB} is sent back to the controller through the opto-coupler, and then the DRPC can adjust the ON-time T_{AUX} of M_H to resonate the L_r with the clamp capacitor C_{clamp}. The resonance can prevent the GaN switch M_L in primary side from being damaged by the high voltage stress since the energy will not accumulate at the C_{OSS}. Since energy is efficiently retained between L_r and C_{clamp}, it is possible to pull low the V_{SW} for fast and full ZVS.

If the sensed V_{FB} from the opto-coupler system indicates a light load condition, the mode selector (MS) switches the system to the QR mode [7] where the system operates in a DCM. When the energy in the magnetic inductor L_m is discharged to zero, L_m will resonate with the C_{OSS} at V_{SW}. During the resonance time, the valley detector (V_{DET}) will detect the local minimum of V_{SW} through the auxiliary winding. When the V_{SW} reaches its valley, the switch M_L will turn ON to reduce the switching loss of the M_L.

The Schottky diode will form an RCD clamp circuit with the passive components to suppress the voltage spike at the V_{SW} caused by L_r. In very light mode, the converter enters FF-back mode, the off time will rise linearly to decrease the switching frequency and to reduce switching loss. As the load continuously decreases, the ACF controller will bring converter into the green mode under ultra-light-load condition and apply a fixed off-time on the low side switch M_L.

B. Compensation of Proposed ACF

The proposed flyback can be modeled in Fig. 8(a). Since only during the OFF-time period of the low-side GaN switch M_L, the DRPC module functions for resonant operation, the modeling of the DRPC can be ignored without affecting the stability analysis. The transfer function from v_{FB} to v_{OUT} can be expressed as (16), where S_e and S_N are slew rates of sawtooth signal and current sensing signal, respectively. The transfer function contains two poles ω_{P1} and ω_{P2}, one left-half plane zero ω_{Z1}, and one right-half-plane (RHP) zero ω_{ZRHP}, which are shown in (17)

$$\frac{v_{\text{OUT}}}{v_{\text{FB}}} \propto V_{\text{IN}} \sqrt{\frac{f_S}{2}\frac{R_L}{L_P}} \frac{1}{(S_e+S_N)} \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\left(1+\frac{s}{\omega_{ZRHP}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \tag{16}$$

$$\omega_{P1} = \frac{2}{C_{\text{OUT}}R_L},\ \omega_{P2} = \left(\frac{N_P}{N_S}\right)^2 \frac{R_L}{L_P(M+1)^2}$$

$$\omega_{Z1} = \frac{1}{C_{\text{OUT}}R_C},\ \omega_{ZRHP} = \left(\frac{N_P}{N_S}\right)^2 \frac{R_L}{L_P M\,(M+1)}$$

$$\text{where}\ \ M = \frac{N_P}{N_S}\frac{V_{\text{OUT}}}{V_{\text{IN}}}. \tag{17}$$

ω_{P1} locates at low frequencies, while ω_{P2} locates at high frequencies. Although an undesirable RHP zero ω_{ZRHP} exists, due to its high frequency position, its influence on the system becomes insignificant. Therefore, Type II compensator can be used for the proposed flyback converter, which contains two poles and one zero as depicted in Fig. 8(b). The transfer function of the compensator can be expressed in (18), where CTR is the current transfer ratio of the photocoupler. By the adjustment of the ratio of R_d and R_c, the requirement of different CTR of the photo-coupler can be met. The compensation poles and zero are $\omega_{P0(\text{compensated})}$, $\omega_{P1(\text{compensated})}$, and $\omega_{Z1(\text{compensated})}$, which are shown in (19). $\omega_{P1(\text{compensated})}$ and $\omega_{Z1(\text{compensated})}$ are about 35 KHz and 300 Hz, respectively

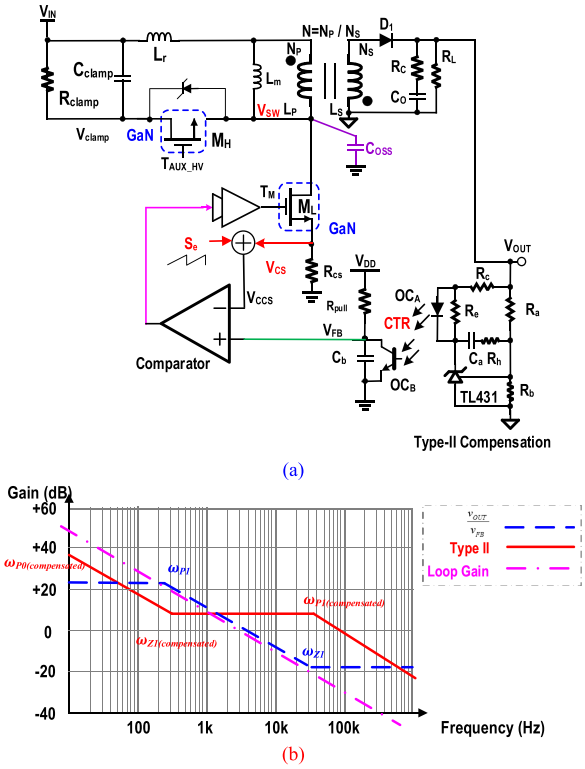


Fig. 8. (a) Modeling of the proposed flyback converter. (b) Bode plot with the compensator.

$$G_{\text{COMP(TYPEII)}} = \text{CTR}\frac{R_d}{R_c}\cdot\frac{1+s(R_a+R_h)C_a}{sR_aC_a(1+sR_dC_b)} \tag{18}$$

$$\omega_{P0(\text{compensated})} = 0, \omega_{P1(\text{compensated})} = \frac{1}{R_dC_b}$$

$$\text{and}\ \ \omega_{Z1(\text{compensated})} = \frac{1}{(R_a+R_h)C_a}. \tag{19}$$

Fig. 9(a) shows the bandwidth is 3 kHz when the converter operates in ACF mode at $V_{\text{in}} = 127$ V, and the bandwidth is 1.7 kHz when the converter opertates in QR mode in the condition of 75% full load. In Fig. 9(b), the phase margin of converter is 88° and 85° in ACF mode and QR mode, respectively.

C. Operation Modes for Light Load Conditions

When loading drops below 75% of full load, the system operates in QR mode and the M_H of ARC is disabled. The V_{DET} can detect the valley voltage and calculate the number

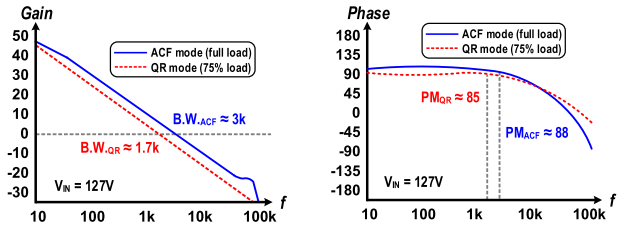


Fig. 9. Bode plots. (a) Loop gain. (b) Phase margin.

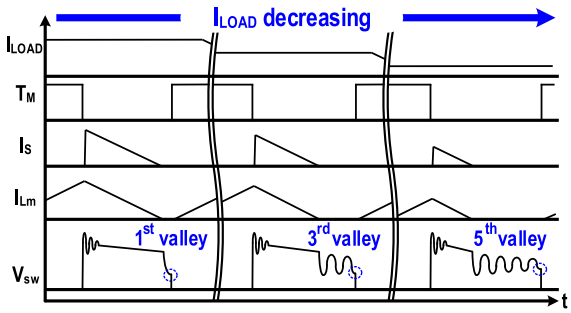


Fig. 10. Operating waveforms of QR mode at different valley switching.

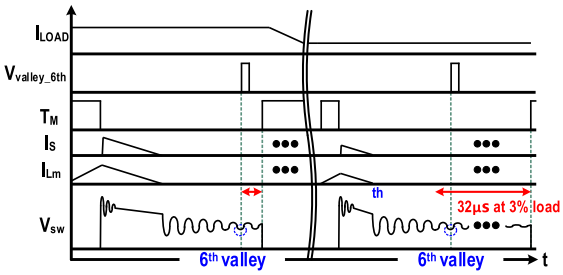


Fig. 11. Operating waveforms of FF mode.

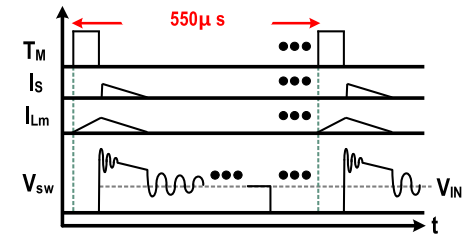


Fig. 12. Operating waveforms of green mode.

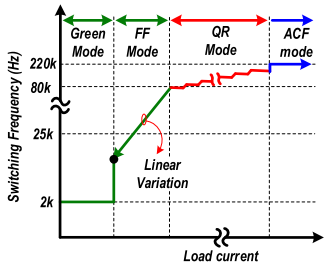


Fig. 13. Switching frequency versus the loading current.

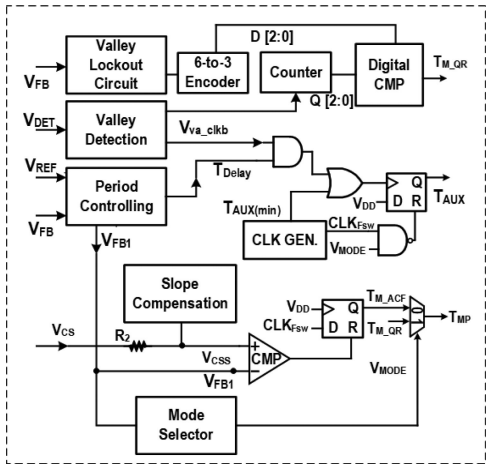


Fig. 14. Architecture of proposed ACF controller.

of valleys in Q_{R_TM} control block. Different loads will turn ON M_L with appropriate numbers of valley. Fig. 10 shows different valley number is selected by different loading condition. When valley detector counts to the sixth valley in QR mode and loading continuously drops, the converter will be switched into the FF mode to enhance efficiency in further light load condition by adding dead time which is inversely proportional to output current. Thus, the decreased frequency can reduce switching loss. The waveforms of FF mode is shown in Fig. 11. If the output current keeps further dropping into the ultralight load, the converter will enter green mode, where the 550 μs timer is enabled with the frequency of around 2 kHz to save power [5]. The operating waveforms of green mode is shown in Fig. 12. Therefore, the overall operation modes versus the switching frequency are presented in Fig. 13.

III. Cirucit Implementations

The architecture of the proposed ACF controller is depicted in Fig. 14 with mainly three control modules: DRPC, QR mode, and FF and green mode. The DRPC module can dynamically control signal $T_{\rm AUX}$, which is proportional to $V_{\rm FB}$ to ensure full ZVS. The QR part is mainly composed of the valley lockout circuit, valley detector, and an encoder. The operation modes in accordance with load current are shown in Fig. 13.

A. Circuit Design of DRPC Module

In Fig. 15(a), the DRPC technique generates the controlling signal $T_{\rm AUX}$ which is proportional to $V_{\rm FB}$ and ensures that full ZVS is achieved to lower the voltage stress on the switchers. During the delay time $T_{\rm Delay}$, the energy in L_m can be reduced to zero. If the high-side switch M_H does not turn ON during this time, L_m will resonate with $C_{\rm OSS}$, which causes the switching node $V_{\rm SW}$ in a QR state. In order to prevent the auxiliary switch M_H from turning ON when the $V_{\rm SW}$ reaches its valley and causing an increase in the switching loss of the M_H, the auxiliary winding

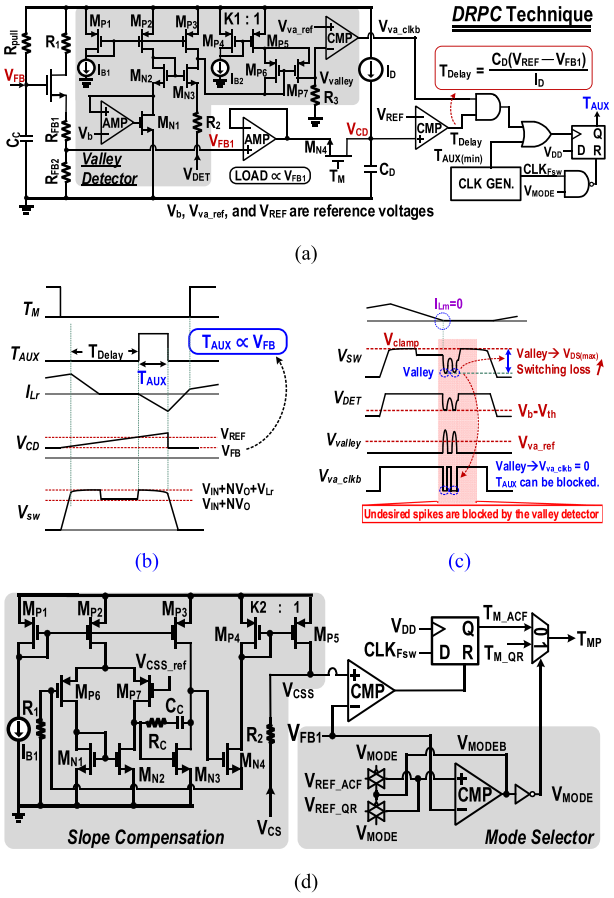


Fig. 15. (a) Proposed DRPC technique to implement an active clamp mode. (b) Operating waveforms of the DRPC. (c) Timing diagram shows the valley detector is used to block the undesired spikes. (d) ON-time control for low side switch.

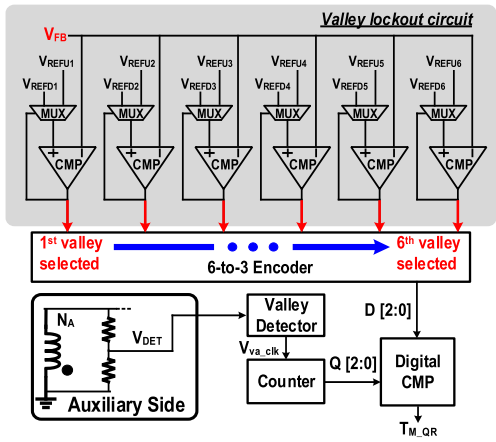


Fig. 16. Valley lockout circuit in the QR mode.

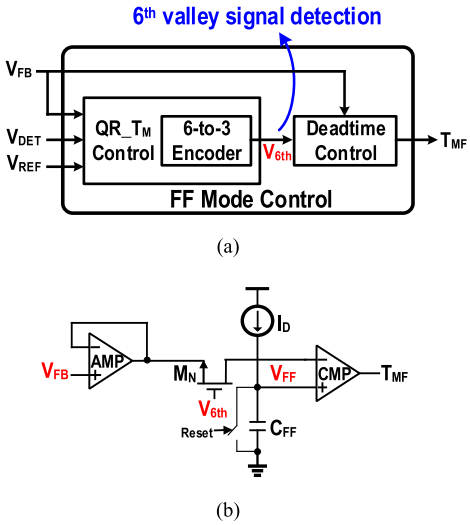


Fig. 17. (a) Dead time control for frequency foldback mode. (b) Deadtime control circuit.

of the transformer is used to detect the $V_{\rm SW}$ through the $V_{\rm DET}$. When $V_{\rm SW}$ resonates to its valley, $V_{\rm DET}$ produces $V_{\rm va\_clkb}$ to block $T_{\rm AUX}$ and to avoid large switching losses on the M_H.

In Fig. 15(b), within $T_{\rm Delay}$, the energy in L_m can be decreased to zero. However, if M_H does not turn ON during this time, L_m will resonate with $C_{\rm OSS}$ to force $V_{\rm SW}$ in a QR state, as shown in Fig. 15(c). To prevent the auxiliary switch M_H from being turned ON when the $V_{\rm SW}$ reaches its valley value, resulting in an increase in the switching loss of the M_H, the valley detector is used to detect the $V_{\rm SW}$ through the $V_{\rm DET}$ from the auxiliary winding of the transformer. When $V_{\rm SW}$ resonates to its valley, the $V_{\rm va\_clkb}$ is generated to block $T_{\rm AUX}$ and avoid large switching loss on the M_H.

Fig. 15(d) shows the ON-time control of the low side switch. Two modes including ACF mode and QR mode are used to control the timing of the converter according to the output $V_{\rm MODE}$ of the MS. That is, the $T_{\rm MP}$ is $T_{M\_\rm ACF}$ (or $T_{M\_\rm QR}$) when $V_{\rm MODE}$ is low (or high). When the feedback signal $V_{\rm FB1}$ is less than $V_{\rm REF\_ACF}$ but higher than $V_{\rm REF\_QR}$, the controller operates in the ACF mode. $\rm CLK_{Fsw}$ triggers the low side switch M_L to turn ON. The slope compensation current signal $V_{\rm CSS}$ of the primary side compares the $V_{\rm FB1}$ to determine the ON-time duration of the M_L. On the other hand, when $V_{\rm FB1}$ falls below $V_{\rm REF\_QR}$, the M_S will switch the controller into QR mode. In this mode, $T_{M\_\rm QR}$ controls the ON-time duration of the M_L and the switching frequency is much lower than that in the active clamp mode to improve light load efficiency.

B. Light Loading Mode Control

In Fig. 16, the auxiliary side of the transformer detects the QR valley of $V_{\rm DET}$ and counts the numbers of valleys by the valley detector and counter. According to different $V_{\rm FB}$ value, the valley lockout circuit compares the feedback signal $V_{\rm FB}$ with six pairs of $V_{{\rm REFU},Di}$ (where $i = 1$ to 6) to produce 6-bit data to select one of six valleys through the 6-to-3 encoder for achieving valley lockout. Finally, the $T_{M\_\rm QR}$ is determined by the comparison of D[2:0] and Q[2:0] through the digital comparator (CMP). Then, the QR mode can be achieved.

In Fig. 17(a), the 6-to-3 encoder of $Q_{R\_\rm TM}$ control can detect the sixth valley signal. According to different $V_{\rm FB}$, different dead time in FF mode is selected and maximum dead time is 32 μs after the detection of the sixth valley. Fig. 17(b) shows the

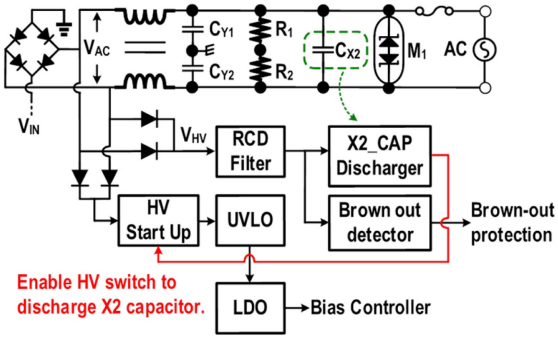


Fig. 18. HV protection topology.

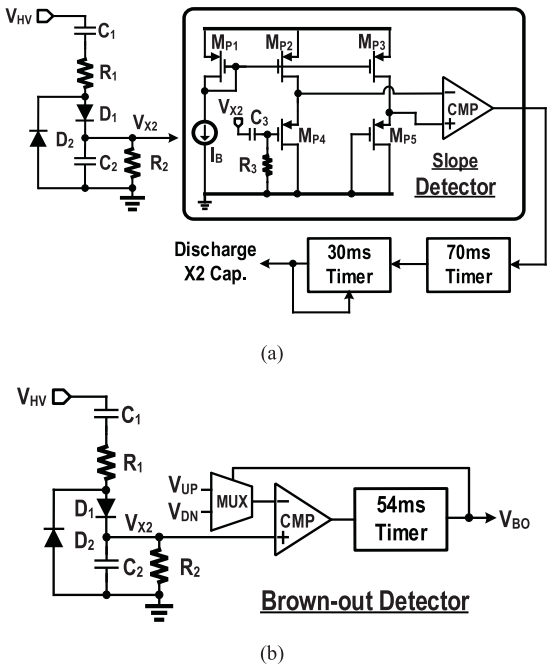


Fig. 19. (a) X2 capacitor discharger. (b) Brown-out detector.

implementation of deadtime control circuit. Since the deadtime is load dependent, light load condition indicates higher $V_{\rm FB}$ and results in higher deadtime.

C. X2 Cap Discharger and Brownout Detection

For safety consideration of ac input voltage from different system abnormal scenarios, in this design, the input X2 capacitor discharge circuitry and brownout detection are also implemented. The protection topology is shown in Fig. 18.

The signal of ac input voltage can be obtained by an RCD filter, and the slope detector in Fig. 19(a) can determine whether the ac line is pulled out through detecting the voltage $V_{\rm X2}$. As soon as the ac line is unplugged, the 70 ms timer is enabled and is ready to discharge the X2 capacitor. After the ac line voltage is removed, the 70 ms timer is used with the 30 ms timer to detect a time of 100 ms for the $V_{\rm X2}$ node. After 100ms, the ac input voltage will be repeatedly detected for 30 ms and the X2 capacitor will be discharged every 60 ms until the ac line plugs or the X2 capacitor completes discharge.

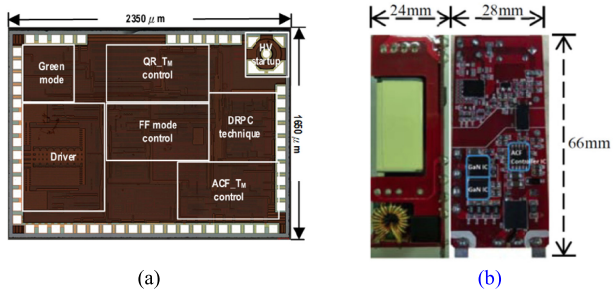


Fig. 20. (a) Chip micrograph. (b) Prototype of the DRPC flyback converter.

TABLE I
EXPERIMENTAL PARAMETERS OF THE HARDWARE

GaN-based ACF Design Parameters	
Technology	0.5μm 700V UHV
Power GaN transistors	Navitas NV6115 and NV6117
Input Voltage (V)	AC 90-264 V
Output Volltage (V)	20 V
Primary Inductor (Lm)	95 μH
Turn Ratio (Np/Ns)	3.25
Leakage Inductance	1.2 μH
Clamp Capacitor (Cclamp)	120 nF
Output Capacitor (Cout)	1 mF, Resr=25 mΩ
Maximum Output Power (W)	65 W
Volume	44.35cm^3
Switching Frequency (Hz)	80k~200 kHz (QR mode) 220 kHz (ACF mode)
Peak Effciency	94% @ 3.42 A
Chip Area (mm^2)	6 mm^2
Power Density (W/cm^3)	1.47 W/cm^3

Similarly, in case of brownout event hits, the voltage amplitude of the ac input signal can be detected by $V_{\rm X2}$ as shown in Fig. 19(b). Once $V_{\rm X2}$ falls below $V_{\rm DN}$, it will cause the undervoltage timer to start counting for 54 ms. After the period, if $V_{\rm X2}$ is still lower than $V_{\rm DN}$, the undervoltage protection will be enabled until the ac input voltage back to above $V_{\rm UP}$.

IV. EXPERIMENTAL RESULTS

The fast ZVS in GaN-based ACF converter with DRPC technique has been manufactured in generic 0.5 μm 700 V ultrahigh voltage MOSFET process. The overall chip size is 2.81 mm^2 including pads. The chip micrograph is shown in Fig. 20(a), and the prototype of the DRPC flyback converter is shown in Fig. 20(b). The experimental parameters are shown in Table I. The power density can be 1.47 W/cm^3 and the maximum power can be 65 W. The range of input ac source is 90–264 $V_{\rm AC}$ and $V_{\rm OUT}$ is 20 V. The primary inductance of transformer is 95 μH and leakage inductance 1.2 μH. Other off-chip components are output capacitor 1 mF with $R_{\rm esr}$ 25 mΩ, clamp capacitor of 120 nF, and optocoupler PC817. The GaN switches are NV6115 and NV6117, which are manufactured by Navitas Semiconductor, for low-side and high-side switches, respectively.

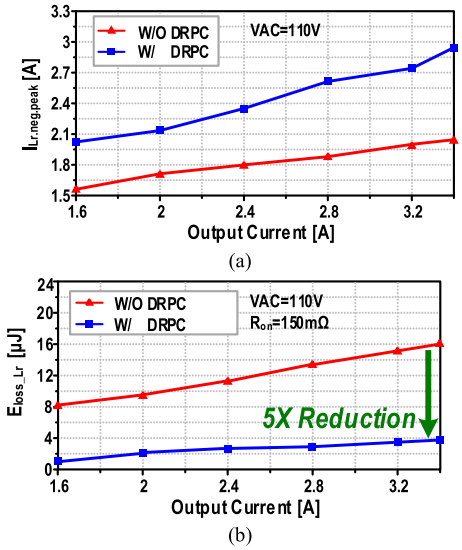


Fig. 21. Test of ACF converter with and without DRPC technique. (a) Measured $I_{\mathrm{Lr.neg.peak}}$ versus output current. (b) Measured Eloss_L_r versus output current.

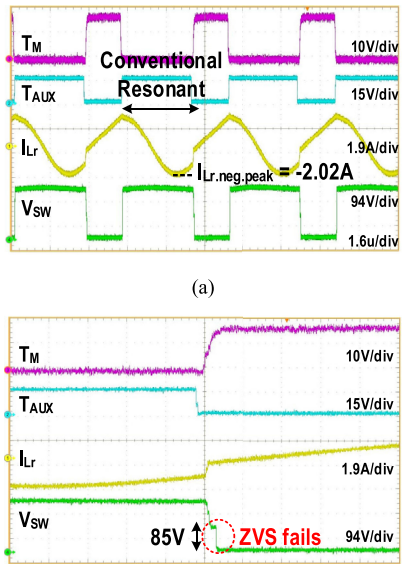


Fig. 22. (a) Measurement result of conventional ACF. (b) Energy loss causes ZVS to fail.

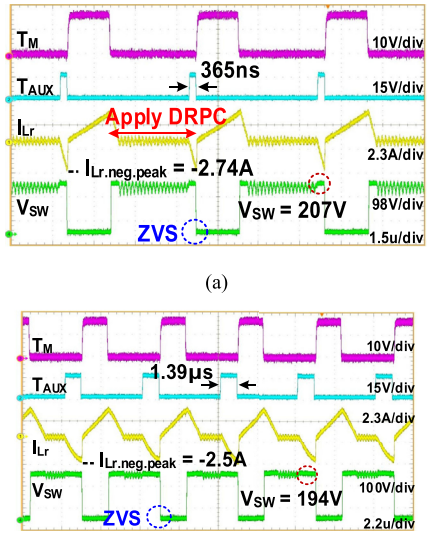


Fig. 23. (a) Measurement result of proposed ACF. (b) Dynamically adjust T_{AUX} to avoid V_{SW} too large.

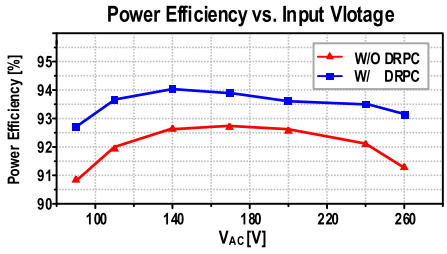
The advantages of DRPC can dynamically adjust the T_{AUX} to prevent the converter from lacking energy when ZVS operation is achieved. When operating at active clamp mode in the heavy load condition, the system is at 220 kHz constant switching frequency. In order to improve the light load efficiency, the switching frequencies of QR mode and green mode are 80–200 and 2 kHz, respectively. The following experimental results include the ACF results with the proposed DRPC technique and the ACF results without the proposed DRPC technique. Without the DRPC technique, the flyback converter operates with the conventional ACF technique similar to [4].

Fig. 21(a) shows the higher $I_{\mathrm{Lr.neg.peak}}$ by the DRPC technique under the variations of different loading that mitigates the issue that the $I_{\mathrm{Lr.neg}}$ in conventional AFC design is too small to reach ZVS condition. Thus, as shown in Fig. 21(b), by means of the DRPC, the converter can have around five times loss reduction, while the R_{ON} is 500 mΩ. In Fig. 22(a), conventional active resonant waveforms are shown, and the leakage inductance causes large energy loss. In Fig. 22(b), it is obvious that the energy loss is so large that ZVS fails. In Fig. 23(a), because of the L_r energy loss reduced by the DRPC, the operation can achieve fast and full ZVS. In Fig. 23(b), the DRPC dynamically adjusts T_{AUX} of the auxiliary switch to avoid large voltage stress on V_{SW}. In Fig. 24(a), when the ac input voltage ranges from 90 to 264 V, the peak efficiency is 94%. The efficiency in Fig. 24(b) can be kept higher than 93.5% under the output load current from 1.6 to 3.2 A. The efficiency improvement is around 1.5% compared to that without DRPC technique. The X2 capacitor discharger and brown-out detector protect the ac input voltage from abnormalities, as shown in Fig. 25. The discharge time is effectively shortend and thus the power loss at standby mode can be reduced.

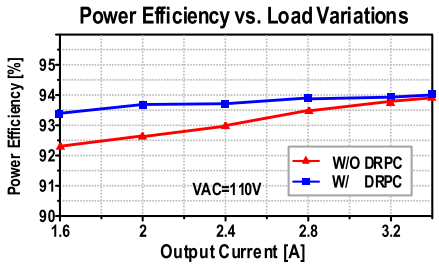
The dynamic measurement results are shown in Figs. 26–29. When the ac input voltage starts from 0 to 220 V, the stable time of the flyback with the proposed ACF control needs 59.6 ms to regulate the output to 20 V, as shown in Fig. 26. When the ac input voltage changes from 220 to 110 V and vice versa, the output voltage remains at 20 V, as shown in Fig. 27. When load changes between 1.8 A (equal to 80% maximum load) and 0.45 A (equal to 20% maximum load), the undershoot and overshoot voltages are 216 and 280 mV, respectively, as shown in Fig. 28. At full load, the output voltage ripple is 58.4 mVp-p, as shown in Fig. 29. The comparisons between the proposed flyback converter and prior arts are listed in Table II. The efficiency is improved particularly at the light load conditions because of the proposed DPRC technique. Consequently, the peak conversion efficiency is better than those of the prior arts.

TABLE II
COMPARISON WITH THE PRIOR ARTS

	[1] TIE'16	[2] TIE'18	[3] APEC'16	[4] TPE'10	This Work
Input Voltage (V_{rms})	90-264-V_{RMS}	90-264-V_{RMS}	90-264-V_{RMS}	90-264-V_{RMS}	**90-264-V_{RMS}**
Operating Mode	QR	ACF	ACF	ACF	**ACF**
Output Voltage (V)	14V	20V	19.5V	16V	**20V**
Maximum Output Power	40W	45W	65W	64W	**65W**
Switching Frequency	25-125kHz	180-280kHz	1MHz	65kHz	**QR:80-200k/ACF:220k**
Maximum Efficiency	89.1%	94.5%	93.5%	92.6%	**94%**
L_r [H]	NA	3µ	NA	1.5µ	**1.2µ**
C_{Clamp} [F]	NA	1µ	100n	220n	**120n**
L_r Energy recovery	No	Medium	Low	Medium	**High**



(a)



(b)

Fig. 24. Test of ACF converter with and without DRPC technique. (a) Efficiency versus input ac voltage. (b) Efficiency versus output load current.

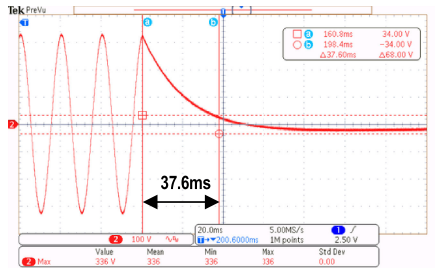


Fig. 25. Voltage across the X2 capacitor becomes zero to protect the ac input voltage from abnormalities @230 V_{ac}.

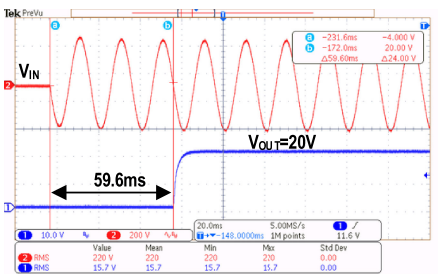


Fig. 26. Measured start up time.

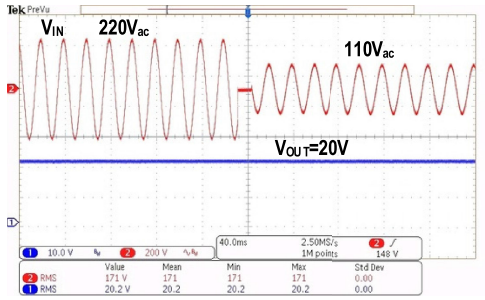


Fig. 27. Line transient response when V_{IN} changes from 220 to 110 V_{ac} and vice versa.

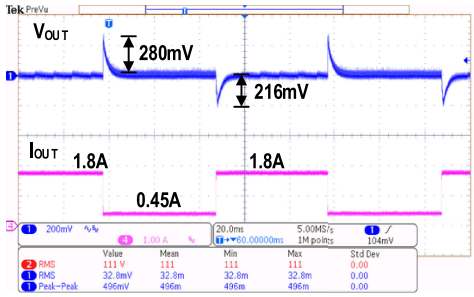


Fig. 28. Load transient response when I_{OUT} changes from 1.8 to 0.45 A and vice versa.

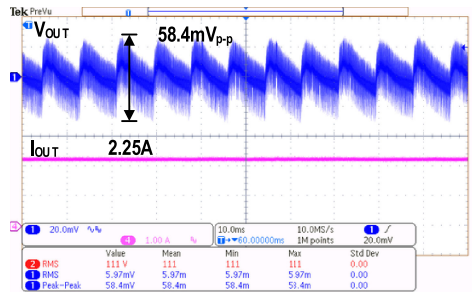


Fig. 29. Measured V_{OUT} ripple when I_{OUT} is 2.25 A.

V. CONCLUSION

A GaN-based ACF converters with DRPC technique that can achieve fast ZVS is presented in this article. The DRPC technique can facilitae the reduction of the energy loss resulted from ARC path and leakage inductance. The proposed ACF converter can operate in ACF mode, QR mode, FF mode, and green mode with the switching frequency that can vary depending on load

current. While loading is changing, the DRPC technique can dynamically optimize the switch ON-time to mitigate voltage overstress on the components in the primary winding. The leakage loss is significantly reduced in full load condition, and thereby more electrical energy is transferred to the secondary side. The proposed ACF achieves fast and full ZVS together with the peak efficiency up to 94%.

REFERENCES

[1] J. Park, "Quasi-resonant (qr) controller with adaptive switching frequency reduction scheme for flyback converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3571–3581, Jun. 2016.

[2] L. Xue, "Highly efficient secondary-resonant active clamp flyback converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 767–770, Feb. 2018.

[3] X. Huang, J. Feng, W. Du, F. Lee, and Q. Li, "Design consideration of mhz active clamp flyback converter with gan devices for low power adapter application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2334–2341.

[4] J. Zhang, "A high efficiency flyback converter with new active clamp technique," *IEEE Trans. Ind. Electron.*, vol. 25, no. 7, pp. 1775–1785, Jul. 2010.

[5] Y. Kang, C. Chiu, M. Lin, C. Yeh, J. Lin, and K. Chen, "Quasiresonant control with a dynamic frequency selector and constant current startup technique for 92% peak efficiency and 85% light-load efficiency flyback converter," *IEEE Trans. Ind. Electron.*, vol. 29, no. 9, pp. 4959–4969, Sep. 2014.

[6] P.-H. Liu, "Design consideration of active clamp flyback converter with highly nonlinear junction capacitance," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 783–790.

[7] R. Perrin, N. Quentin, B. Allard, C. Martin, and M. Ali, "High-temperature gan active-clamp flyback converter with resonant operation mode," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1077–1085, Sep. 2016.

[8] N. Quentin, R. Perrin, C. Martin, C. Joubert, B. Lacombe, and C. Buttay, "GaN active-clamp flyback converter with resonant operation over a wide input voltage range," in *Proc. IEEE Int. Exhib. Conf. Power Electron. Intell. Motion Renewable Energy Energy Manage.*, 2016, pp. 1–8.

[9] L. Xue and J. Zhang, "Active clamp flyback using gan power ic for power adapter applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2441–2448.

[10] K. H. Liu and F. C. Lee, "Zero-voltage switching technique in dc/dc converters," *IEEE Trans. Power Electron.*, vol. 5, no. 3, pp. 293–304, Jul. 1990.

[11] Y.-K. Lo and J.-Y. Lin, "Active-clamping zvs flyback converter employing two transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2416–2423, Nov. 2007.

[12] A. Emrani, E. Adib, and H. Farzanehfard, "Single-switch soft-switched isolated dc–dc converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1952–1957, Apr. 2012.

[13] H.-J. Chiu *et al.*, "A single-stage soft-switching flyback converter for power-factor-correction applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2187–2190, Jun. 2011.

[14] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 162–169, Jan. 1996.

[15] Y.-K. Lo, C.-F. Wang, J.-Y. Lin, and C.-Y. Lin, "Analysis and design of a dual-mode flyback converter," in *Proc. IEEE Int. Conf. Sustain. Energy Technol.*, Dec. 2010, pp. 1–3.

[16] J.-M. Kwon, W.-Y. Choi, and B.-H. Kwon, "Single-switch quasi-resonant converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1158–1163, Apr. 2009.

[17] J.-M. Kwon, W.-Y. Choi, and B.-H. Kwon, "Single-stage quasi-resonant flyback converter for a cost-effective pdp sustain power module," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2372–2377, Jun. 2011.

[18] P. Liu, "Small signal analysis of active clamp flyback converters in transition mode and burst mode," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 241–248.

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