A Current-Mode-Hysteretic Buck Converter With Constant-Frequency-Controlled and New Active-Current-Sensing Techniques

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***Abstract*—This article presents a hysteretic-current-controlled buck converter with constant-frequency-controlled and active-current-sensing (ACS) techniques. This converter used phase–frequency-locked techniques to achieve constant switching frequency. Even if the input voltage or output load current changes, the switching frequency will be as stable as possible at 1 MHz. The proposed ACS circuit will not generate sparks, so the current feedback loop does not need a sample-and-hold circuit, and that will reduce the transient response time. The proposed buck converter has been fabricated with TSMC 0.35 μm CMOS 2P4M technology; the total area of the chip is 1.5 mm $\times$ 1.5 mm. The measurement results of this buck converter show that the maximum power efficiency is 90% when the output voltage is 2.5 V and the load current is 300 mA. The output voltage range is 2.5–1 V, and the maximum load current is 600 mA. When the load current varies between 100 and 500 mA, the load transient response is 2.6 μs/2.2 μs and undershoot/overshoot is 20 mV/30 mV. The switching frequency of this buck converter is locked at 1 MHz and the voltage error is within 1%.**

***Index Terms*—Active-current-sense circuit, buck, current-mode buck converter, hysteretic control, phase–frequency-locked techniques.**

I. Introduction

ELECTRICITY brings convenience to people's lives. In recent years, many technologies have changed people's lives, and portable devices are the main reason. With the rapid popularity of artificial intelligence, virtual reality, and the Internet of things, all of this requires electricity.

For batteries of portable devices that are usually limited in capacity, the power efficiency will affect the competitiveness of the product that is why power management for portable devices is very important.

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Currently, electronic products have fast processing speed and high image resolution, so they need to use high-speed central processing unit and graphics processing unit. Therefore, the transient responses of a power converter are more stringent than that of a power converter of general products.

Switching converters are widely used for power management because it has better power efficiency than linear regulators. According to the feedback loop, the controlled types of power management can be divided into the current mode and voltage mode [1]–[3].

The difference between digital voltage-mode control and analog current-mode control is pulsewidth modulation [4]. Digital voltage-mode control used many external clocks, but analog current-mode control only used itself inductor current ramp [2]. The transient response of analog current-mode control switching converter is better than that of digital voltage-mode control switching converters [5].

There are many ways to implement an analog current-mode control converter. Hysteretic-current control (HCC) has been widely used recently [6] because it has a fast transient response [2]. However, because the switching frequency is in continuous conduction mode (CCM), it depends on the actual value of the inductance, which makes filter design and synchronization difficult [2]. In practical application, the load current is not constant and can be changed rapidly, so undershoot/overshoot is extremely important for buck converters. Moreover, when the load current changes, the transient response time is also important [7].

This article presents a constant-frequency HCC buck converter. The proposed HCC buck converter adds a phase–frequency-locked loop (PLL) to achieve a quasi-fixed switching frequency in CCM, thereby improving efficiency and solving the problem of switching frequency variation [8]. The proposed active-current-sensing (ACS) circuit obtains inductor current and directly feeds back the ramp current information without an external ramp generator, which can reduce the output voltage ripple. Moreover, the proposed ACS circuit does not generate sparks when power MOSFETs switch ON and OFF so that the current feedback loop does not need a sample-and-hold circuit to eliminate the sparks generated by the traditional ACS circuit [6]. Because the current feedback loop has no sample-and-hold circuit and ramp generator, the HCC circuit and nonoverlapping circuit are different from those of the traditional HCC buck

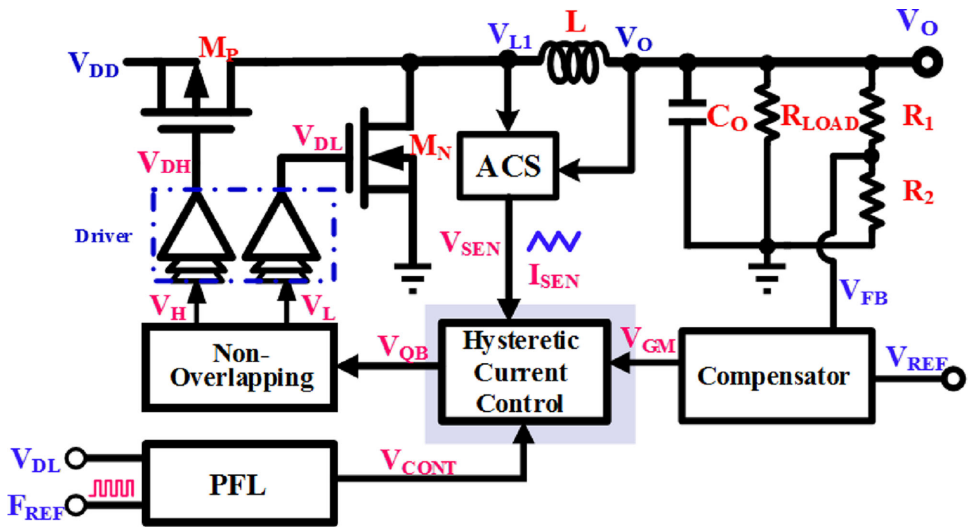

Fig. 1. Block diagram of the proposed buck converter.

converter [6]. Therefore, the transient response of the proposed HCC buck converter is faster than that of the traditional HCC buck converter [6]. In addition, the HCC does not need a ramp compensator because it could adjust by itself when the duty becomes larger.

II. Circuit Descriptions

The proposed constant-frequency current-mode-hysteretic buck converter, which is shown in Fig. 1, includes an ACS, a compensator, a hysteresis-current-controlled circuit, a phase–frequency-locked circuit, a nonoverlapping circuit, and a driving circuit [9], [10].

The proposed buck converter has three feedback loops. The first feedback loop is a voltage feedback loop. The feedback voltage $V_{\rm FB}$ and the reference voltage $V_{\rm REF}$ are sent to a compensator to generate $V_{\rm GM}$, which is sent to the HCC circuit. The second feedback loop is a current feedback loop. The ACS circuit senses the inductor information to generate $V_{\rm SEN}$ and $I_{\rm SEN}$ signals. The PLL includes a phase–frequency detector (PFD), a charge pump (CP) circuit, and a low-pass filter. The PFD detects the frequency and phase difference between the external clock and the signal of power transistor to produce the up/down control signals. This control signal can charge or discharge the low-pass filter at the output to generate an analog voltage signal $V_{\rm CONT}$, which can provide a control signal for the HCC circuit. The HCC circuit generates $V_{\rm QB}$, which will be sent to nonoverlapping circuit and driver to generate the driving signals $V_{\rm DH}$ and $V_{\rm DL}$ to control power MOSs, M_p and M_n, respectively.

A. ACS Circuit

The ACS circuit is shown in Fig. 2(a). The voltages V_{L1} and V_O across the inductor are sent to the transconductance amplifier (GM), as shown in Fig. 2(b), through the voltage dividers. Because this GM is not rail-to-rail GM, the voltage dividers are used to proportionally adjust the V_{L1} and V_O to the linear area of GM. The output of GM integrates the capacitor to produce V_C that approximates the inductor current. The voltage dividers are inside the chip and the four resistors R_{R1}, R_{R2}, R_{L1}, and R_{L2} should be approximately equal with matching layout methods. Fig. 2(c) shows the mismatch of the voltage dividers simulated using Hspice Monte Carlo. The deviation of each resister is $\pm 5\%$ (95–105 kΩ). The results show that all $V_{\rm out}$ almost overlap, so the resistance mismatch can be ignored in the calculation.

M_{P1} and R_A of the second-stage operational amplifier (OPA) form negative feedback, and their virtual short-circuit characteristic makes the voltage of R_A close to the input voltage V_C. The OPA circuit is the same as the GM circuit in Fig. 2(b). M_{P1} and M_{P2} are the current mirrors, which copy the current through the closed-loop feedback to $I_{\rm SEN}$. Fig. 2(d) shows the mismatch of the current mirror simulated using Hspice Monte Carlo. The deviation of the width of M_{P1} and M_{P2} is 1.9–2.1 μm. The results show that all $V_{\rm out}$ almost overlap, so the current mirror mismatch can be ignored in the calculation. The output voltage $V_{\rm SEN}$ adjusts the duty cycle by the compensator. The current $I_{\rm SEN}$ sensed by the new ACS circuit is sent to the hysteretic-current-controlled circuit. R_A and C_C adjust $I_{\rm SEN}$ through the closed-loop feedback, so even if there is an error, the influence of the error is small.

The OPA and the resistor obtain a voltage that can provide the voltage to the current circuit and generate a signal $I_{\rm SEN}$ for the hysteretic-current-controlled circuit. The relationship between I_L and $I_{\rm SEN}$ is derived as

$$V_C = \frac{1}{C_C}\int \frac{G_m}{2}\left(V_{L1}-V_o\right)dt \tag{1}$$

$$I_{\rm SEN} = \frac{V_C}{R_A} = \frac{1}{2R_AC_C}\int G_m\left(V_{L1}-V_o\right)dt \tag{2}$$

$$I_L = \frac{1}{L}\int \left(V_{L1}-V_O\right)dt \tag{3}$$

$$\therefore I_L : I_{\rm SEN} = \frac{1}{L} : \frac{G_m}{2R_AC_C} \tag{4}$$

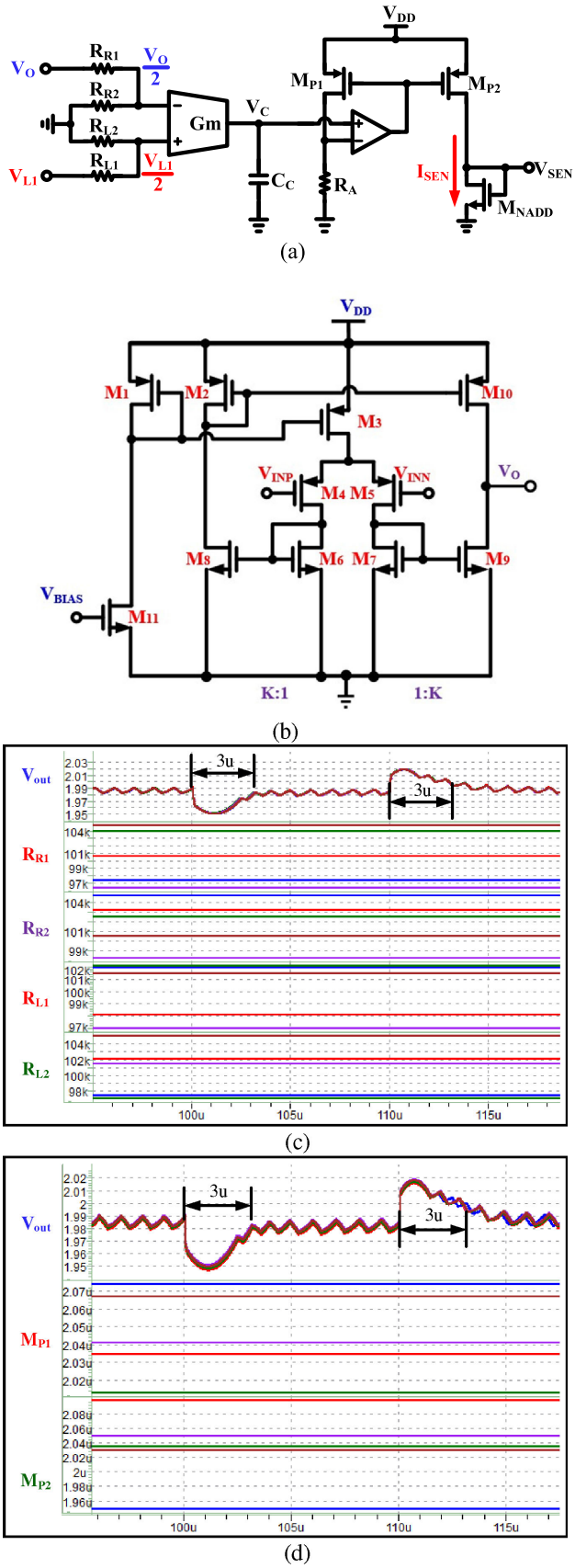

Fig. 2. (a) ACS circuit. (b) GM and OPA circuit. (c) Resister divider mismatch simulation. (d) Current mirror mismatch simulation.

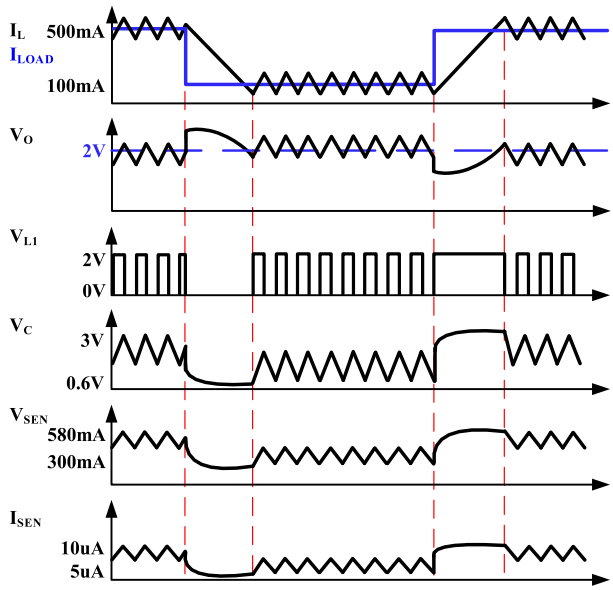

Fig. 3. Signal waveforms related to ACS circuit during $I_{\rm load}$ changes.

Fig. 3 shows the signal waveforms related to ACS circuit, including I_L, V_O, V_{L1}, V_C, $V_{\rm SEN}$, and $I_{\rm SEN}$, during the change of $I_{\rm load}$.

B. Hysteretic-Current-Controlled Circuit

The hysteretic-current-controlled circuit is shown in Fig. 4, where the circuit of OPA is shown in Fig. 2(b); $I_{\rm SEN}$ is the output current of the ACS, $V_{\rm GM}$ is the output voltage of the compensator, and $V_{\rm CONT}$ is the output voltage of PLL. The output voltage $V_{\rm QB}$ of the HCC circuit will be sent to the nonoverlapping circuit. The input voltage $V_{\rm GM}$ is converted to $I_{\rm GM}$ by M_{N1}. $I_{\rm GM}$ can be copied in proportion using current mirrors.

$$I_{\rm GM} = \frac{1}{2}\,\mu_n C_{\rm OX}\left(\frac{W}{L}\right)_{MN1}\left(\frac{1}{2}V_{\rm GM} - V_{\rm TN}\right). \quad (5)$$

The PLL output voltage $V_{\rm cont}$ is converted to I_{RK} by the OPA and R_K, as shown in Fig. 2(b). The I_{RK} can be copied to I_H and I_L in proportion to the current mirrors. $I_{\rm GM} + I_H$ and $I_{\rm GM} - I_L$ are the upper current limit and the lower current limit, respectively. V_{o1} and V_{o2} are converted from $I_{\rm GM} + I_H$ and $I_{\rm GM} - I_L$, respectively. Fig. 5 shows the switching frequency, which is related to $I_{\rm GM} + I_H$ and $I_{\rm GM} - I_L$. The value of the current band range can then be adjusted to design the switching frequency of the converter.

If $I_{\rm SEN} < I_{\rm GM} + I_H$, then V_{O1} is low; if $I_{\rm SEN} > I_{\rm GM} + I_H$, then V_{O1} is high. If $I_{\rm SEN} > I_{\rm GM} - I_L$, then V_{O2} is low; if $I_{\rm SEN} > I_{\rm GM} - I_L$, then V_{O2} is high. Then, the duty cycle is generated by *R–S* flip-flop and sent to a nonoverlapping circuit.

$$I_{RK} = I_H = I_L \quad (6)$$

$$I_{RK} = \frac{V_{\rm CONT}}{R_K}. \quad (7)$$

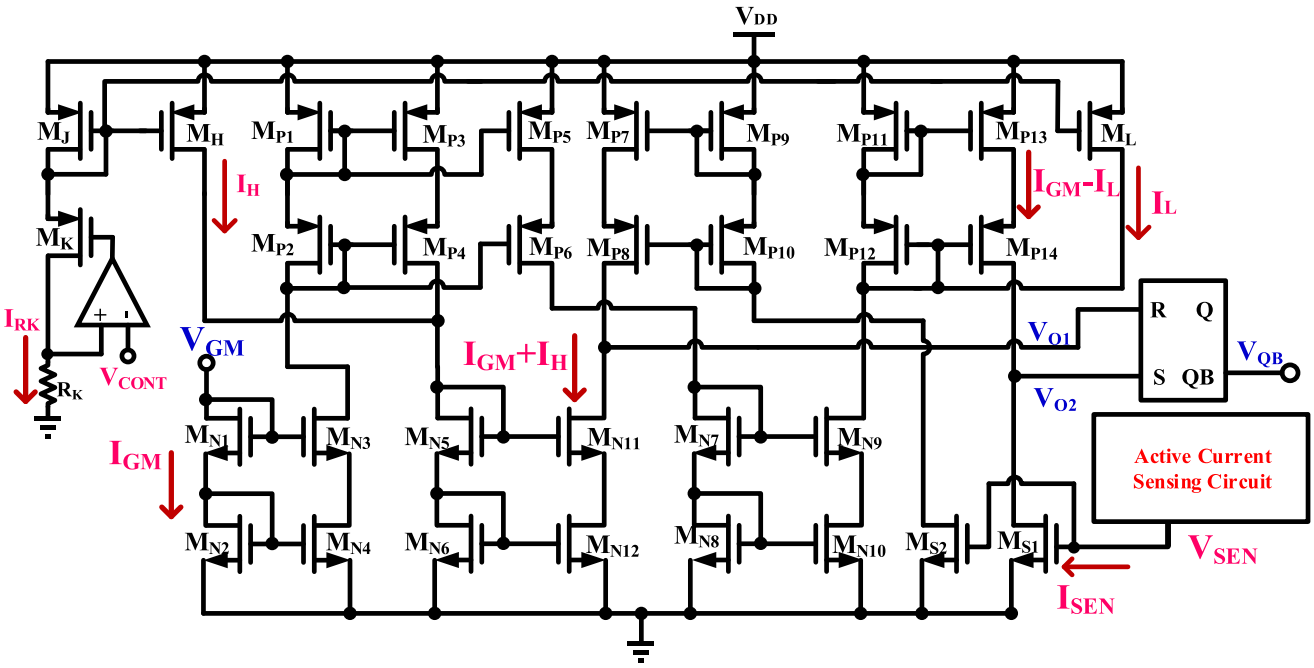

Fig. 4. Hysteretic-current-controlled circuit.

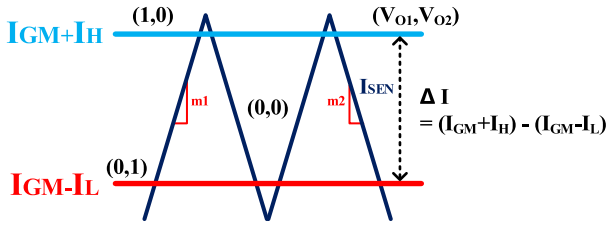

Fig. 5. Signal of a hysteretic-current-controlled circuit.

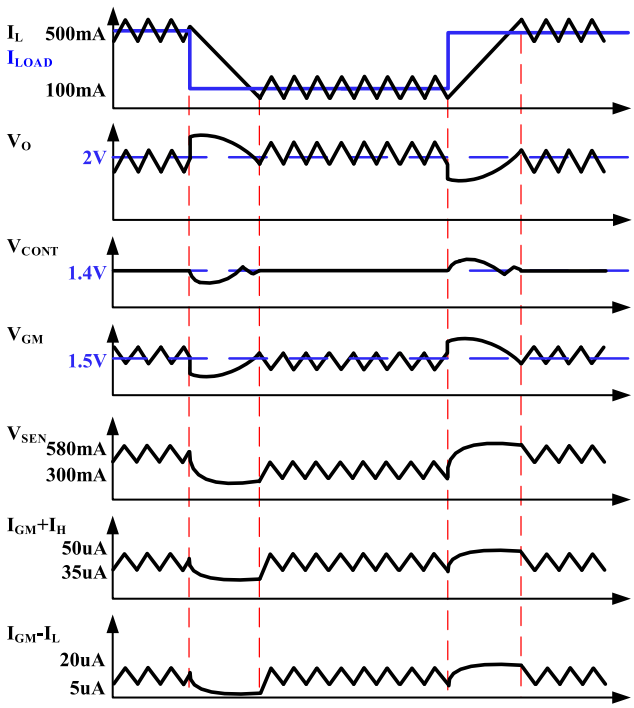

Fig. 6. Signal waveforms related to the HCC circuit during $I_{\rm load}$ changes.

The higher the $V_{\rm CONT}$, the higher the ΔI and the lower the frequency, and vice versa. ΔI is used to control the switching frequency of the system. Therefore, the buck converter is like a voltage-controlled oscillator.

When the load current is switched from light load to heavy load, then $R_{\rm load}$ is decreased, V_o is decreased, $V_{\rm GM}$ is increased, the current band is increased, the duty cycle is increased, I_L is increased, $I_{\rm SEN}$ is increased, and V_o will be increased until returning to a stable level. When the load current is switched from light load to heavy load, it is just the opposite. The duty cycle is adjusted by the feedback loop.

Fig. 6 shows the signal waveforms related to HCC circuit, including $V_{\rm CONT}$, $V_{\rm GM}$, $V_{\rm SEN}$, $I_{\rm GM}+I_H$, and $I_{\rm GM}-I_L$, during the change of $I_{\rm load}$.

C. Compensator

In the switching converters, the output voltage is affected by the output load and the input voltage. The compensator in the feedback loop can improve the regulation ability and reduce the recovery time. Usually, the compensators are composed of an OPA or an operational transconductance amplifier and passive components. The compensators can be divided into three categories: Type I, Type II, and Type III [7]. The Type III compensator requires two more components than the Type II compensator. The proposed buck converter uses Type III compensator, as shown in Fig. 7, which includes an OPA, three resistors (R_1, R_2, and R_3), and three capacitors (C_1, C_2, and C_3). The output voltage of the buck converter is divided by dividing the resistors and sent to compensator to compare with an

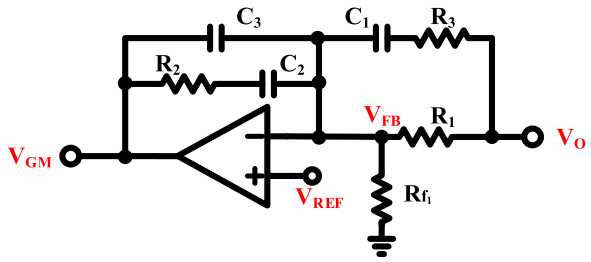

Fig. 7. Compensator circuit.

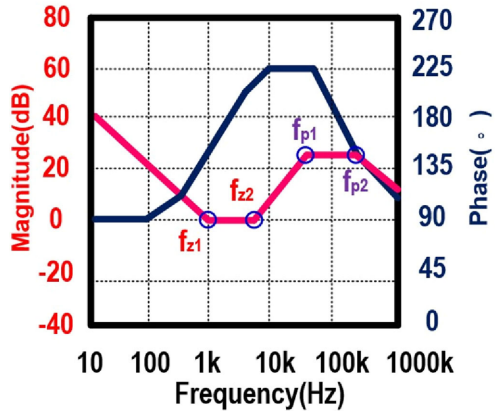

Fig. 8. Bode plots of the compensator.

external reference voltage. The compensator can adjust dc gain, unit-gain-frequency, and phase margin to stabilize the system output. The transfer function can be expressed as

$$\frac{V_{\mathrm{GM}}}{Vo} = \frac{(1+s(R_1+R_3)C_1)\cdot(1+sR_2C_2)}{sR_1(C_2+C_3)\cdot\left(1+sR_2\cdot\frac{C_2C_3}{C_2+C_3}\right)\cdot(1+sR_3C_1)}. \tag{8}$$

Fig. 8 shows the compensation bode plot. The compensator uses the value of resistances and capacitances to determine the positions of its poles and zeros. These poles and zeros improve the overall system phase margin and the dc gain of the frequency to further improve the circuit stability and closed-loop frequency response. The transfer function can be expressed as

$$f_{Z1} = \frac{1}{2\pi\cdot R_2\cdot C_2} \tag{9}$$

$$f_{Z2} \approx \frac{1}{2\pi\cdot(R_1\cdot C_1)},\ R_1 \gg R_3 \tag{10}$$

$$f_{p1} = \frac{1}{2\pi\cdot R_3\cdot C_1} \tag{11}$$

$$f_{p2} \approx \frac{1}{2\pi\cdot(R_2\cdot C_3)}, C_2 \gg C_3. \tag{12}$$

D. Phase–Frequency Detector

The proposed PLL is shown in Fig. 9. The PLL consists of a PFD, a CP, and a low-pass filter. The circuit diagram of the PFD

Fig. 9. Phase–frequency-locked loop.

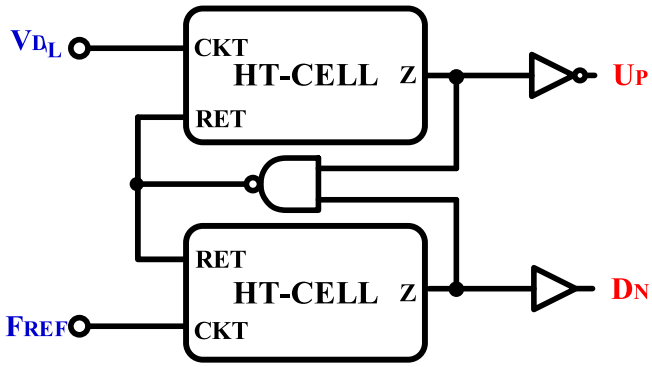

Fig. 10. PFD circuit.

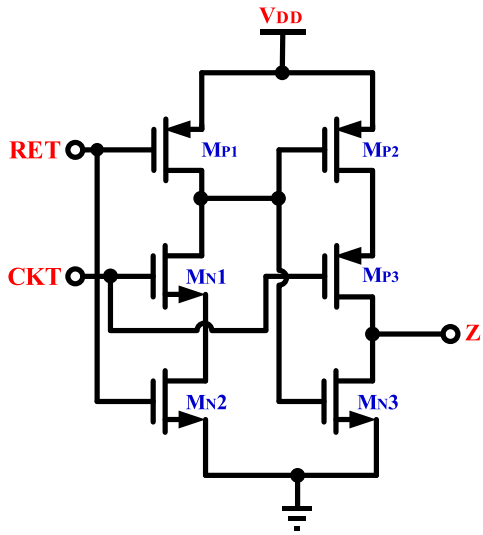

Fig. 11. HT-CELL.

is shown in Fig. 10. It is composed of two half-transparent cells (HT-CELL) and one NAND logic gate.

The HT-CELL is a negative-trigger flip-flop, as shown in Fig. 11. The dynamic logic gate is used to replace a static logic gate in the digital circuit. The HT-CELL is composed of six transistors and uses less logic.

E. Charge Pump

PFD outputs two digital signals to the CP. The CP circuit is shown in Fig. 12, which is used to convert a digital signal into an analog signal.

F. Low-Pass Filter

The low-pass filter is shown in Fig. 13. It converts the output current of the CP into a voltage to filter out high-frequency

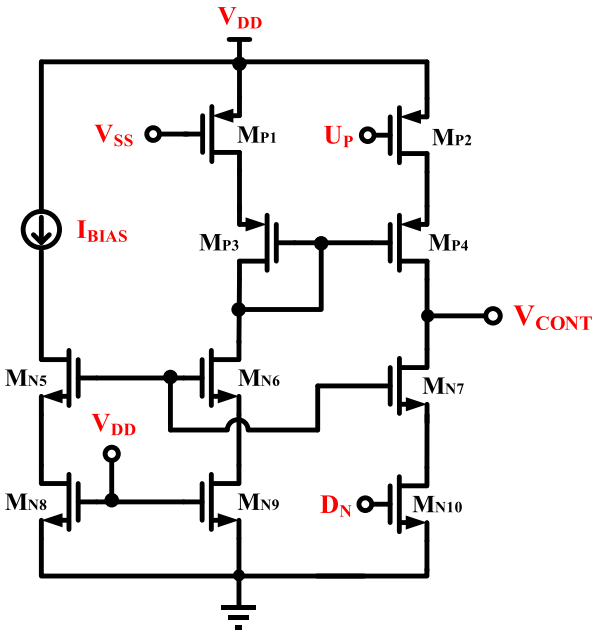

Fig. 12. CP.

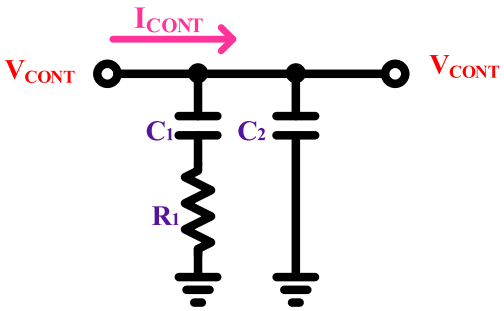

Fig. 13. Low-pass filter.

noise [3]. The parameters of the passive components will affect the system loop bandwidth, and the loop bandwidth affects the system stability and locks the switching frequency. The filter is a second-order low-pass filter, which has one more capacitor C_2 than the first-order *RC* filter. The purpose of PLL is to smooth the output waveform and improve the frequency stability of the oscillator.

$$F(s) = \frac{s + \omega_z}{\frac{1}{\omega_{p1}} s^2 + s} \tag{13}$$

$$\omega_Z = \frac{1}{R_1 \cdot C_1} \tag{14}$$

$$\omega_{p1} = \frac{C_1 + C_2}{C_2 \cdot R_1 \cdot C_1}. \tag{15}$$

III. Experimental Results

This article implements a constant-frequency hysteresis-controlled buck converter and adds a PLL so that the switching frequency is not affected by external factors. The operating frequencies are 1 MHz. Fig. 14 shows a photomicrograph of the proposed buck converter with a chip area of 1.5 mm × 1.5 mm.

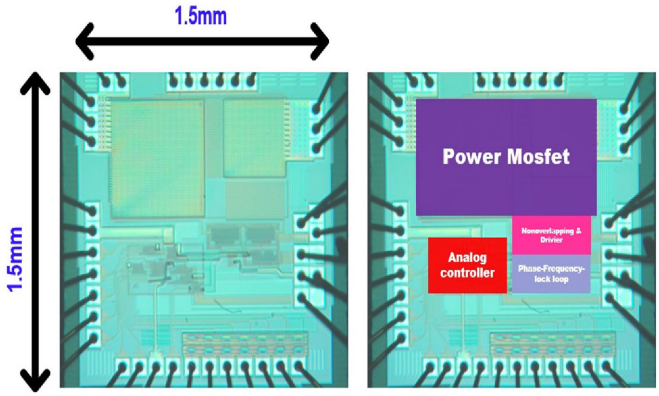

Fig. 14. Micrograph of the proposed buck converter.

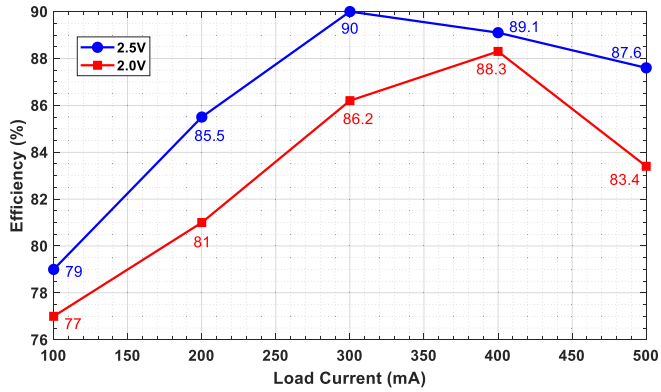

Fig. 15. Power efficiency versus load current measurement.

Fig. 15 shows the efficiency results of the current-mode-hysteretic buck converter with constant-frequency-controlled and new ACS techniques. When the output voltage is 2.5 and 2.0 V and the load current ranges from 100 to 500 mA, the overall conversion efficiency is higher than 70%. When the output voltage is 2.5 V and the load current is 300 mA, the maximum conversion efficiency is 90%.

Fig. 16(a) and (b) shows the measured results of the transient response of the load current changes. When the output voltage is 2 V and the load current is changed from 100 to 500 mA and from 500 to 100 mA, the transient responses are 2.6 μs and 2.2 μs, respectively.

Fig. 17(a) and (b) shows the measurement results of the output voltage and inductor current. At a switching frequency of 1 MHz, Fig. 17(a) shows, when the output voltage is 2 V and the inductor current is 100 mA, the ripple voltage is 37.83 mV. Fig. 17(b) shows when the switching frequency is 1 MHz, the output voltage is 2 V, and the inductor current is 500 mA, the ripple voltage is 59.29 mV.

Fig. 18(a) shows the simulation comparison of the switching frequency variation between the proposed enhanced-hysteretic-current-controlled (ECC) buck converter with PLL and without PLL when the load current is changed from 100 to 500 mA. Fig. 18(b) shows the simulation comparison of the switching frequency variation between the proposed ECC buck converter

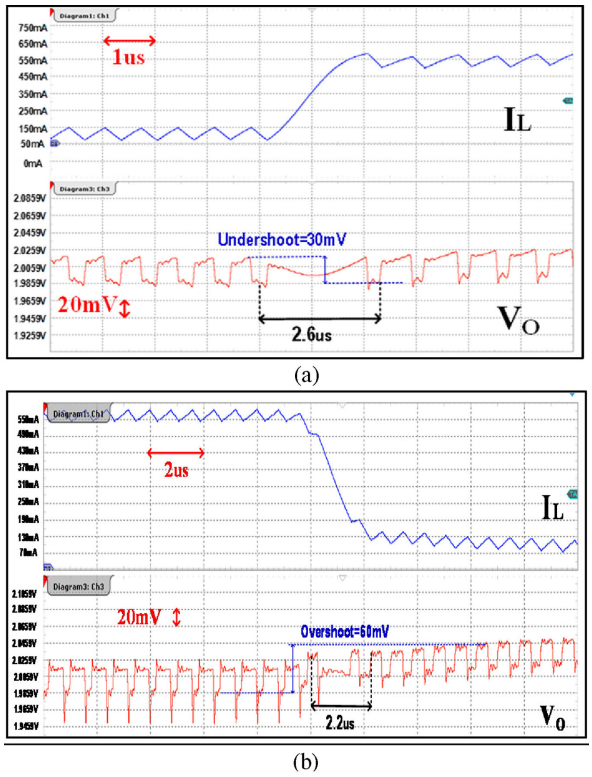

Fig. 16. Load transient response of the proposed converter when the output voltage is 2 V, (a) load current I_L changes from 100 to 500 mA, and (b) load current I_L changes from 500 to 100 mA.

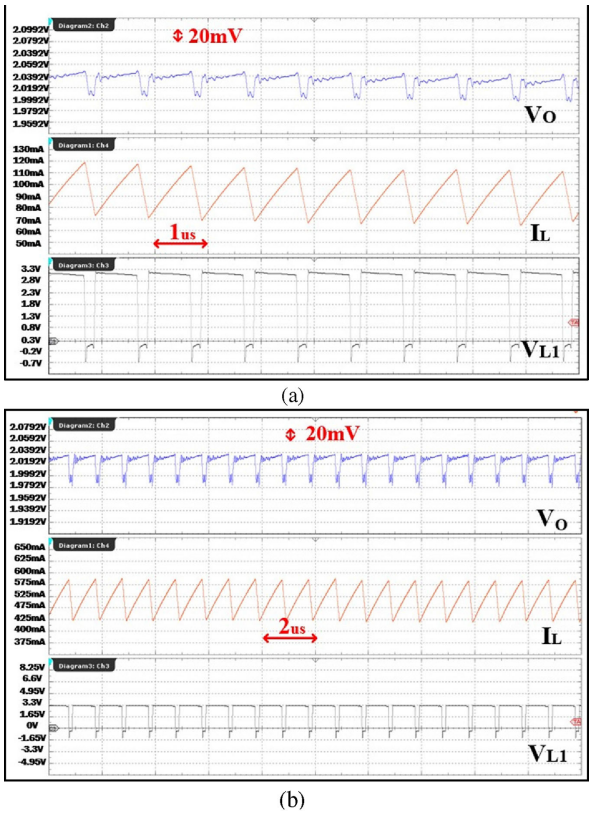

Fig. 17. Measurement results of the output voltage and inductor current. (a) $V_o = 2$ V and $I_L = 100$ mA. (b) $V_o = 2$ V and $I_L = 500$ mA.

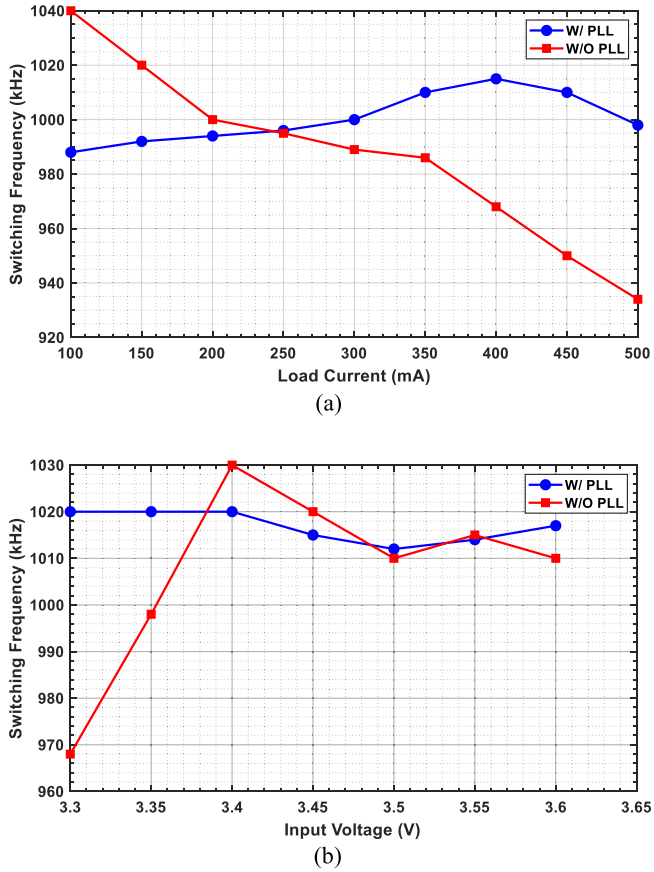

Fig. 18. Simulation comparisons of the switching frequency variation between the proposed ECC buck converter with PLL and without PLL at (a) load current change and (b) input voltage change.

TABLE I
PERFORMANCE SUMMARY

Technology		TSMC 0.35-μm 2P4M
Input Voltage Range		3.3-3.6V
Output Voltage Range		0.9-2.5V
Max Output Ripple		59.289mV
Max. Load Current		600mA
Switching Frequency		1MHz
Inductor		4.7μH
Output-Capacitor		10μF
Transient Response	100mA to 500mA	2.6μs
	500mA to 100mA	2.2μs
Transient Voltage	Undershoot	30 mV
	Overshoot	60 mV
Max. Power Efficiency		90%
Chip Area(with PADS)		2.25 mm^2

TABLE II
PERFORMANCE COMPARISONS WITH PREVIOUS REPORTED BOOST CONVERTERS

References	2018[11]	2019[12]	2019[12]	This work
Control Scheme	Hysteretic	Hysteretic	Hysteretic	Hysteretic PLL
Technology(μm)	0.35	0.065	0.065	0.35
Input Voltage Range(V)	2.7-4.2	2.8-4.2	1.8-4.5	3.3-3.6
Output Voltage Range(V)	1.2-1.8	1.3-2.2	0.9-1.5	0.9-2.5
Inductor(μH)	2.2	2.2	2.2	4.7
Output-Capacitor(μF)	4.7	10	2.2	10
Switching Frequency(MHz)	2.5	1	1-1.18	1
Max Load Current(mA)	600	1500	300	600
Load Current Step(mA)	500	900	299	400
Transient Response(μs)	**4.7/5.2**	**3.4 /3.6**	**40/15**	**2.6/2.2**
Transient Voltage(mV)	**47/44**	**120/97**	**37/34**	**30/60**
Peak Efficiency (%)	92	96.3	94.92	90
Chip Area(mm^2)	0.9	NA	0.18	2.25
FOM	**0.81**	**2.13**	**0.45**	**2.73**

$\text{FOM} = \frac{\text{Peak Efficiency}(\%)\times\text{Load Current Step}(\text{mA})}{\text{Transient Response}(\mu\text{s})\times\text{Switching Frequency}(\text{MHz})\times\text{Transient Voltage}(\text{mV})} \times 10^{-3}$. [15]
The bold value are very important specifications of buck converters in FOM.

with PLL and without PLL when the input voltage is changed from 3.3 to 3.6 V.

Fig. 18(a) and (b) shows that the proposed ECC buck converter with PLL has less frequency variation, so the proposed ECC buck converter with PLL has a stable switching frequency to stabilize the output voltage of the proposed ECC buck converter.

Table I presents the performance of the current-mode-hysteretic control with a constant-frequency buck converter. The input voltage range is 3.3–3.6 V. When the output voltage is 2.5 V and the output current is 300 mA, the maximum efficiency of the circuit is 90%.

Table II is the performance of the proposed converter with the other previous converters. The proposed buck converter has a faster transient response and a lower transient voltage than the other converters. From figure of merit (FOM), the proposed buck converter has a better overall performance than that of the converter in [11] and [12] but worse than that of the converter in [12]. However, the transient voltages in [12] are 120 and 97 mV, which are 5.5%–9.2% of its output voltage. Those transient voltages might cause an error of the devices.

IV. CONCLUSION

A current-mode-hysteretic buck converter with PLL is proposed in this article. The PLL solves the problem of switching frequency variation to improve efficiency [8]. The proposed ACS circuit does not generate sparks when power MOSs switch ON, so it can simplify the current feedback loop to accelerate the transient response and to reduce the output voltage ripple. The HCC circuit and the nonoverlapping circuit are faster than those of the traditional HCC buck converter. Hence, the transient response of the proposed HCC buck converter is faster than the transient response of the traditional HCC buck converter. The proposed buck converter has been implemented with TSMC 0.35 μm 2P4M CMOS processes. The overall performance of the proposed buck converter is better than the other HCC modulation buck converter.

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