# Unidirectional Asymmetric Hybrid Nine-Leg Rectifier With Floating H-Bridge Capacitors

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***Abstract*—This article proposes a unidirectional cascaded topology of a power rectifier. It is composed of a three-leg cell with half-controlled legs series connected with one H-bridge cell per phase. The dc links of the H-bridge cells operate with floating capacitors. The floating capacitor voltages regulation is solved by means of the common-mode voltage manipulation. Control and pulsewidth modulation strategies are presented to regulate the capacitor voltages and grid currents. The design of passive elements is also shown. The topology has its harmonic distortion content, semiconductor losses, and average switching frequency values compared to those of conventional solutions. Experimental results validate the proposed topology and strategy.**

***Index Terms*—AC–DC power converters, power electronics, pulse width modulation.**

## I. Introduction

THREE-phase controlled power rectifiers play an important role in power conversion systems. Applications of these converters cover wind energy conversion systems (WECSs), adjustable-speed drives, uninterrupted power supplies, battery energy storage systems, power supplies for telecommunications, etc., [1]. In this context, the conventional two-level three-leg converter [here named TLC, see Fig. 1(a)] is a well-consolidated topology. On the other hand, to process higher amount of power while employing conventional semiconductor devices, multilevel converters have also been considered for ac–dc applications [2].

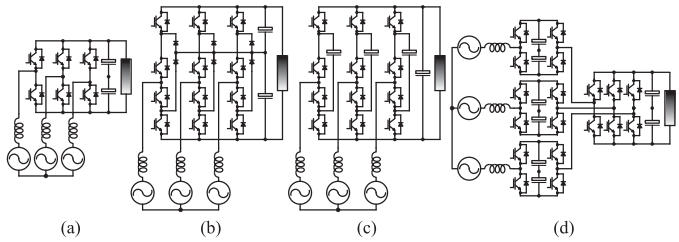


Fig. 1. Conventional full-controlled rectifiers. (a) Three-leg converter (TLC). (b) Neutral-point clamped converter (NPCC). (c) Flying capacitor converter (FCC). (d) Hybrid multilevel converter (HMC) [10].

Multilevel converters, compared to the two-level ones, present drawbacks, such as increased number of semiconductor devices and dc-link capacitors. However, they present several advantages, such as enhanced quality of the output voltages, which allows operation at lower switching frequency, low electromagnetic interference, low voltage stress on semiconductor switches, reduced $dv/dt$, higher efficiency, etc., [3].

The most common multilevel converters include diode-clamped, flying-capacitor [here named FCC, see Fig. 1(c)], cascaded H-bridge (CHB), and modular multilevel converters (MMC) [2], [4]. Fig. 1(b) shows an example of a diode-clamped converter with three-level legs, commonly known as neutral-point clamped converter (here named NPCC). Diode-clamped converters with legs that generate more than three-levels present severe modulation index limitations in high-power factor applications regarding the dc-link capacitors balance. Hence, these converters are not a practical solution for high power factor rectifiers [5]. Besides, hybrid converter topologies were proposed by series-connecting converter cells of different types or/and with different dc-link voltage. [6]–[15]. These converters represent good alternatives in terms of number of voltage levels per switches, providing lower harmonic distortion for same number of semiconductor devices compared with conventional multilevel solutions [6].

In this context, a three-phase hybrid multilevel converter has been proposed for machine drives [7], composed of a three-leg cell series-connected with one H-bridge cell per phase. It was also studied for other applications, such as active power filter [8], six-phase machine drive [9], and bidirectional power

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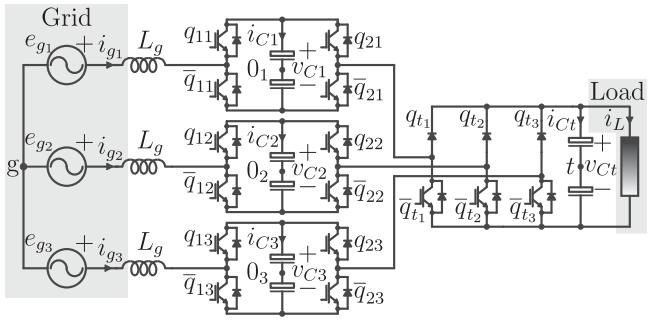


Fig. 2. Proposed unidirectional rectifier (UHMC).

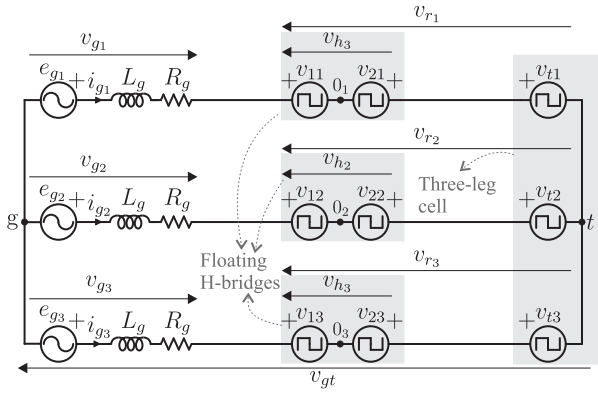


Fig. 3. Equivalent circuit of the proposed topology.

rectifier [10]. This topology is here named HMC [see Fig. 1(d)]. A generalized version for any number of cascaded H-bridge cells was presented in [11] and [12]. In [13], the concept of floating capacitor was first introduced for HMC, making the converter to operate without dc sources at the H-bridge cells. Hence, a control strategy is needed to regulate the voltage of the floating capacitors.

Different strategies have been proposed in the literature for floating capacitor control in multilevel cascaded converters [10]–[12], [14], [15]. The features of each balancing scheme are related with the considered pulsewidth modulation (PWM) technique, because the floating capacitors voltage are regulated by manipulating the converter commutation pattern. However, in multilevel converters, it is expected that the output voltages present an optimized performance, in order to minimize the converter harmonic distortion. Additionally, it is desired that, whenever it is possible, the chosen switching states minimize the converter switching power losses.

In [10], the floating capacitor voltage control was performed considering a level-shifted PWM (LSPWM) and the voltage balance was made by manipulating the common-mode voltage with a third-harmonic injection technique, first proposed in [16]. Moreover, this technique allows to achieve same voltage generation capability of a space-vector PWM (SVPWM) strategy, with similar output voltage quality [16]. This common-mode voltage technique was extensively applied in other works to redistribute power among the phases of the converter [17].

It is worth noting that some applications, such as WECSs and power supplies for telecommunication, do not require converter regenerative operation. In addition, in some aerospacial applications, it is forbidden [18]. In these applications, the converter can or must be unidirectional with some controlled switches replaced by diodes, reducing cost and volume of the converter [19].

The main contributions of this article are as follows.

1) Proposition of a unidirectional version of the HMC, considering the three-leg cell operating with half-controlled legs. The proposed rectifier is named UHMC in this article (see Fig. 2).
2) Improvement of the PWM and balancing voltage algorithm presented in [10] for the HMC and its adaptation to the proposed UHMC. Also, the mechanism that allows this strategy is detailed and the floating dc links capacitance design is shown.

Here, the three-leg cell is connected to a dc load, whereas the H-bridges have floating capacitors. The proposed rectifier is compared with the conventional topologies presented in Fig. 1 considering semiconductor losses, harmonic distortion, average switching frequency, number, rating, and size of components. Finally, simulation and experimental results are presented for validation purposes.

## II. Converter Model

Considering the equivalent circuit of the proposed topology shown in Fig. 3, it is possible to derive the main equations of the system in time domain. The dynamic behavior of grid currents is defined by

$$e_{gj} - v_{gj} = R_g i_{gj} + L_g \frac{di_{gj}}{dt} \tag{1}$$

where the subscript $j = \{1, 2, 3\}$ indicates each of the three phases of the system, $v_{gj}$ are the resultant voltages of the converter, $e_{gj}$ are the grid voltages, and $i_{gj}$ represent the grid currents. $L_g$ and $R_g$ represent the inductance and inner resistance of the filter inductors, respectively. The resultant voltage $v_{gj}$ is determined by

$$v_{gj} = v_{rj} - v_{gt} \tag{2}$$

where $v_{gt}$ is the voltage between neutral point $g$ and dc-link midpoint $t$, i.e., the common-mode voltage, and $v_{rj}$ are the equivalent multilevel pole voltages given by

$$v_{rj} = v_{1j} - v_{2j} + v_{tj}. \tag{3}$$

Here, $v_{tj}$ are the pole voltages of the three-leg cell. $v_{1j}$ and $v_{2j}$ are the pole voltages of the H-bridge cells. Besides that, considering a three-wired system ($v_{g1} + v_{g2} + v_{g3} = 0$), $v_{gt}$ is given by

$$v_{gt} = \frac{1}{3}(v_{r1} + v_{r2} + v_{r3}). \tag{4}$$

In addition, the pole voltages are determined by

$$v_{tj} = \frac{v_{Ct}}{2}(2q_{tj} - 1) \tag{5}$$

$$v_{ij} = \frac{v_{Cj}}{2}(2q_{ij} - 1) \tag{6}$$

where $v_{Cj}$ and $v_{Ct}$ are the dc-link voltages, and $i = \{1, 2\}$ represents the two legs of the H-bridge. $q_{ij}$ and $q_{tj}$ are binary variables representing the switching states, with the value 1 representing the upper switch turned-ON state and 0 representing the turned-OFF state.

The three-leg cell is composed of half-controlled legs, where the upper switches are diodes. Hence, if $i_{gj} < 0$, then $q_{tj} = 0$, i.e., during the current negative half cycle, the diodes remain blocked and do not allow the leg to commute. During the positive half cycle ($i_{gj} > 0$), the duty cycle of the switch $q_{tj}$ is determined by the PWM technique.

Finally, the currents in the dc links of the H-bridges ($i_{Cj}$) and three-leg cell ($i_{Ct}$) are determined, respectively, by

$$i_{Cj} = i_{gj}(q_{j1} - q_{j2}) = C_h \frac{dv_{Cj}}{dt} \tag{7}$$

$$i_{Ct} = i_{g1}q_{t1} + i_{g2}q_{t2} + i_{g3}q_{t3} - i_L = C_t \frac{dv_{Ct}}{dt} \tag{8}$$

where $i_L$ is the load current, and $C_h$ and $C_t$ are the dc-link capacitance values of the H-bridges and three-leg cell, respectively.

## III. Pulsewidth Modulation (PWM)

### A. Calculation of the Reference Common-Mode Voltage $v^*_{gt}$

Based on (1), the converter reference multilevel pole voltages are

$$v^*_{rj} = v^*_{gj} + v^*_{gt} \tag{9}$$

where the superscript * denotes reference variables, $v^*_{gj}$ are the converter reference resultant voltages, defined by current control, and $v^*_{gt}$ is the reference common-mode voltage, whose calculation is detailed as follows.

A hybrid PWM strategy is considered to generate the reference common-mode voltage $v^*_{gt}$ [10], [16]. This technique consists in calculating its maximum and minimum values and using an apportioning factor to perform the variation of $v^*_{gt}$ within these limits. In this article, this technique is modified to adapt its use to the proposed unidirectional converter UHMC. In this way, the reference common-mode voltage is given by

$$v^*_{gt} = \mu^* v^*_{gtM} + (1 - \mu^*) v^*_{gtm} \tag{10}$$

where $0 \leq \mu^* \leq 1$, such that when $\mu^*$ varies from 0 to 1, and $v^*_{gt}$ varies from its minimum to its maximum value. This apportioning factor $\mu^*$ represents a degree of freedom in the generation of converter voltages and it is used in this article to perform the control of the dc-link voltage of the H-bridge cells.

The minimum ($v^*_{gtm}$) and maximum ($v^*_{gtM}$) values of the reference common-mode voltage can be derived by analyzing the three equations defined by (9). Each of these equations define one local maximum and one local minimum values for $v^*_{gt}$. The local minimums defined for each phase are $v_{gtmj} = -v^*_{Ch} - \frac{v^*_{Ct}}{2} - v^*_{gj}$, where $v^*_{Ch}$ and $v^*_{Ct}$ are the reference dc-link voltages of the three-leg cell and H-bridges, respectively. Additionally, the generation of $v^*_{gt}$ must respect the voltage generation limits of the three phases of the converter simultaneously. Consequently, the global minimum ($v^*_{gtm}$) is then the maximum of these three local minimums

$$v^*_{gtm} = -v^*_{Ch} - \frac{v^*_{Ct}}{2} + \max\{-v^*_{g1}, -v^*_{g2}, -v^*_{g3}\}. \tag{11}$$

The calculation of the maximum $v^*_{gtM}$ follows a similar procedure, but it requires a modification from the equations applied to the bidirectional case [10]. The local maximums are $v_{gtMj} = -v^*_{Ch} + v^*_{tjM} - v^*_{gj}$, where $v^*_{tjM}$ is the maximum value for the reference pole voltages of the three-leg cell

$$v^*_{tjM} = \begin{cases} \frac{v^*_{Ct}}{2}, & i_{gj} \geq 0 \\ -\frac{v^*_{Ct}}{2}, & i_{gj} < 0. \end{cases} \tag{12}$$

These $v^*_{tjM}$ change depending on the currents polarity because the legs of the three-leg cell are half controlled. Then, for example, if $i_{g1} > 0$, the duty cycle of the switch $q_{t1}$ is able to commute and $v^*_{t1M} = \frac{v^*_{Ct}}{2}$. On the other hand, if $i_{g1} < 0$, the upper switch composed by a diode is turned-OFF and $q_{t1} = 0$. In this condition, the only possible value of this pole voltage is $v_{t1} = -\frac{v_{Ct}}{2}$, then the maximum value of its reference is also $v^*_{t1M} = -\frac{v^*_{Ct}}{2}$. The same logic is valid for phases 2 and 3.

Moreover, similarly to (11), the global maximum $v^*_{gtM}$ is the minimum of the three local maximums ($v^*_{gtM}$), leading to

$$v^*_{gtM} = v^*_{Ch} + \min\{v^*_{t1M} - v^*_{g1}, v^*_{t2M} - v^*_{g2}, v^*_{t3M} - v^*_{g3}\}. \tag{13}$$

### B. Level-Shifted PWM (LSPWM)

After the reference multilevel pole voltages $v^*_{rj}$ are calculated by (9)–(13), an LSPWM approach is performed in each phase considering the reference $v^*_{rj}$. In this context, the UHMC operates asymmetrically with $v^*_{Ct} = 3v^*_{Ch}$. This dc-link voltage ratio allows the converter to generate the maximum number of levels equally spaced from each other (six levels). Fig. 4 illustrates the considered LSPWM strategy.

The six levels generated by the converter define five sectors [$z = (1, 2, 3, 4, 5)$]. The sector where the reference is located is

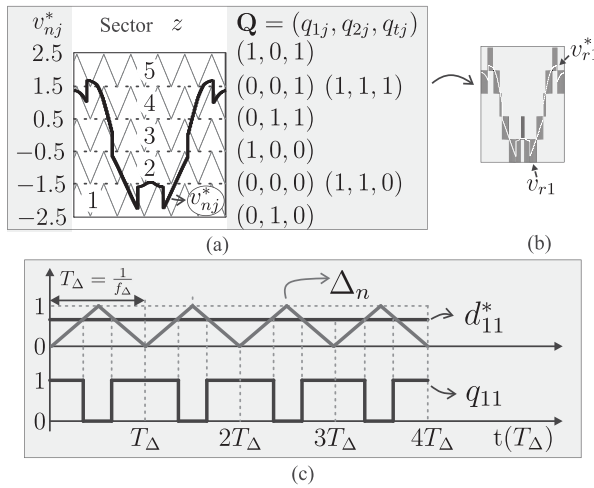


Fig. 4. LSPWM description. (a) Levels at normalized voltage $v^*_{nj}$, sectors $z$, and switching states $\mathbf{Q}$. (b) Resultant voltage waveform. (c) Illustration of comparison between reference duty cycles and normalized carrier.

TABLE I
DUTY CYCLES $\mathbf{d_j^*} = (d_{tj}^*, d_{1j}^*, d_{2j}^*)$ CALCULATION AND SWITCH-STATE COMMUTATION OF EACH LEG FOR IMPLEMENTATION OF LSPWM

| $z$ | $d_{tj}^*$ | $d_{1j}^*$ | $d_{2j}^*$ | $(q_{1j}, q_{2j}, q_{tj})$ |
|---|---|---|---|---|
| 5 | 1.0 | $v_{nj}^* - 1.5$ | 0.0 | $(0,0,1) \rightarrow (1,0,1)$ |
| 4 | 1.0 | $v_{nj}^* - 0.5$ | 1.0 | $(0,1,1) \rightarrow (1,1,1)$ |
| 3 | $v_{nj}^* + 0.5$ | $0.5 - v_{nj}^{*}$ ** | $v_{nj}^* + 0.5$ | $(1,0,0) \rightarrow (0,1,1)$ |
| 2 | 0.0 | $v_{nj}^* + 1.5$ | 0.0 | $(0,0,0) \rightarrow (1,0,0)$ |
| 1 | 0.0 | $v_{nj}^* + 2.5$ | 1.0 | $(0,1,0) \rightarrow (1,1,0)$ |

** With carrier $\Delta_n$ phase shift of 180°.

determined by

$$z = \left\lceil \frac{5(v_{rj}^* + 0.5v_{Ct}^* + v_{Ch}^*)}{v_{Ct}^* + 2v_{Ch}^*} \right\rceil. \tag{14}$$

Then, the LSPWM can be implemented by comparing the reference with five level-shifted carriers. An equivalent implementation is obtained by level shifting the reference instead of the carriers and comparing this level-shifted reference with a single carrier. Table I presents the calculation of the duty cycles of each leg ($d_{tj}^*$, $d_{1j}^*$ and $d_{2j}^*$) for the equivalent level-shift implementation and the resultant switch state commutation, where $v_{nj}^*$ is a normalized reference voltage calculated by

$$v_{nj}^* = \frac{v_{rj}^*}{v_{Ct}^* + 2v_{Ch}^*} = \frac{3v_{rj}^*}{5v_{Ct}^*}. \tag{15}$$

Finally, the generation of the instantaneous switching states of the H-bridge switches is made by

$$q_{ij} = \begin{cases} 1, & \text{if } d_{ij}^* \geq \Delta_n \\ 0, & \text{if } d_{ij}^* < \Delta_n. \end{cases} \tag{16}$$

For the three-leg cell, the commutation takes into account the current polarity, then it is given

$$q_{tj} = \begin{cases} 1, & \text{if } d_{tj}^* \geq \Delta_n \text{ and } i_{gj} \geq 0 \\ 0, & \text{if } d_{tj}^* < \Delta_n \text{ or } i_{gj} < 0. \end{cases} \tag{17}$$

This commutation logic is illustrated for leg $q_{11}$ in Fig. 4(c), where $\Delta_n$ is a normalized carrier and $f_\Delta$ is the carrier frequency. From Table I, for $z = 3$, the duty cycle $d_{1j}^*$ must be compared with a carrier phase shift of 180°, because in this sector, the switches $q_{1j}$ present inverted comparison logic to generate the required switching states.

## IV. STEADY-STATE ANALYSIS OF FLOATING CAPACITORS

This section presents the mechanisms of charging and discharging the floating capacitors and steady-state analysis to evaluate the effectiveness of the control actions and their limitations.

### A. Steady-State Equations

Since the converter only allows unidirectional power flow, a current control is performed in order to maintain converter currents and voltages synchronization [19]. If the synchronization is not established, the converter will not synthesize properly their voltages and it will cause distortions in voltages and currents around the zero-crossing moments of the currents. Then, considering a sinusoidal balanced steady-state operation, a phasor diagram is composed, as shown in Fig. 5, where $I_g$, $E_g$, and $V_g^*$ are the amplitudes of the grid currents, voltages, and the converter reference voltages. Also, $w_o = 2\pi f_o$ and $f_o$ is the fundamental frequency of grid voltages.

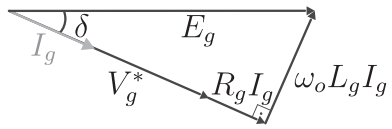


Fig. 5. Phasor diagram for the unidirectional converter operation.

In this way, the average power processed by the converter ($P_g$) is

$$P_g = \frac{3}{2} V_g^* I_g = P_l + P_{\text{loss}} \tag{18}$$

where $P_l$ is the load power and $P_{\text{loss}}$ are the converter total losses. Also, from the phasor diagram of Fig. 5, applying the Pythagorean theorem, it is derived

$$E_g^2 = (\omega_o L_g I_g)^2 + (V_g^* + R_g I_g)^2. \tag{19}$$

Multiplying (19) by $V_g^*$, replacing (18) in it and isolating $V_g^*$, we have

$$V_g^* = \sqrt{\frac{3E_g^2 - 4P_g R_g}{6} + \sqrt{\frac{E_g^4}{4} - \frac{6P_g R_g E_g^2 + 4P_g^2 \omega_o^2 L_g^2}{9}}}. \tag{20}$$

Finally, the converter modulation index ($m_a$) is defined by

$$m_a = \frac{\sqrt{3} V_g^*}{v_{Ct}^* + 2v_{Ch}^*} = \frac{3\sqrt{3} V_g^*}{5v_{Ct}^*}. \tag{21}$$

As defined in (21), $0 \leq m_a \leq 1$, for the converter operating in the linear region of voltage generation. In a steady-state balanced operation, the generation of the duty cycles can be fully defined by these two normalized parameters: the apportioning factor $\mu^*$ and the modulation index $m_a$.

### B. Charge and Discharge Mechanisms of the H-Bridges

The H-bridge cells have floating dc links, i.e., no source or load is connected to their capacitors. This fact makes it necessary to control the H-bridge dc-link voltages by manipulating the converter switching states to charge and discharge the capacitors. The charging state of floating capacitors can be determined by analyzing (7). Instantly, the capacitor of phase $j$ charges if $i_{Cj} > 0$ and discharges if $i_{Cj} < 0$. If $i_{Cj} = 0$, no change occurs. Fig. 6 shows for one phase its corresponding current path and specifies if it either charges, discharges, or performs no change (neutral state) on the floating capacitor voltage as a function of the grid current. The switching states that have $q_{tj} = 1$ ($\mathbf{Q_1}$, $\mathbf{Q_3}$, $\mathbf{Q_5}$ and $\mathbf{Q_7}$) are marked as forbidden for $i_{gj} < 0$. These states cannot be applied by the converter in this current condition because the diode blocks with the attempt to perform reverse current flow, leading to $q_{tj} = 0$.

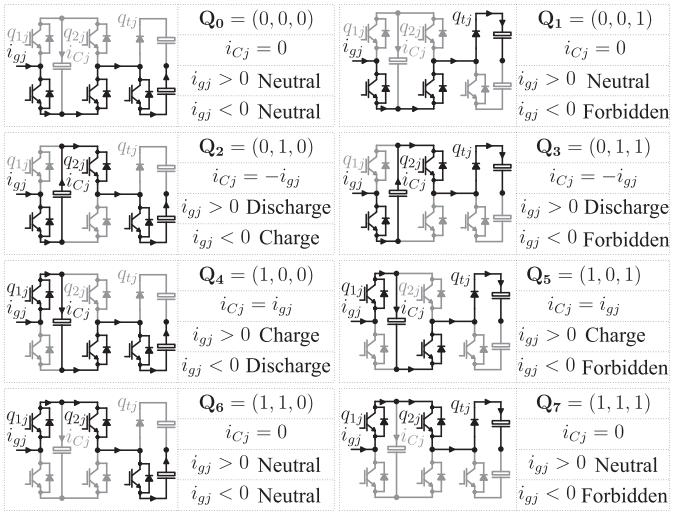


Fig. 6. Charge or discharge of floating capacitors as a function of the converter switching states $\mathbf{Q} = (q_{1j}, q_{2j}, q_{tj})$ and grid currents $i_{gj}$.

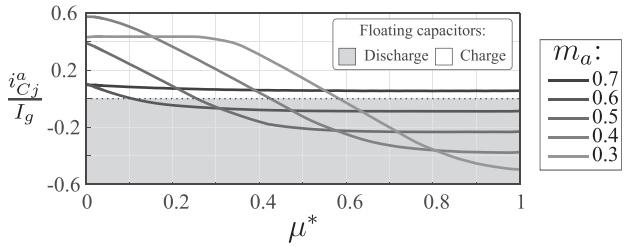


Fig. 7. Average dc-link current $i^a_{Cj}$ normalized by the amplitude of grid current $I_g$ as a function of the apportioning factor $\mu^*$ for different conditions of modulation index.

In addition, the average value of $i_{Cj}$ in one grid period is given by

$$i^a_{Cj} = \frac{1}{T_o}\int_0^{T_o} i_{Cj}dt = \frac{1}{T_o}\int_0^{T_o} (q_{1j} - q_{2j}) i_{gj} dt. \qquad (22)$$

In a steady-state operation, the capacitors' voltages are in their reference values and $i^a_{Cj} = 0$. However, in a transient operation, the converter must be able to impose $i^a_{Cj} > 0$ and $i^a_{Cj} < 0$ to charge and discharge the floating capacitors and regulate their voltages. In terms of a control strategy, this manipulation of the average dc-link currents of the H-bridges is performed in this article by the parameter $\mu^*$.

### C. Influence of $\mu^*$ and $m_a$ on the Floating-Capacitor Voltages in a Steady-State Operation

To evaluate the influence of $\mu^*$ and $m_a$ on the charging state of floating capacitors, steady-state simulations were performed. Figs. 7 –9 present the average current $i^a_{Cj}$ normalized by the grid currents amplitude $I_g$ under different conditions of $\mu^*$ and $m_a$, considering a balanced steady-state operation.

If a constant value is set for $\mu^*$ in one grid period, the three-phase symmetry makes the three average currents to have the same value ($i^a_{C1} = i^a_{C2} = i^a_{C3}$). This means that with constant $\mu^*$, the three floating capacitors either charge or discharge simultaneously and the common-mode voltage does not distribute power among phases, but among cascaded cells. Fig. 7 shows, for different conditions of modulation index, that the average currents vary continuously as a function of $\mu^*$, decreasing as $\mu^*$ goes from 0 to 1. In this way, for any modulation index, $\mu^* = 0$ causes the maximum value of $i^a_{Cj}$ and $\mu^* = 1$ causes the minimum value of $i^a_{Cj}$.

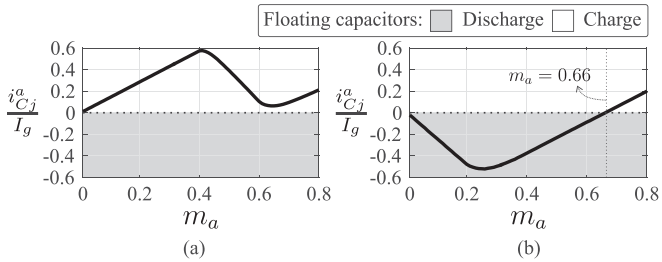


Fig. 8. Average dc-link current $i^a_{Cj}$ normalized by the amplitude of grid current $I_g$ as a function of the modulation index for constant $\mu^*$. (a) $\mu^* = 0$. (b) $\mu^* = 1$.

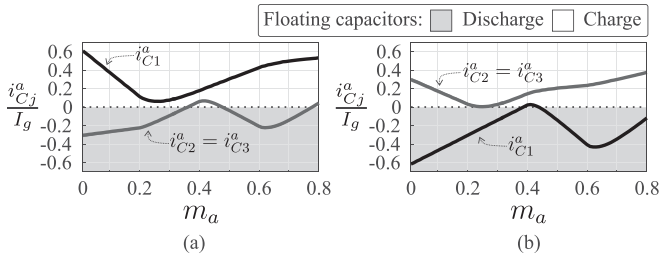


Fig. 9. Average dc-link current $i^a_{Cj}$ normalized by the amplitude of grid current $I_g$ as a function of the modulation index for constant $\mu^*$. (a) $\mu^* = 1$ for $i_{g1} \geq 0$ and $\mu^* = 0$ otherwise. (b) $\mu^* = 0$ for $i_{g1} \geq 0$ and $\mu^* = 1$ otherwise.

For $\mu^* = 0$ [see Fig. 8(a)], in any modulation index $i^a_{Cj} > 0$, i.e., the three floating capacitors charge. On the other hand, if $\mu^* = 1$ [see Fig. 8(b)], $i^a_{Cj} < 0$ for $m_a < 0.66$. This implies that $\mu^* = 1$ is able to discharge the three floating capacitors for $m_a < 0.66$.

If one particular capacitor needs to be charged or discharged in detriment of the others, instead of simultaneously charging or discharging all of them, a different control action needs to be taken. Although in a steady-state balanced operation, the three floating capacitors tend to present same voltage; during a transient one, there may appear unbalances among their voltages. In order to mitigate this, if the apportioning factor is changed as a function of one grid current, it is possible to exchange power among the converter phases by charging the floating capacitor of one phase and discharging the other two or vice versa. In Fig. 9, this mechanism is exemplified for $\mu^*$ varying as a function of $i_{g1}$. In Fig. 9(a), it is made $\mu^* = 1$ for $i_{g1} \geq 0$ and $\mu^* = 0$ otherwise. In this condition, $i^a_{C1} > 0$ and $i^a_{C2} = i^a_{C3} < 0$ for any modulation index. This implies that the floating capacitor of phase 1 charges and the other two discharge. In Fig. 9(b), the opposite occurs. It is made $\mu^* = 0$ for $i_{g1} \geq 0$ and $\mu^* = 1$ otherwise. Then, the floating capacitor of phase 1 discharges and the other two charge. The same analysis is valid if the currents of the other phases ($i_{g2}$ or $i_{g3}$) are considered.

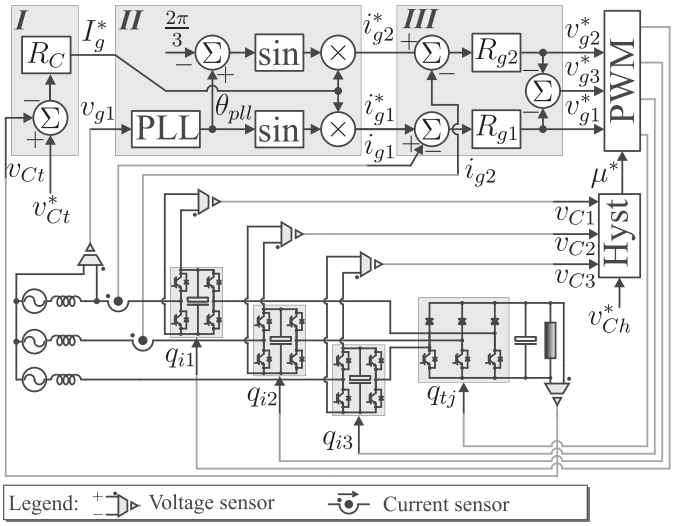


Fig. 10. Block diagram of a control strategy: I. Load voltage control; II. Generation of reference currents; III. Current control.

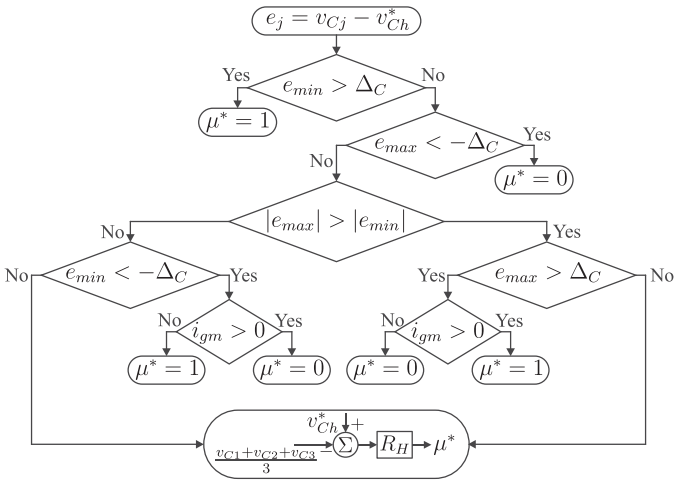


Fig. 11. Flowchart of voltage control of floating capacitors (Hyst block of Fig. 10).

Thus, $m_a = 0.66$ is the maximum modulation index (MMI) achieved by the proposed floating capacitors control. For higher values of modulation index, the control of floating capacitors could not be accomplished because there would not be a control action to discharge the three capacitors simultaneously.

## V. Control Strategy

Fig. 10 presents the control block diagram of the proposed UHMC. The required sensors are also represented. This topology requires two current sensors for the grid currents, and five voltage sensors; one voltage sensor for the PLL voltage synchronization, and four dc-link measurements.

### A. Control of Load Voltage $v_{Ct}$

The control of the dc-link voltage $v_{Ct}$ is performed by a cascaded control, divided in three parts (I, II, and III). Initially, in I, the load voltage error ($v_{Ct}^* - v_{Ct}$) is evaluated by a conventional proportional integral (PI) controller ($R_C(s) = k_{pC} + \frac{k_{iC}}{s}$) and returns the amplitude ($I_g^*$) for the reference currents .

In II, the instantaneous reference grid currents $i_{g1}^*$ and $i_{g2}^*$ are generated synchronized with the voltage in the converter mains ($v_{g1}$) by means of a fictitious power phase-locked loop (PLL block) [20]. Then, in III, the grid current errors ($i_{g1}^* - i_{g1}$ and $i_{g2}^* - i_{g2}$) are evaluated by resonant controllers (blocks $R_{g1}$ and $R_{g2}$) that return the converter reference voltages $v_{g1}^*$ and $v_{g2}^*$. These double-sequence controllers, proposed in [21], are proper for operation with a sinusoidal reference. Only two currents can be controlled because in a three-wired system $i_{g1} + i_{g2} + i_{g3} = 0$, then it is made $v_{g3}^* = -v_{g1}^* - v_{g2}^*$ and $i_{g3}$ is automatically regulated. The transfer function of $R_{g1}$ and $R_{g2}$ is

$$R_{g1}(s) = R_{g2}(s) = 2\frac{K_{pi} + K_{ii}s}{s^2 + \omega_o^2}. \tag{23}$$

In this article, these controllers present a discrete implementation in a digital signal processor (DSP). The discrete models used here can be found in [22].

### B. Voltage Control of Floating Capacitors

The control of the dc-link voltages of the H-bridge cells is represented in Fig. 10 by the Hyst block, which is detailed in Fig. 11. It is considered a hybrid control strategy, considering a hysteresis-based algorithm and a conventional PI control.

The dc-link voltage errors ($e_j = v_{Cj} - v_{Ch}^*$) are evaluated as well as their maximum and minimum values ($e_{\max} = \max\{e_1, e_2, e_3\}$ and $e_{\min} = \min\{e_1, e_2, e_3\}$). If all errors are higher than $\Delta_C$ ($e_{\min} > \Delta_C$), it means that all floating capacitors have exceeded their upper limits and need to be discharged, then constant $\mu^* = 1.0$ is set. If all errors are lower than $-\Delta_C$ ($e_{\max} < -\Delta_C$), it means that all three floating capacitor voltages are below their lower limit and need to be charged, then constant $\mu^* = 0.0$ is set.

In the other cases, the algorithm acts to control the dc-link voltage that has the higher absolute error ($|e_{\max}|$ or $|e_{\min}|$). To do so, a control current $i_{gm}$ is considered, where $m$ is the phase that contains the floating capacitor with the higher absolute voltage error ($m \in \{1, 2, 3\}$). Then, if $e_{\max} > \Delta_C$ and $|e_{\max}| > |e_{\min}|$, that is, the floating capacitor with higher error needs to be discharged, then it should be set $\mu^* = 1.0$ when $i_{gm} \geq 0$ and $\mu^* = 0.0$ when $i_{gm} < 0$. On the other hand, if $e_{\min} < -\Delta_C$ and $|e_{\min}| > |e_{\max}|$, that is, the floating capacitor with higher error needs to be charged, then it should be set $\mu^* = 0.0$ when $i_{gm} \geq 0$ and $\mu^* = 1.0$ when $i_{gm} < 0$.

Finally, if all three floating capacitors are within the hysteresis limits, a PI controller is implemented [$R_H(s) = k_{pH} + \frac{k_{iH}}{s}$], evaluating the average error of the three voltages, in order to find a constant value for $\mu^*$ between $\mu^* = 0.0$ and $\mu^* = 1.0$ that leads the floating capacitors to a steady-state operation.

### C. Hysteresis Band Design

Although a hysteresis algorithm is applied for the floating capacitors control, the hysteresis band does not define the floating capacitors oscillation in a steady-state operation. When the three floating capacitor voltages are within the hysteresis band,

a PI control is applied, leading to a steady-state value of dc-link voltage, with lower oscillation than the hysteresis band.

Conversely, the hysteresis band $\Delta_C$ must be chosen such that $\Delta_C > 0.5\Delta v_{Cj}$, where $\Delta v_{Cj}$ is the peak-to-peak voltage ripple, because the hysteresis control cannot reduce or eliminate this ripple. On the other hand, it must be chosen to limit the maximum dc-link voltage error during a transient. A practical value can be chosen as $\Delta_C = 2\Delta v_{Cj}$.

## VI. Passive Elements Design

### A. Floating Capacitors Design

Here, the capacitance of H-bridges dc link is designed using the steady-state voltage oscillation criterion. The floating capacitors present a voltage ripple in the fundamental frequency of the grid ($f_o$). Phase 1 will be considered for calculation, but the behavior of the other two phases is similar. Considering that in a steady-state operation, $i_{g1} = I_g \sin(2\pi f_o t)$ and (7), the voltage ripple of the floating capacitors ($\Delta v_{Cj}$) can be calculated by

$$\Delta v_{Cj} = \frac{1}{C_h}\int_0^{\frac{T_o}{2}} I_g \sin(2\pi f_o t)(q_{1j} - q_{2j})dt. \tag{24}$$

The factor $q_{1j} - q_{2j}$ varies along the grid cycle and depends on the converter operation point. The worst case in terms of voltage ripple would occur if $q_{1j} - q_{2j} = 1.0$ during all half cycle. In this case, (24) would lead to

$$C_{h_{\max}} = \frac{I_g}{\pi f_o \Delta v_{Cj_{\max}}} \tag{25}$$

where $\Delta v_{Cj_{\max}}$ is the maximum peak-to-peak voltage oscillation in volts, $I_g$ is the amplitude of grid currents in amperes, and $f_o$ is the grid fundamental frequency in Hz. This value of capacitance is an upper limit that does not need to be exceeded and often will lead to an overdimensioned capacitor. On the other hand, dynamic simulations have shown that the capacitor must not be less than half of this value, in order to guarantee the specified voltage ripple. Then, the minimum capacitance is

$$C_{h_{\min}} = \frac{I_g}{2\pi f_o \Delta v_{Cj_{\max}}}. \tag{26}$$

### B. Load DC-Link Capacitor Design

The main dc-link capacitor presents a voltage ripple with frequency of $6f_o$. The dc-link capacitor is here designed such that the *RC* constant of the dc link is at least six times the period of this ripple ($R_l C_t = \frac{6}{6f_o}$) to guarantee control stability [23]. In this way, the minimum capacitance can be calculated by

$$C_{t_{\min}} = \frac{1}{R_l f_o} = \frac{P_g}{f_o {v^*_{Ct}}^2}. \tag{27}$$

### C. Filter Inductors Design

Here, it is considered that in any PWM period ($T_\Delta$), the converter voltage $v_{gj}$ alternate between two voltage levels distanced of $\Delta V$ from each other. Therefore, the voltage component $v_{rp}$ that generates the current ripple $i_{rp}$ also alternate between two levels ($V_{\text{up}}$ and $V_{\text{dw}}$) with a duty cycle $D$, with $0 \leq D \leq 1$ and $V_{\text{up}} - V_{\text{dw}} = \Delta V$. Moreover, $v_{rp}$ presents null average value in each PWM period. With these premises, for one PWM period, it is possible to derive

$$v_{rp} = \begin{cases} V_{\text{up}} = (1-D)V_\Delta, & \text{for } 0 < t \leq DT_\Delta \\ V_{\text{dw}} = -DV_\Delta, & \text{for } DT_\Delta < t \leq T_\Delta. \end{cases} \tag{28}$$

In this way, neglecting the resistance $R_g$ ($R_g << \omega_o Lg$), the current ripple $\Delta i_{rp}$ is

$$\Delta i_{rp} = \int_0^{DT_\Delta} \frac{v_{rp}}{L_g} dt = \frac{D(1-D)\Delta V T_\Delta}{L_g}. \tag{29}$$

From (29), the maximum ripple occurs when $D = 0.5$. Additionally, $\Delta V$ depends on the number of levels generated by the converter and the dc-link voltage. For the UHMC with $v^*_{Ct} = 3v^*_{Ch}$, $\Delta V = \frac{2v^*_{Ct}}{9}$. Hence, the minimum inductance is

$$L_{g_{\min}} = \frac{\Delta V}{4\Delta i_{\max} f_\Delta} = \frac{v^*_{Ct}}{18\Delta i_{\max} f_\Delta} \tag{30}$$

where $\Delta i_{\max}$ is the maximum grid currents ripple in amperes.

TABLE II
Parameters Considered for Comparisons

| Parameter | Value | Description |
|---|---|---|
| $E_g$ | 220 V | Grid voltage RMS value |
| $P_l$ | 5 kW | Load power |
| $f_o$ | 60 Hz | Grid fundamental frequency |
| $v_{Ct}$ | 490 V | Three-leg cell DC-link voltage (UHMC and HMC) |
| $v_{Cj}$ | 163 V | H-bridge cells DC-link voltages (UHMC and HMC) |
| $v_C$ | 540 V | DC-link voltages of TLC, NPCC and FCC |

## VII. Comparative Analysis

In this section, the proposed UHMC is compared with the conventional converters shown in Fig. 1 in terms of number, rating, and size of their components, harmonic distortion, semiconductor losses, and average switching frequency. The considered parameters are shown in Table II. In addition, the considered balancing technique is compared with conventional ones.

### A. Number, Rating, and Size of Components

The converters HMC and UHMC present floating H-bridges series connected to the three-leg cell. This allows these converters to operate with lower load voltages than the NPCC, FCC, and TLC. Considering the amplitude of the required voltage at grid side $V^*_g$, the minimum dc-link voltage for NPCC, FCC. and TLC is $v^*_{C\ \min} = \sqrt{3}V^*_g = 1.732V^*_g$. On the other hand, considering MMI 0.66, the minimum load voltage of UHMC and HMC is, from (21)

$$v^*_{Ct\ \min} = \frac{3\sqrt{(3)}}{5 \cdot 0.66} V^*_g = 1.575V^*_g. \tag{31}$$

This allows the UHMC and HMC to reduce 9% of the load voltage. Then, for $V^*_g = 220\sqrt{2}$, $v^*_{Ct\ \min} = 490$ V in these topologies. However, for NPCC, FCC, and TLC, $v^*_{C\ \min} = 540$ V. These dc-link voltages make conventional and proposed converters to operate with MMI and they were considered on the

TABLE III
NUMBER AND REVERSE BLOCKING VOLTAGES OF SEMICONDUCTOR DEVICES

| Topology | Device | Number | Voltage (p.u) |
|---|---|---|---|
| TLC | IGBTs | 6 | 1.0 |
| NPCC | IGBTs | 12 | 0.5 |
| | Clamping Diodes | 6 | 0.5 |
| FCC | IGBTs | 12 | 0.5 |
| HMC | IGBTs | 12 | 0.3 |
| | IGBTs | 6 | 0.91 |
| UHMC | IGBTs | 12 | 0.3 |
| | IGBTs | 3 | 0.91 |
| | Diodes | 3 | 0.91 |

1 p.u. = 540 V.

TABLE IV
NUMBER, RATING, AND SIZE OF PASSIVE COMPONENTS

| Top. | Comp. | N° | Rat. (p.u) | Size |
|---|---|---|---|---|
| TLC | Ind. | 3 | 1.0 | $\frac{v_C}{6\Delta i_{max} f_\Delta} = 9mH$ |
| | Cap. | 1 | 1.0 | $\frac{P_g}{f_o {v_C}^2} = 286\mu F$ |
| NPCC | Ind. | 3 | 1.0 | $\frac{v_C}{12\Delta i_{max} f_\Delta} = 4.5mH$ |
| | Cap. | 2 | 0.5 | $\frac{4P_g}{f_o {v_C}^2} = 1.14mF$ |
| FCC | Ind. | 3 | 1.0 | $\frac{v_C}{12\Delta i_{max} f_\Delta} = 4.5mH$ |
| | Cap. | 1 | 1.0 | $\frac{2P_g}{f_o {v^*_{Ct}}^2} = 572\mu F$ |
| | Fly.C. | 3 | 0.5 | $\frac{I_g}{2\Delta v_{Cj_{max}} f_\Delta} = 40\mu F$ |
| HMC | Ind. | 3 | 1.0 | $\frac{v^*_{Ct}}{18\Delta i_{max} f_\Delta} = 2.72mH$ |
| and | Cap. | 1 | 0.91 | $\frac{P_g}{f_o {v^*_{Ct}}^2} = 347\mu F$ |
| UHMC | Flo.C. | 3 | 0.3 | $\frac{I_g}{2\pi f_o \Delta v_{Cj_{max}}} = 3.34mF$ |

1 p.u. = 540 V and 1 p.u. = 10.71 A.

comparisons. Table III shows the number and reverse blocking voltage of semiconductor devices for proposed and conventional converters. For FCC and NPCC, the reverse voltage is half of the total dc-link voltage. For TLC, HMC, and UHMC, the reverse voltage is equal to the dc-link voltage of the cell.

Table IV specifies, for each passive component, the number (N°), size, and rating (Rat.) for proposed and conventional topologies, considering carriers frequency $f_\Delta = 10$ kHz. For inductors, the rating specifies the peak current, and for the capacitors, the dc-link voltage. The inductors (Ind.) were designed for same maximum peak-to-peak current ripple $\Delta i_{\max} = 1$ A. Following the same method presented in Section VI-C, for NPCC and FCC, $\Delta V = \frac{v_C}{3}$ and for TLC, $\Delta V = \frac{2v_C}{3}$. The main dc-link capacitors (Cap.) were designed with the same method presented in Section VI-B. These capacitors were then designed such that the *RC* time constant of the dc-link was six times the fundamental period of voltage ripple. TLC presented ripple frequency of $6f_o$ [23]. NPCC and FCC presented ripple of $3f_o$ [24], [25]. Also, NPCC has two series-connected capacitors, then each one must have the double of capacitance of the resultant capacitor. The flying capacitors (Fly.C.) of the FCC and floating capacitors (Flo.C.) of UHMC and HMC have been designed considering maximum voltage ripple of 5%. The design of flying capacitors can be found in [26].

TABLE V
HARMONIC DISTORTION COMPARISON

| | THD | WTHD | $N_{lvl}$ | MMI |
|---|---|---|---|---|
| TLC | 8.15% | 0.4576% | 2 | 1.0 |
| NPCC | 3.94% | 0.2018% | 3 | 1.0 |
| FCC | 3.94% | 0.2003% | 3 | 1.0 |
| HMC | 2.83% | 0.1574% | 6 | 0.657 |
| UHMC | 2.88% | 0.1520% | 6 | 0.66 |

Grid current THD and converter voltage WTHD for $f_\Delta = 10$ kHz, number of levels per phase $N_{\text{lvl}}$, and MMI.

### B. Harmonic Distortion

The harmonic distortion is here evaluated by the total harmonic distortion (THD) of grid currents ($i_{gj}$) and weighted THD (WTHD) of converter voltages ($v_{gj}$). These were obtained via simulations and calculated as defined in [17], considering PWM carriers frequency $f_\Delta = 10$ kHz and filter inductors $L_g = 4$ mH. The results are summarized in Table V. It also shows the number of levels per phase ($N_{\text{lvl}}$) and the MMI.

The currents THD of the UHMC was 65% lower than in the TLC, 27% lower than in the NPCC and FCC, and 2% higher than in the HMC. Considering the converter voltages WTHD, the UHMC presented the best performance among the studied converters. UHMC presented WTHD 67%, 25%, 25%, and 3% lower compared with the TLC, NPCC, FCC, and HMC, respectively.

Although the proposed converter presents a limitation of modulation index (MMI = 0.66), it generates more levels ($N_{\text{lvl}}$) at its AC voltages than the conventional NPCC, FCC, and TLC. For example, if the UHMC operates with $m_a = 0.6$, it still fully generates four levels at $v_{rj}$, while NPCC, FCC, and TLC operating with unitary modulation index generate three, three, and two levels, respectively. Compared with the HMC, the UHMC generates same number of levels and presents similar modulation index limitation. These features can be observed in Fig. 12, which shows the resultant voltage $v_{g1}$ for proposed and conventional converters. It can be seen that the TLC [see Fig. 12(a)] and NPCC and FCC [see Fig. 12(b)] presented fewer number of levels and larger voltage steps than the UHMC [see Fig. 12(d)]. Additionally, UHMC and HMC [see Fig. 12(c)] developed similar voltage waveforms.

### C. Semiconductor Losses

Semiconductor losses were estimated from simulations considering the losses model and procedure described in [22]. It includes switching losses ($P_{\text{sw}}$) and conduction losses ($P_{cd}$). The switching losses include the transistor turn-ON and turn-OFF losses and the antiparallel diode turn-OFF losses. Besides, $P_{cd}$ considers both transistor and antiparallel diode. Hence, the total losses were calculated by $P_{\text{loss}} = P_{\text{sw}} + P_{cd}$. In addition, to

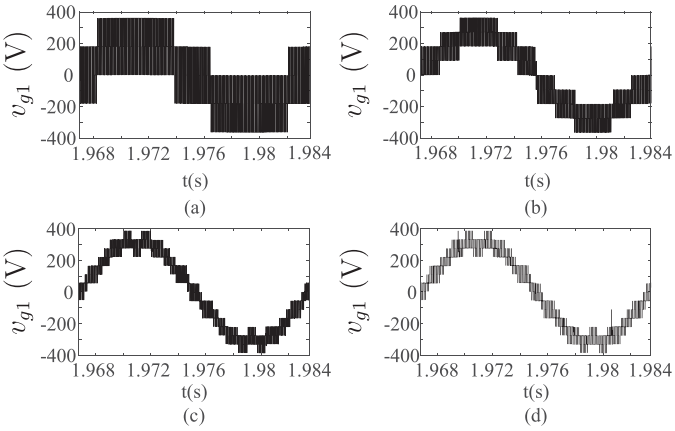


Fig. 12. Resultant voltage $v_{g1}$ for conventional and proposed topologies. (a) TLC. (b) NPCC and FCC. (c) HMC. (d) UHMC.

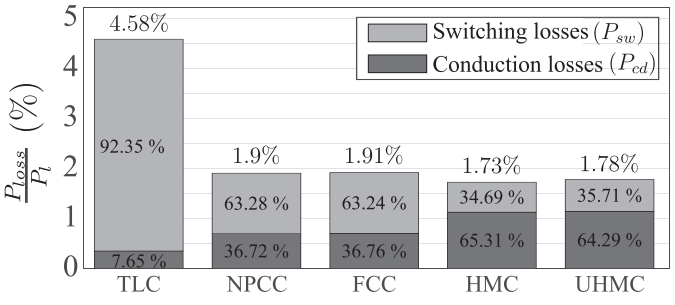


Fig. 13. Semiconductor losses $P_{\text{loss}}$ normalized by load power $P_l = 5$ kW for currents THD $= 5\%$.

TABLE VI
AVERAGE SWITCHING FREQUENCY ($f_{\text{AVG}}$) COMPARISON, NUMBER OF SWITCHES PER PHASE ($N_{\text{SW}}$), AND CARRIERS FREQUENCY $f_\Delta$

| | | $f_\Delta = 10$ kHz | THD = 5% | |
|---|---|---|---|---|
| Top. | $N_{sw}$ | $f_{avg}$ (kHz) | $f_\Delta$ (kHz) | $f_{avg}$ (kHz) |
| TLC | 2 | 8.9 | 16.67 | 14.11 |
| NPCC | 4 | 4.93 | 7.69 | 3.85 |
| FCC | 4 | 4.93 | 7.69 | 3.85 |
| HMC | 6 | 1.2 / 5.5* | 5.26 | 0.61 / 2.91* |
| UHMC | 6 | 1.11 / 5.52* | 5.71 | 0.62 / 3.13* |

*Average frequency of three-leg cell/H-bridges.

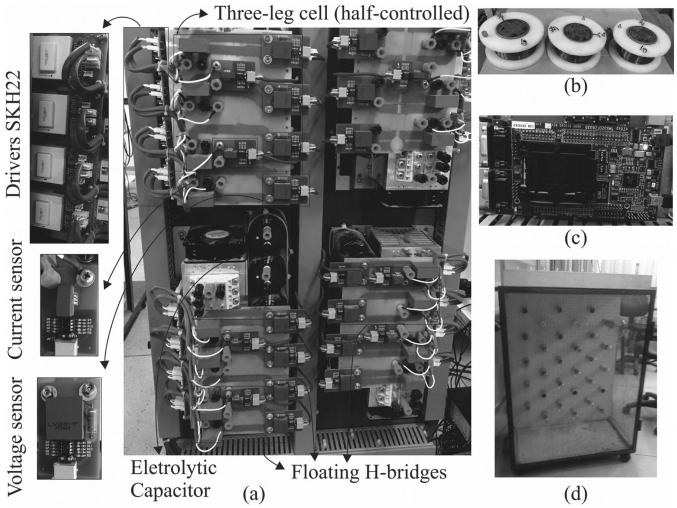


Fig. 14. Experimental setup. (a) Converter modules. (b) Inductors. (c) DSP TMS320F28335 board. (d) Resistive load.

allow a fair comparison among different topologies, all converters operated meeting same currents THD (5%). To do so, the same filter inductor was considered ($L_g = 4$ mH) and the PWM carriers frequency ($f_\Delta$) of each converter was adjusted. The losses results are summarized in Fig. 13.

The total losses in the UHMC were 74%, 6% and 6% lower comparing with TLC, NPCC and FCC, respectively. Compared with the HMC, the losses in the UHMC were 3% higher.

Since there are no parallel cells in the considered converters, the conduction losses are proportional to the number of switches. The proposed converter has more switches than the TLC, NPCC, and FCC, hence the conduction losses of UHMC were higher. However, this is compensated by the reduction in the switching losses. The switching losses ($P_{\text{sw}}$) depend on the dc-link voltage of each cell and the number of commutations. To clarify the behavior of switching losses, the average switching frequency of converters is analyzed as follows.

### *D. Average Switching Frequency*

The average switching frequencies $f_{\text{avg}}$ were obtained from simulations and calculated by $f_{\text{avg}} = \frac{N_{\text{com}}}{T_o N_{sw}}$, where $N_{\text{com}}$ is the total number of commutations of one converter/cell in one fundamental grid period $T_o = \frac{1}{f_o}$ and $N_{\text{sw}}$ is the number of switches per phase of the considered converter/cell. Table VI shows $f_{\text{avg}}$ of proposed and conventional converters for both constant carriers frequency $f_\Delta = 10$ kHz and same currents THD (5%). For HMC and UHMC, two values of $f_{\text{avg}}$ are shown, the first refers to the three-leg cell and the second to the H-bridge cells, because their dc-link voltages are different, then each one contributes in a different way for the switching losses.

For the UHMC, the higher voltage three-leg cell presented lower average switching frequency, and the lower voltage H-bridge cells presented higher average switching frequencies. This feature contributed to the reduction of the switching losses, since the higher voltage legs would generate higher losses compared with the lower voltage cells for same average switching frequency. It was also observed in the HMC.

Compared with the TLC, all switches of UHMC presented lower average switching frequency. Considering that the switches of the UHMC were operating also with lower voltages, the UHMC presented lower switching losses than the TLC, which is observed in the results of Fig. 13.

Moreover, to make the current THD equal in all considered converters, the UHMC operated with carriers frequency 65%, 24% and 24% lower compared with TLC, NPCC and FCC, respectively. This was possible because for the same carriers frequency, the UHMC generated lower harmonic distortion than the NPCC, FCC and TLC. This allowed a further reduction in the average switching frequencies of UHMC. In this scenario, both

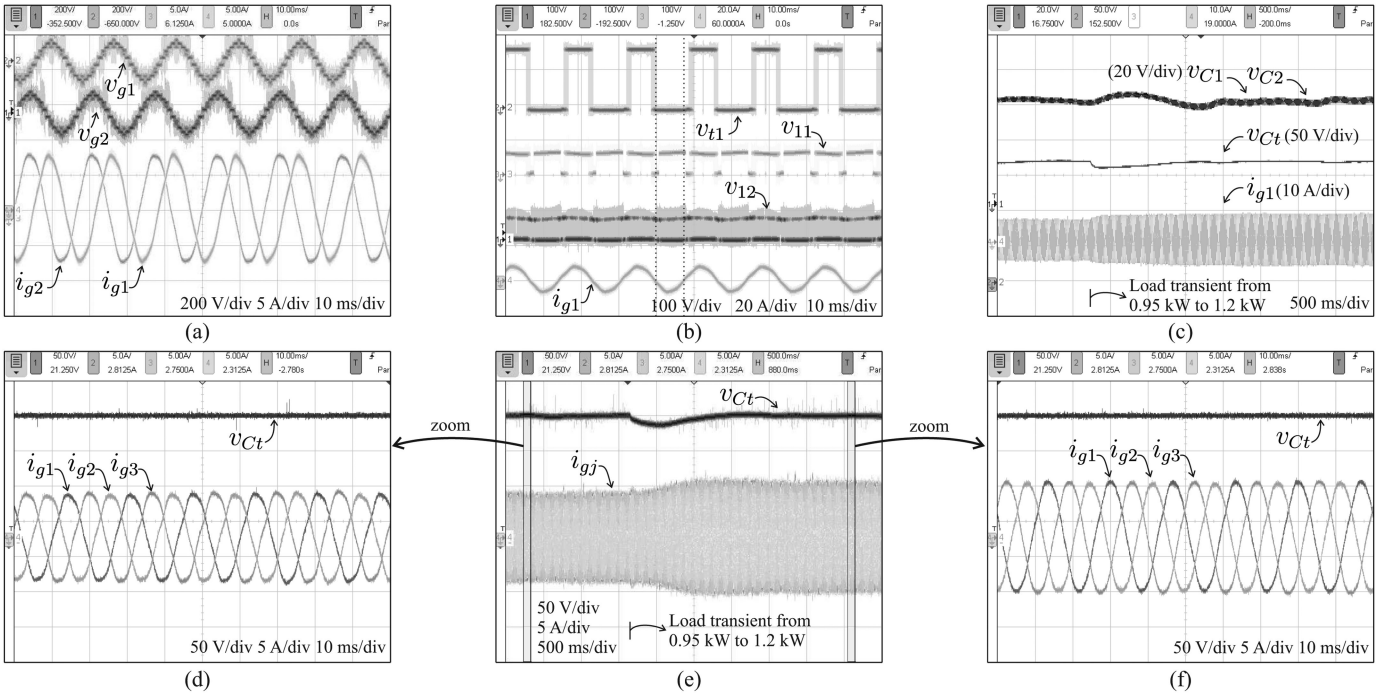


Fig. 15. Experimental results. Converter resultant voltages ($v_{g1}$ and $v_{g2}$), grid currents ($i_{g1}$, $i_{g2}$, and $i_{g3}$), pole voltages ($v_{t1}$, $v_{11}$, and $v_{12}$) and dc-link voltages ($v_{C1}$, $v_{C2}$, $v_{C3}$, and $v_{Ct}$). (a) Steady-state operation. (b) Pole voltages and current in the steady-state operation. (c) Impact of transient on floating-capacitor voltages. (d) Zoomed view before transient. (e) Power transient from $P_g = 0.95$ kW to $P_g = 1.2$ kW. (f) Zoomed view after transient.

H-bridge and three-leg cells of UHMC presented lower average switching frequency than in the NPCC and FCC.

### *E. Comparison of Balancing Techniques*

This section compares conventional techniques to control dc-link voltages of floating H-bridges [11], [12], [14], [15] with the one proposed in this article, considering the application of these techniques to the proposed UHMC.

In [12], the main converter commutes at low frequency and the floating H-bridges only generate harmonic content with an LSPWM. Also, in [14], LSPWM is applied and the control is performed choosing the redundant switching states. Neither of these techniques can be applied to the proposed UHMC in the operation discussed in this article ($v^*_{Ct} = 3v^*_{Ch}$). In this operation, there are no redundancies in the voltage generation of each phase ($v_{rj}$) [14] and the three-leg cell cannot operate with low frequency in the complete cycle [12].

The control strategy in [11] returns the reference voltages of each converter cell, making it not possible to apply either LSPWM or SVPWM. The PWM in this case is solved with a phase-shifted PWM. The PWM of the three-leg half-controlled cell would operate independently from the H-bridge cells. In this case, when two of the grid currents are simultaneously negative, two legs of the three-leg cell would be blocked by the diodes. Hence, such a cell would not be able to synthesize properly the average voltage in all three phases during half cycle. This would jeopardize the waveform quality of voltages and currents. In addition, as the H-bridges would not have loads connected to their dc links, and their reference voltages would be practically zero. These features would greatly increase the average switching frequency of both H-bridges and three-leg cell, therefore increasing converter losses. Additionally, the voltage generation capability would be limited by the three-leg cell resulting in maximum modulation index MMI = 0.6. These features demonstrate that the solution proposed in [11] is not competitive if applied to the proposed converter.

In [15], Méllo *et al.* applied n SVPWM. In each PWM period, it evaluates all redundant vectors that optimize the voltage generation and chooses the ones that respect the diodes conduction states and better contribute to the control of the H-bridges. Naturally, it optimizes the converter operation at the cost of using a complex modulation technique and high computational effort. Performing a simulation applying this method to UHMC, it operated with MMI=0.66 and WTHD=0.154%. Comparing with Table V, the proposed technique achieves similar voltage generation capability and harmonic distortion with reduced complexity.

## VIII. Experimental Results

Experimental results were performed through a down-scaled prototype for proof concept. Fig. 14 shows the experimental setup. The power converters are based on SKM50GB123D IGBT modules connected with SKHI22 drivers from SEMIKRON. Control and PWM modulation were accomplished by DSP TMS320F28335. In the setup, the upper switches of the three-leg cell had their transistors disabled, to make these legs half controlled. The main experimental setup

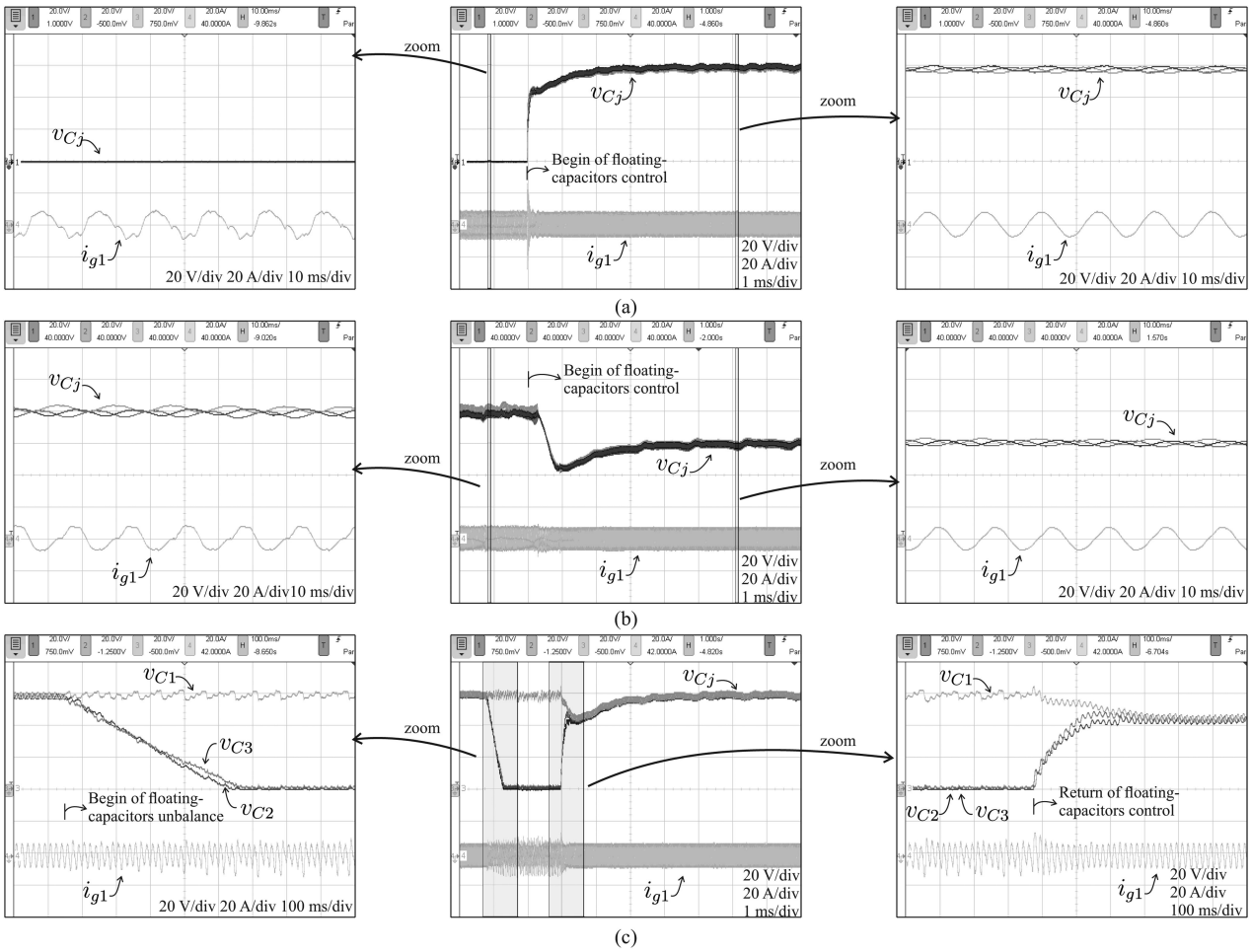


Fig. 16. Experimental results. Validation of floating-capacitor control. Grid current ($i_{g1}$) and floating-capacitor voltages ($v_{C1}$, $v_{C2}$, and $v_{C3}$). (a) Initialization of floating capacitors. (b) Control of floating capacitors with initial overvoltage. (c) Control of floating capacitors with initial unbalanced voltages.

TABLE VII
PARAMETERS CONSIDERED FOR EXPERIMENTS

| Parameter | Value | Description |
|---|---|---|
| $L_g$ | 7 mH | Inductance of filter inductor |
| $R_g$ | 0.4 Ω | Resistance of filter inductor |
| $E_g$ | 110 V | Grid voltage peak value |
| $P_g$ | 1.2 kW | Total converter power |
| $f_o$ | 60 Hz | Grid fundamental frequency |
| $v^*_{Ct}$ | 180 V | Three-leg cell DC-link reference voltage |
| $v^*_{Ch}$ | 60 V | H-bridge cells DC-link reference voltage |
| $C_t$ | 16.45 mF | Three-leg cell DC-link capacitor |
| $C_h$ | 9.4 mF | H-bridge cells DC-link capacitor |
| $\frac{\Delta_C}{v^*_{Ch}}$ | 30% | Hysteresis band |
| $k_{pC}$ | 0.00002 | Proportional gain of $R_C$ |
| $k_{iC}$ | 0.00002 | Integral gain of $R_C$ |
| $k_{pi}$ | 0.03 | Proportional gain of $R_{g1}$ and $R_{g2}$ |
| $k_{ii}$ | 1500.0 | Integral gain of $R_{g1}$ and $R_{g2}$ |
| $k_{pH}$ | 0.0002 | Proportional gain of $R_H$ |
| $k_{iH}$ | 0.0002 | Integral gain of $R_H$ |

parameters are listed in Table VII and the experimental outcomes are presented in Figs. 15 and 16.

Steady-state results are shown in Fig. 15(a) and (b). Fig. 15(a) presents the converter resultant voltages and grid currents. The multilevel feature is evident, which reflects in nearly sinusoidal currents, and converter voltages are synchronized with their currents due to the unidirectional operation. In Fig. 15(b), it is possible to observe that $q_{tj}$ and $q_{1j}$ did not commute in most of the cycle and $v_{12}$ commuted every PWM cycle, which is expected from Table I. Also, it is possible to observe with the vertical dashed lines that for $i_{g1} < 0$, $v_{t1} = -90$ V, because the diodes of the three-leg cell blocked for negative current and $q_{t1} = 0$.

Fig. 15(c)–(f) presents results of a load power transient from $P_g = 0.95$ kW to $P_g = 1.2$ kW. The load transient caused a peak-to-peak voltage oscillation of the floating capacitors of 12% [see Fig. 15(c)] and a maximum voltage drop on the load of 7% [see Fig. 15(e)], returning to its reference value in 1.2 s. In steady state, the floating capacitors presented $\Delta v_{Cj} = 3.2$ V of peak-to-peak voltage oscillation, i.e., 5.3%.

The control of floating capacitors was validated with the results of Fig. 16. The control is observed for different initial voltage conditions: all capacitors discharged [see Fig. 16(a)], all capacitors overcharged [see Fig. 16(b)], and unbalanced voltages [see Fig. 16(c)]. Zoomed views are shown on the left and right screens. Once the control is activated, the capacitors

reach their reference value (60 V) in about 3 s. Smaller values of capacitance would generate faster transient responses, although it would cause higher steady-state voltage oscillation. Also, when capacitor voltages are different from their reference value, the grid current $i_{g1}$ becomes distorted since the converter is not able to generate properly their voltages. However, when control reaches steady state, the quality of current waveform is restored.

## IX. Conclusion

This article proposed a hybrid asymmetric unidirectional rectifier with a half-controlled three-leg cell series-connected with floating H-bridge cells (UHMC). A modification in the common-mode voltage calculation has been proposed to adapt the conventional strategies to the UHMC. The control of floating capacitors has been detailed as well as the mechanisms of capacitor charging and discharging. The proposed voltage balance control manipulates the common-mode voltage by means of the apportioning factor $\mu^*$, allowing to optimize the voltage generation with LSPWM. Converter model, PWM, and control strategy have been presented as well as the design of passive elements.

The UHMC presented better performance in terms of harmonic distortion and semiconductor losses compared to the conventional solutions, TLC, NPCC, and FCC. Besides that, the UHMC operated with semiconductor devices with reduced voltage rating and reduced switching frequency. Compared with HMC, the UHMC presented similar performance with reduced number of controlled switches.

## References


[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] D. Mukherjee and D. Kastha, "A reduced switch hybrid multilevel unidirectional rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2070–2081, Mar. 2019.

[4] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[5] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[6] J. Pereda and J. Dixon, "Cascaded multilevel converters: Optimal asymmetries and floating capacitor control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4784–4793, Nov. 2013.

[7] H. Weng *et al.*, "A four-level converter with optimized switching patterns for high-speed electric drives," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 1585–1591.

[8] A. M. Maciel, C. B. Jacobina, V. B. Melo, E. C. dos Santos, and E. L. L. Fabrcio, "Three-phase shunt active power filter based on the interconnection of single-phase and three-phase converters," in *Proc. Brazilian Power Electron. Conf.*, Oct. 2013, pp. 1239–1244.

[9] C. B. Jacobina, V. F. M. B. Melo, N. Rocha, and E. R. C. da Silva, "Six-phase machine conversion system with three- and single-phase series converters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3846–3856, Nov. 2014.

[10] A. Felinto, C. B. Jacobina, E. L. L. Fabricio, V. F. M. B. Melo, and J. P. R. A. Mello, "Investigation of power rectifier under non-sinusoidal input based on hybrid multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 2779–2786.

[11] Y. Su, P. Wu, and P. Cheng, "Design and evaluation of a control scheme for the hybrid cascaded converter in grid applications," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3139–3147, Mar. 2020.

[12] Y. Zhang, G. Adam, S. Finney, and B. Williams, "Improved pulse-width modulation and capacitor voltage-balancing strategy for a scalable hybrid cascaded multilevel converter," *IET Power Electron.*, vol. 6, no. 4, pp. 783–797, Apr. 2013.

[13] H. Liu, L. M. Tolbert, S. Khomfoi, B. Ozpineci, and Z. Du, "Hybrid cascaded multilevel inverter with pwm control method," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 162–166.

[14] K. Sivakumar, A. Das, R. Ramchand, C. Patel, and K. Gopakumar, "A hybrid multilevel inverter topology for an open-end winding induction-motor drive using two-level inverters in series with a capacitor-fed h-bridge cell," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3707–3714, Nov. 2010.

[15] J. P. R. A. Méllo, C. B. Jacobina, and M. B. de Rossiter Corrêa, "Three-phase unidirectional rectifiers with open-end source and cascaded floating capacitor h-bridges," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2534–2549, May 2018.

[16] V. Blasko, "Analysis of a hybrid pwm based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May 1997.

[17] A. C. N. Maia, C. B. Jacobina, N. B. de Freitas, and M. A. Vitorino, "Investigation of three-phase ac-dc-ac multilevel nine-leg converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4156–4169, Sep. 2016.

[18] Y. Wang, D. Panda, T. A. Lipo, and D. Pan, "Open-winding power conversion systems fed by half-controlled converters," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2427–2436, May 2013.

[19] R. P. R. de Sousa, C. B. Jacobina, F. A. d. C. Bahia, and L. de Macedo Barros, "Open-end unidirectional topologies with reduced controlled switch count," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2833–2844, May 2019.

[20] R. M. S. Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug. 2008.

[21] C. B. Jacobina, M. B. d. Correa, T. M. Oliveira, A. M. N. Lima, and E. R. C. da Silva, "Current control of unbalanced electrical systems," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 517–525, Jun. 2001.

[22] E. L. L. Fabricio, S. C. S. Júnior, C. B. Jacobina, and M. B. de Rossiter Corrêa, "Analysis of main topologies of shunt active power filters applied to four-wire systems," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2100–2112, Mar. 2018.

[23] H. Qi, Y. Wu, and Y. Bi, "The main parameters design based on three-phase voltage source PWM rectifier of voltage oriented control," in *Proc. Int. Conf. Inf. Sci., Electron. Elect. Eng.*, 2014, vol. 1, pp. 10–13.

[24] M. Hammami, R. Mandrioli, and G. Grandi, "Capacitor voltage switching ripple in three-phase three-level neutral point clamped inverters with sinusoidal carrier-based PWM," in *Proc. Int. Symp. Ind. Electron.*, 2018, pp. 1–6.

[25] M. Hammami, M. Vujacic, and G. Grandi, "DC-link current and voltage ripple harmonics in three-phase three-level flying capacitor inverters with sinusoidal carrier-based PWM," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2018, pp. 664–669.

[26] J. A. Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 50–61, 2019.


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