Turn-ON Delay Based Real-Time Junction Temperature Measurement for SiC MOSFETs With Aging Compensation

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***Abstract*—Online junction temperature (T_j) measurement enables robust power converter operations by providing overtemperature protection and condition monitoring of the power devices. For SiC MOSFETs, the real-time T_j information is especially critical as limited field data are available regarding the reliability. In this article, utilizing the turn-ON delay time as temperature sensitive electrical parameter, an online T_j measurement is realized through an intelligent gate drive. Specifically, the turn-ON delay time is translated into the pulsewidth of a digital signal through the conditioning/logic circuits. During T_j measurements, the adjustable gate resistance circuit is activated to improve the measurement sensitivity beyond 600 ps/°C. Using the high-resolution capture module (300-ps resolution) in the system microcontroller, this pulsewidth is measured and then converted to junction temperature with a resolution of <0.5 °C. A prototype is built to validate the online T_j measurement method. The switching test results show that the circuit is able to precisely measure $T_{d,\mathrm{on}}$ and offers a good linearity/sensitivity for T_j estimation. In the continuous operation, the junction temperature of a decapsulated device using an infrared camera and T_j obtained from the circuit match well with <1 °C difference under various operating conditions. In addition, the gate-oxide degradation's impact on $T_{d,\mathrm{on}}$ is considered for SiC MOSFETs, and an aging compensation scheme is discussed to maintain the measurement accuracy throughout the device's lifetime. It is shown that the proposed circuit provides an accurate real-time T_j measurement for SiC MOSFETs, which can be deployed to improve the power converters' reliability.**

***Index Terms*—Junction temperature, reliability, SiC MOSFETs, temperature sensitive electrical parameters (TSEPs).**

I. Introduction

POWER devices are one of the most essential components in power converters, and the safe operation of these devices is critical for robust and reliable power electronics converter systems. In the end products, the temperature variation and overload transient can trigger long-term reliability and short-term overtemperature issues in the devices, thus negatively affect the system robustness [1]–[5]. In order to minimize these risks, online junction temperature measurement of the power device is necessary especially for safety and mission-critical applications. The awareness of the device junction temperature enables overtemperature management, device condition monitoring, and device lifetime extension [6]–[8]. For the emerging silicon carbide (SiC) MOSFETs with low ON-resistance and switching loss [9]–[12], the real-time junction temperature measurement is especially valuable as limited field data are available regarding their reliability.

Among the various online junction temperature T_j measurement methods for SiC MOSFETs, the temperature sensitive electrical parameters (TSEPs) are widely adopted through cost-effective plug-in circuits, and they can provide an indirect indication of the device's junction temperature [13]. Compared to the direct methods using on-chip sensors [14] or optical sensors embedded into the package [15], [16], most TSEPs-based T_j measurement methods are noninvasive and do not require device or package modifications. This is highly valuable for practical applications as these simple plug-in circuits can be easily added or integrated to existing systems.

Previously, various TSEPs have been utilized for real-time T_j measurement in SiC MOSFETs, as summarized in Table I. Relying on the temperature coefficients of the channel resistance and drift region resistance, the ON-resistance of the SiC MOSFETs can be used for T_j estimation. Online measurement can be realized by measuring the device's current/voltage simultaneously [17] or measuring the time constant of the current ringing decay [18]. However, due to the competition effect of the different temperature coefficients in the channel resistance and drift-region resistance [19], [20], the ON-resistance change over T_j is nonlinear and some devices show nonmonolithic characteristic [21], [22]. To improve the linearity, the turn-ON *di/dt* rate can be used for T_j estimation in SiC MOSFETs [17], [23]. Real-time measurement is possible by detecting the peak voltage across the source parasitic inductance during turn-ON. The sensitivity can be increased by slowing down the turn-ON process [23]. Similarly, the turn-OFF delay time also has a linear relationship with T_j at a given load current [24]–[26], and the sensitivity

Manuscript received February 26, 2020; revised June 5, 2020; accepted July 9, 2020. Date of publication July 14, 2020; date of current version September 22, 2020. This work was supported in part by the National Science Foundation under Award 1454311, and in part by the Semiconductor Research Corporation (SRC)/Texas Analog Center of Excellence (TxACE) under the Task ID 2712.026. Recommended for publication by Associate Editor J. Popovic-Gerber. *(Corresponding author: Fei Yang.)*

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This article has supplementary downloadable material available at https://ieeexplore.ieee.org, provided by the authors.

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Digital Object Identifier 10.1109/TPEL.2020.3009202

TABLE I
COMPARISON OF TSEPs FOR ONLINE JUNCTION TEMPERATURE MEASUREMENT IN SiC MOSFETs

TSEP	Linearity	Sensitivity	Load Dependency	Aging's Impact Factor
on-resistance [17], [18]	not good	low	yes	gate oxide + package degradation
turn-on *di/dt* [17], [23]	medium	high at large R_g	yes	gate oxide + package degradation
turn-off delay [24]–[26]	good	high at large R_g	yes	gate oxide + package degradation
threshold voltage [17]	good	low	no	gate oxide degradation
internal R_g [28]–[30]	depends on the gate design		no	unknown
turn-on delay [31], [32]	good	high at large R_g	no	gate oxide degradation

can be improved by increasing the turn-OFF gate resistance with intelligent gate drive circuits [26]. However, the TSEPs like ON-resistance, turn-ON *di/dt,* and turn-OFF delay time are load dependent. As the load current changes, the calibration curve also shifts. Hence, a complicated mapping is required for online T_j estimation.

To address the load dependence, other TSEPs like threshold voltage, internal gate resistance, and turn-ON delay time are considered as well. Specifically, the threshold voltage has decent linearity and online measurement is possible by sensing the gate voltage at the instance the device starts to conduct the load current [17]. Considering the low sensitivity of $V_{\rm th}$ over T_j and the fast switching transient, an accurate and fast analog-to-digital converter (ADC) is required. However, for high-voltage SiC MOSFETs with an isolation barrier between the power stage and control unit, even the state-of-the-art-isolated ADCs fail to meet the accuracy and speed requirements simultaneously [27]. Thus, online measurement becomes unpractical. Relying on the temperature coefficient of the device's internal gate resistance, the peak gate current during the turn-ON delay period can also be used for T_j measurement in SiC MOSFETs [28]–[30]. Online measurement can be realized with the peak gate current detection circuit. However, as discussed in [30], the linearity and sensitivity of this method highly depend on the gate metallization material, gate layout, and fabrication process. Consequently, this T_j measurement method has stringent requirements on the device manufacturer and is limited to certain SiC MOSFETs with controlled gate designs. Based on $V_{\rm th}$ versus T_j relationship, the turn-ON delay time is another good TSEP. Utilizing the parasitic inductance in the power loop, the turn-ON delay time is measured and used for T_j measurement in Si MOSFET [31]. Good linearity is observed, and high sensitivity can be achieved by slowing down the switching transient [31]. Recently, it is validated in SiC MOSFETs as well: the turn-ON delay time is measured when a gate impulse is injected, and a good linearity is observed from the oscilloscope measurement results [32].

Briefly, the turn-ON delay time is a promising TSEP with good linearity, sensitivity, and is not affected by the load current. Nonetheless, the circuit design for turn-ON delay time measurement and online implementation are not discussed exhaustively in previous studies. Therefore, the first goal of this article is to develop a turn-ON delay measurement circuit and achieve real-time junction temperature measurement for SiC MOSFETs with minimum impact on the converter's normal operation.

In addition to linearity and sensitivity of TSEPs, another critical design consideration in online T_j measurement circuit is the measurement consistency over the device's lifetime. In the literature, the existing junction temperature measurement methods assume that the device's parameter remains unchanged over the device aging. However, both the gate oxide and the package element can degrade as the device starts to age, and the TSEPs are affected as summarized in Table I. These issues are more severe in the SiC MOSFETs due to the immaturity in device and package technology [33], [34]. According to [35]–[38], the gate-oxide degradation or instability in SiC MOSFETs can cause TSEPs like ON-resistance, threshold voltage, turn-ON *di/dt*, turn-OFF delay time, and turn-ON delay time to change. As a result, the T_j measurement becomes inaccurate. Meanwhile, the package degradation (i.e., the wire bond liftoff and crack) can also affect the TSEPs such as ON-resistance, turn-ON *di/dt,* and turn-OFF delay time, thus leading to large T_j measurement errors [37]. Hence, targeting at the measurement accuracy and consistency over device aging, the other goal of this article to design an aging compensation scheme for the selected TSEP and ensure an accurate measurement of T_j throughout the device's lifetime.

The rest of this article is organized as follows. In Section II, the turn-ON delay time measurement circuit is introduced utilizing the system-available microcontroller, and the operation for online T_j measurement is discussed. Afterward, the key circuit design considerations for online T_j measurements are discussed. A prototype is built, and the linearity, sensitivity, and accuracy of the real-time junction temperature measurement method are validated experimentally in Section III. In Section IV, the aging compensation scheme together with circuit implementation is briefly discussed considering the gate-oxide degradation in SiC MOSFETs. Finally, the conclusions are given in Section V summarizing the experimental results.

II. JUNCTION TEMPERATURE ESTIMATION BASED ON TURN-ON DELAY TIME MEASUREMENT CIRCUIT

The turn-ON delay time is a TSEP and can be expressed as [39]

$$T_{d,\rm on} = R_g \cdot C_{iss} \cdot \ln\left(\frac{V_{cc} - V_{ee}}{V_{cc} - V_{\rm th}}\right) \tag{1}$$

where R_g is the total gate resistance, C_{iss} is the input junction capacitance, and V_{cc} and V_{ee} are the positive and negative drive voltages of the gate drive circuit, respectively.

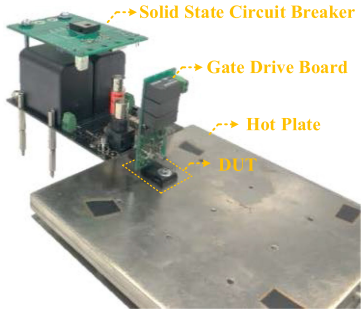

Fig. 1. Real picture of the test setup for switching characteristic evaluation.

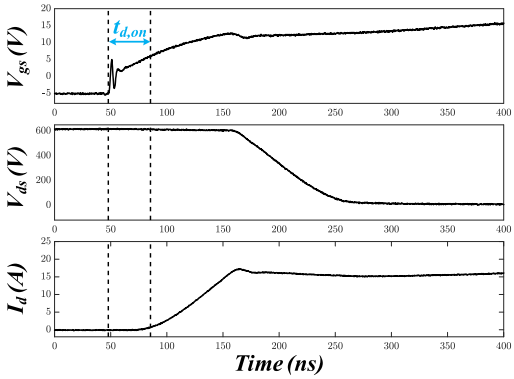

Fig. 2. Illustration of the turn-ON delay time during the switching transient.

A. Validation of Turn-ON Delay Time as TSEP

Ignoring the internal gate resistance's change at different junction temperatures, the variation of turn-ON delay time at different T_j is mainly caused by the temperature effect on $V_{\rm th}$. Therefore, a good linearity is expected. Also, once $V_{\rm th}$ is defined, the turn-ON delay time is load-independent making it suitable for online T_j measurement. In addition, as can be seen from (1), the sensitivity of this TSEP can be adjusted by changing the gate resistance's value. To validate these benefits, a double-pulse test (DPT) circuit is built, and $T_{d,\rm on}$ of a commercial SiC MOSFET is tested at different T_j, as shown in Fig. 1.

In this validation experiment, the device's junction temperature is controlled by the hot plate and calibrated through a TSEP following the procedure discussed in [40]. A negative drive voltage of -5 V is applied, and a commercial gate driver with high common-mode noise immunity is used. From the DPT setup, the device's gate voltage and drain current can be measured. Hence, the turn-ON delay time can be obtained from the oscilloscope measurement and it is defined as the interval from the point when V_{gs} starts increasing to the instance when the mean value of the drain current reaches 200 mA, as indicated in Fig. 2.

Fig. 3 shows the experimental result of $T_{d,\rm on}$ versus T_j at different external gate resistances. The dc-link voltage is at 600 V, and the load current is 20 A. It is observed that as T_j goes up, the threshold voltage drops linearly, and the turn-ON delay time decreases accordingly. Meanwhile, like the behaviors of turn-OFF delay discussed in [25] and [26], the sensitivity of the turn-ON delay time can be improved by increasing the

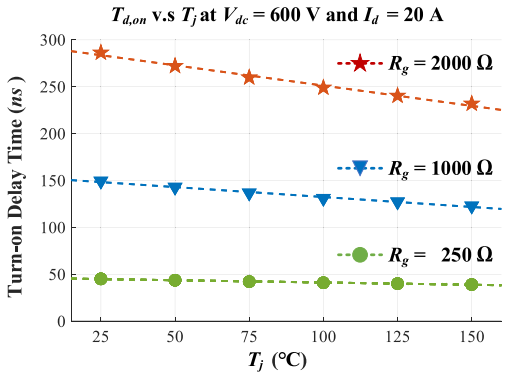

Fig. 3. Turn-ON delay time variation over T_j at different external gate resistance.

TABLE II
LINEAR-FITTED PARAMETERS FOR $T_{d,\rm on}$ VERSUS T_j AT VARIOUS R_g

R_g	Absolute value of the Slope	Values at 0 °C
250 Ω	48.4 ps/°C	46.2 ns
1000 Ω	211.9 ps/°C	153.6 ns
2000 Ω	432.1 ps/°C	294.4 ns

external turn-ON gate resistance. As summarized in Table II, the sensitivity increases significantly from 48.4 to 432.1 ps/°C when the gate resistance is increased.

B. Proposed Turn-ON Delay Measurement Circuit for Online Junction Temperature Measurement

It can be seen from the abovementioned test that the turn-ON delay time varies linearly with the junction temperature, and the sensitivity is adjustable through the change of external gate resistance. However, it is still challenging to measure the short interval accurately, and the gate drive circuit needs to be adapted to be capable of varying the gate resistance. To deal with these issues, a turn-ON delay time measurement circuit is proposed utilizing the system-available microcontroller as discussed in the following section.

Fig. 4 illustrates the circuit diagram of the proposed intelligent gate drive for turn-ON delay time measurement and online junction temperature estimation. Specifically, the starting point of the turn-ON delay period is indicated by the rising edge of the gate voltage. To capture this instant, the gate voltage of the SiC MOSFETs is sensed and compared with a reference. Once the gate voltage starts to rise and hits the reference value, the comparator output changes from low to high as indicated by the orange waveform in Fig. 4. The ending point of the turn-ON delay is represented by the rising edge of the drain current. To obtain this time instant, the common source inductance $L_{\rm cs}$ within the packaged device is utilized as indicated in Fig. 4. This $L_{\rm cs}$ can be the package's parasitic inductance between the kelvin source and power source for 4-pin TO packaged device or power modules [41], [42]. Alternatively, it can be the self-parasitic inductance of the source lead in a 3-pin TO packaged device [43]. When the device starts to commutate the load current, the drain current i_d increases and flows through $L_{\rm cs}$. Consequently,

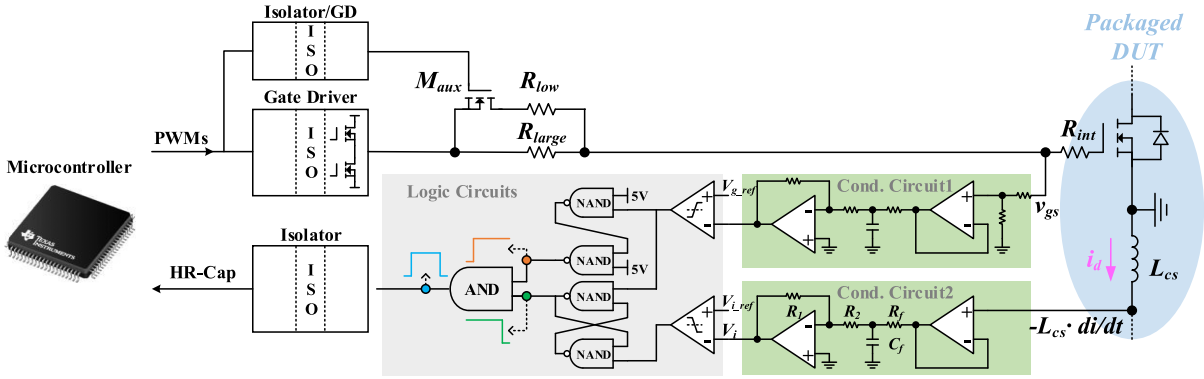

Fig. 4. Circuit diagram of the proposed turn-ON delay time measurement circuit for T_j estimation.

a voltage is generated across it. This $L_{\rm cs} \cdot di_d/dt$ signal is sensed by the conditioning circuit, and detailed circuit designs will be discussed in Section III. By comparing this analog signal with a proper reference value, the current rise stage can be captured. As indicated by the green waveform in Fig. 4, the final current rise edge is indicated by a falling edge at the flip-flop circuit's output. The flip-flop logic circuit (implemented with two NAND gates) is needed to improve the circuit's noise immunity, and the details will be provided in later sections.

These two edge signals (one rising edge capturing the beginning of turn-ON delay and one falling edge representing the end of turn-ON delay period) are then fed to the logic AND chip, and the turn-ON delay time can be represented by the pulsewidth of the output digital signal, as illustrated by the blue waveform in Fig. 4. This digital signal is finally transmitted to the system microcontroller side through the digital isolator with high common-mode noise immunity. The pulsewidth can be calculated in the high-resolution capture (HR-Cap) module of the C2000 microcontroller from Texas Instruments Incorporated. The consistency of the HR-Cap measurements has been validated in our previous work to measure the turn-ON time of SiC MOSFETs [44], [45]. In this design, the turn-ON delay time $T_{d,\rm on}$ can be accurately calculated in the HR-Cap module with a high resolution of 300 ps.

In addition, to ensure the measurement accuracy and sensitivity, a large gate resistance is preferred during the turn-ON delay period as discussed previously. Thus, the gate drive circuit is modified with adjustable gate resistance. In this design, the external gate loop resistance's value can be adjusted by turning ON/OFF the auxiliary switch $M_{\rm aux}$ shown in Fig. 4. Specifically, $M_{\rm aux}$ is ON in normal operations and a low external gate resistance is used to reduce the switching loss of the SiC MOSFETs. To measure the junction temperature of the device, the auxiliary switch is turned OFF, and a large external gate resistance $R_{\rm large}$ is implemented during the measurement period. With large external gate resistance, high sensitivity can be achieved. According to the previous validation test result, the sensitivity is 432.1 ps/°C in the large $R_{g,\rm ext}$ case. Considering the 300-ps resolution in the HR-Cap module, the measurement error of the junction temperature is less than 1 °C. Once the junction temperature is obtained during the turn-ON delay period, the gate resistance immediately switches back to the normal value by turning ON $M_{\rm aux}$. In this way, a low gate resistance value is used in the turn-ON current rise and voltage falling periods where most of the switching loss is generated. Consequently, the switching loss is controlled during the measurement switching cycle, and the converter's normal operation is not affected. Afterward, $M_{\rm aux}$ remains in ON-state (low gate loop resistance) until it receives the next command from the controller for T_j measurement.

Note that though discrete components are used in this design, all the conditioning circuits, logic circuits, and adjustable gate resistance circuits can be integrated into the gate driver IC. For example, a segment drive with adjustable gate resistance can be used to replace the external switch $M_{\rm aux}$ and gate resistors [46], [47]. The integration of all these function circuits helps to reduce the footprint of the gate drive board and simplify the design.

III. Circuit Design Consideration and Experimental Verification

In this section, the key circuit design considerations are discussed and supported with experimental comparison results. Afterward, the circuit is implemented to an SiC MOSFET for online junction temperature measurement. Both double-pulse switching test and continuous operation are conducted, and the circuit's measurement accuracy is validated experimentally.

A. Test Setups

A DPT setup is first utilized to evaluate turn-ON delay time measurement circuit for online T_j estimation. The circuit diagram of the DPT is shown in Fig. 5. The low-side SiC MOSFET is the device under test (DUT), and its drain current, drain-to-source voltage, and gate voltage are measured with high-bandwidth coaxial current sensor and passive voltage probes. An SiC Schottky diode is used in the high side, and the power loop layout is carefully designed to maximize the device's switching performance. Meanwhile, the decoupling capacitors are located close to the switching devices. The proposed online junction temperature measurement circuit is implemented to the low-side SiC MOSFETs together with its gate drive circuit. The controller sends the switching signals to the gate drive circuit and auxiliary

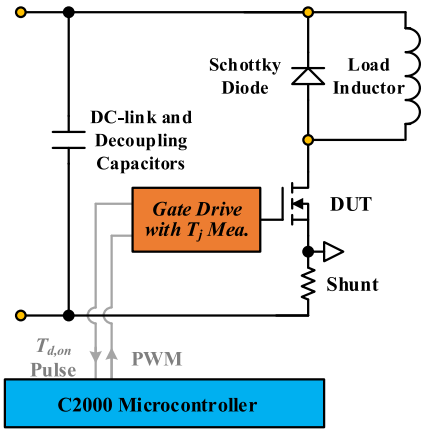

Fig. 5. Circuit diagram of the DPT system.

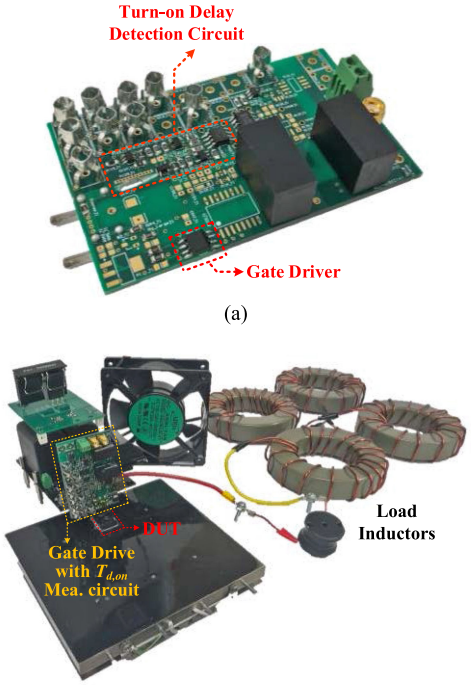

Fig. 6. Photograph of the test setups. (a) Gate drive board with T_j measurement circuit. (b) DPT setup.

switch. On the other hand, the turn-ON delay pulse signal is sent back to the microcontroller's HR-Cap module for calculating $T_{d,\mathrm{on}}$ in real-time as discussed previously.

The picture of the gate drive board is shown in Fig. 6(a). The turn-ON delay time measurement circuits are implemented on the same board. Fig. 6(b) demonstrates the picture of the whole DPT setup. The DUT is attached to the heat sink with a thermal interface material in between for electrical isolation, and the intelligent gate drive with online T_j measurement sits right on top of the SiC MOSFETs. To mitigate the load's impact on the switching transient, five load inductors are connected in series to minimize the parasitic capacitance of the load. A fan is used to cool down the gate drive circuit during the temperature-dependent switching test.

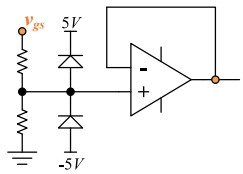

Fig. 7. Circuit diagram of resistor divider and voltage follower.

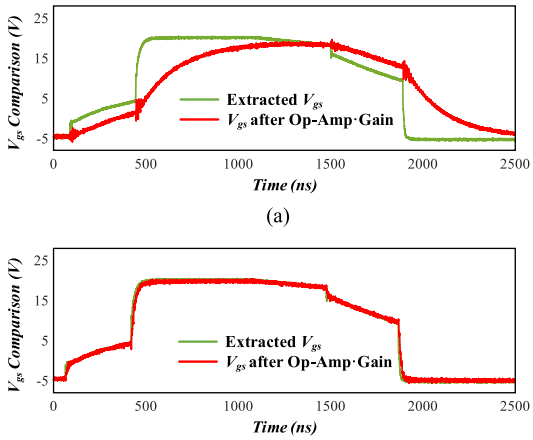

Fig. 8. Experimental comparison results of parasitic capacitance's impact on edge detection. (a) With protection diodes. (b) Without protection diodes.

B. Circuit Design Considerations

To achieve an accurate measurement of the turn-ON delay time and junction temperature, the circuits must be designed properly. Specifically, signal integrity and noise-immunity are two major issues and the corresponding design considerations are discussed as follows.

1) Parasitic Capacitance's Impact on Signal Integrity: In the condition circuits shown in Fig. 4, a resistive divider and voltage follower are used in the first stage to adjust the analog signals (e.g., gate voltage) to an allowable voltage range of the op-amp as indicated in Fig. 7. To protect the op-amp from overvoltage spikes, two voltage limiting diodes are commonly used on the input of the op-amp to clamp the input voltage to the op-amp's supply voltages. However, in normal operations, the input signal is within the supply voltage ($\pm$5 V in this case). Thus, the protection diodes are in the blocking state and act as two junction capacitors. These junction capacitors together with the voltage divider form an *RC* filter and can potentially limit the bandwidth of the circuit. As a result, the output of the op-amp cannot follow the input gate signal timely, and this delay will cause a misalignment in the edge detection for v_{gs}, thus affecting the accuracy of turn-ON delay time measurement.

To verify this analysis, a comparison experiment is carried out on the DPT setup. Specifically, the op-amp's output voltage waveforms are compared with and without the protection diodes, as illustrated in Fig. 8. As can be seen from Fig. 8(a), a low-pass filter effect is noticed with the protection diodes, and a large distortion is observed between the real gate signal and the

op-amp's output. As a result, the edge detection for the start of turn-ON delay is postponed, thus leading to wrong turn-ON delay time measurement. On the contrary, no deviation is found when the protection diodes are removed, as indicated in Fig. 8(b). Therefore, from the circuit design's point of view, it is important to reduce the junction capacitance of the protection diodes and ensure signal integrity. In practice, the protection diodes can be eliminated, and the resistor divider can be properly designed to avoid overvoltages at the op-amp's input.

2) Conditioning Circuit Design for Current Rise Detection: To successfully capture the current rise instant, the gain and response time of the conditioning circuits need to be properly designed. As can be seen from Fig. 4, the conditioning circuit consists of a voltage follower, *RC* filter, and inverting circuit with adjustable gains. The overall transfer function from the drain current i_d to the conditioning circuit's output v_i can be calculated by

$$G_i(s) = \frac{i_d(s)}{v_i(s)} = -L_{\rm cs}\cdot s\cdot 1\cdot \frac{1}{R_fC_f\cdot s+1}\cdot\left(-\frac{R_1}{R_2}\right) = \frac{L_s}{R_fC_f}\cdot\left(\frac{R_1}{R_2}\right)\cdot\frac{1}{1+1/R_fC_f\cdot s}. \quad (2)$$

Since the goal is to capture the current rise instant, the high-frequency performance of $G_i(s)$ is critical. According to (2), the $\frac{1}{1+1/R_fC_f\cdot s}$ term is approaching unity at high frequency, and the high-frequency gain can be derived as

$$|G_i(s)|_{s\to\infty} = \frac{L_{\rm cs}}{R_fC_f}\cdot\left(\frac{R_1}{R_2}\right). \quad (3)$$

As can be seen, the value of the common-source inductance can affect the gain of the circuit. Therefore, to deal with various package designs of different $L_{\rm cs}$, the ratio of R_1/R_2 is adjusted such that $L_{\rm cs}\cdot\frac{di_d(t)}{dt}$ signal can be properly extracted and compared with a reference value to indicate the current rise instant. The reference value can be adjusted as well by changing the resistor dividers. The combination of gain and reference adjustments helps to improve the signal for precise detection of the current rise instant.

In addition, to quickly capture the current rise instant, the response time of the conditioning circuit is improved with the aid of the high-bandwidth and high slew-rate op-amps. Fig. 9 shows the experimental waveforms of the $L_{\rm cs}\cdot\frac{di_d(t)}{dt}$ signal, the conditioning circuit's output signal v_i together with the device's gate voltage and drain current. The load current is 20 A. As can be seen, v_i can follow the input $L_{\rm cs}\cdot\frac{di_d(t)}{dt}$ well with the high-frequency noises filtered.

3) Improvement of Noise Immunity: The noise immunity is another issue to be dealt with in the circuit design. In the T_j measurement circuit, a large external gate resistance is used during the turn-ON delay measurement period. Hence, the $L_{\rm cs}\cdot di_d/dt$ signal changes slowly and is compared to a reference for detecting the ending point of the turn-ON delay period. However, as discussed previously, the gate drive quickly switches to a low gate resistance value after the turn-ON delay period for the sake of reducing the switching loss and minimizing the impact on converter operation. As a result, a ringing current is generated

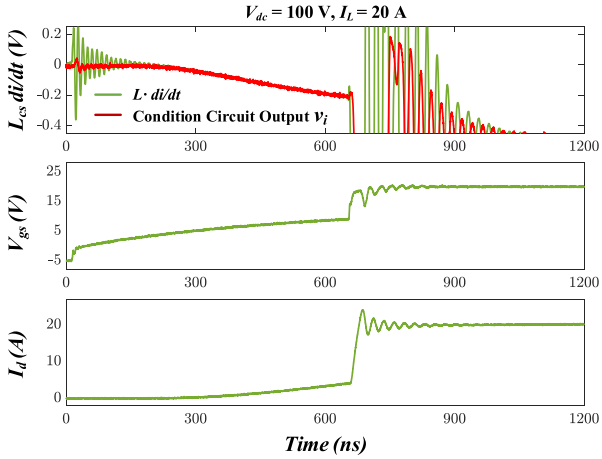

Fig. 9. Signal comparison before and after the conditioning circuit.

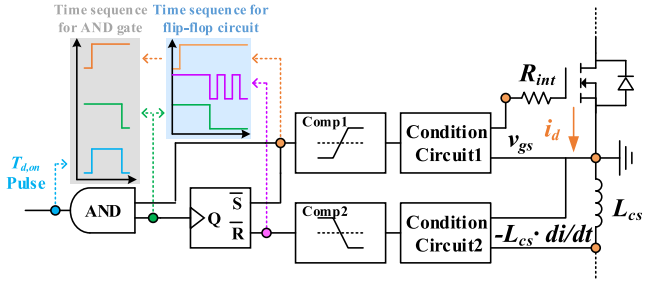

Fig. 10. Illustration of the time sequence in logic circuits.

in i_d due to the power loop parasitic inductance and junction capacitance of the high-side device, and this ringing current causes the $L_{\rm cs}\cdot di_d(t)/dt$ signal to be noisy. The noises can rupture the comparator as well, and its output swings between high to low as indicated by the purple waveform in Fig. 10. If this signal is directly used with the rising edge signal (indicating the start of turn-ON delay time shown in the orange waveform) in the AND gate, the final turn-ON delay signal transmitted to the microcontroller becomes noisy, and the turn-ON delay time cannot be accurately calculated in the HR-Cap module.

To solve this issue, a flip-flop logic circuit is used to eliminate the swings due to ringing noise. To be specific, the starting point of the turn-ON delay period is derived by comparing the rising edge of the gate voltage to a reference and is represented by a rising edge at the comparator1's output, as shown in the orange waveform in Fig. 10. Since the gate ringing is relatively decent, the comparator1's output remains high during the turn-ON period and it is fed to the SET pin of the flip-flop circuit. On the other hand, the noisy comparator2's output (as indicated by the purple waveform) goes to the RESET pin. Through the flip-flop circuit, only the first falling edge of comparator2's output can trigger a reset in the flip-flop circuit's output. Thus, purely one falling edge is obtained at the flip-flop circuit's output, as illustrated by the green waveform in Fig. 10, and it represents the ending point of the turn-ON delay period. This output signal is then used together with the comparator1's output to generate a pulse

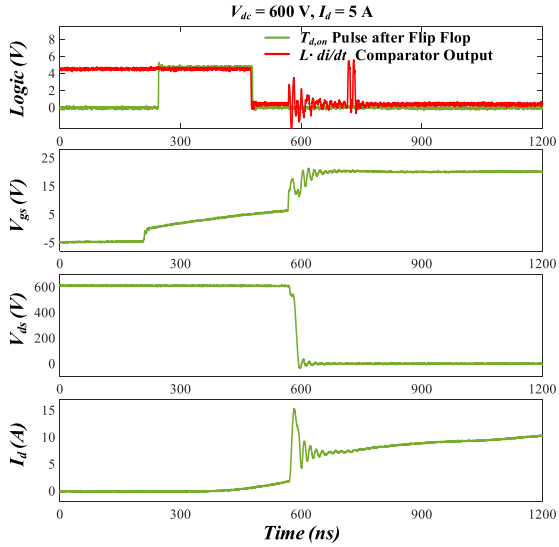

Fig. 11. Experimental comparison of the logic output with and without flip-flop circuits.

signal indicating the turn-ON delay period, as shown in the blue waveform in Fig. 10. In this way, the ringing induced noise will not affect the turn-ON delay pulse signal and an accurate calculation of $T_{d,\mathrm{on}}$ is ensured.

To validate the design, an experiment is carried out where the comparator2's output and the final $T_{d,\mathrm{on}}$ pulse signal is compared simultaneously in a hard switching condition. The dc-link voltage is 600 V, the load current is 5 A, and the experimental waveforms are shown in Fig. 11. In this test, a large external gate resistance of 2000 Ω is initially used during the turn-ON delay period. Then, $R_{g,\mathrm{ext}}$ is set to 10 Ω, and a fast switching transient together with current ringing is observed. Consequently, comparator2's output starts to swing due to the noises in the input $L_{\mathrm{cs}} \cdot di_d/dt$ signal, as illustrated in Fig. 11. In contrast, with the implementation of the flip-flop circuit, the final turn-ON delay pulse signal is not affected by the ringing noises. Therefore, the flip-flop circuit is proved to be valuable in improving noise immunity.

4) Mitigating Propagation Delay's Impact and Isolator Selection: The logic circuits in Fig. 4 can introduce propagation delays in both the v_{gs} measurement path and $L_{\mathrm{cs}} \cdot di_d(t)/dt$ sensing path, which are used to indicate the starting and ending points of the turn-ON delay period, respectively. To mitigate the propagation delay's impact on turn-ON delay time measurement, identical logic circuits are used for v_{gs} and $L_{\mathrm{cs}} \cdot \frac{di_d(t)}{dt}$ sensing paths. Moreover, considering the variation of propagation delays among different chips, the same logic IC with multiple-input and multiple-output is used for both measurements. In this way, the propagation delays in v_{gs} and $L_{\mathrm{cs}} \cdot \frac{di_d(t)}{dt}$ sensing paths are similar. The turn-ON delay time is defined as the time difference between the rising edge output from v_{gs} sensing path and the falling edge signal from $L_{\mathrm{cs}} \cdot \frac{di_d(t)}{dt}$ measurement loop, as indicated in Fig. 10. Hence, the propagation delays in each path cancel out, and the pulsewidth of the $T_{d,\mathrm{on}}$ pulse signal represents the turn-ON delay time.

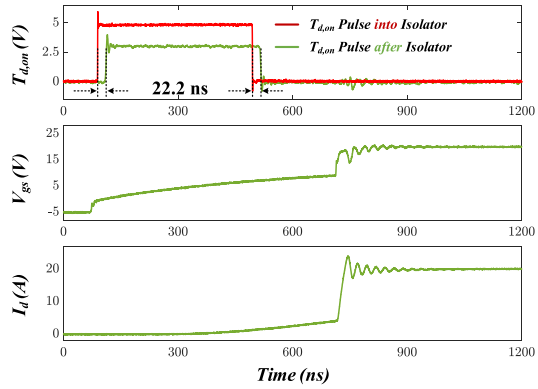

Fig. 12. Propagation delay of the digital isolator.

As discussed previously, this $T_{d,\mathrm{on}}$ pulse is eventually transmitted to the microcontroller side through the digital isolator for turn-ON delay time measurement from the HR-Cap module. To maintain signal integrity, the digital isolator needs to be properly selected. First, the isolator needs to reliably block the high voltage between the power loop and controller ground. Second, the resolution of the digital isolator or pulsewidth distortion time is critical as the turn-ON delay time is calculated from the pulsewidth of the digital signal transmitted. Based on the validation test in Fig. 3, the sensitivity of turn-ON delay time versus T_j is 432.1 ps/°C and can be further increased under larger gate resistance. Therefore, to ensure the measurement accuracy within 1 °C, a digital isolator with a resolution of less than 500 ps is desired. Thus, the commercial isolators ADN465x from Analog Devices (100 ps distortion time) and ISO772x from Texas Instruments Incorporated (500 ps distortion time) are selected. Finally, the common-mode transient immunity (CMTI) of the isolator needs to be considered as the high-side device is subject to the high *dv/dt* noises in the fast-switching SiC MOSFETs. The ISO772x and ADN465x have a typical CMTI of 100 and 50 kV/μs, respectively, which is sufficient for the 1.2-kV SiC MOSFETs used in following tests. Considering all these requirements, the digital isolator ISO772x from Texas Instruments Incorporated is selected. The propagation delay of the isolator is also considered in the circuit design. The selected isolator has the same propagation delay for the rising and falling edge signals. Therefore, when the $T_{d,\mathrm{on}}$ pulse signal is transmitted through the isolator, the pulsewidth (representing the turn-ON delay time) remains unchanged. To verify this, an experiment is carried out, and the digital signals before and after the isolator are compared, as shown in Fig. 12. As can be seen, the same propagation delay of 22.2 ns is observed for the rising and falling edge of $T_{d,\mathrm{on}}$ signal. The measurement result is slightly higher than the propagation delays specified in the datasheet (6–16 ns). One of the causes is that voltage probes with different measurement delays are used on each side: a differential probe is used on the controller side, whereas a passive probe is used on the power side. In the calibration test, the differential probe is found to lag the passive probe by 11 ns. Subtracting this measurement delay difference, a propagation delay of 11.2 ns is derived for the digital isolator, which coincides with the datasheet range.

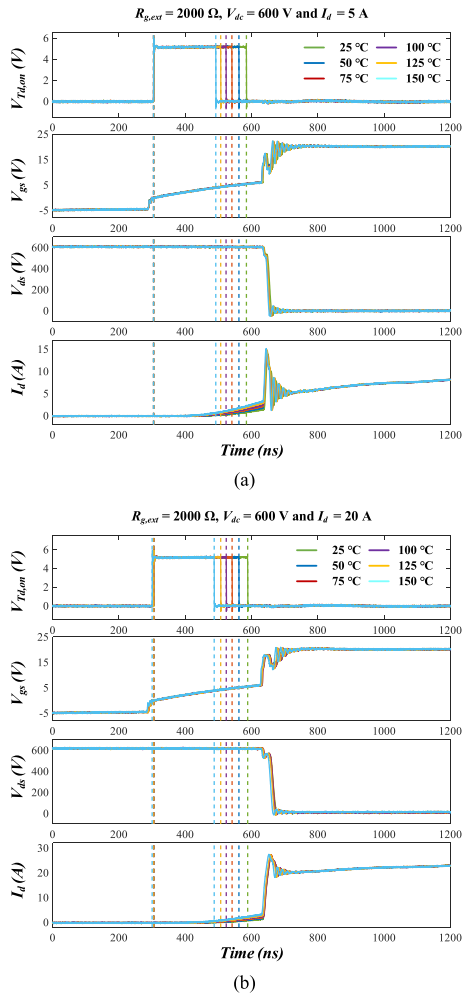

Fig. 13. Experimental waveforms of the switching transient and turn-ON delay pulse at different T_j. (a) 5-A load current. (b) 20-A load current.

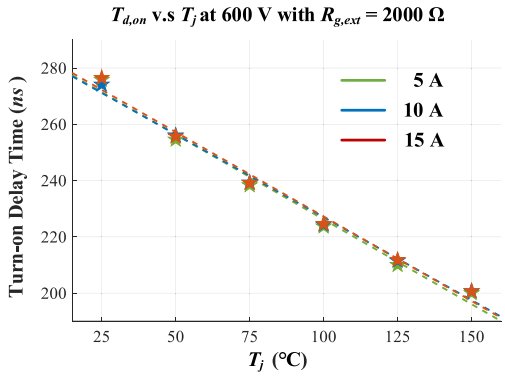

Fig. 14. Experiment results of measured turn-ON delay time at different T_j.

C. Experimental Results in DPT

Once the circuit is carefully designed, it is implemented on a commercial SiC MOSFETs for experimental validations of online junction temperature measurement. At first, the experiments are performed in a DPT system, and the circuit diagram and test setups are demonstrated in Figs. 5 and 6, respectively. To achieve an accurate setting of the device's junction temperature, the thermal resistance between the device and the hot plate is considered, and the temperature difference is compensated. Specifically, the real T_j of the SiC MOSFET is derived from the body diode voltage at low-current injection, and the hot plate's temperature setting is adjusted accordingly to achieve the desired junction temperature.

Considering the low input capacitance (259 pF) of this specific SiC MOSFET, a large external gate resistance of 2000 Ω is used during the turn-ON delay period to improve the measurement sensitivity. Specifically, by turning OFF the auxiliary switch $M_{\rm aux}$ shown in Fig. 4, a large gate resistance is initially implemented for $T_{d,\rm on}$ measurement, as indicated in Fig. 13. Once the turn-ON delay time is obtained, the gate resistance quickly changes to a low value, and a fast switching transient is realized during the turn-ON current rise and voltage falling periods as illustrated in Fig. 13. Hence, the device's switching loss is not compromised with the adaptive gate drive. In Fig. 13, the experimental switching waveforms and turn-ON delay pulse signals are also presented at different T_j with a dc-link voltage of 600 V. The results at 5 and 20 A are shown in Fig. 13(a) and (b), respectively. It is observed that as the junction temperature increases, the device starts to commutate the load current at an earlier stage due to the threshold voltage decrease. Accordingly, the measured turn-ON delay pulse reduces as indicated in Fig. 13.

The variation of the turn-ON delay pulse signal is recorded in the oscilloscope and measured offline. Fig. 14 summarizes the measurement results of $T_{d,\rm on}$ at different junction temperatures. As shown in Fig. 14, the measured turn-ON delay time decreases with decent linearity as the junction temperature goes up. In terms of sensitivity, for 1-°C's temperature increase, the turn-ON delay time decreases by ∼600 ps. This variation can be accurately measured in the HR-Cap module with 300-ps resolution (corresponding to an accuracy of 0.5 °C). In addition, it is observed that the turn-ON delay time variation over T_j remains the same as the load current changes. Therefore, the load information is not needed for online T_j measurement, thus simplifying the implementation.

D. Experimental Results in Continuous Operation

1) Test Setups and Calibration for Continuous Operation: The functionality and accuracy of the proposed online junction temperature measurement method are also evaluated in converter operation for SiC MOSFETs. Since the proposed T_j measurement circuit targets at the hard-switching device, a simple buck converter is considered. For ac current operations, the measurement circuit will be enabled during the hard-switching half-cycle and disabled in the other half-cycle where the soft-switching occurs. In this experiment, the DPT setup is modified into a buck converter for continuous operation, and the circuit diagram together with the real picture of the setup is shown in Fig. 15. The low-side SiC MOSFET is still the hard-switching device, whereas the high-side diode provides the freewheeling path. The detailed parameters of the buck converter are summarized in Table III.

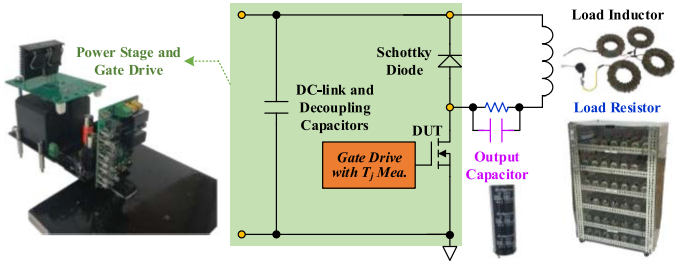

Fig. 15. Circuit diagram and real photograph of the set up for continuous operation.

TABLE III
CONVERTER PARAMETERS

Parameters	Values
Switching Frequency	200 kHz
Inductor	650 µH
Output Capacitor	180 µF
Load Resistor	21 Ω at room temperature

Fig. 16. Decapsulated device for T_j measurement from IR camera.

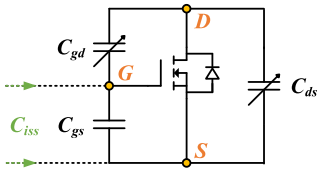

Fig. 17. Illustration of parasitic capacitances within the SiC MOSFETs.

The DUT is modified to be accessible for T_j measurement from the infrared (IR) camera and the IR measurement result is used as a reference to validate the proposed method. Specifically, the device is partially decapsulated to expose the die without affecting the electrical package interconnections. Then, the die surface is painted to black, as shown in Fig. 16, and the emissivity of the IR camera is adjusted to ensure a precise T_j measurement. During the steady state of the converter operation, the IR camera measurement result can represent the device's real junction temperature. The estimated T_j from the turn-ON delay measurement circuit is then compared with the IR measurement for accuracy verifications.

Since the package of the device is decapsulated for IR measurement, the breakdown voltage of the SiC MOSFET decreases. Hence, to ensure the safe operation of the device, the dc-link voltage is reduced to 100 V in continuous operations. As the dc-link voltage drops, the input capacitance C_{iss} increases due to the nonlinearity of the junction capacitance. To be specific, Fig. 17 shows the parasitic capacitances inside the SiC MOSFETs.

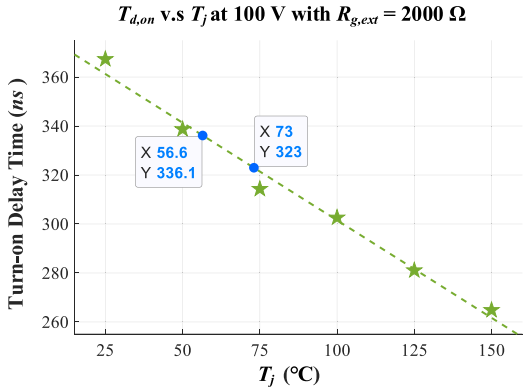

Fig. 18. Experiment results of measured turn-ON delay time versus T_j at dc-link voltage of 100 V.

The gate-to-source capacitance $C_{\rm gs}$ is in parallel with the series connection of gate-to-drain capacitance $C_{\rm gd}$ and drain-to-source capacitance $C_{\rm ds}$, and the input capacitance can be expressed as

$$C_{iss} = C_{\rm gs} + \frac{C_{\rm gd} \cdot C_{\rm ds}}{C_{\rm gd} + C_{\rm ds}}. \tag{4}$$

The gate-to-source capacitance originates from the gate-oxide material in between the gate metallization and doping material in the source, and it remains the constant as the gate-to-source voltage varies. However, $C_{\rm gd}$ and $C_{\rm ds}$ are the junction capacitance within the device's p-n junction, and their values change according to the applied voltage: the junction capacitance decreases as the voltage increases. When the dc-link voltage is reduced from 600 to 100 V, both $C_{\rm gd}$ and $C_{\rm ds}$ increase. Accordingly, the input capacitance goes up. The increase in C_{iss} causes the turn-ON delay time to rise according to (1). Therefore, before the continuous operation test, the turn-ON delay time's variation over T_j is recalibrated in the DPT test at a dc-link voltage of 100 V, and the result is shown in Fig. 18.

Similar to the previous DPT result at 600 V, a large $R_{g,\rm ext}$ of 2000 Ω is used during the turn-ON delay measurement phase. Good linearity is observed from Fig. 18, and the absolute value of $T_{d,\rm on}$ does increase compared to the 600 V results in Fig. 14. In addition, as the input capacitance goes up, the sensitivity is also improved according to (1). From the experimental result in Fig. 18, the sensitivity increases to 796.5 ps/°C at a dc-link voltage of 100 V.

2) Online Junction Temperature Measurement Results and Accuracy Verification: With the calibration curve, the device's junction temperature is measured in real-time using the proposed circuit and the result is compared with the IR measurement for verification. In addition to these T_j measurements, the inductor's current i_L is measured by the TCP0030A current probe during the continuous operation. The DUTs gate-to-source voltage $v_{\rm gs}$, drain-to-source voltage $v_{\rm ds}$, turn-ON delay pulse signal $T_{d,\rm on}$, and the gate signal for the auxiliary switch $v_{\rm gs\_aux}$ are recorded as well.

Fig. 19 illustrates the steady-state continuous operation waveforms captured from the oscilloscope at a load current of 8.2 A. As can be seen, the auxiliary switch's gate signal $v_{\rm gs\_aux}$ remains

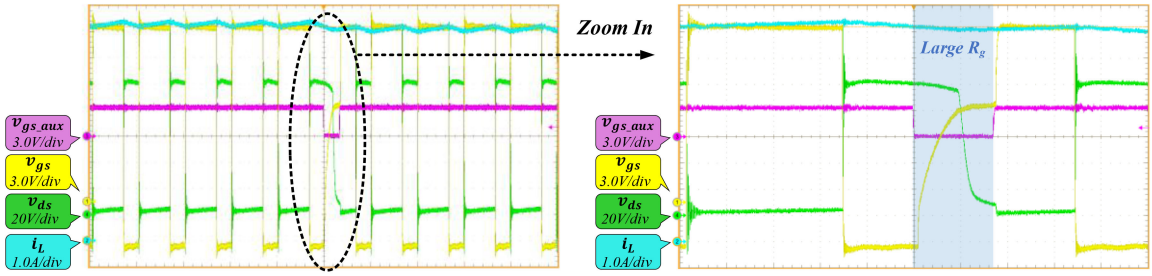

Fig. 19. Continuous operating waveforms at a steady state of 100 V/8.2 A.

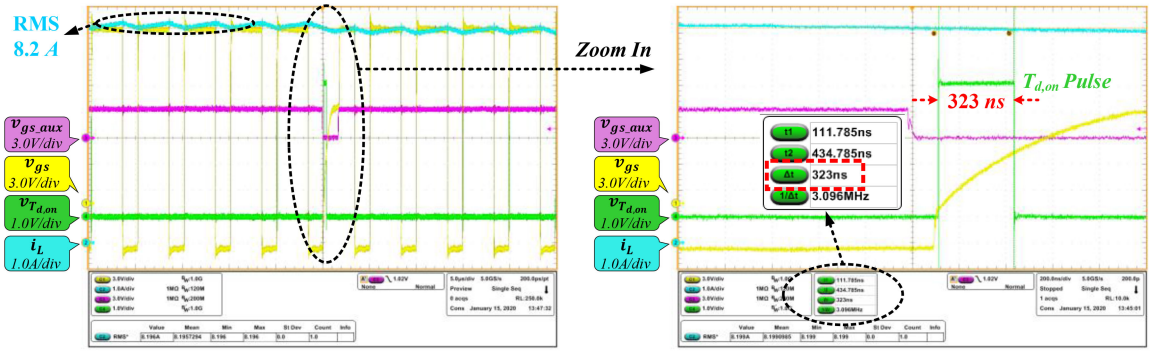

Fig. 20. Continuous operating waveforms and turn-ON delay pulse signal at a steady state of 100 V/8.2 A.

high in normal converter operation and a low gate resistance is used to reduce the switching loss. With low gate resistance, the ringing is observed in $v_{\rm gs}$ and $v_{\rm ds}$, and the fast-switching transient enables the SiC MOSFET to operate at 200 kHz. At intervals of the continuous operation, the junction temperature is measured by the proposed circuit as indicated in the zoom-in waveform of Fig. 19. In each measurement switching cycle, the gate signal of the auxiliary switch sets to low at the beginning for a large gate resistance to improve the measurement sensitivity based on $T_{d,\rm on}$. Once the junction temperature is obtained, the auxiliary switch immediately turns OFF, and the converter resumes the normal operation within one switching period.

Under the same operating condition (100-V dc-link with a load current of 8.2 A), the continuous waveforms together with the turn-ON delay pulse $T_{d,\rm on}$ signal are displayed in Fig. 20. As indicated in the zoom-in waveform, the oscilloscope's cursor is utilized to indicate the pulsewidth of $T_{d,\rm on}$, and the turn-ON delay time is measured to be 323 ns. Referring to the turn-ON delay versus T_j relationship shown in Fig. 18, a junction temperature of 73.0 °C is derived in real-time converter operation.

The IR camera measurement at the same instant is shown in Fig. 21. A maximum junction temperature of 72.5 °C is observed in the center of the die. Considering the small die size of this low-current SiC MOSFET, a uniform temperature distribution is expected for this specific device. Consequently, the mean junction temperature of the device is close to the maximum junction temperature. Comparing the circuit measurement (73.0 °C) to the IR result (72.5 °C), a tiny T_j difference is observed. Hence, the accuracy of the proposed junction temperature measurement circuit is validated experimentally. In addition to the results

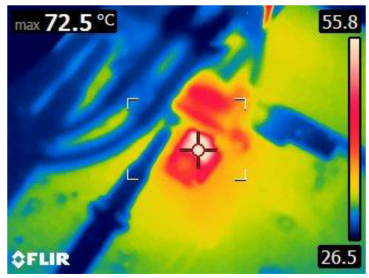

Fig. 21. IR measurement result at a steady state of 100 V/8.2 A.

shown in Figs. 19–21, the experimental measurements from IR camera and the online T_j estimation circuit are also compared in a recorded video. As can be seen from the attached *active content* (see Supplementary Information), the consistency and accuracy of the proposed online junction temperature method are verified as well.

The measurement accuracy of the proposed circuit is also evaluated at another operating condition where the load current is reduced to 7.4 A, and the steady-state experimental waveforms are plotted as illustrated in Fig. 22. At a lower I_L, the junction temperature decreases, and the measured turn-ON delay pulse increases to 336.1 ns. According to the calibration curve shown in Fig. 18, a junction temperature of 56.6 °C is obtained. On the other hand, the device's real T_j is measured to be 55.9 °C from the IR camera, as indicated in Fig. 23. As can be seen, the results match well, and the accuracy of the proposed online T_j measurement method is validated under different operating conditions.

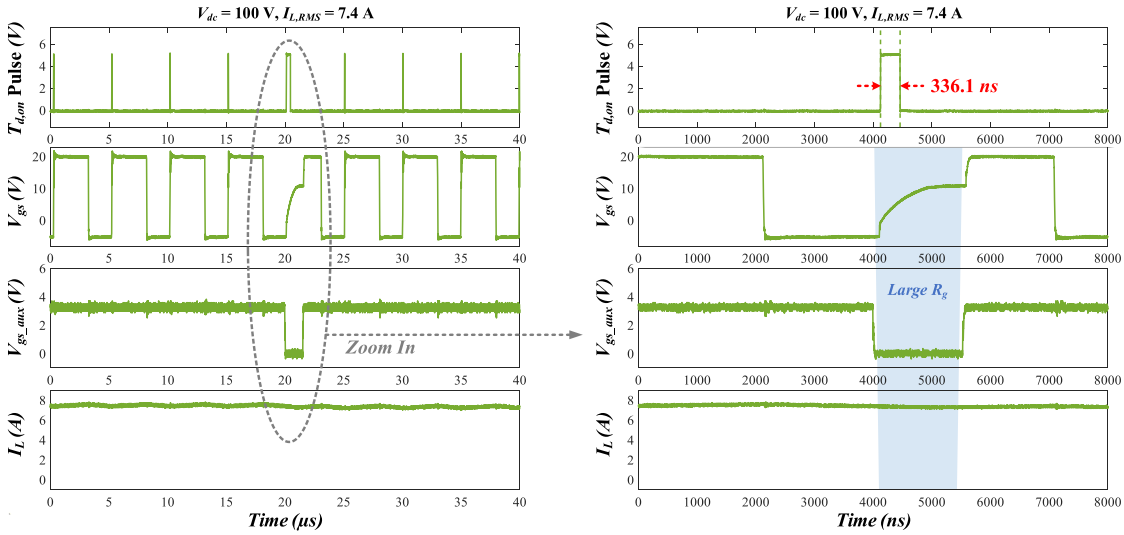

Fig. 22. Verification of measurement accuracy at another operating point of 100 V/7.4 A.

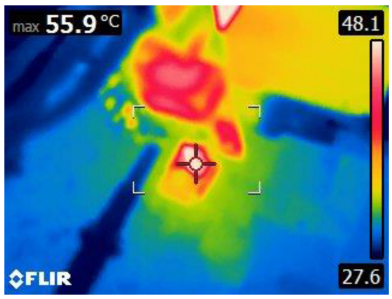

Fig. 23. IR measurement result at a steady state of 100 V/7.4 A.

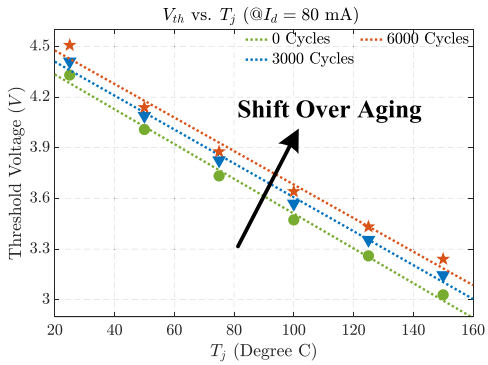

Fig. 24. Threshold voltage shift over aging at different T_j.

IV. Aging Compensation Scheme

As discussed previously, the device's aging can affect the TSEPs making the junction temperature measurement unreliable over the aging process. In this section, an aging compensation scheme is discussed for the $T_{d,\mathrm{on}}$-based online junction temperature measurement method.

A. Threshold Voltage Shift Over Aging

For the state-of-the-art SiC MOSFETs, a high density of traps still exists in the SiC/SiO_2 interface due to the vacancies and carbon atoms [48], [49]. Together with the reduced bandgap offset between SiC and SiO_2, electrons can tunnel into the gate oxide under the long-term gate bias, thus leading to the threshold voltage shift [50]. Therefore, considering the repetitive gate bias stress during long-term converter operation, a permanent change in V_{th} occurs over aging. As a result, the turn-ON delay time is shifted according to (1), and T_j estimated from $T_{d,\mathrm{on}}$ becomes inaccurate.

Fig. 24 shows the experimental result of the threshold voltage shift over aging for an SiC MOSFET. The selected fresh device has the same part number and batch code as the previous DUT. In the aging test, the dc power cycling method is implemented, and the operation of the setup has been discussed in [51]. Specifically, the device is heated by its own conduction loss, and the nominal ON-state voltage (20 V in this case) is constantly applied to stress the gate oxide of the device. Once the device's junction temperature reaches the maximum T_j setting, the device is turned OFF with zero gate bias. Consequently, the load current is removed, and the device starts to cool down to the minimum T_j setting. At intervals of the aging test, the threshold voltage of the device is characterized 5 h after the gate bias stress. The measurement delay ensures that the interface traps have achieved the equilibrium state, and only the permanent shift of V_{th} due to the near-interface trap is measured [48]. As can be seen in Fig. 24, at various junction temperature, a positive bias temperature instability is observed as the gate voltage swings between 20 and 0 V. At different aging cycles, the variations of the V_{th} versus T_j curve are summarized in Table IV.

TABLE IV
Linear-Fitted Parameters for V_{th} Versus T_j at Different Aging Cycles

Aging Cycles	Sensitivity	Values at 0 °C
0	-10.3 mV/°C	4.54 V
3000	-10.0 mV/°C	4.61 V
6000	-9.9 mV/°C	4.68 V

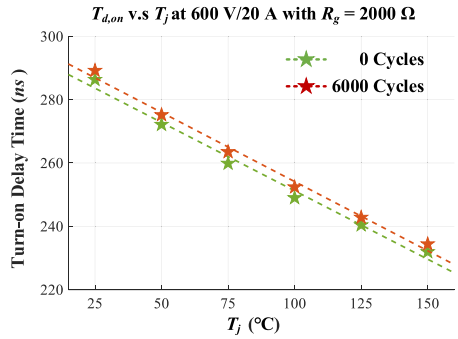

Fig. 25. Turn-ON delay time variation over aging at different T_j.

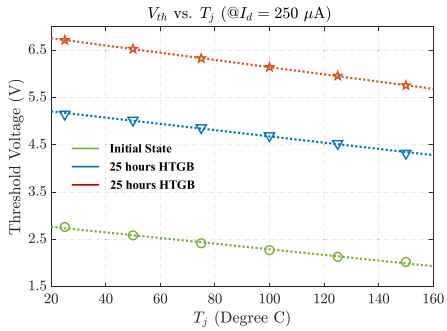

Fig. 26. Threshold voltage shift over aging under the HTGB test.

It is observed that the sensitivity remains almost the same after aging. However, an offset is noticed due to the positive threshold voltage shift.

Due to the threshold voltage shift, the turn-ON delay time is also affected after the gate-oxide degradation. Utilizing the DPT setup discussed in Fig. 1, the experimental result of the $T_{d,\mathrm{on}}$ variation over aging at different T_j is summarized in Fig. 25. As can be seen, the turn-ON delay time does go up due to the positive V_{th} shift induced in the dc power cycling test, but the slopes of the fitted curves remain the same. In terms of aging's effect on T_j measurement, the positive shift of the $T_{d,\mathrm{on}}$ versus T_j curve causes an underestimation of the device's real junction temperature, and the measurement error reaches to ∼8 °C at 6000 aging cycles. The underestimation of the device's real T_j is undesirable since the overtemperature in the device can bring reliability issues or cause device failures. It is worth pointing out that the aging test is stopped at 6000 aging cycles because of the device's package failure under large temperature swings. In real applications, the gate bias stress time can be longer, and a larger V_{th} shift is expected. Fig. 26 shows the experimental result of the threshold voltage shift for an SiC MOSFET under the high-temperature gate bias (HTGB) test. The selected fresh device has the same part number and batch code as the previous DUT. A positive gate bias of 40 V (twice the nominal gate voltage) is applied to expedite the aging process, and the device's temperature is set to 150 °C. The threshold voltage of the device is characterized at every 25 h after a relaxing time of one day. As can be seen in Fig. 26, a higher threshold voltage shift is observed in the HTGB test, whereas the sensitivity of the V_{th} versus T_j curve remains almost the same. Due to the threshold voltage shift, the T_j measurement error based on turn-ON delay time can be more severe after aging.

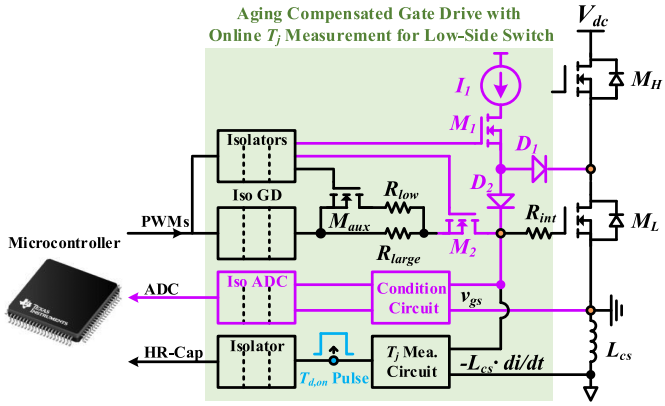

Fig. 27. Aging compensation circuit for precise T_j measurement.

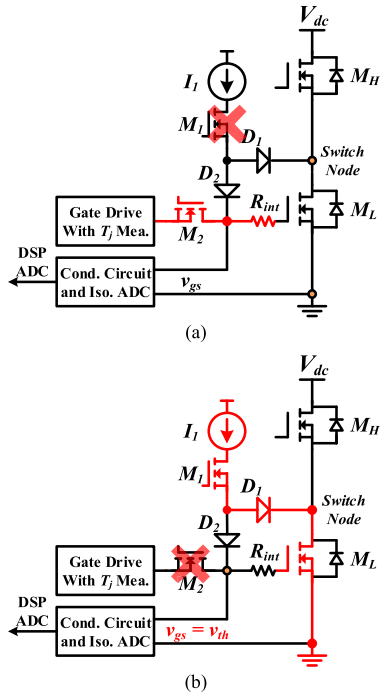

Fig. 28. Operation of the aging circuits. (a) Normal converter operation period. (b) Threshold voltage measurement period.

B. Circuit Implementation for Aging Compensation

To achieve a consistent and accurate junction temperature measurement over the device's lifetime, an aging compensation circuit is added to the previous intelligent gate drive, and its circuit diagram is highlighted by the purple lines in Fig. 27. Previously, this circuit has been successfully used to measure the threshold voltage of the Si-insulated-gate bipolar transistor (IGBT) [52] and gallium nitride device [53].

The circuit consists of a current source I_1, two diodes, two control switches, and one isolated ADC. During the converter normal operation, M_1 is turned OFF, and no current is injected from the current source circuit, as indicated in Fig. 28(a). At the

same time, M_2 is in ON-state, and the gate drive circuit functions normally to turn-ON/OFF the SiC MOSFETs. A high-voltage Schottky diode is used for D_1 to protect the threshold voltage measurement circuit from the high voltage in the middle point of the phase leg, and a diode with low junction capacitance is selected to mitigate its impact on the DUTs switching loss.

The threshold voltage of the DUT can be measured when the converter stops operation or in idle state. The circuit operation diagram is shown in Fig. 28(b). At first, the gate drive output goes to zero or negative. Then, M_2 is turned OFF, and a low constant current I_1 is injected by turning ON M_1. The injected current initially flows through D_2 and starts to charge the input capacitance of the SiC MOSFET. Once the gate voltage reaches to the defined threshold voltage, the switch-node voltage falls, and the injected low current conducts through the MOSFET. In the steady state, the gate voltage remains at $V_{\rm th}$, and this value is measured by the microcontroller through the conditioning circuits and isolated ADC. Throughout the aging of the device, the measured $V_{\rm th}$ values together with the ambient temperature information (measured either from the controller's on-chip ambient temperature sensor or an external on-board ambient temperature sensor) are stored in the controller when the converter is not operating. Based on the sensitivity of $V_{\rm th}$ over T_j (which is found to be consistent over aging from the results shown in Figs. 24 and 26), the percentage of the threshold voltage offset is derived over aging. This offset (in percentage) is then added to the $T_{d,\rm on}$ versus T_j curve to compensate the aging's impact.

V. Conclusion

The turn-ON delay time is a favorable TSEP in terms of its linearity, sensitivity, and load independence. In this article, a real-time junction temperature measurement method with aging compensation is proposed based on $T_{d,\rm on}$.

Utilizing an adjustable gate resistance circuit, a high sensitivity of 600 ps/°C is achieved for $T_{d,\rm on}$. Combining with the 300-ps measurement resolution in the HR-Cap module, the turn-ON delay time can be precisely measured. The circuit design considerations are discussed and validated with experimental results. It is shown that the parasitics and logic circuits require careful design considerations to ensure signal integrity and noise immunity.

A DPT and buck converter is built to test the feasibility/accuracy of the online junction temperature measurement method in both switching test and continuous operation. In the experiments, by comparing the circuit result to the IR camera measurement, it is validated that the proposed method can achieve a precise online junction temperature measurement with a measurement error of less than 1 °C.

Considering the long-term gate-oxide degradation in SiC MOSFET, an aging compensation scheme is proposed to mitigate the aging's effect on T_j measurement accuracy. Through the threshold voltage measurement circuit, the offset of the $T_{d,\rm on}$ versus T_j curve can be compensated throughout the device's lifetime. However, the isolated ADC in the circuit adds cost to the system. Besides, the $V_{\rm th}$ measurement needs to be implemented when the converter is not operating, and this may not be allowable in some applications.

In future work, the proposed circuit is to be integrated into the gate drive IC. Also, the gains of the conditioning circuits and reference values are designed adjustable, thus enabling the flexibility to deal with package designs of different common-source inductance.

Yet, there are several challenges in terms of real practice implementations. First, for ultralow-parasitic inductance package designs, the extracted $L_{\rm cs} \cdot \frac{di_d(t)}{dt}$ signal and more easily subject to noises. This will bring challenges to the conditioning circuit designs. Another challenge is that a calibration process is required before the system operation, which is a common problem for all TSEP-based T_j measurement methods. For the proposed method, the device variations, package design, and layout can all affect the turn-ON delay measurement result. Therefore, a careful calibration is required to mimic the real system conditions.

Acknowledgment

The author would like to acknowledge Dr. G. Wang and Dr. S. W. Butler from Texas Instruments Incorporated for their suggestions.

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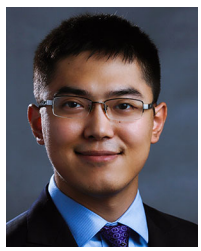

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