Third Quadrant Conduction Loss of 1.2–10 kV SiC MOSFETs: Impact of Gate Bias Control

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***Abstract*—The third quadrant (3rd-quad) conduction of power MOSFETs involves competing current sharing between the metal-oxide-semiconductor (MOS) channel and the body diode controlled by the gate bias ($V_{\rm G}$). For 1.2 kV SiC planar MOSFETs, it is well known that a positive $V_{\rm G}$ higher than the threshold voltage enables parallel conduction through both channels, which reduces the 3rd-quad voltage drop and conduction loss. This work, for the first time, unveils that this fact does not hold for higher voltage (e.g., 3.3 kV and 10 kV) SiC planar MOSFETs. By combining the static characterization, simulation, and modeling, it is revealed that, once the MOS channel turns ON, the body diode in high-voltage MOSFETs turns ON at a source-to-drain voltage ($V_{\rm SD}$) much higher than the built-in potential of the PN junction. In 10 kV SiC MOSFETs, the body diode does not turn ON over the entire practical $V_{\rm SD}$ range if the MOS channel is on. As a result, the positive $V_{\rm G}$ leads to completely unipolar conduction, which could induce a higher voltage drop than the bipolar body diode at high temperatures. A buck converter based on a 10 kV SiC MOSFET half-bridge module was built and tested, which validated that a negative $V_{\rm G}$ control provides the smallest 3rd-quad voltage drop and conduction loss at high temperatures. Finally, based on the revealed physics for planar MOSFETs, the optimal $V_{\rm G}$ control for the 3rd-quad conduction in trench MOSFETs is discussed. These results provide critical device understandings of 1.2–10 kV SiC MOSFETs and important application guidelines for 10 kV SiC MOSFETs.**

***Index Terms*—Body diode, conduction loss, dc–dc converter, gate control, high temperature, high voltage, MOSFETs, silicon carbide, third quadrant (3rd-quad) operation.**

I. Introduction

THANKS to the higher critical electric field and thermal conductivity of SiC than Si, SiC devices are ideal for medium-voltage (1.2–35 kV) power electronics applications [1]–[4]. Among different SiC power switches, SiC MOSFETs offer the most desirable features from the user's perspectives, including normally-OFF operation and fast switching [1]. Following the commercialization of 1.2 and 1.7 kV SiC MOSFETs, precommercialized 3.3 and 10 kV planar SiC MOSFETs have become available from several vendors [2]–[4].

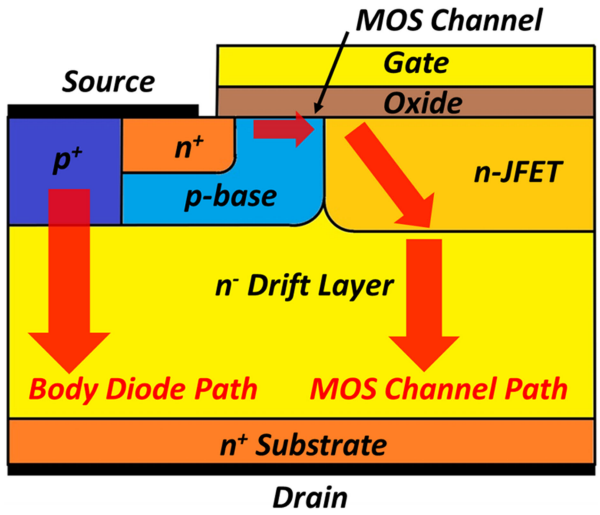

Fig. 1. Schematic of a SiC planar MOSFET unit-cell. The MOS channel path and the body diode path in the 3rd-quad conduction are marked.

It is critical to understand the third quadrant (3rd-quad, also called reverse conduction) behaviors of SiC MOSFETs for power switching applications, particularly the ones with bidirectional current flows, such as synchronous buck converters, motor drives, and synchronous rectifiers. As shown in Fig. 1, there are two paths in the SiC planar MOSFET for 3rd-quad current conduction: one through the MOS channel and the other through the body diode. The MOS channel has a zero turn-ON voltage, while the body diode has lower differential conduction resistance due to conductivity modulation [5]. Studies on 1.2 kV SiC planar MOSFETs [6], [7] have revealed that the 3rd-quad voltage drop ($V_{\rm 3rd}$) can be effectively lowered by turning ON the MOS channel (i.e., $V_{\rm G} > V_{\rm th}$, $V_{\rm G}$ is the gate bias and $V_{\rm th}$ the threshold voltage), which takes the advantages of both paths: the MOS channel turns ON from zero bias, and the body diode turns ON at a higher $V_{\rm SD}$ (3–4 V), which further reduces the differential resistance. However, there is still a lack of comprehensive studies on the 3rd-quad behaviors of higher voltage (3.3–10 kV) SiC MOSFETs, particularly the current sharing physics under different $V_{\rm G}$ and temperatures in these devices. Prior work on 10 kV SiC MOSFETs only studied the body diode characteristics [3] and the 3rd-quad

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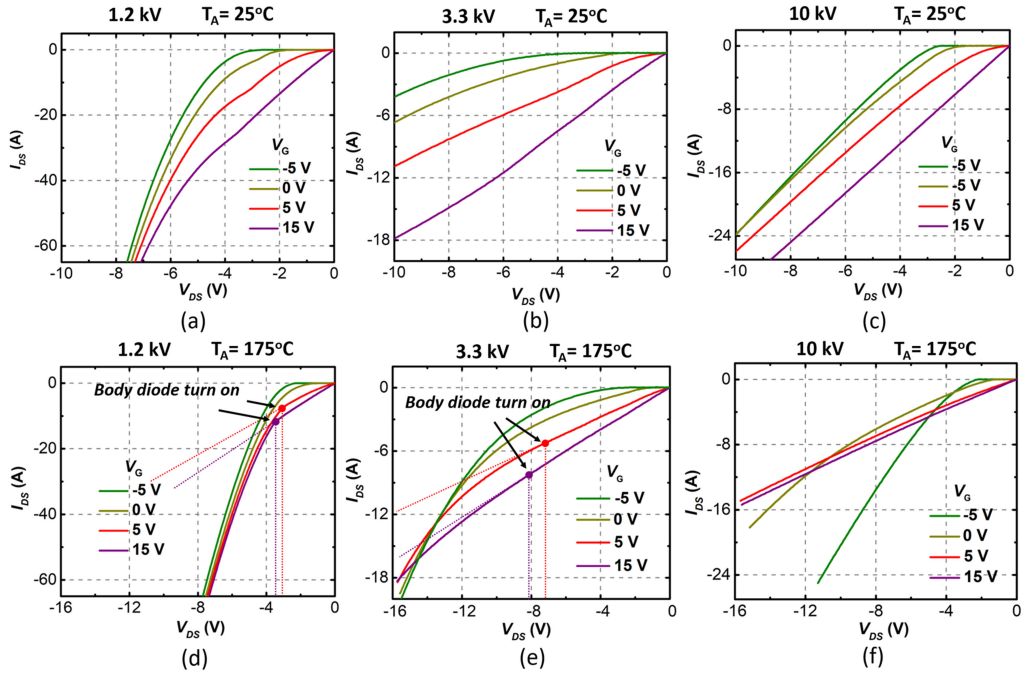

Fig. 2. Typical 3rd-quadrant characteristics of 1.2 kV SiC MOSFETs (19 A rated), 3.3 kV SiC MOSFETs (5 A rated), and 10 kV SiC MOSFETs (16 A rated), all measured at V_G of −5, 0, 5, and 15 V, and at the temperature of 25 °C and 175 °C. The body diode turn-ON at positive V_G is marked.

conduction in the subthreshold turn-ON region [8], all at zero or negative V_G.

This work presents the first comparative study on the 3rd-quad behaviors of 1.2, 3.3, and 10 kV SiC planar MOSFETs under different V_G and temperatures. The static current–voltage (I–V) characterization of 3.3 and 10 kV SiC MOSFETs revealed a higher V_{3rd} at positive V_G than the one at negative V_G under high temperatures. This behavior is contrary to that of 1.2 kV devices and has not previously been reported in the literature. Theoretical explanations were developed for the first time and were further validated by physics-based simulations. Analytical device models for SPICE simulations were then developed. To understand the circuit-level implications of these device findings, a buck converter based on a 10 kV SiC MOSFET half-bridge module was developed. The V_{3rd} of the low-side device was tested at different V_G and temperatures. The converter test results agree with the static test results and analytical models. Based on the physics unveiled for planar MOSFETs, the impact of V_G on the V_{3rd} of trench MOSFETs was finally discussed.

The rest of article is organized as follows. Section II presents the static characterization results, physical theories, and device simulation. Section III illustrates the device analytical models. Section IV presents the converter setup and tests. Section V discusses the 3rd-quad characteristics of SiC trench MOSFETs. Finally, Section VI concludes this article.

II. Static Characterization, Physical Theories, and Device Simulation

A. Static Characterization

The devices tested in this article include the engineering samples of 10 and 3.3 kV SiC planar MOSFETs as well as the commercial 1.2 kV SiC planar MOSFETs, from multiple vendors including Wolfspeed (1.2 kV, 10 kV), GeneSiC (1.2 kV, 3.3 kV), and Rohm (1.2 kV). For commercially available devices, the devices with the same voltage rating but different current ratings were also tested. The experimental findings and device physics discussed in this work have been validated for all the tested devices and are not manufacturer specific.

Fig. 2 shows the typical 3rd-quad I–V characteristics of 1.2, 3.3, and 10 kV SiC planar MOSFETs at different V_G (−5, 0, 5, and 15 V) and under two temperatures (25 and 175 °C). For 1.2 kV devices, under both temperatures, $V_G > V_{th}$ leads to a lower V_{3rd} due to the parallel current conduction in the MOS channel and body diode. The kink in the I–V curves under V_G of 5 V and 15 V shows the body diode turn ON, which occurs at a source-to-drain voltage (V_{SD}) of ∼3.5 V. These results are consistent with the ones reported in [6].

For 3.3 and 10 kV devices, at 175 °C, the I–V curves under different V_G show crossovers, suggesting a lower V_{3rd} controlled by negative V_G at high current levels. At V_G of 5 and 15 V, the body diode turns ON at V_{SD} of ∼8 V in 3.3 kV devices, which is larger than the one in 1.2 kV devices. At positive V_G, no body-diode turn-ON is shown in 10 kV devices.

B. Physical Theories

In this section, the 3rd-quad behaviors of 1.2, 3.3, and 10 kV SiC planar MOSFETs will be discussed under different V_G conditions, as they involve different device physics.

$\underline{V_G = -5\ V}$. At a sufficiently negative V_G, the MOS channel is completely OFF. The body diode turns ON when V_{SD} exceeds the knee voltage (V_{knee}) of the SiC PN junction, which equals

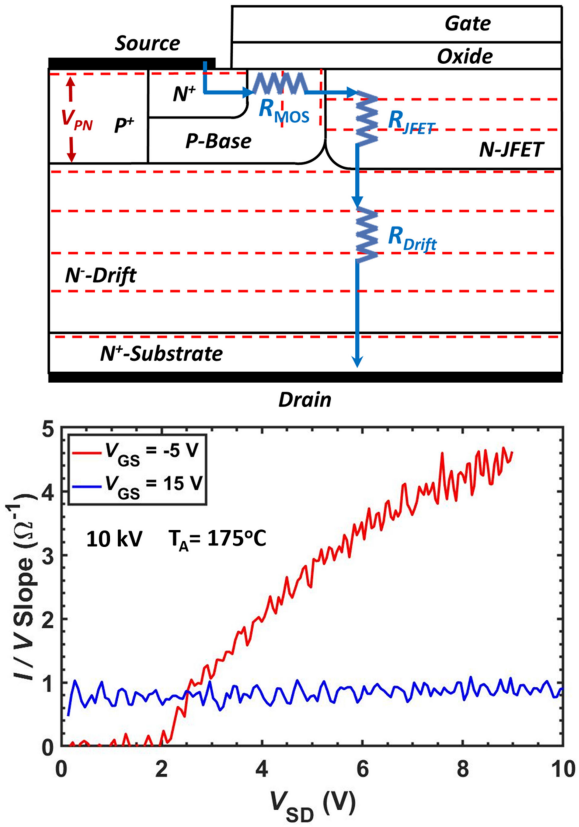

Fig. 3. (Top) Schematic of the established potential distribution in device by the electron current through MOS channel, JFET region, and drift region. The dashed lines show the equipotential lines normal to the current flow. (Bottom) The differential conductance as a function of V_{SD} at V_G of -5 V and 15 V in 10 kV SiC MOSFETs at the temperature of 175 °C.

the built-in potential of the SiC PN junction and are mainly determined by the ionized donor concentration (N_D) and acceptor concentration (N_A) in the drift region and the p-base region, respectively, as well as the intrinsic carrier density (n_i)

$$V_{\text{knee}} \approx (kT/q)\ln(N_D N_A/n_i^2). \tag{1}$$

For a SiC PN junction with not too low N_D and N_A, V_{knee} is close to the bandgap of SiC, i.e., $V_{\text{knee}} \sim 3$ V.

$\underline{V_G = \mathbf{15\ V}}$. At $V_G > V_{th}$, the MOS channel turns ON, and a unipolar electron current flows in the device. This electron current then establishes the potential distribution following the Ohm's law in the device, which is determined by V_{SD} and the resistance components, as shown in Fig. 3. As the p-base forms an Ohmic contact to the source electrode, the voltage that falls onto the PN junction in the body diode (V_{PN}) is approximately the voltage drop across the MOS channel (R_{MOS}) and the junction field-effect-transistor (JFET) (R_{JFET}) region. If we ignore the contact and substrate resistance and define the drift region resistance as R_{DRIFT}, V_{PN} can be written as

$$V_{PN} \approx V_{SD}\left(R_{MOS} + R_{JFET}\right)/R_{ON} \tag{2}$$

where

$$R_{ON} \approx R_{MOS} + R_{JFET} + R_{DRIFT}\ . \tag{3}$$

Due to the potential distribution established by the unipolar current, the body diode no longer turns ON at the V_{knee} of PN junction. Here, we define the body diode turn-ON voltage (V_{BD-on}) as the V_{SD} when the current through the body diode starts to be comparable to the one through the MOS channel, where a change in the *I–V* curve slope is shown. V_{BD-on} can be estimated by the condition that V_{PN} exceeds the V_{knee} of the PN junction ($V_{PN} \geq V_{\text{knee}}$)

$$\begin{aligned} V_{BD-on} &\approx V_{\text{knee}} R_{ON}/(R_{MOS} + R_{JFET}) \\ &\approx V_{\text{knee}}\left[1 + R_{DRIFT}/(R_{MOS} + R_{JFET})\right]. \end{aligned} \tag{4}$$

As the device voltage is mainly sustained by the lowly doped and thick drift region, the resistance of an optimal drift region scales up with the breakdown voltage, usually following a power law. As a result, with the increase in device voltage rating, the percentage of R_{DRIFT} in R_{ON} increases. From (4), V_{BD-on} also increases, which explains the experimental results shown in Fig. 2(d) and (e). In a 10 kV SiC MOSFET, as $R_{DRIFT} >> R_{MOS} + R_{JFET}$, the body diode does not turn ON over the entire V_{SD} safe-operating range up to 16 V. Fig. 3 shows the extracted differential conductance as a function of V_{SD} at V_G of -5 V (body diode conduction) and 15 V at 175 °C. The differential conductance at V_G of 15 V remains constant with the increased V_{SD} and is much smaller than that of body diode at high V_{SD}. This further verifies that the body diode does not turn ON at $V_G = 15$ V. It should be pointed out that (4) illustrates an approximation of V_{BD-on}. A more accurate model that considers the uneven potential distribution inside the device cell will be developed in Section III.

Now, we discuss how this delayed body-diode turn-ON impacts the V_{3rd} of high-voltage MOSFETs under different temperatures. Benefited from conductivity modulation, the differential resistance of the bipolar body diode increases much slower or even decrease with temperature when compared to the one of the unipolar MOS channel and drift region. The advantage of body diode conduction at high temperatures is more pronounced for high-voltage devices. For example, the body diode of 10 kV SiC MOSFETs shows advantages over a parallel junction barrier Schottky diode at high temperatures [3]. Besides, V_{knee} typically decreases with the increased temperature [9] due to the higher n_i, as can be seen from (1). This factor further lowers the voltage drop of body diode at higher temperatures.

As shown in Fig. 2(a) and (d), at $V_G > V_{th}$, in 1.2 kV devices, since V_{BD-on} is small (~3.5 V), the body diode turns ON before the *I–V* curve intersects the curve with negative V_G, at both 25 °C and 175 °C. This suggests that the V_{3rd} at $V_G = 15$ V is always lower than the V_{3rd} at $V_G = -5$ V. In 3.3 kV and 10 kV MOSFETs, the delayed body-diode turn-ON at $V_G = 15$ V leads to a larger differential resistance, particularly at high temperatures, which offsets the benefits that comes from the lower turn-ON voltage of the MOS channel when compared to the body diode. As a result, the *I–V* curves at $V_G = 15$ V and $V_G = -5$ V intersects; at high current levels and high temperatures, a lower V_{3rd} is provided by $V_G = -5$ V.

$\underline{V_G = \mathbf{0\ V}}$. At $V_G = 0$ V, the MOS inversion channel is OFF, but a "surface channel" through the p-base region close

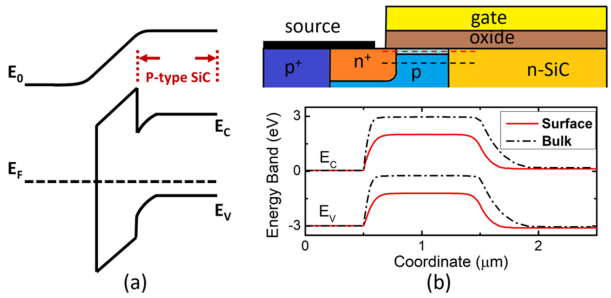

Fig. 4. (a) Energy band diagram showing the electrostatics of the vertical MOS structure. (b) Simulated energy band diagram along the two cutline in the surface NPN channel and the bulk NPN channel, respectively, showing a lowered barrier in the p-base region in the surface channel.

to the SiC/oxide interface forms. This surface channel has a $V_{\rm knee}$ smaller than the $V_{\rm knee}$ of the body diode (or PN junction); therefore, as shown in Fig. 2(a)–(f), the turn-ON voltage of the *I*–*V* curves at $V_{\rm G} = 0$ V is 2–2.5 V and smaller than that of the body diode. The creation of this "surface channel" with a smaller turn-ON voltage originates from the interplay between the MOS electrostatics in the vertical direction and the NPN electrostatics in the lateral direction. Due to the work function difference between the gate metal (or polysilicon) and SiC, the p-SiC region close to the SiC/oxide interface is depleted [see Fig. 4(a)]. This depletion by the vertical MOS structure lowers the potential barrier of the p-base region in the lateral NPN channel [see Fig. 4(b)], leading to a smaller $V_{\rm knee}$. The formation of this "surface channel" has also been discussed in [8], [10], and [11]. The $V_{\rm knee}$ of this NPN channel gradually increases when $V_{\rm G}$ decreases below zero due to the weakened MOS depletion. At $V_{\rm G} \leq -5$ V, as the surface p-SiC region changes from depletion mode to accumulation mode, the $V_{\rm knee}$ of NPN channel is no longer smaller than the body diode. The body diode then dominates the 3rd-quad current.

Once this NPN surface channel turns ON at $V_{\rm G} = 0$ V, the current establishes the potential distribution following the Ohm's law within the device, in the same way as the MOS channel does at $V_{\rm G} = 15$ V. As a result, $V_{\rm BD-on}$ is determined by (4) and becomes much larger than ∼3.5 V in high-voltage SiC MOSFETs. This delayed body-diode turn-ON explains the cross-overs between the *I*–*V* curves at $V_{\rm G} = 0$ V and $V_{\rm G} = -5$ V, as can be seen in Fig. 2(e) and (f). Note the differential resistance and voltage drop at $V_{\rm G} = 0$ V are smaller than the ones at $V_{\rm G} = 15$ V, particularly at high temperatures. This is because the NPN channel has a bipolar nature, and its resistance is lower than the unipolar MOS channel at high temperatures.

C. Physics-Based Simulation

To validate our theories of delayed body-diode turn-ON, physics-based technology computer-aided design (TCAD) simulations were performed in Silvaco Atlas, based on similar physical models described in [12]–[14]. The conductivity modulation, velocity saturation, temperature-dependent carrier mobility, and incomplete dopant ionization were accounted for in the simulation models. The simulation was then calibrated to the

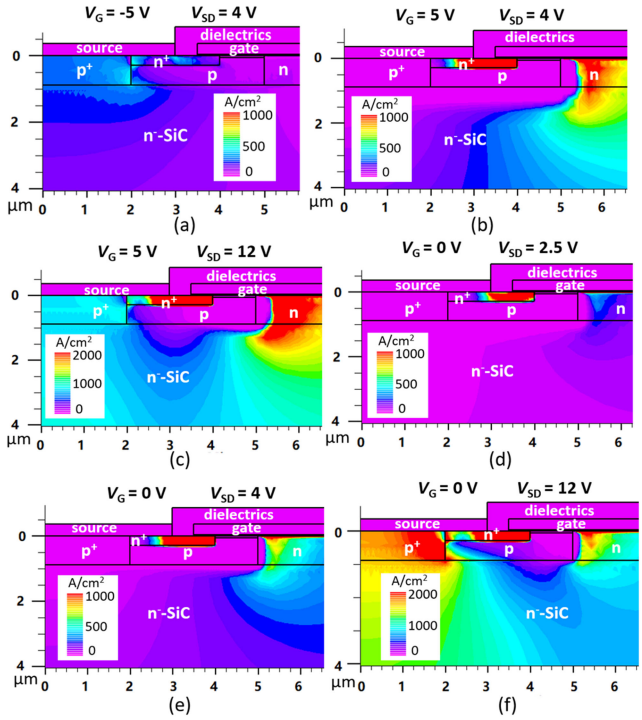

Fig. 5. Simulated current density distribution in the 3.3 kV SiC planar MOSFETs at different $V_{\rm G}$ and $V_{\rm SD}$ conditions.

experimental *I*–*V* curves in the first and third quadrants. In this section, we present the simulation results of 3.3 kV SiC MOSFETs, as 3.3 kV SiC MOSFET shows a $V_{\rm BD-on}$ (∼8 V) higher than the $V_{\rm knee}$ of PN junction (∼3 V) but still within the normal $V_{\rm SD}$ operating range.

Fig. 5 shows the simulated current density distribution in the 3rd-quad conduction of 3.3 kV SiC MOSFETs. As shown in Fig. 5(a), at $V_{\rm G}$ of −5 V and $V_{\rm SD}$ of 4 V, the current flows entirely through the body diode. Fig. 5(b) and (c) shows the simulated current density at $V_{\rm G}$ of 5 V ($> V_{\rm th}$). At $V_{\rm SD}$ of 4 V, the body diode does not turn ON, validating the delayed body-diode turn-ON. At $V_{\rm SD}$ of 12 V, the body diode turns ON, showing parallel conduction through the MOS channel and the body diode. Fig. 5(d)–(f) shows the simulated current density at $V_{\rm G}$ of 0 V. As shown in Fig. 5(d), the NPN "surface channel" turns ON at $V_{\rm SD}$ of 2.5 V and the body diode is still OFF. After this "surface channel" turns ON, at $V_{\rm SD}$ of 4 V, the body diode keeps OFF [see Fig. 5(e)], validating the delayed body diode turn-ON due to the potential distribution set by the conducting "surface channel". At $V_{\rm SD}$ of 12 V, the body diode is ON, and the current shows parallel conduction in both channels. These simulation results are consistent with experimental results shown in Fig. 2(b) and (e) and validated our theoretical explanations.

III. Device Models for 3rd-Quad Behaviors

The objective of this section is to develop easy-to-use analytical models to describe and predict the $V_{\rm 3rd}$ of SiC planar MOSFETs with different voltage classes, at a negative $V_{\rm G}$ and a $V_{\rm G} > V_{\rm th}$, the two gate-bias controls usually used in power

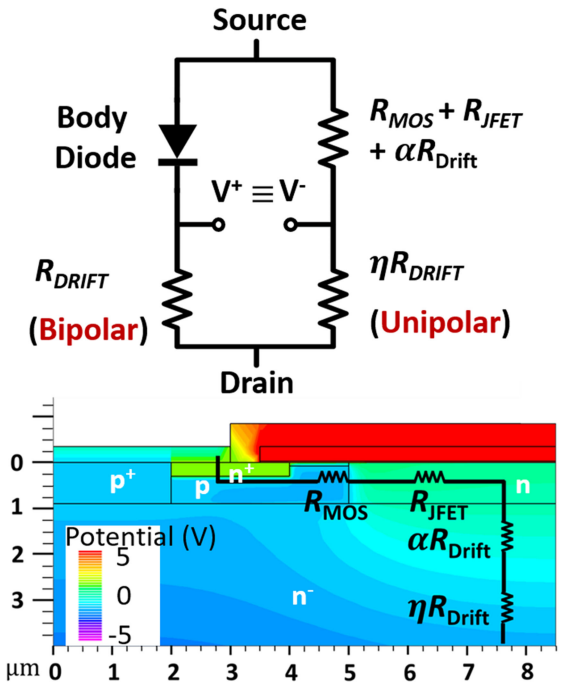

Fig. 6. (Top) Equivalent circuit for the 3rd-quad conduction of SiC planar MOSFET. R_{DRIFT} have different values for the unipolar and bipolar conduction. (Bottom) Simulated potential distribution in the top region of 3.3 kV SiC MOSFET at 5 V V_G. Major resistance components are marked.

converters. While the V_{3rd} at a negative V_G is merely the forward voltage drop of the PN diode, the V_{3rd} at $V_G > V_{th}$ is much more complicated. The key is to model V_{3rd} at $V_G > V_{th}$ is to obtain V_{BD-on}. To this end, we will first extend the V_{BD-on} model based on (4) to establish a correlation between V_{BD-on} and the device voltage rating (or breakdown voltage).

A. $V_{BD\text{-}on}$ Estimation

According to the theories developed in Section II, an equivalent circuit model for the 3rd-quad current conduction in planar MOSFETs is developed, as shown in Fig. 6. All the resistance components listed are the specific values ($\Omega \cdot \mathrm{cm}^2$) normalized with respect to the device die size or active region. Fig. 6 shows the simulated potential distribution within the device at $V_G > V_{th}$. When compared to the approximate model shown in Fig. 3, the equipotential lines originated from the PN junction penetrate into the drift region rather than extend laterally along the lower boundary of the JFET region. This is due to the current spreading effect and suggests that a portion of R_{DRIFT} (defining the portion as α) needs to be accounted for when calculating the voltage drop across the PN junction [i.e., V^+ and V^- in Fig. 6(a)]. Equation (4) can be rewritten as

$$V_{BD-on} = V_{knee} R_{ON}/(R_{MOS} + R_{JFET} + \alpha R_{Drift}) \ \ (\alpha < 1). \tag{5}$$

Defining $\eta = 1 - \alpha$, (5) is transformed into

$$\begin{aligned} V_{BD-on} &= V_{knee}/[(R_{MOS} + R_{JFET} + \alpha R_{Drift})/R_{ON}] \\ &= V_{knee}/[(R_{ON} - \eta R_{DRIFT})/R_{ON}] \\ &= V_{knee}/(1 - \eta R_{DRIFT}/R_{ON}) \cdot (\eta < 1). \end{aligned} \tag{6}$$

In (6), V_{knee} and R_{ON} can be extracted from the datasheet or the static *I–V* characteristics. To separate R_{DRIFT} from R_{ON}, all the three major components of R_{ON} are modeled as follows.

Assuming the MOSFET operates in the linear region, R_{MOS} is proportional to the reciprocal of the gate overdrive

$$R_{MOS} \propto 1/(V_G - V_{th}) \tag{7}$$

where V_{th} is the threshold voltage extracted from the device datasheets or static transfer characteristics.

R_{JFET} depends on the geometry and doping concentration of the JFET region [15] and usually is not disclosed in the datasheets. As R_{JFET} is not dependent on the device voltage rating and is usually a very small component in the R_{ON} of high-voltage devices, we approximate R_{JFET} as a constant value

$$R_{JFET} = \text{cons.} \tag{8}$$

Note (8) is not the most accurate assumption, but neither a bad one, particularly for devices from the same manufacturer. Even for the devices from different manufactures, the reported specific R_{JFET} in the literature shows variations in a quite limited range. The reported JFET region designs in 1.2 kV [16], [17], 3.3 kV [18], [19], 10 kV [20], [21], and 13 kV [22] SiC planar MOSFETs have a similar JFET depth of 0.7–1 μm, a JFET width to cell pitch ratio of 0.2–0.3, and a doping concentration of 1–2 $\times$ 10^{16} cm^{-3}. Based on these parameters, the resulted variations in the specific R_{JFET} of the devices with different voltage ratings are usually negligible compared to the R_{DRIFT} that increases significantly with the increased voltage rating.

The specific resistance of the ideal unipolar drift region increases with the square of breakdown voltage (V_{BV}) [23]. The drift region resistance in the state-of-the-art high-voltage SiC MOSFETs is very close to this theoretical limit [1]. Therefore, R_{DRIFT} can be approximated as

$$R_{DRIFT} \propto V_{BV}^2 \tag{9}$$

where the V_{BV} for 1.2–10 kV-rated SiC MOSFETs can be extracted from [1] or simply approximated with a 20% margin over the device voltage rating.

Finally, the correction factor η is tuned to match the experimental $V_{BD\text{-}on}$ extracted at different V_G for each device. For example, as shown in Fig. 7, with an η of 0.80, the modeled $V_{BD\text{-}on}$ of 3.3 kV SiC MOSFETs agrees well with experiment over a wide range of V_G, whereas no correction ($\eta = 1$) leads to overestimation in $V_{BD\text{-}on}$. The η values fitted from experimental data for 1.2 kV and 3.3 kV SiC MOSFETs were also validated with the simulated potential distribution in each device.

Table I summarizes the estimated $V_{BD\text{-}on}$ from the abovementioned analytical models for 1.2, 3.3, and 10 kV devices. The modeled $V_{BD\text{-}on}$ agrees with the experimental data for 1.2 kV and 3.3 kV MOSFETs. In addition, the model predicts a $V_{BD\text{-}on}$ of 28–66 V in 10 kV MOSFETs at V_G of 5–15 V, by using a $\eta \approx 0.97$, which is extracted from the simulated potential distribution in 10 kV MOSFETs. This is consistent with the experimental results shown in Fig. 2(f) that the body diode does not turn ON up to V_{SD} of 16 V. The modeled $V_{BD\text{-}on}$ suggests that, once the

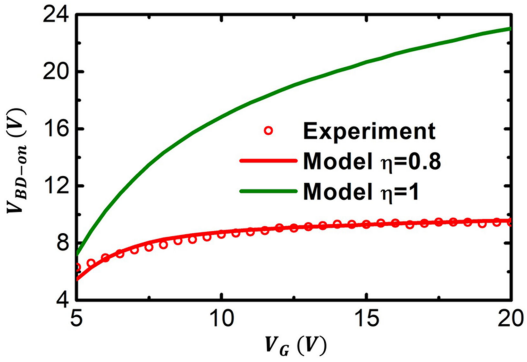

Fig. 7. VBD-ON extracted from static tests at 175 °C and from the device model. With an $\eta = 0.8$ correction, the model agrees with experiment.

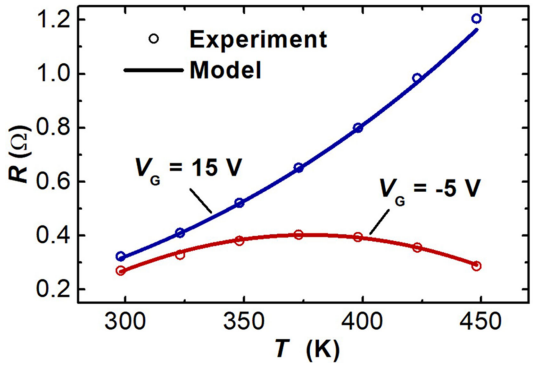

Fig. 8. Differential resistance of the MOS channel path ($V_G = 15$ V) and the body diode path ($V_G = -5$ V) extracted from experimental data and analytical models at different temperatures.

TABLE I
$V_{BD\text{-}on}$ FROM EXPERIMENTS AND MODELS

Voltage Rating (kV)	η	V_{GS} (V)	$V_{BD\text{-}on}$ (exp) (V)	$V_{BD\text{-}on}$ (model) (V)
1.2	0.6	5	3.17	3.30
		10	3.20	3.32
		15	3.30	3.36
3.3	0.8	5	6.32	5.47
		10	8.62	8.77
		15	9.31	9.31
10	0.97	5	N/A	28.14
		10	N/A	52.12
		15	N/A	65.86

MOS channel is ON, the body diode of 10 kV MOSFETs will not turn ON under practical 3rd-quad conditions. The fundamental root cause of the high $V_{\text{BD-on}}$ in 10 kV MOSFETs is the much larger R_{DRIFT} when compared to the channel/JFET resistances. As a very thick and low-doped drift region is always required for a high-voltage MOSFET, a very high $V_{\text{BD-on}}$ is expected to be universal in all 10 kV SiC planar MOSFETs instead of being manufacturer specific.

It can be seen in Table I that the fitted η value increases with the device voltage rating, which shows its physical significance. The equipotential lines penetrating from the PN junction into the drift region varies very little in the devices with different voltage ratings, while the R_{DRIFT} increases with the device voltage rating. This leads to a smaller α and a closer-to-unit η for higher voltage devices.

It is important to note that existing SPICE circuit models for SiC planar MOSFETs simply put a MOSFET in parallel with the body diode, which do not capture the impact of the MOS channel conduction on the body-diode turn-ON. The model proposed in this article provides a more accurate description of the 3rd-quad behavior of SiC MOSFETs and can be easily implemented in circuit-based simulations.

B. Temperature-Dependent I–V Characteristics

The discussions in Section II suggest the importance to develop a datasheet-driven $V_{3\text{rd}}$ model for high-voltage SiC MOSFETs, which can be used to determine the optimal V_G control to minimize the 3rd-quad conduction loss at a given I_{SD} and temperature (T). In this section, we develop the $V_{3\text{rd}}$ model for Wolfspeed's third-generation 10 kV SiC MOSFETs as a case study, which also lays a foundation for the converter test in Section IV.

For model calibration, static 3rd-quad characterizations are first carried out from 25 °C up to 175 °C with a 25 °C step at V_G of 15 V and −5 V. At V_G of 15 V, as illustrated in Section III-A, the current completely goes through the MOS channel and the device R_{on} is dominated by R_{DRIFT}. Given the unipolar nature, the temperature dependence of R_{DRIFT} is mainly induced by electron mobility degradation at high temperatures, and R_{DRIFT} can be modeled as

$$R_{\text{DRIFT}}(V_G > V_{\text{th}}) = R_{\text{DRIFT},25}[(T+273)/298]^K \quad (10)$$

where $R_{\text{DRIFT},25}$ is the R_{DRIFT} at 25 °C, and K is a temperature coefficient. The value of K appears to vary with devices according to [24] and [25]. As shown in Fig. 8, K of Wolfspeed 10 kV SiC MOSFET tested in this work is fitted to be ∼3.2.

At V_G of −5 V, the current goes through the body diode. The forward voltage drop of the body diode can be described as

$$V_{3\text{rd}}(V_G = -5\,V) = V_{\text{knee}} + R_{\text{DIODE}} I_{SD} \quad (11)$$

where R_{DIODE} represents the total differential resistance of the bipolar current path through the body diode and drift region. Significant conductivity modulation has been observed in the body diode of 10 kV SiC MOSFETs [26]. Due to the bipolar nature, R_{DIODE} does not increase monotonically with temperature. At high temperatures, on the one hand, conductivity modulation is enhanced due to the increased lifetime of the injected holes, the decreased V_{knee} of PN junction, and the increased acceptor ionization in p-base [27]; on the other hand, the carrier mobility decreases due to the increased phonon scattering. As shown in Fig. 8, we found that a quadratic polynomial equation can well fit the temperature dependence of R_{DIODE} with a peak R_{DIODE} at ∼100 °C.

The temperature-dependent 3rd-quad I–V characteristics of 10 kV SiC planar MOSFETs can be well reproduced based on (10) and (11), as shown in Fig. 9. Below 75 °C, within the safe operating range of V_{SD} and I_{SD}, no intersection shows up

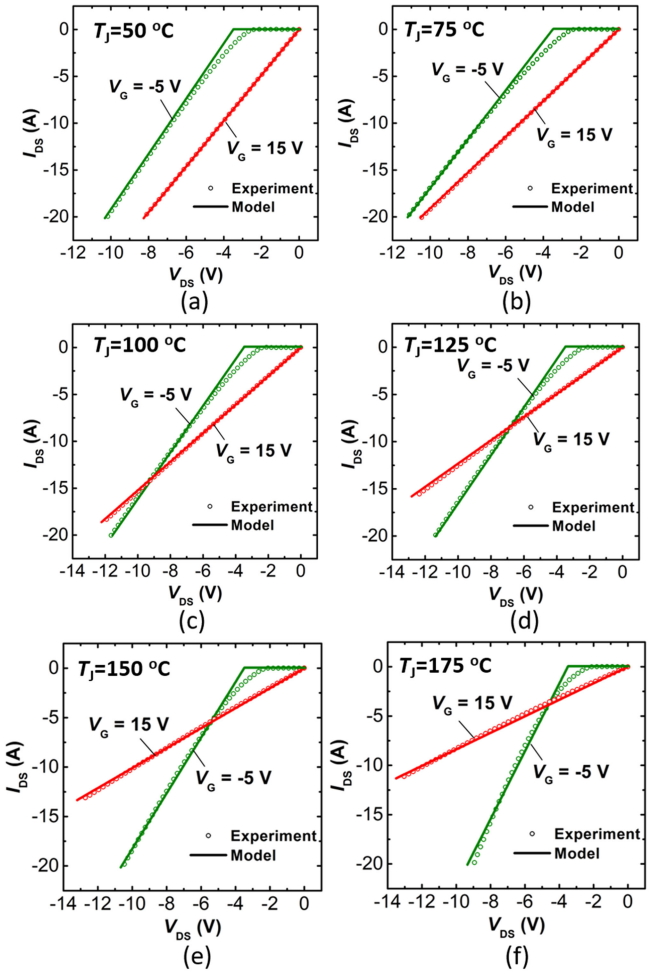

Fig. 9. Experimental (dot) and modeled (solid line) 3rd-quad I-V characteristics of the 10 kV SiC MOSFET at different junction temperatures for V_G of −5 V and 15 V.

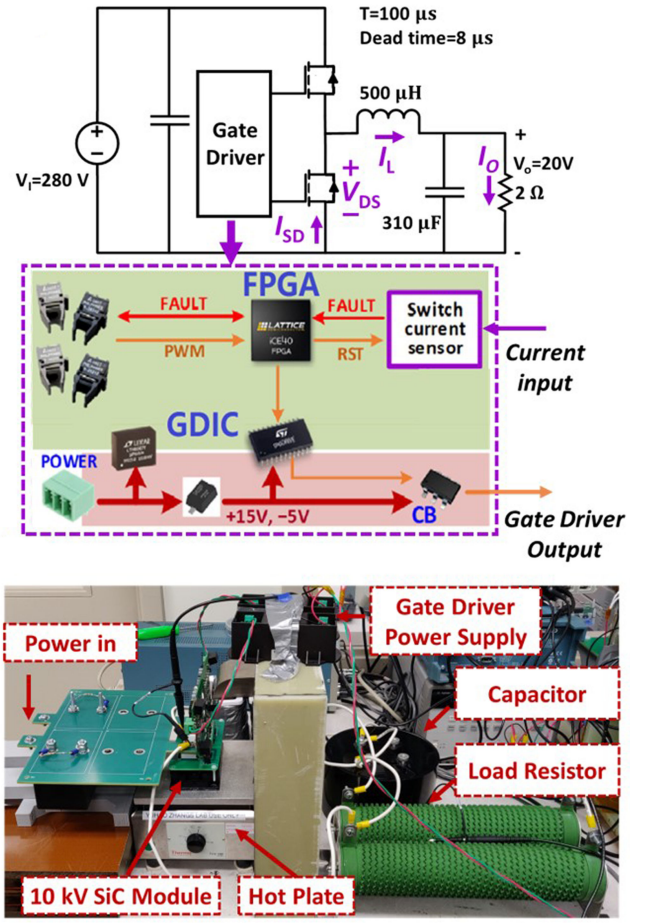

Fig. 10. (Top) Schematic of the developed buck converter using a 10 kV SiC MOSFET half-bridge module and a customized gate driver. (Bottom) Photograph of the test set up.

between V_G of −5 and 15 V. The crossing point (at ∼15 A) first appears at 100 °C and continues to drop at higher temperatures. At 175 °C, the early crossover at 4 A indicates that a negative V_G control is preferred for most of I_{SD} operation.

IV. Buck Converter Test

To further validate if a negative V_G control can lead to a smaller V_{3rd} in 10 kV SiC MOSFETs in switching conditions, a synchronous dc–dc buck converter was built up using a 10 kV SiC MOSFET half-bridge power module.

A. Test Setup

The circuit schematic and the test setup are shown in Fig. 10. The input voltage is 280 V, and the load resistor is 2 Ω, The customized gate driver design for a 10 kV SiC MOSFET is based on the one described in [28]. The switching period is set to 100 μs. The switching frequency is 10 kHz, which is usually implemented in the hard-switching of 10 kV SiC MOSFET power modules [8], [29], [30]. The test was performed under different temperatures, and the module case temperature (T_C) was controlled by a hot plate and calibrated by a thermal camera. Device junction temperature (T_J) was estimated by

$$T_J \approx T_C + R_{\theta JC} L \tag{12}$$

where $R_{\theta JC}$ is the module junction-to-case thermal resistance, L is the power loss on the module that can be estimated by

$$L = V_{\text{in}}\, I_L D - V_{\text{out}} I_L \tag{13}$$

where I_L is inductor current, V_{in} and V_{out} are input voltage and output voltage, and D is the duty cycle of the buck converter.

At each temperature, two V_G, −5 V and 15 V, were used to control the low-side MOSFET in the 3rd-quad conduction. Due to the concern of false turn-ON [31], V_G of 0 V is rarely used in real converter applications and is, therefore, not studied in our converter tests. For V_G of 15 V, the dead time is set to 8 μs with V_G of −5 V in the dead time. Under different test conditions, the input voltage and output current were maintained at 280 V and 10 A, respectively, by modulating the buck converter duty cycle. The relatively small input voltage 280 V is chosen to minimize the switching loss in the converter test, which facilitates the measurement of the 3rd-quad voltage drop and the comparison of 3rd-quad conduction loss under different test conditions. The

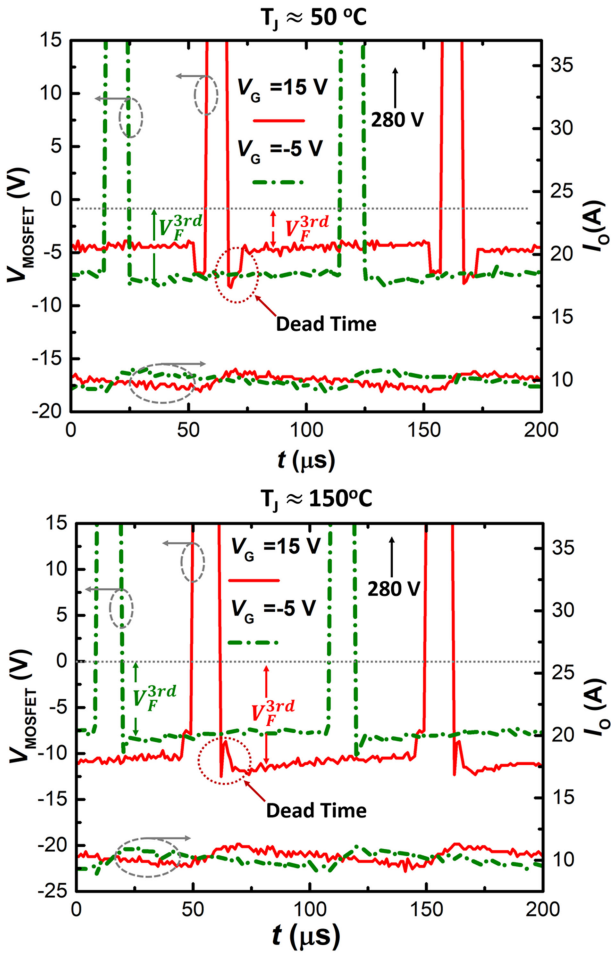

Fig. 11. Two switching periods in the waveform of the low-side MOSFET at T_J of (top) 50 °C and (bottom) 150 °C, controlled by V_G of −5 V and 15 V for the 3rd-quad conduction. Voltage waveforms are shown at the top part of each figure and the output current waveforms at the bottom part.

duty cycle (D) is chosen to be small (around 10%) to make the low-side device mainly work in the 3rd-quad conduction. During the test, the output voltage, output current, and the voltage drop on the low-side MOSFET were measured.

B. Test Results and Analysis

Fig. 11 shows two switching periods in the test waveforms of the low-side MOSFET, with V_G of −5 V and 15 V for 3rd-quad control, and at the T_J of 50 °C and 150 °C, respectively. At T_J of 50 °C, V_G of 15 V leads to lower V_{3rd}. However, at T_J of 150 °C, V_G of −5 V provides a lower V_{3rd}. This trend is consistent with our static test results and device models. Note the same reverse recovery loss is expected for two V_G controls, due to the need for dead time for the 15 V V_G control. Hence, the conduction loss determines the total loss of the low-side device. It can, therefore, be inferred that a negative V_G leads to the minimal loss for 3rd-quad operation of 10 kV SiC MOSFETs at high temperatures.

Table II shows the extracted D and V_{3rd} under different test conditions. As the output current (and power) at the load resistor is kept constant, a larger duty cycle suggests more energy provided by the input power supply and a higher power loss in the converter system. For example, at T_J of 150 °C, the duty cycle for V_G of 15 V is higher than that for V_G of −5 V, indicating a higher loss for V_G of 15 V. These converter test results verify that a negative V_G is optimal to control the 3rd-quad conduction of 10 kV SiC MOSFETs at high T_J and I_{SD}.

TABLE II
COMPARISON OF THE JUNCTION TEMPERATURE, MEASURED DUTY CYCLE, AND THIRD-QUAD VOLTAGE DROP IN DIFFERENT TESTS

T_J (°C)	V_G (V)	D	V_{3rd} (V)
50	-5	10.4%	~7
	15	9.5%	~4.5
100	-5	10.9%	~7.4
	15	10.7%	~7.2
150	-5	10.8%	~7.5
	15	11.9%	~10.5

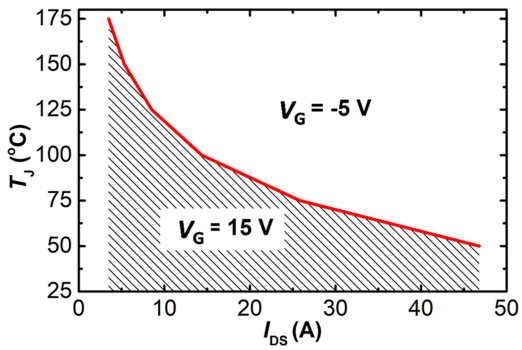

Fig. 12. T_J - I_{DS} boundary for the optimal V_G (−5 V and 15 V) that leads to the smallest V_{3rd} for the tested Wolfspeed third-generation 16 A, 10 kV SiC MOSFETs.

With a good agreement between static tests, converter tests, and device models, the optimal V_G to control the 3rd-quad conduction of 10 kV SiC planar MOSFETs can be confidently determined under different load currents and device junction temperatures. Fig. 12 shows the extracted T_J–I_{SD} boundary curve for the tested Wolfspeed third-generation 10 kV, 16 A MOSFET. The conditions above this curve call for a negative V_G control, while the ones below this curve would prefer a $V_G > V_{th}$ control for the device 3rd-quad conduction.

V. THIRD QUADRANT BEHAVIOR OF SiC TRENCH MOSFETS

Trench MOSFETs allow for a higher gate density and smaller specific on-resistance compared to the planar MOSFETs with similar voltage ratings. Up to now, SiC trench MOSFETs have been commercialized at the voltage class of 1.2 kV. Based on the device physics unveiled for planar MOSFETs, we will investigate the competing current sharing in the 3rd-quad conduction of trench MOSFETs in this section. The standard trench MOSFET structure and two commercial 1.2 kV trench MOSFETs are investigated. The discussions in this section would also be useful for the design and application of future SiC trench MOSFETs with higher voltage ratings.

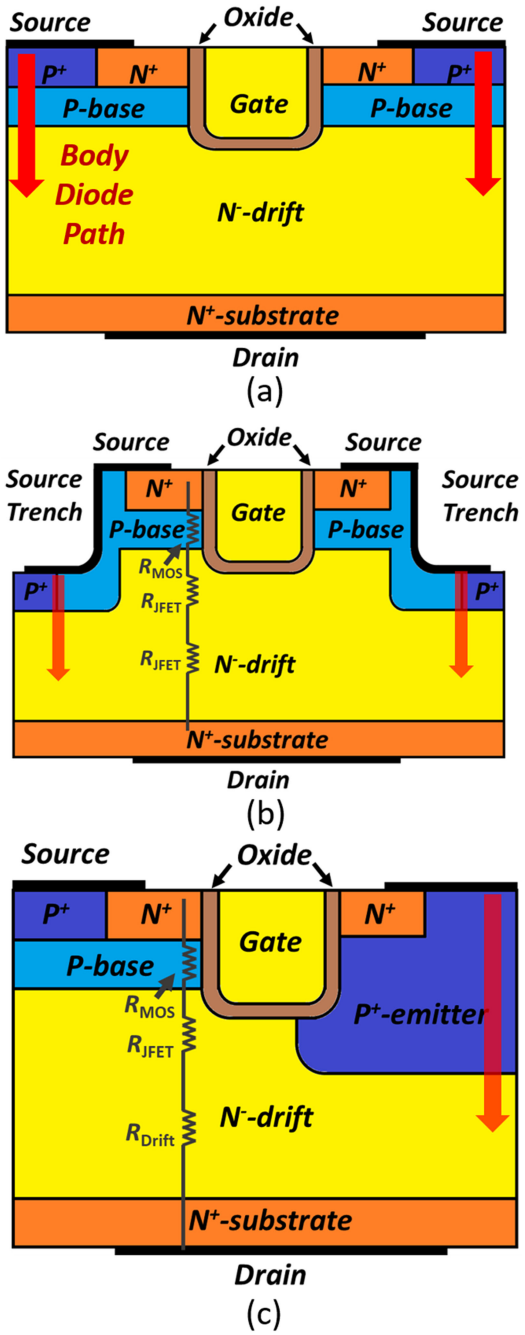

Fig. 13. Schematic of the unit-cell of (a) standard trench MOSFETs, (b) Rohm's double-trench MOSFET, and (c) Infineon CoolSiC$_{\mathrm{TM}}$ asymmetric trench MOSFETs. The body diode path is shown in each structure.

Fig. 13(a) shows the standard structure of a SiC trench MOSFET. As there is no JFET region in this structure, at $V_{\mathrm{G}} > V_{\mathrm{th}}$, the body diode turn-ON voltage can be written based on (4)

$$V_{\mathrm{BD-on}} = V_{\mathrm{knee}} \left(R_{\mathrm{MOS}} + R_{\mathrm{DRIFT}}\right) / R_{\mathrm{MOS}} = V_{\mathrm{knee}} \left[1 + R_{\mathrm{DRIFT}} / R_{\mathrm{MOS}}\right] . \quad (14)$$

From the comparison between (4) and (14), $V_{\mathrm{BD-on}}$ of trench MOSFETs is expected to be much higher than the one of planar

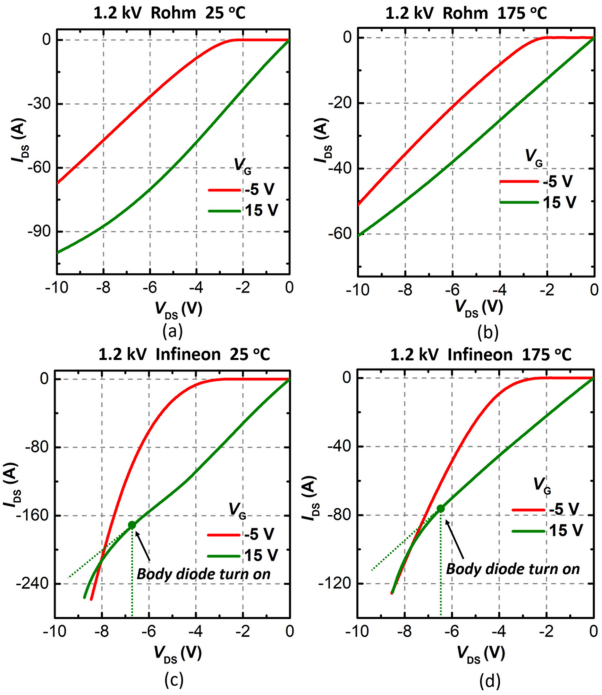

Fig. 14. 3rd-quad I-V characteristics of Rohm's double-trench MOSFETs at (a) 25 °C and (b) 175 °C. 3rd-quad I-V characteristics of Infineon's CoolSiCTM MOSFETs at (c) 25 °C and (d) 175 °C.

MOSFETs with similar voltage rating, due to the lack of R_{JFET} and a smaller R_{MOS} (as a consequence of the higher channel density). This implies that the body diode may not turn ON over the entire V_{SD} safe-operating range, and the $V_{\mathrm{G}} > V_{\mathrm{th}}$ control would lead to a completely unipolar 3rd-quad conduction.

The device structures of commercial SiC trench MOSFETs may deviate from the standard one. For example, Rohm's third-generation trench MOSFETs feature a double trench (DT) structure [32]–[34], as shown in Fig. 13(b); Infineon's CoolSiC$^{\mathrm{TM}}$ features an asymmetric structure with a deep P^{+} emitter [35], [36], as shown in Fig. 13(c). The common feature in these two structures that differs from the standard one is a source-connected P^{+} region penetrated deeply into the drift region beyond the bottom of the trench gate. This structure is designed mainly to shield the trench gate from the high electric field in the reverse biases. As the PN junction between the P^{+} emitter and the drift region is deeper than the end of the MOS channel, this deep P^{+} design would induce an effective JFET region. As a result, when calculating the $V_{\mathrm{BD-on}}$, an effective R_{JFET} needs to be added in (14), making $V_{\mathrm{BD-on}}$ equation the same as (4).

Fig. 14 shows the *I–V* characteristics of commercial 1.2 kV SiC trench MOSFETs from Rohm (SCT3080KL, 31 A rated) and Infineon (IMZ120R045M1, 52 A rated) at 25 °C and 175 °C, at V_{G} of −5 V and 15 V. At V_{G} of −5 V, the 3rd-quad conduction is through the body diode in both devices. As shown in Fig. 14(a) and (b), at V_{G} of 15 V, no body-diode turn-ON is observed at V_{SD} up to 10 V in Rohm's DT MOSFET, and therefore, the 3rd-quad characteristics are symmetric to the 1st-quad characteristics (including the current saturation at high V_{SD}). This implies a $V_{\mathrm{BD-on}}$ higher than 10 V in Rohm's devices. As shown in

Fig. 14(c) and (d), at $V_{\rm G}$ of 15 V, the body diode turns ON at $V_{\rm SD}$ of $\sim$7 V in Infineon's devices. The larger $V_{\rm BD-on}$ in Rohm's devices compared to the one in the Infineon's can be attributed to the wider effective JFET region in the device unit-cell ($\sim$3 μm in Rohm's device versus $\sim$1 μm in Infineon's device [37]) and, therefore, a smaller effective $R_{\rm JFET}$. It should be noted that $V_{\rm BD-on}$ of Infineon's 1.2 kV trench MOSFETs ($\sim$7 V) is larger than that of the 1.2 kV planar MOSFETs [$\sim$3.5 V, as shown in Fig. 2(d)], due to the inherently smaller $R_{\rm MOS}$ and effective $R_{\rm JFET}$ in trench MOSFETs.

In summary, although the 3rd-quad characteristics of SiC trench MOSFETs show a dependence on specific device structures, their $V_{\rm BD-on}$ is generally expected to be larger than the one of the planar MOSFETs with the same voltage rating. While $V_{\rm G}$ of 15 V generally gives smaller $V_{\rm 3rd}$ for 1.2 kV SiC trench MOSFETs in the normal current operating range, the 3rd-quad conduction of future higher voltage (e.g., 2.5, 3.3 kV, etc.) SiC trench MOSFETs could be similar to that of 10 kV planar MOSFETs. A negative $V_{\rm G}$ is probably optimal to control the 3rd-quad conduction of higher voltage SiC trench MOSFETs at high junction temperatures and high load currents.

Meanwhile, if $V_{\rm G} > V_{\rm th}$ is preferred in some applications, a larger effective $R_{\rm JFET}$ would facilitate to reduce $V_{\rm BD\text{-}on}$ and $V_{\rm 3rd}$, which, however, increases the total $R_{\rm on}$. For $V_{\rm G} > V_{\rm th}$, there will be a tradeoff between the device $R_{\rm on}$ and the 3rd-quad conduction loss. This tradeoff needs to be carefully considered in the design of future high-voltage trench MOSFETs.

VI. Conclusion

This article presents the first comparative study on the 3rd-quad behaviors of 1.2, 3.3, and 10 kV SiC MOSFETs, with the focus on understanding the competing current sharing between the MOS channel and the body diode at different $V_{\rm G}$. At $V_{\rm G} > V_{\rm th}$, the body diode was found to turn ON at a much higher $V_{\rm SD}$ than the built-in potential of the PN junction in higher voltage SiC planar MOSFETs. Comprehensive device physics accounting for this phenomenon has been revealed and validated by TCAD simulation. Analytical models have been developed to correlate $V_{\rm BD-on}$ with the device voltage rating, which demonstrates that the body diode would not turn ON with the MOS channel in 10 kV SiC planar MOSFETs in the practical $V_{\rm SD}$ range. Then, the 3rd-quad conduction and voltage drop of 10 kV SiC planar MOSFETs are carefully studied by the static tests, device modeling, and converter tests. It is found that, in contrast to the optimal $V_{\rm G}$ control for 1.2 kV MOSFETs, a negative $V_{\rm G}$ would lead to smaller $V_{\rm 3rd}$ and conduction loss for 10 kV MOSFETs at high junction temperatures and load currents. Finally, the 3rd-quad characteristics of trench MOSFETs are discussed. This work provides new insights into understanding the 3rd-quad behaviors of SiC MOSFETs as well as the key guidelines for their circuit applications.

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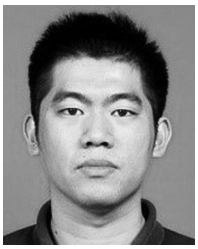

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