Novel Series *LC* Resonance-Pulse-Based ZCS Current-Fed Full-Bridge DC–DC Converter: Analysis, Design, and Experimental Results

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***Abstract*—A current-fed full-bridge converter availing series resonance pulse to enable zero-current switching (ZCS) and voltage clamping of the semiconductor devices is proposed. Overlap in switching states of the devices enforces a short resonance pulse, due to series tank which naturally reduces the current to zero in the outgoing semiconductor devices. It causes zero-current commutation of the devices eliminating voltage spike across the semiconductor devices. Essentially, pulse-resonance offers reduced circulating current resulting in lower conduction losses and not demanding overrated components. The proposed converter enables ZCS for wide variation in source voltage by implementing variable frequency fixed duty modulation eliminating the traditional requirement for additional clamping circuitry in conventional current-fed converters. Detailed experimental results on proof-of-concept hardware prototype rated at 500 W are demonstrated to verify the proposed claims and converter performance. With all other merits, proposed converter maintains high efficiency.**

***Index Terms*—Current-fed dc–dc converter, series resonance, zero-current switching.**

I. Introduction

THE accelerating pace of electrification via renewable energy sources is shifting focus toward decarbonization and distributed generation with the potential to combat increasing environmental crisis and to promote sustainable development. Renewable technologies in a number of industries provide the electricity demand locally that reduces the power loss by eliminating unnecessary conversion stages and, ultimately, lower energy costs. Therefore, dc microgrid is gaining popularity due to reduced conversion stages, energy efficient, and the less complex system. Sources such as photo-voltaic (PV)/fuel-cells along with additional energy storage exhibit huge potential for dc microgrid applications like dc modern data center (operating at 380 V), auxiliary battery charging system, solar water pumping system, railway loads, and light emitting diode (LED) street lights. These applications require nearly steady power demand at constant dc-bus voltage throughout their operation. However, owing to the challenges of low dc voltage output and intermittent characteristics, utilizing alternative energy sources like PV/fuel-cells for such applications, require a power conditioning unit for the efficient utilization of the source as well as to maintain regulated dc voltage at the load terminal under varying source voltages. Hence, isolated dc–dc converter with exceptionally high-voltage gain, low source current ripple, unidirectional power flow, galvanic isolation, and high efficiency is essential to boost-up the voltage required to feed different dc and ac loads.

Boost derived current-fed converter seems to be a more viable solution as compared to the voltage-fed counterpart for such applications owing to its inherent high-voltage gain capability, low input current ripple, and short-circuit protection due to the presence of large input inductor [2], [3]. However, hard-switching semiconductor devices and large voltage spike across the semiconductor devices at turn-OFF considerably reduces the conversion efficiency and limits high-frequency (HF) operation. Therefore, to overcome these impediments, current-fed topologies with novel soft-switching techniques are encouraged to implement high-efficiency, high-power density, and light weight system.

Traditionally dissipative snubbers were adopted to alleviate the historic problem of large voltage overshoot across semiconductor devices at their turn-OFF while compromising on the conversion efficiency [4], [5]. Moreover, snubber-based topologies are generally hard switched limiting their operation at low frequency. On the other hand, active clamping employs additional floating controlled devices and a large HF capacitor to reroute the leakage energy to achieve zero voltage switching (ZVS) of the semiconductor devices. It results in better efficiency, yet the use of active clamping circuits is avoided because of the higher current stresses experienced by the components, increased cost, increased circuit complexity, and reduction in the boost capacity [6]–[10], [11], [12]. Concept of snubberless natural-commutation and device voltage clamping through load-side controlled devices for half-bridge current-fed topology has been introduced in [13]. It retains the converter boost capacity and accomplishes full-range soft-switching of the semiconductor devices. However, the additional load-side controlled devices increases the cost and complexity of the converter while restricting its usage for bidirectional applications only. Authors

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have extended this concept to current-fed full-bridge [14] and push–pull configurations. Push–pull configuration has a merit as it requires single boost inductor and two controlled devices with common ground needing simplified gate driving circuit [15].

With the expectation to further improve the efficiency and reduce the size of the converter by means of HF operation, a wide category of resonant converters were introduced. This facilitated the sinusoidal voltage/current to achieve ZCS or ZVS of the semiconductor devices with its inherent ability to utilize the circuit parasitic. However, these converters suffer from high circulating and peak currents compelling the use of over-rated components. This is true for both voltage-fed and current-fed resonant converter. This article focuses on current-fed literature only. Current-fed resonant converters with fixed-frequency modulation to achieve ZCS of the devices exhibit difficulty in preserving the full-range ZCS for source voltage and load current variations as reported in [16]. In [17], current-fed converter utilizing multiresonant tank to achieve low circulating energy and ZCS of the switches is presented. Concept of self-adaptable resonant energy is presented for current-driven full-bridge converter with *LCL* resonance in [18] and series *LC* resonance in [19], where ZCS is obtained by incorporating a switched-capacitor snubber utilizing two additional active switches. Although, the switches are soft-commutated, the advantage is offset by some drawbacks, such as hard-switching for wide variation in source voltage, high component count, and increased cost and complexity.

To further minimize the peak current stress, conduction loss, and extend the soft-switching range, research is recently inclined toward quasi-resonant converters. Researchers have demonstrated and justified the concept of impulse-commutation for variable frequency controlled current-fed full-bridge [20], half-bridge [21], and push–pull [22] configurations, where resonance occurs between the leakage inductance and the parallel resonant capacitor for a short duration to achieve ZCS turn-OFF and voltage clamping of the semiconductor devices. Resonant capacitor stores full-load resonant energy under all operating conditions due to its shunt connection and, therefore, requires a finite time to charge the capacitor in every half-switching cycle resulting in duty-cycle loss. Also, due to fixed resonant energy, significantly large portion of that energy circulates through components at light-load conditions resulting in high conduction losses and, hence, lower light-load efficiency. In addition, a large frequency variation is witnessed for the slight variation in the source voltage. This concept is extended to three-phase configurations for high-power applications, as reported in [23] and [24]. Adaptive resonant energy in full-bridge (FB)-ZCS dc–dc converter using *LCC* (dual-capacitor) circuit is introduced in [25]. The research and investigation done and reported so far belongs to parallel resonance-pulse based ZCS current-fed converters. However, a series resonance-pulse assisted ZCS concept for current-fed topologies has not yet explored. Initial simulation results and investigation on the proposed series resonance-pulse concept are reported in [26].

This article investigates a series *LC* resonant-pulse assisted current-fed full-bridge topology with voltage-doubler configuration for achieving ZCS and voltage clamping of the semiconductor switches utilizing series *LC* resonance during switching

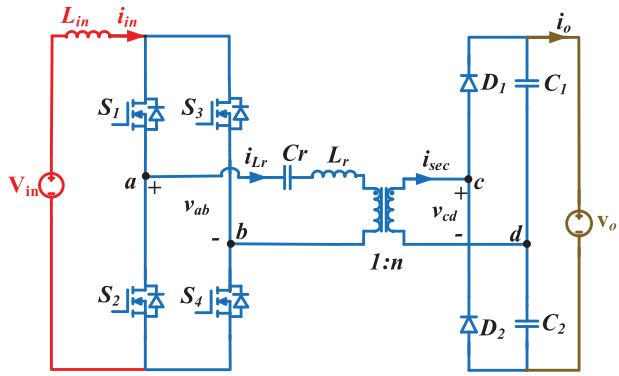

Fig. 1. Proposed series-*LC* resonant-pulse current-fed full-bridge dc–dc converter with voltage doubler.

overlap time. Moreover, owing to the load-dependent resonant energy due to series placed resonant capacitor, lower peak currents, and lower $I_{\mathrm{Lrp}}/I_{\mathrm{in}}$ ratio are observed due to low resonant energy for output power below the rated power. The proposed converter maintains regulated output voltage for wide variation in source voltage (30–58 V) exhibiting a short switching frequency range.

Considering the aforementioned advantages, the proposed converter is a viable solution for utilizing low-voltage sources like PV/fuel-cell for battery charging and constant power motor drive applications, for example, solar water pumping system. Converter operation and detailed steady-state analysis is briefed in Section II. Variable frequency control with fixed duty is employed to achieve the desired ZCS operation over wide range of source voltage. Systematic converter design to achieve desired objective is explained in Section III. A proof-of-concept laboratory prototype rated at 500 W is developed and tested to demonstrate the converter performance and verify the expected claims. Experimental results are discussed in Section IV.

II. Operation and Analysis of the Proposed Converter

The proposed series resonance-pulse current-fed full-bridge voltage doubler circuit is shown in Fig. 1. Series resonance exploits the transformer leakage inductance and a series capacitor to achieve soft-switching. Output voltage regulation is achieved by implementing variable frequency control for wide range of source voltage for a constant load application. Fixed duty cycle (D) is chosen such that it provides adequate time to ensure soft-commutation for all the operating conditions. Moderate frequency variation is observed for the entire range of the source voltage allowing relatively easy control implementation and simpler magnetic design as compared to the converters with wide switching frequency variation. Fig. 2 shows the steady-state operating waveforms of the converter with $D > 0.5$. Switch pairs S_1, S_4 and S_2, S_3 are modulated with gate signals 180° phase shifted having a small overlap. For the simplified analysis, the following assumptions are made.

1) Sufficiently large value of boost inductor is chosen to maintain low ripple current at the input.
2) All semiconductor devices are ideal and lossless.

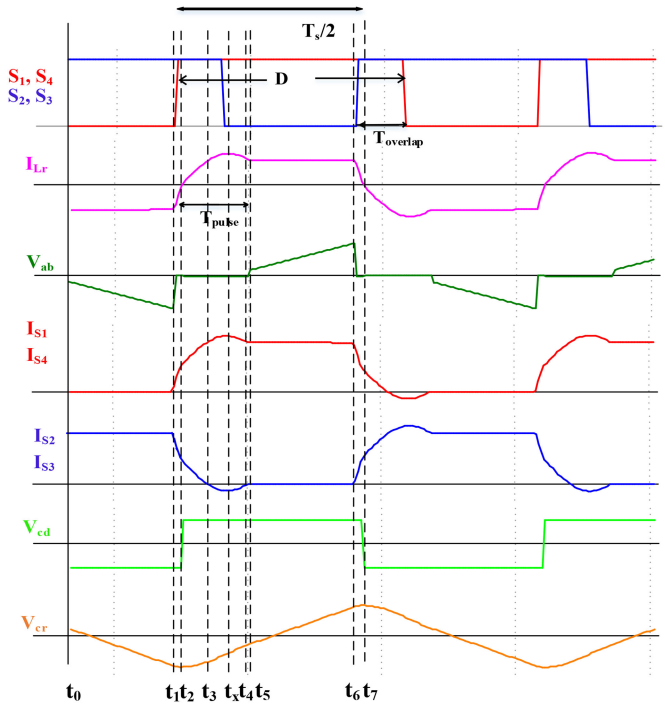

Fig. 2. Steady-state operating waveforms of the proposed converter topology.

3) The output filter is large enough to maintain the constant output voltage.
4) High value of magnetizing inductance of HF transformer is considered.

Analysis has been studied for the half-switching cycle over five time intervals, as depicted in Fig. 3. Mathematical expressions assist in determining components ratings and validate theoretical converter performance.

A. *Interval 1 ($t_0 - t_1$): [Refer Fig. 3(a)]*

During $t_0 - t_1$ switches S_2 and S_3 are conducting allowing negative current through the transformer primary. Power is transferred to the load through diode D_2 and C_1, as shown in Fig. 3(a) with a negative voltage across the transformer $(-\frac{V_o}{2n})$. During this interval, the series resonant capacitor is discharged due to negative current through the resonant tank resulting in linearly decreasing bridge output voltage

$$i_{\mathrm{Lr}}(t) = -I_{\mathrm{in}} \tag{1}$$

$$i_{S2}(t) = i_{S3}(t) = I_{\mathrm{in}} \text{ and } i_{S1}(t) = i_{S4}(t) = 0 \tag{2}$$

$$V_{\mathrm{cr}}(t) = V_{\mathrm{cr}}(t_o) + \frac{1}{C_r}\int_{t_o}^{t} -I_{\mathrm{in}} dt \tag{3}$$

$$\text{At instant } t = t_1, \quad V_{\mathrm{cr}}(t_1) = V_{\mathrm{cr1}} = V_{\mathrm{cr}}(t_o) - \frac{I_{\mathrm{in}}}{C_r} T_{10} \tag{4}$$

$$V_{\mathrm{ab}}(t_1) = \left(V_{\mathrm{cr1}} - \frac{V_o}{2n}\right). \tag{5}$$

And voltage V_{ab} clamped to zero at the end of this interval.

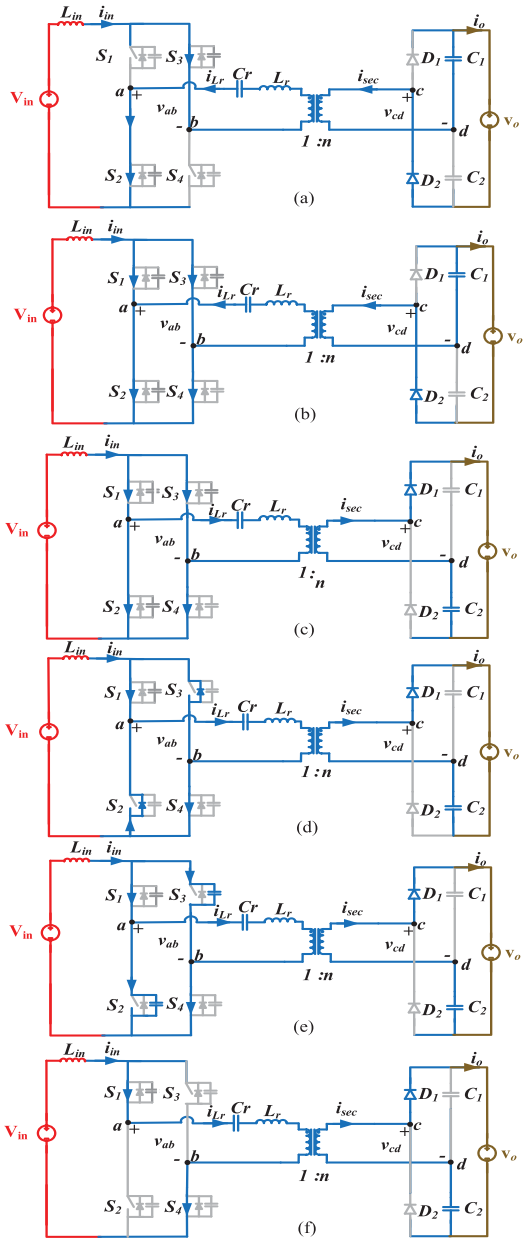

Fig. 3. Equivalent circuits of the proposed converter for different intervals of operation.

B. *Interval 2 ($t_1 - t_2$): [Refer Fig. 3(b)]*

At instant t_1, switches S_2 and S_3 are already conducting while S_1 and S_4 are turned-ON and the device capacitance across switches discharges rapidly in a short time. Now, the current in the incoming switch pair S_1, S_4 starts increasing while the current through pair S_2, S_3 starts dropping that can be expressed as

$$i_{\mathrm{Lr}}(t) = -I_{\mathrm{in}} + \frac{1}{L_r}\left(\frac{V_o}{2n} - V_{\mathrm{cr}}(t)\right)(t - t_1) \tag{6}$$

$$i_{S2}(t) = i_{S3}(t) = I_{\mathrm{in}} - \frac{1}{2L_r}\left(\frac{V_o}{2n} - V_{\mathrm{cr}}(t)\right)(t - t_1) \tag{7}$$

$$i_{S1}(t) = i_{S4}(t) = \frac{1}{2L_r}\left(\frac{V_o}{2n} - V_{\mathrm{cr}}(t)\right)(t - t_1) \tag{8}$$

$$V_{\rm cr}(t) = V_{\rm cr}(t_1) - \frac{I_{\rm in}}{2C_r}(t - t_1). \tag{9}$$

Current through the transformer primary increases linearly and reaches to zero at end of this mode

$$i_{\rm Lr}(t_2) = 0, \quad V_{\rm ab}(t_2) = 0 \tag{10}$$

$$V_{\rm cr}(t_2) = -V_{\rm crp} = V_{\rm cr1} - \frac{I_{\rm in}}{2C_r}T_{21}. \tag{11}$$

From (6) and (10), time duration T_{21} can be computed as

$$T_{21} = \frac{I_{\rm in}L_r}{\frac{V_o}{2n} - V_{\rm cr}(t_2)}. \tag{12}$$

Peak value of the series resonant capacitor charge can be estimated using the following equation:

$$V_{\rm cp} = \frac{I_{\rm in}}{2C_r\, f_s}\left(1 - f_n\left(1 - \frac{1}{\pi}\sin^{-1}\left(\frac{I_{\rm in}Z_r}{V_{\rm eq}}\right) + \frac{I_{\rm in}Z_r}{2\pi V_{\rm eq}}\right)\right) + \frac{V_o}{2n}. \tag{13}$$

C. Interval 3 ($t_2 - t_3$): [Refer Fig. 3(c)]

During this mode all the switches are conducting. At instant t_2, the transformer current changes its polarity and the primary reflected voltage is clamped to $\frac{V_o}{2n}$ causing diode D_1 to conduct. Resonance between L_r and C_r results in sinusoidally increasing current through switch pair S_1, S_4 while current through switch pair S_2, S_3 decreases in the same manner. The resonant frequency f_r and characteristics impedance Z_r is given as

$$f_r = \frac{1}{2\pi\sqrt{L_rC_r}}, \quad Z_r = \sqrt{\frac{L_r}{C_r}} \tag{14}$$

$$i_{\rm Lr}(t) = \frac{1}{Z_r}\left(\frac{V_o}{2n} - V_{\rm cr}(t_2)\right)\sin(\omega_r(t - t_2)) \tag{15}$$

$$i_{s1}(t) = i_{S4}(t) = \frac{I_{\rm in}}{2} + \frac{1}{2Z_r}\left(\frac{V_o}{2n} - V_{\rm cr}(t_2)\right)\sin\omega_r(t - t_2) \tag{16}$$

$$i_{S2}(t) = i_{S3}(t) = \frac{I_{\rm in}}{2} - \frac{1}{2Z_r}\left(\frac{V_o}{2n} - V_{\rm cr}(t_2)\right)\sin\omega_r(t - t_2) \tag{17}$$

$$V_{\rm cr}(t) = \left(\frac{V_o}{2n} + V_{\rm cr}(t_2)\right) * \cos(\omega_r(t - t_2)). \tag{18}$$

At the end of this mode, resonant current $i_{\rm Lr}$ reaches $I_{\rm in}$ while the current through switchs S_2, S_3 reaches zero

$$i_{\rm Lr}(t_3) = I_{\rm in} \tag{19}$$

$$i_{S2}(t_3) = i_{S3}(t_3) = 0. \tag{20}$$

From (15) and (20), time duration of this mode can be computed as

$$T_{32} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{I_{\rm in}Z_r}{\frac{V_o}{2n} + V_{\rm crp}}\right). \tag{21}$$

D. Interval 4 (t_3–t_4): [Refer Fig. 3(d)]

During this mode, the resonance initiates between L_r and C_r with all switches conducting. A positive voltage across the resonant inductor causes transformer primary current to overpass $I_{\rm in}$. This additional current allows body diode conduction leading to ZCS turn-OFF of device S_2 and S_3. During this mode, resonant current reaches its peak value at instant t_x that can be estimated as

$$I_{\rm LrP} = i_{\rm Lr}(t_x) = \frac{1}{Z_r}\left(\frac{V_o}{2n} + V_{\rm crp}\right). \tag{22}$$

And for ZCS operation, $I_{\rm Lr\_peak} > I_{\rm in}$ which implies

$$Z_r < \frac{\left(\frac{V_o}{2n} + V_{\rm crp}\right)}{I_{\rm in}}. \tag{23}$$

Resonance period terminates at instant t_4 and current $I_{\rm Lr}$ again reduces to $I_{\rm in}$. At instant t_4, switchs S_1 and S_4 take over and the power is transferred to the load through diode D_1 and C_2

$$i_{\rm Lr}(t_4) = I_{\rm in}. \tag{24}$$

From (21), (22), and (25), time duration of this mode can be computed

$$T_{42} = \frac{1}{\omega_r}\left(\pi - \sin^{-1}\left(\frac{I_{\rm in}Z_r}{\frac{V_o}{2n} + +V_{\rm crp}}\right)\right) \tag{25}$$

$$T_{43} = T_{42} - T_{23}. \tag{26}$$

E. Interval 5 ($t_4 - t_5$): [Refer Fig. 3(e)]

At t_4, current $i_{\rm Lr}$ reaches $I_{\rm in}$ and switches S_2 and S_3 have been turned-OFF with ZCS, the device capacitance across the switches gets charged and the switch voltage $V_{\rm DS}$ for the two switches build up

$$i_{\rm Lr}(t_4) = I_{\rm in}, \; i_{S1}(t_4) = i_{S4}(t_4) = I_{\rm in} \tag{27}$$

$$i_{S2}(t_4) = i_{S3}(t_4) = 0. \tag{28}$$

Consequently, time instant t_5 onward, the operating interval repeat in the same sequence for the other half-cycle when switch pair, S_1, S_4 conduct and positive current flows through the transformer transferring the power to the load through diode D_1 and C_2, as shown in Fig. 3(f). Therefore, duration of the half-switching cycle can be considered as

$$T_{50} = T_{61} = \frac{T_s}{2}. \tag{29}$$

III. Design of the Converter

This section illustrates the systematic design procedure for the proposed converter. Optimized converter parameters are obtained to ensure output voltage regulation and soft-switching.

A. DC Voltage Gain

Gain characteristics curve in Fig. 4 depicts converter dc voltage gain variation with normalized frequency (f_n), for different values of HF transformer turns ratio. This curve allows careful selection of switching frequency range and turns ratio of the

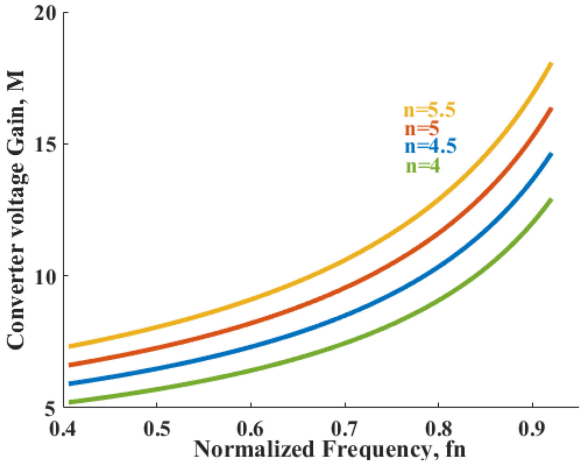

Fig. 4. Converter voltage gain characteristics curve.

transformer to provide the desired dc voltage gain for the given input voltage variation at a rated load. Utilizing power balance theory and average output current expression, a relation between input and output voltage can be obtained

$$I_{\text{in}} * V_{\text{in}} = \eta \frac{{V_o}^2}{R_{\text{FL}}} \tag{30}$$

$$I_{o,\text{avg}} = \frac{V_o}{R_{\text{FL}}} = \frac{I_{\text{Lr,avg}}}{n} = \frac{1}{n}.\frac{2}{T_s}\int_0^{T_s/2} i_{\text{Lr}}(t)\ \text{dt} \tag{31}$$

$$= \frac{2f_s}{n}\left[\int_{t_2}^{t_4} i_{\text{Lr}}(t)\ \text{dt} + \int_{t_4}^{t_6} I_{\text{in}}\ \text{dt} + \int_{t_6}^{t_7} i_{\text{Lr}}(t)\ \text{dt}\right]. \tag{32}$$

Therefore, time intervals derived in Section II and using (30) and (32), voltage gain expression in terms of control variables like f_n, V_o, V_{in}, and load R_{FL} can be estimated as

$$M = \frac{n\left(1 - \frac{f_n r_n X}{2\pi}\left(1 - \sqrt{1-k^2}\right)\right)}{\left(1 - f_n\left(1 - \frac{1}{\pi}\sin^{-1}k + \frac{k}{2\pi}\right)\right)} \tag{33}$$

where n: Turn ratio of HF transformer; $k = \frac{2M}{nr_nX}$

f_n : Normalized frequency, $= \frac{f_s}{f_r}$

r_n : Normalized load resistance, $= \frac{R_{\text{FL}}}{n^2 Z_r}$.

Consequently, output voltage regulation can be preserved by varying converter switching frequency for source voltage variation at rated load employing (33).

B. Selection of Semiconductor Devices Based on Voltage and Current Stress

1) Voltage Stress: The maximum voltage stress across the semiconductor device can be estimated from

$$V_{\text{sw1-4, rated}} = V_{\text{crp}} + \frac{V_o}{2n} \tag{34}$$

$$V_{D1} = V_{D2} = V_o. \tag{35}$$

As evident from (34), peak voltage across the primary side semiconductor devices depends on the resonant capacitor charge and turns ratio of the HF transformer. Also, the switch voltage rating is critical in optimizing switch conduction losses owing to its dependency on $R_{\text{ds,on}}$, which is intrinsic to the device rating. To further enhance the converter efficiency, rectifier diodes with low V_{FD} and low Q_{RR} were selected to minimize diode conduction losses and electromagnetic interference issues occurring at high-switching frequencies.

2) Current Stress: Root mean square (rms) current expressions for semiconductor devices and other components are given by the following expressions:

$$I_{\text{sw\_rms}} = \left[I_{\text{in}}^2\left(\frac{1}{2} - f_n\left(\frac{1}{4} - \left(\frac{1}{4k}\right)^2 + \frac{k}{6\pi}\right.\right.\right.$$
$$\left.\left.\left. - \left(\frac{\sqrt{1-k^2}}{8\pi k}\right)\right) + \frac{1}{\pi}\left(\left(\frac{1}{4k}\right)^2 - \frac{1}{2}\right)\sin^{-1}k\right)\right]^{\frac{1}{2}} \tag{36}$$

$$I_{\text{Lr\_rms}} = \left[I_{\text{in}}^2\left(1 - f_n\left(1 - \frac{1}{2}\left(\frac{1}{k}\right)^2 + \frac{2k}{3\pi}\right.\right.\right.$$
$$\left.\left.\left. + \left(\frac{\sqrt{1-k^2}}{2\pi k}\right)\right) + \frac{1}{2\pi}\left(\left(\frac{1}{k}\right)^2 - 2\right)\sin^{-1}k\right)\right]^{\frac{1}{2}} \tag{37}$$

$$I_{D1-2,\text{avg}} = I_o. \tag{38}$$

Current expressions allow analytical estimation of conduction losses in the converter for a given design specifications to validate the design parameters and, hence, converter performance.

C. Selection of HF Transformer Turns Ratio

Selection of HF transformer turns ratio (n) is such that it must deliver the desired voltage gain at desired switching frequency range while keeping the limiting the conduction losses. It is evident from (34), (36), and (37) that turns ratio also impacts voltage stress, current stress, and power dissipation on the semiconductor devices. As a result, lower turns ratio can surge the maximum voltage across the primary side switches, which compels the use of high voltage rating switches with inherently high on-state resistance escalating conduction losses. However, large turns ratio yields higher switch RMS current as evident from (36) further contributing to the conduction losses. Therefore, selection of turns ratio is critical in appropriate switch selection with minimized conduction losses. As a tradeoff, turns ratio of 5.2 is chosen for this design to meet the desired voltage gain and switching frequency.

D. Soft-Switching Boundary

Series resonant energy is utilized to achieve ZCS of the semiconductor devices under all operating conditions. Switch current must drop to zero before the gating signal is removed. In this case, resonant capacitor charge solely depends on the input current and, hence, decides the desired characteristic impedance Z_r to ensure ZCS. It can be perceived from Fig. 2 that the peak of the resonant current I_{LrP} must be greater than the input current

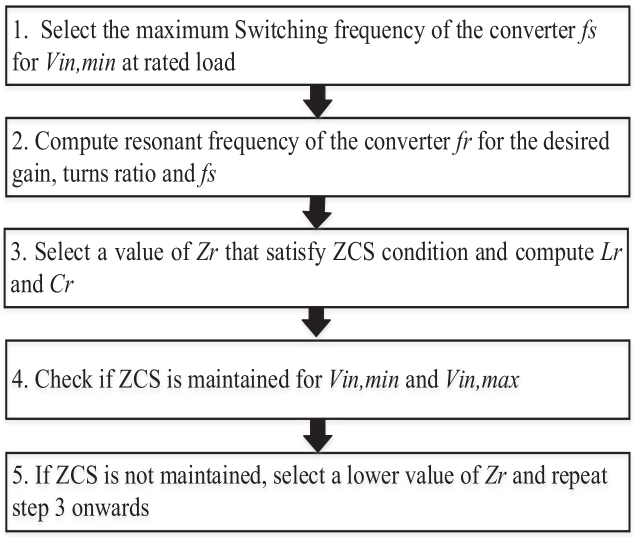

Fig. 5. Flowchart depicting the resonant tank design.

I_{in} to allow antiparallel diode conduction before the gating pulse is forced off. This condition results in the following expression:

$$Z_r < \frac{2 * \left(\frac{V_o}{2n} + V_{\text{cr}_p}\right) * \ R_{\text{FL}} * V_{\text{in}}}{{V_o}^2}. \tag{39}$$

However, selection of Z_r is a tradeoff between ZCS operating range, conduction losses, and switching frequency range. For this design example $Z_r = 6.45$ is chosen.

E. Design of the Resonant Tank Parameters

Adequate design of the resonance tank is critical in achieving full-range ZCS for wide-range input voltage with reduced circulating currents and reduced conductions losses. Characteristic impedance Z_r is computed using (39) for the maximum voltage gain with minimum source voltage at rated load. Thereafter, the resonant tank design follows the flowchart shown in Fig. 5. The values of L_r and C_r are computed to be 5.5 μH and 132 nF, respectively.

F. Duty Cycle Calculation

In the proposed converter, resonant period determines the soft-switching boundary and, hence, appropriate duty cycle can be determined to ensure wide range ZCS. This condition necessitates turn-OFF of the semiconductor devices before the resonant pulse dies out. This implies

$$T_{32} \ < \ T_{\text{overlap}} < \ T_{42} \tag{40}$$

where $T_{\text{overlap}} = \frac{2D-1}{2} T_s$.

Operating boundary for duty cycle is given by the inequality

$$0.5 + D_{12} + D_{23} < D < 0.5 + D_{12} + D_{23} + D_{34} \tag{41}$$

where D_{12}, D_{23}, and D_{34} can be estimated from time intervals given in the Section II. Therefore, a duty cycle of 0.75 is chosen to ensure ZCS for the entire range of source voltage at rated load condition.

TABLE I
DESIGN PARAMETERS

Parameter	Value
Resonant Inductor, L_r	5.5μH
Resonant Capacitor, C_r	132nF
Input Inductor, L_{in}	100μH
Output Capacitor, C_1, C_2	80μF
Turns ratio, n	5.2

TABLE II
CONVERTER SPECIFICATIONS

Parameter	Value
Input Voltage, V_{in}	30-58V
Output voltage, V_o	380 V
Maximum output power, P_o	500W
Switching frequency, f_{sw}	135-160 kHz
Duty ratio, D	0.73

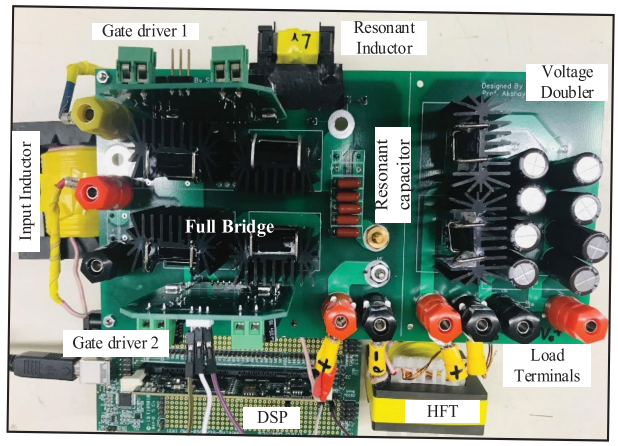

Fig. 6. Proof-of-concept 500-W prototype of the proposed converter.

IV. EXPERIMENTAL RESULTS

Considering aforementioned design constraints, converter parameters can be estimated that are listed in Table I. This section illustrates steady-state experimental results for the converter specifications given in Table II to demonstrate the performance of the converter. A proof-of-concept 50-W laboratory prototype has been developed, as shown in Fig. 6. Components specifications for the hardware prototype are listed in Table III. The prototype has been tested to validate the expected claims for supply voltage range of 30–58 V at rated load condition. The gating signals for the semiconductor devices were generated using Texas instrument (TI)-digital signal processor (DSP) evaluation board. It has been observed that the experimental waveforms relate closely with analytically predicted steady-state operating waveforms.

Steady-state experimental results for case (1) $V_{\text{in}} = 30$V at 500 W and 160 kHz switching frequency are depicted in Fig. 7. The gating pulses for the switch pair S_1, S_4, resonant current I_{Lr} and voltage appearing across the switches V_{DS} are shown in Fig. 7(a). The commutation of the semiconductor devices

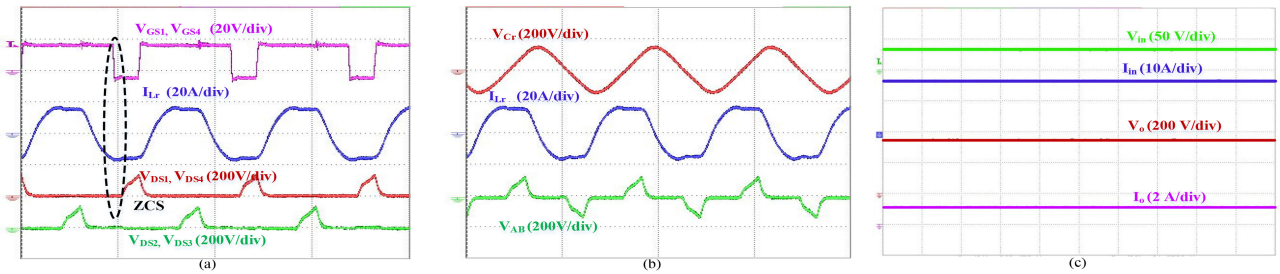

Fig. 7. Experimental results for $V_{\rm in} = 30$ V. (a) Gate-source voltage $V_{\rm GS1}$, $V_{\rm GS4}$, resonant current $I_{\rm Lr}$, and drain-to-source voltages. (b) Resonant capacitor charge $V_{\rm Cr}$, resonant current $I_{\rm Lr}$, and bridge output voltage $V_{\rm AB}$. (c) Input current and voltage $I_{\rm in}$, $V_{\rm in}$, output current and voltage I_o, V_o (time scale: 5 μs/div).

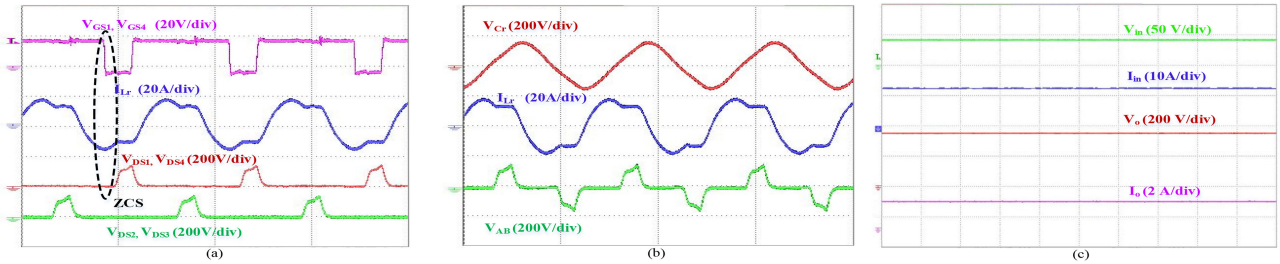

Fig. 8. Experimental results for $V_{\rm in} = 40$ V. (a) Gate-source voltage $V_{\rm GS1}$, $V_{\rm GS4}$, resonant current $I_{\rm Lr}$, and drain-to-source voltages. (b) Resonant capacitor charge $V_{\rm Cr}$, resonant current $I_{\rm Lr}$, and bridge voltage $V_{\rm AB}$. (c) Input current and voltage $I_{\rm in}$, $V_{\rm in}$, output current and voltage I_o, V_o (time scale: 5 μs/div).

TABLE III
COMPONENT SPECIFICATION OF THE LABORATORY PROTOTYPE

Component	Specifications
Boost inductor L_{in}	55 x 28 x 21 EE ferrite Core, 100μH
Converter Switches,	SCT3060ALGC11-ND, 650V,39A,60mΩ
Series Resonant Inductor, L_r	EE ferrite core, 3.42μH
Resonant Capacitor, C_r	135nF 1kV Film capacitor
HF Transformer	EE ferrite core, Primary turns, N_1=10, secondary turns N_2=52, L_{lk}= 1.64μH
Rectifier Diodes D_1, D_2	STPSC20065D, 650V, 20A,V_f= 0.8V
Output Capacitor, C_1, C_2	80μF 450V electrolytic capacitor, 10nF film capacitor
Gate driver IC	HCNW3120
DSP board	TMS230F28335

occur during switching overlap, where resonance sets in, transferring the current form the outgoing switch pair (S_1, S_4) to the incoming switch pair (S_2, S_3). It should be noted that the resonance results in sinusoidally varying transformer current that naturally decreases the switch current to zero and later its body diode takes over and hence gating signal is removed after switch current reaches zero, thereby, preventing any overshoot across the switch and results in ZCS turn-OFF. Fig. 7(b) depicts steady-state waveforms for the resonant capacitor charge $V_{\rm cr}$, bridge voltage $V_{\rm AB}$, and resonant current $I_{\rm Lr}$ that matches closely with the analytical waveforms. It should be noted that the series capacitor charges linearly when only one switch pair is conducting owing to the constant current ($I_{\rm in}$) and, hence, defines the energy transfer region, transferring power from input to the load. The peak switch voltages are settled at 160 V and a peak resonant current of 18.5 A at 30 V source voltage are observed.

Fig. 8(a) depicts the steady-state experimental waveforms for case (2), $V_{\rm in} = 40$V and $f_{\rm sw} = 150$kHz at full load. It should be noted that sinusoidally varying resonant current allows body-diode conduction resulting in ZCS turn-OFF of the semiconductor devices and eliminates voltage spike during turn-OFF. Relatively higher $I_{\rm Lrp}/I_{\rm in}$ ratio is observed for higher source voltages.

Steady-state experimental results for case (3), $V_{\rm in} = 50$V at full-load with switching frequency being 140 kHz are illustrated in Fig. 9. Fig. 9(a) confirms ZCS at turn-OFF and alleviates voltage overshoot across the semiconductor devices. Fig. 9(b) demonstrates the typical waveform for the resonant capacitor voltage, resonant current, and full-bridge output voltage conforming the analysis.

Experimental results for case (4) $V_{\rm in} = 58$ V and $f_{\rm sw} = 134$ kHz are depicted in Fig. 10. Natural commutation for semiconductor devices for the worst case scenario (98% variation from the $V_{\rm min}$) has been observed. Regulated load voltage of 380 V is attained for all the scenarios as shown in Figs. 7(c), 8(c), 9(c) and 10(c). It should be observed that at higher input levels, the ratio of peak current to the input current ($I_{\rm Lrp}/ I_{\rm in}$) is relatively higher. Also, increased peak capacitor voltage is observed for higher source voltages. Experimental results for source voltage variation from 30 to 50 V under 80% load and light-load (20%) condition are depicted in Figs. 11 and 12, respectively. It is clear from Fig. 11 that ZCS operation and device voltage

TABLE IV
COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHER ZCS CURRENT-FED FULL-BRIDGE CONVERTERS

Description	[14]	[20]	[18]	[19]	[25]	Proposed
Switch count	8	4	6	6	4	4
Diodes count	0	4	8	8	6	2
Switch voltage stress	$\frac{V_o}{n}$	$\frac{V_o}{n}$	$\frac{V_o}{n}$	$\frac{V_o}{n}+V_{cr}$,	$\frac{V_o}{2n}+V_{cr}$,	$\frac{V_o}{2n}+V_{cr\_pk}$
Control technique	Variable duty	Variable frequency	Phase shift modulation	Phase shift modulation	Phase shift modulation	Variable Frequency
Soft switching method	Secondary modulation	Parallel LC resonance	LCL resonance	Series LC resonance	LCC resonance	Series LC resonance
Switching Frequency	100kHz	40-150kHz	20kHz	20kHz	20kHz	135-160kHz
Duty cycle loss	-	High	Moderate	High	Low	Low
Resonant energy	-	Fixed	Adaptive	Adaptive	Adaptive	Adaptive
Source voltage range	12V	22-27V	530V+ 20%	530V+ 20%	125V	(30-58)V
Maximum efficiency	93% (250W rated)	92% (1kW load)	94% (5kW load)	93% (5kW load)	- (1kW load)	95.6% (500W load)

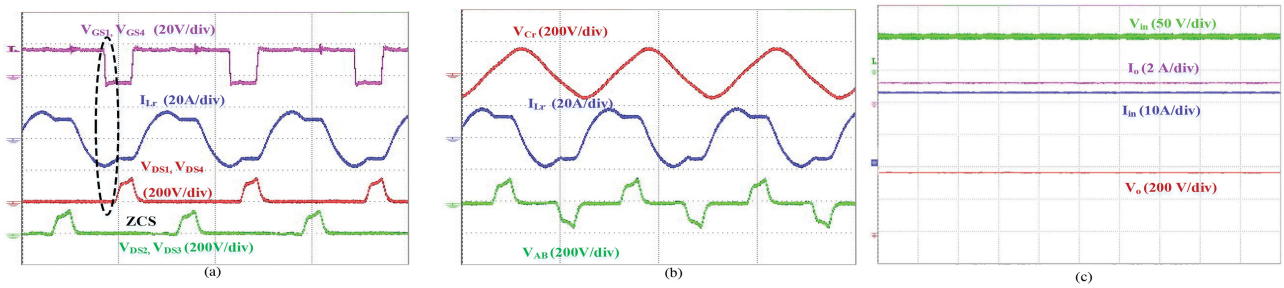

Fig. 9. Experimental results for $V_{\rm in} = 50$ V. (a) Gate-source voltage $V_{\rm GS1}$, $V_{\rm GS4}$, resonant current $I_{\rm Lr}$, and drain-to-source voltages. (b) Resonant capacitor charge $V_{\rm Cr}$, resonant current $I_{\rm Lr}$, and bridge voltage $V_{\rm AB}$. (c) Input current and voltage $I_{\rm in}$, $V_{\rm in}$, output current and voltage I_o, V_o (time scale: 5 μs/div).

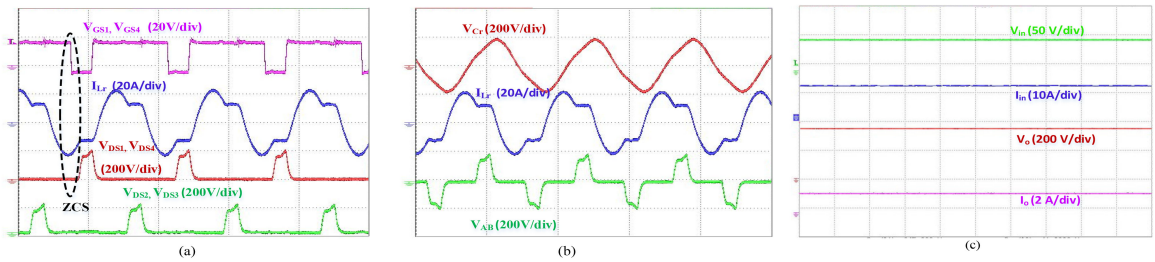

Fig. 10. Experimental results for $V_{\rm in} = 58$ V. (a) Gate-source voltage $V_{\rm GS1}$, $V_{\rm GS4}$, resonant current $I_{\rm Lr}$, and drain-to-source voltages. (b) Resonant capacitor charge $V_{\rm Cr}$, resonant current $I_{\rm Lr}$, and bridge voltage $V_{\rm AB}$. (c) Input current and voltage $I_{\rm in}$, $V_{\rm in}$, output current and voltage I_o, V_o (time scale: 5 μs/div).

clamping is preserved even under light-load (20%) condition for wide source voltage variation by utilizing variable frequency control. It should be observed that the ratio of peak current to the input current ($I_{\rm Lrp}/\ I_{\rm in}$) is lower than rated-load condition and, therefore, results in improved part-load efficiency. However, the switching frequency variation is more sensitive to load variations than source voltage variations. As a result, proposed converter allows safe ZCS operation from full-load to 20% load with switching frequency range of 75–160 kHz. Fig. 13 shows the steady-state experimental waveforms for current through and voltage across the rectifier diode for different source voltages at rated load condition. It should be noticed that the proposed

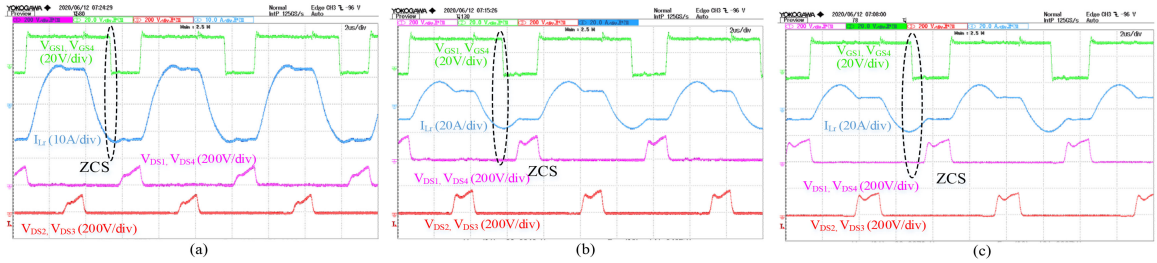

Fig. 11. Experimental steady-state results for source voltages. (a) $V_{\text{in}} = 30$ V. (b) $V_{\text{in}} = 40$ V. (c) $V_{\text{in}} = 50$ V at 80% load condition (time scale: 2 μs/div).

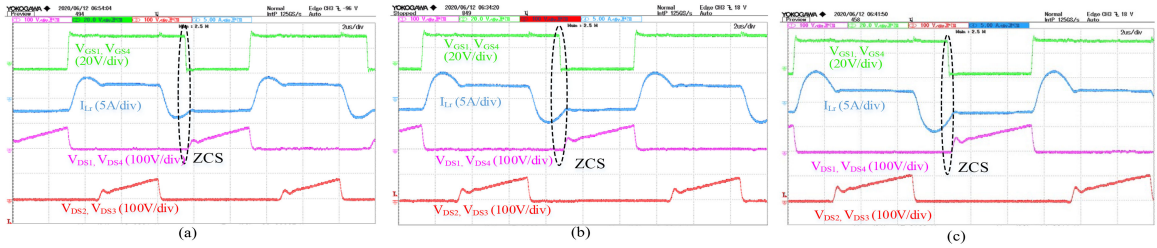

Fig. 12. Experimental steady-state results for source voltages. (a) $V_{\text{in}} = 30$ V. (b) $V_{\text{in}} = 40$ V. (c) $V_{\text{in}} = 50$ V at 20% load condition (time scale: 2 μs/div).

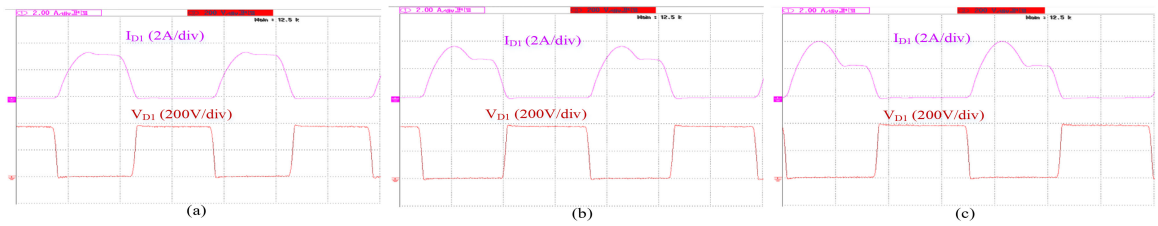

Fig. 13. Experimental results for rectifier diode current and voltage at rated-load (500 W) for (a) $V_{\text{in}} = 30$ V. (b) $V_{\text{in}} = 40$ V. (c) $V_{\text{in}} = 50$ V.

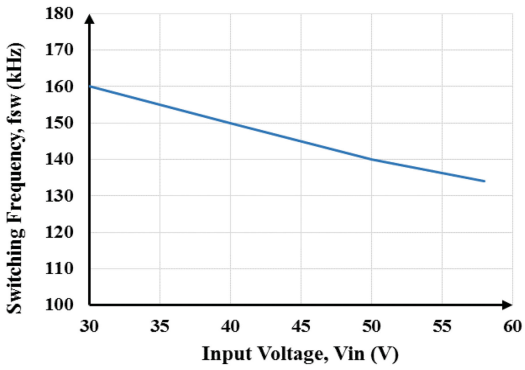

Fig. 14. Switching frequency variation with input voltage variation.

TABLE V
FREQUENCY RANGE COMPARISON OF THE PROPOSED CONVERTER WITH EXISTING CONVERTERS

	[20]	[21]	[22]	Proposed
Source voltage range	22- 27V	42-48V	38-50V	30-58V
Switching frequency range	55-135 kHz	50-170 kHz	77-200 kHz	135-160 kHz
Rated Load	1000W	500W	500W	500W

design is able to achieve wide range soft-switching and device voltage clamping to integrate sources with huge variability in dc voltage. Soft-commutation of the semiconductor devices significantly improves the converter efficiency and allows safe operation at high switching frequency. The findings in Fig. 14 elucidate the switching frequency trend for the source voltage variation at rated load. The frequency range observed is between 135 and 160 kHz at full-load condition. This characteristic curve affirms the need for variable frequency operation to preserve output voltage regulation and natural commutation of the active devices. It should also be observed from Table V that frequency variation is less sensitive to input voltage variation as compared to other converter topologies. Comparison of measured experimental efficiency and calculated efficiency at rated load for different source voltages is depicted in Fig. 15. Maximum full-load efficiency of 95.6% for $V_{\text{in}} = 58$ V and minimum efficiency of 93.2% for $V_{\text{in}} = 30$ V is observed on the hardware prototype. Also, the maximum efficiency under light-load is recorded to be 93.5%. Table VI depicts the converter power loss for different input voltages at rated load. The individual component losses are computed using loss equations given in Table VII and selected components datasheet parameters.

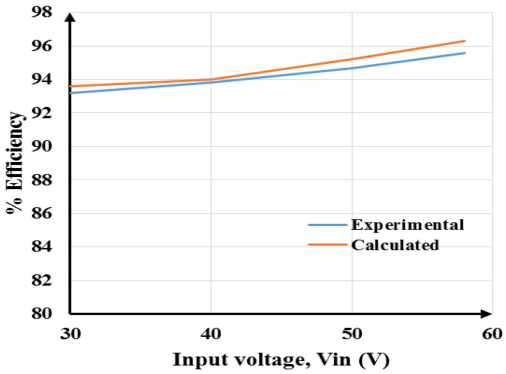

Fig. 15. Experimental efficiency curve with input voltage variation.

TABLE VI
POWER LOSS DISTRIBUTION IN THE CONVERTER

Power loss type (in W)	V_{in} 58V	V_{in} 50V	V_{in} 40V	V_{in} 30V
Switch turn-ON loss	2.29	2.14	1.84	1.58
Switch conduction losses	11.23	13.53	20.22	21.78
Total rectifier diode loss	2.51	2.31	2.11	1.81
Total boost inductor loss	1.55	2.25	3.75	5.64
Total HF transformer loss	2.03	1.92	1.81	1.50
Gate drive loss	0.044	0.046	0.049	0.054
Other losses (capacitor loss/stray loss)	0.35	0.30	0.20	0.13

It should also be observed that the switching losses are primarily due to hard turn-ON of the primary side MOSFETs while the rectifier diodes hold negligible turn-ON loss. Conduction loss covers the substantial part of the total converter loss, which is observed in semiconductor switches, diodes, HF transformer, and boost inductors. In an attempt to have lower switch turn-ON and switch conduction losses, MOSFET with considerably low output capacitance and low $R_{\mathrm{ds,on}}$ is chosen. SiC Schottky diodes are utilized for the secondary side rectifier to enable smooth turn-OFF with reduced reverse recovery/ turn-OFF loss. Moreover, the HF transformer is designed with ferrite core and low magnetizing current ripple to realize minimum core losses. Parasitic of the converter are optimized to eradicate the need for additional lossy snubbers. Besides, converter efficiency has been further enhanced by optimizing gate drive circuit by using different gate resistors for turn-ON and turn-OFF path and efficient printed circuit board layout for the prototype with minimum parasitic, and adequate probing. Table IV provides a detailed comparison between the proposed configuration and other single-phase current-fed full-bridge topologies. It is witnessed that the proposed converter exhibits advantages like reduced passive and active component count, higher efficiency and wide range soft switching compared to existing topologies.

V. CONCLUSION

A series resonant tank assisted partial resonance-pulse operated current-fed full-bridge dc/dc converter is conceptualized and investigated in this article. The objective is to obtain ZCS and voltage-clamping of the semiconductor switches without any external clamping circuits. Detailed steady-state operation and analysis of the current-fed full-bridge converter with series resonance is presented. Resonance pulse is successful to obtain wide range ZCS of the semiconductor devices and alleviates any voltage overshoot at device turn-OFF while limiting the conduction losses. In addition, strict output voltage regulation over wide disturbance in the source voltage (30–58 V) makes the design apropos for alternative sources like PV/fuel cell. Furthermore, it brings merits of stiff dc input current and lower circulating current avoiding over-rated devices resulting in improved efficiency. Peak efficiency of 95.6% at full-load for 58 V is observed. It allows short switching frequency variation of 135–160 kHz for the set variation in source voltage at full-load on proof-of concept hardware prototype. Considering aforementioned merits, the proposed topology is suitable for battery charging and constant power motor drive applications.

APPENDIX

A. DC voltage gain derivation

$$
\begin{aligned}
|I_{o,\mathrm{avg}}| = \frac{V_o}{R_{\mathrm{FL}}} = \frac{I_{\mathrm{Lr,avg}}}{n} &= \frac{1}{n}.\frac{2}{T_s}\int_0^{T_s/2} i_{\mathrm{Lr}}(t)\ \mathrm{dt} \\
&= \frac{1}{n}.\frac{2}{T_s}\int_{t_2}^{t_7} i_{\mathrm{Lr}}(t)\ \mathrm{dt} \\
&= \frac{2f_s}{n}\left[\int_{t_2}^{t_4} i_{\mathrm{Lr}}(t)\ \mathrm{dt} + \int_{t_4}^{t_6} I_{\mathrm{in}}\ \mathrm{dt} + \int_{t_6}^{t_7} i_{\mathrm{Lr}}(t)\ \mathrm{dt}\right] \\
&= \frac{2f_s}{n}\left[\int_{t_2}^{t_4} \frac{1}{Z_r}\left(\frac{V_o}{2n} + V_{\mathrm{crp}}\right)\sin(\omega_r(t-t_2))\ \mathrm{dt}\right. \\
&\qquad + \int_{t_4}^{t_6} I_{\mathrm{in}}\ \mathrm{dt} + \int_{t_6}^{t_7} I_{\mathrm{in}} \\
&\qquad \left. - \frac{1}{L_r}\left(\frac{V_o}{2n} + V_{\mathrm{crp}}\right)(t-t_1)\ \mathrm{dt}\right].
\end{aligned}
$$

Expression for $\mathrm{I}_{o,\mathrm{avg}}$ can be obtained upon integrating above-mentioned equation for the respective time intervals as given follows:

$$
\begin{aligned}
T_{42} &= \frac{1}{\omega_r}\left(\pi - \sin^{-1}\left(\frac{I_{\mathrm{in}}Z_r}{\frac{V_o}{2n} + V_{\mathrm{crp}}}\right)\right) \\
T_{64} &= \frac{T_s}{2} - T_{42} - T_{21} \\
T_{76} &= T_{21} = \frac{I_{\mathrm{in}}L_r}{V_{\mathrm{crp}} + \frac{V_o}{2n}}.
\end{aligned}
$$

Now, in order to obtain the voltage gain expression in terms of converter parameters like V_o, V_{in}, and load R_{FL}, the following conversions are utilized and substituted in average output current

expression:

$$I_{\text{in}} = \frac{{V_o}^2}{R_{\text{FL}}\, V_{\text{in}}} = M \frac{V_o}{R_{\text{FL}}}$$
$$|I_{o,\text{avg}}| = \frac{V_o}{R_{\text{FL}}}$$
$$\frac{V_o}{V_{\text{in}}} = M$$
$$k = \frac{I_{\text{in}} Z_r}{\frac{V_o}{2n} + V_{\text{crp}}}.$$

Also, $(\frac{V_o}{2n} + V_{\text{crp}})$ can be rewritten as, $= \frac{V_o}{2n}.\ X$, where X can be defined as

$$X = \left(1 + \frac{2nV_{\text{crp}}}{V_o}\right).$$

Therefore, gain expression can be achieved in terms of converter parameters is given as

$$M = \frac{n\left(1 - \frac{f_s R_{\text{FL}} X}{f_r 2\pi n^2\, Z_r}\left(1 - \sqrt{1-k^2}\right)\right)}{\left(1 - \frac{f_s}{f_r}\left(1 - \frac{1}{\pi}\sin^{-1}k + \frac{Mn\, Z_r}{2\pi R_{\text{FL}} X}\right)\right)}.$$

Furthermore, gain expression is derived in terms of control variables like f_n, and load R_{FL} that is given as

$$M = \frac{n\left(1 - \frac{f_n r_n X}{2\pi}\left(1 - \sqrt{1-k^2}\right)\right)}{\left(1 - f_n\left(1 - \frac{1}{\pi}\sin^{-1}k + \frac{k}{2\pi}\right)\right)}$$

where

f_n Normalized frequency, $= \frac{f_s}{f_r}$

r_n Normalized load resistance, $= \frac{R_{\text{FL}}}{n^2\, Z_r}$

$$k = \frac{I_{\text{in}} Z_r}{\frac{V_o}{2n} + V_{\text{crp}}} = \frac{2M}{n r_n X}.$$

B. Converter loss calculation

TABLE VII
LOSS EQUATIONS USED TO COMPUTE THE CONVERTER LOSSES

Description	Equation
Switch conduction loss	${I_{sw,rms}}^2 * R_{Ds,on}$
Switch turn-on loss	$\frac{1}{2} C_{oss} {V_{sw}}^2 f_{sw}$
Total rectifier diode loss	$V_{Df} * I_{D,avg} + {I_{D,rms}}^2 * R_D + V_d\, Q_{rr}\, f_{sw}$
Total HF Transformer loss	${I_{Lr,rms}}^2 * R_{winding} + P_{C,limit}\, V_e$
Total boost inductor loss	${I_{in}}^2 * R_{L,DC} + P_{C,limit}\, V_e$
Gate drive loss	$C_{iss} V_g^2 f_s$
Capacitor loss	${I_{cout,rms}}^2 * R_{ESR}$

where
I_{sw} = Switch rms current, A
RDS = Switch drain-to-source on-state resistance, Ω
V_{sw}, = Switch average voltage during turn-OFF, V
fsw = Switching frequency, Hz
Coss = Switch output capacitance, F
ID = Diode rms current, A
RD = Diode turn-ON resistance, Ω
ID, = Diode average current, A
VDf = Diode forward voltage, V
Rwinding = Transformer dc resistance, Ω
IL, = Boost inductor rms current, A
RL = Inductor dc resistance, Ω
ICout, = Capacitor ripple rms current, A
RESR = Capacitor equivalent series resistance, Ω
Pc,= Core loss limit, mW/cm^3
Ve = Effective core volume, cm^3
Ciss = Switch input capacitance, F
fsw = Switching frequency, Hz
Vg = Switch driving voltage, V
V_d = Diode blocking voltage, V

REFERENCES

[1] P. Biczel, "Power Electron. converters in DC microgrid," in *Proc. Compat. Power Electron.*, 2007, pp. 1–6.

[2] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "A comparison of soft-switched DC–DC converters for fuel-cell to utility-interface application," in *Proc. IEEE Power Convers. Conf.*, 2007, pp. 588–594.

[3] A. K. Rathore and U. R. Prasanna, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated dc/dc converters for fuel cell vehicles," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2012, pp. 3212–3219.

[4] E. S. Kim, K. Y. Joe, H. Y. Choi, Y. H. Kim, and Y. H. Cho, "An improved soft switching Bi-directional PSPWM FB DC/DC converter," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, 1998, pp. 740–743.

[5] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, "Isolated bidirectional full-bridge DC/DC converter with a flyback snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1915–1922, Jul. 2010.

[6] R. Watson and F. C. Lee, "A soft-switched, full-bridge boost converter employing an active-clamp circuit," in *Proc. IEEE Power Electron. Spec. Conf.*, 1996, pp. 1948–1954.

[7] V. Yakushev, V. Meleshin, and S. Fraidlin, "Full-bridge isolated current fed converter with Active clamp," in *Proc. 14th IEEE Appl. Power Electron. Conf. Expo.*, 1999, pp. 560–566.

[8] E. S. Park, S. J. Choi, J. M. Lee, and B. H Cho, "A soft-switching active clamp scheme for isolated full-bridge boost converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, vol. 2, pp. 1067–1070.

[9] J.-T. Kim, B.-K. Lee, T.-W. Lee, S.-J. Jang, S.-S. Kim, and C.-Y. Won, "An active clamping current-fed half-bridge converter for fuel-cell generation system," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, pp. 4709–4714.

[10] S.-K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.-H. Lee, "A new active clamping zero-voltage switching PWM currentfed half-bridge converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1271–1279, Nov. 2005.

[11] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design and experimental results of wide range ZVS active-clamped L-L type current-fed DC/DC converter for fuel cells to utility interface," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473–485, 2012.

[12] U. R. Prasanna and A. K. Rathore, "Extended range ZVS active-clamped current-fed full-bridge isolated DC/DC converter for fuel cell applications: Analysis, design, and experimental results," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2661–2672, Jul. 2013.

[13] A. K. Rathore and U. R. Prasanna, "Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4482–4491, Oct. 2013.

[14] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[15] P. Xuewei and A. K. Rathore, "Naturally clamped zero-current commutated soft-switching current-fed push-pull dc/dc converter: Analysis, design, and experimental results," *IEEE Trans. Power. Electron.*, vol. 30, no. 3, pp. 1318–1327, Mar. 2015.

[16] C. Iannello, S. Luo, and I. Batarseh, "Full bridge ZCS PWM converter for high-voltage high-power applications," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, no. 2, pp. 515–526, Apr. 2002.

[17] B. Yuan, X. Yang, X. Zeng, J. Duan, J. Zhai, and D. Li, "Analysis and design of a high step-up current-fed multiresonant DC–DC converter with low circulating energy and zero-current switching for all active switches," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 964–978, Feb. 2012.

[18] H. Wang, Q. Sun, H. S. H. Chung, S. Tapuchi, and A. Ioinovici, "A ZCS current-fed full-bridge PWM converter with self-adaptable soft switching snubber energy," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1977–1991, Aug. 2009.

[19] X. Zhang, H. S. Chung, X. Ruan, and A. Ioinovici, "A ZCS full-bridge converter without voltage overstress on the switches," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 686–698, Mar. 2010.

[20] R.-Y. Chen, T.-J. Liang, J.-F. Chen, R.-L. Lin, and K.-C. Tseng, "Study and implementation of a current-fed full-bridge boost DC-DC converter with zero-current switching for high voltage Appl.," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1218–1226, Jul. /Aug. 2008.

[21] K. R. Sree and A. K. Rathore, "Soft-switching non-isolated current-fed inverter for PV/fuel cell Appl.," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 351–359, Jan. /Feb. 2016.

[22] K. R. Sree and A. K. Rathore, "Impulse commutated zero current switching current-fed push-pull converter: Analysis, design, and experimental results," *IEEE Trans. Ind. Electron.*, vol. 632, no. 1, pp. 363–370,

[23] K. R. Sree and A. K. Rathore, "Impulse commutated zero current switching current-fed three-phase DC/DC converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1855–1864, Mar. 2016.
[24] K. R. Sree and A. K. Rathore, "Analysis and design of impulse-commutated zero-current-switching single-inductor current-fed three-phase push–pull converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1517–1562, Mar./Apr. 2017.
[25] R. Suryadevara and L. Parsa, "Adaptive resonant energy realization in FB-ZCS DC-DC converter using dual-capacitor circuit," in *Proc. IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, USA, 2019, pp. 5536–5541.
[26] S. Tandon and A. K. Rathore, "Current-fed full-bridge series LC resonance impulse ZCS commutated DC-DC converter," in *Proc. IEEE Int. Conf. Power Electron., Smart Grid Renewable Energy*, Cochin, India, 2020, pp. 1–6.

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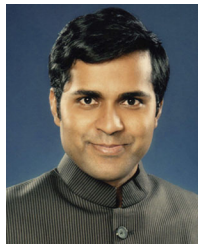

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