Novel Hybrid DC Circuit Breaker Based on Series Connection of Thyristors and IGBT Half-Bridge Submodules

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***Abstract*—Hybrid dc circuit breakers (HCBs) are vital equipment in dc grid systems. However, HCBs are usually costly since massive full-controlled power semiconductors are required to withstand high surge voltage and current stresses during current interrupting. Thyristors are good alternatives in realizing HCBs in view of their low cost and high current carrying capability; however, turning OFF the thyristor fast and reliably is a challenging task. In this article, a novel HCB topology is proposed, of which the solid-state part is realized by hybrid connection of thyristors and insulated gate bipolar transistor (IGBT) half-bridge submodules. The use of IGBT half-bridges provides a negative voltage across the thyristors to turn them OFF; accordingly, thyristors withstand a major of turn-OFF surge voltage instead of IGBTs. By this means, a low-cost HCB can be established while maintaining a high breaking speed. Besides, fast reclose and rebreak function is provided by the proposed topology. Operation principle and design consideration of the novel HCB topology are analyzed in detail, and the effectiveness of the proposed HCB is verified by both software simulation and downscaled experimental results.**

***Index Terms*—Hybrid dc circuit breaker (HCB), insulated gate bipolar transistor (IGBT) submodule, reclose and rebreak, thyristor.**

I. Introduction

HIGH-VOLTAGE direct-current (HVdc) transmission systems have been developed increasingly in recent years. In comparison with traditional point-to-point systems, a multiterminal HVdc network would win out in the following aspects: The reduction in the number of converter stations (reduction in converter cost and loss) and the increase in reliability and redundancy (power can be transmitted even if one line is lost) [1]. However, the enabling of HVdc networks would rely on fast and reliable HVdc circuit breakers (CBs) to handle the short circuit current and isolate the fault. This makes HVdc CBs one of the key technologies to facilitate HVdc networks.

Existing mechanical CBs (MCBs) such as vacuum interrupters\offer very low conduction losses; however, they would have a long breaking time due to the need for arc extinguishing between the contactors [2]–[5]. Solid-state CBs (SSCBs) such as series-connected insulated gate bipolar transistors (IGBTs) can interrupt a fault current within hundreds of microseconds, but they generate massive conducting losses that may account for more than 30% of the station losses [6], [7]. To overcome the drawbacks of pure mechanical or SSCBs, parallel combination of MCB and SSCB is proposed to develop the hybrid dc circuit breaker (HCB) [8]–[29]. The hybrid design would combine the advantages of both MCB and SSCB, preserving negligible conduction losses and ultra-fast current breaking ability, thus attracting increasing attention in recent years.

An HVdc HCB is proposed by ABB in [8]. The main body of the proposed HCB consists of three paralleled branches: a conduction branch which includes a load commutation switch (LCS) formed with series-connected IGBTs and an ultra-fast disconnector (UFD) built with MCB; a main breaker branch composed of large numbers of IGBTs connected in series; and an arrester branch realized by metal-oxide varistors (MOVs). Although deemed as a benchmark, the ABB HCBs still show some limits. First, although the LCS method proposed by ABB is simple in structure and control, the additional conduction losses induced by the series-connected IGBTs lower the transmission efficiency. Second, in the main breaker, a large number of IGBTs are connected in series to conduct the short current and withstand the surge voltage during breaking; however, IGBTs are expensive devices and have relatively small short circuit current carrying capability, thus making the HCB costly in high-power applications.

In order to overcome the aforementioned drawbacks of an ABB HCB, alternative methods on both LCS side and main breaker side are proposed.

A. LCS Side Alternatives

The LCS side alternatives usually focus on reducing the conduction losses of the HCB. The topology described in [9]

Manuscript received December 18, 2019; revised May 25, 2020 and June 27, 2020; accepted July 9, 2020. Date of publication July 21, 2020; date of current version September 22, 2020. This work was supported in part by the fund of the Natural Science Foundation of China under Grant U1966212, and in part by grants from the Power Electronics Science and Education Development Program of Delta Group. Recommended for publication by Associate Editor K. Ngo. *(Corresponding author: Xu Yang.)*

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Digital Object Identifier 10.1109/TPEL.2020.3010965

replaces the LCS with an H-bridge converter and a capacitor, normal current conducts through both the upper arm IGBT and the lower arm diode (or the opposite), and so the conduction losses are reduced in comparison of a single IGBT. Similarly, paralleled IGBTs are adopted in [10] to suppress the conduction losses. Parallel connection method is quite simple, but the required number of full-controlled devices has increased slightly. The topology proposed in [11] and [12] eliminates active switches in the LCS and relies on the arc voltage built across the UFD to commutate the short circuit current. However, this topology may not be applicable to HVdc CBs since the arc voltage is usually within the range of several hundred volts, which is not high enough to conduct all the IGBTs and diodes in the main breaker. In the method proposed in [13]–[15], LCS is replaced by a pair of coupled coils. When a fault occurs, the precharged capacitor connected in series with the primary coil would be discharged, generating a voltage across the secondary coil and force the load current to commutate into the main breaker. The coil has quite small ON-state resistance so its conduction losses can be minimized. Main breaker built with modular multilevel converter (MMC) and an inductor is proposed in [16]; MMC controls the current amplitude in the main breaker, realizing a zero-current breaking of the UFD, so LCS is not needed. But the required semiconductors and breaking time are considerable.

B. Full-Controlled Device-Based Main Breakers

Aiming at increasing the current breaking capability and reducing the overall cost, main breaker side alternatives are also researched. In [9], the main breaker is realized by cascade connected H-bridge converters. Short circuit current could flow through both the IGBTs and the anti-paralleled diodes; thus, the current carrying and breaking capability can be almost doubled. But larger numbers of required semiconductors increase the system cost in return. The work proposed in [17] and [18] utilizes a half-bridge and LC networks to build the main breaker. This topology needs very few semiconductors and eliminates the LCS switch, but the resonant process to commutate the fault current requires a relatively long period. The countercurrent-injected HCB [19] focuses on increasing the current breaking capability of integrated gate-commutated thyristors (IGCTs), but the required auxiliary circuits increase the system complexity greatly. A mixture SSCB topology combining IGCTs and IGBTs is proposed in [20]. The mixture structure contributes to reduce the semiconductor cost while maintaining high performance of the SSCB; however, the current stresses of the IGBTs and IGCTs are very high during the current breaking period. A soft breaking method is proposed in [21]. The IGBTs in the main breaker are turned OFF sequentially, leading to a reduced short current peak; thus the required current capacity of the IGBTs can be reduced. Some multiport HCB topologies have been proposed in [22]–[24]. Due to the sharing of the main breaker part, overall construction cost can be reduced.

C. Thyristor-Based Main Breakers

All the above-mentioned HCBs use gate turn-OFF devices as the main breaker. According to the work presented in [25], IGBT and injection enhanced gate transistor (IEGT) could turn OFF 4–5 times of their rated current after conduction of 5 ms. The IGCT's turn-OFF ability is even lower (less than 2.5 times of its rated current) due to the stray inductance in the gate commutation loop. In comparison with full-controlled semiconductors, thyristors would win out both in current carrying capability and cost effectiveness. A thyristor could conduct 15 times of rated current shortly, and the price could be as low as 1/10 of an IGBT in the same power rating. These features make thyristor attractive alternative devices in building an HVdc main breaker [26]–[29]. Although the cost and current carrying issues could be dealt with, forcing the thyristors to turn OFF becomes a big challenge. A precharged capacitor branch as well as an insulated high-voltage power supply are needed in [26], a pair of auxiliary charging circuit is required in [27], and several delay branches with large capacitors need to be included in [28] and [29]. This leads to the increase of required semiconductors and circuit complexity. Besides, since the capacitors cannot be discharged timely after breaking, these methods offer no fast reclose capability, which is essential in multiterminal dc systems. In HVdc transmission system with overhead lines, temporary faults occur occasionally. In this circumstance, the line should be reconnected after the arc has been distinguished. However, the fault may still remain during the reclosing process and the HCB needs to break again as mentioned in [30] and [31].

In order to overcome the drawbacks of the previous IGBT and thyristor-based main breaker topology, a novel HCB topology is proposed in this article, of which the main breaker is realized by hybrid connection of thyristors and IGBT half-bridge submodules (HBs). The major advancements of the proposed method are summarized as follows.

1) Thyristors withstand a major part of the turn-OFF surge voltage instead of IGBTs. By this means, a low-cost HCB can be established since the required number of full-controlled semiconductors is reduced greatly.
2) The proposed method charges the submodule capacitors during the UFD breaking time through a sequential charging method; therefore, no auxiliary power supplies are required, and the total breaking time is not increased significantly.
3) The proposed method offers fast reclose and rebreak capability.

The rest of this article is organized as follows. The circuit topology and operation principle of the proposed HCB are described in Section II. In Section III, design guidelines of the circuit parameters are proposed and verified by simulation results. In Section IV, a downscaled CB prototype is established and experimentally verified. Section V shows the conclusion of this article.

II. New Hybrid HVdc Circuit Breaker

A. Circuit Topology

In Fig. 1, circuit topology of the proposed HCB is illustrated. Although parallel connection and coupled coils methods [10], [13]–[15] can be adopted in the LCS side to optimize the conduction losses, this work will just focus on optimizing the

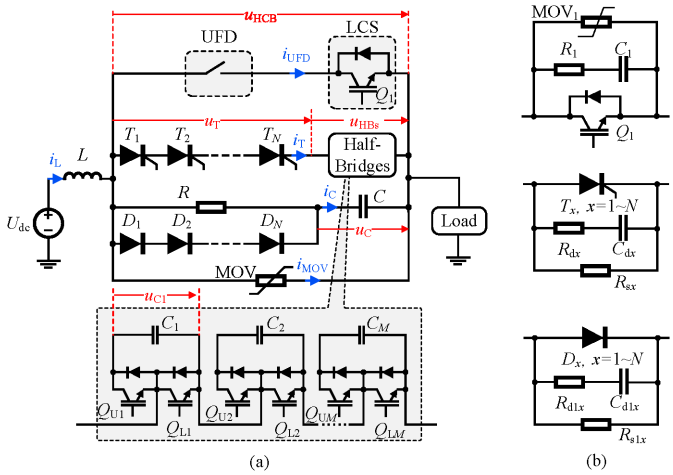

Fig. 1. Proposed HCB. (a) Circuit topology. (b) Auxiliary circuits for the semiconductor devices.

main breaker part. Therefore, the same LCS and UFD from an ABB HCB [8] are used in the proposed topology due to their simplicity and effectiveness.

The main breaker has a branch of series-connected thyristors and IGBT half-bridge submodules; besides, a paralleled branch of resistor–capacitor diode (RCD) snubber is added. As shown in Fig. 1(b), each thyristor and diode have a pair of voltage balancing devices across them, including the static voltage sharing resistors $R_{\rm s}$ ($R_{\rm s1}$) and the dynamic voltage sharing RC snubbers $R_{\rm d}$–$C_{\rm d}$ ($R_{\rm d1}$–$C_{\rm d1}$). The design method of the voltage sharing devices can be found in existing literatures [32] and [33] and will not be included in this article. Apart from that, RC snubber R_1–C_1 and $\rm MOV_1$ are paralleled with the LCS switch to prevent potential overvoltage across it.

B. Normal Break Process

Before the fault occurs, normal dc current flows through UFD and LCS. A normal break process of the proposed HCB includes eight different stages. The load current paths in different stages can be found in Fig. 2(a)–(h), and Fig. 3 shows key waveforms of the HCB during a normal break.

1) Fault begins (t_1–t_2): At time t_1, a short circuit fault occurs at the load side, and the breaker starts to carry the fault current. Due to the existence of the current-limiting inductor L, load current starts to rise linearly as

$$U_{\rm dc} = L \cdot \frac{{\rm d}i_L}{{\rm d}t} \tag{1}$$

where $U_{\rm dc}$ is the dc side voltage and i_L is the current flows through the HCB. Load current path in this stage is shown in Fig. 2(a).

2) Commutation from LCS to thyristors (t_2–t_3): At time t_2, controller detects the fault and sends a break command to the HCB. First, turn-ON drive signal will be sent to thyristors (T_1–T_N) and the lower arm IGBTs ($Q_{\rm L1}$–$Q_{{\rm L}M}$) in half-bridges. Then, the IGBT in LCS will be turned OFF, resulting in a voltage increase across the main breaker, which makes conduction of the main breaker semiconductors. Afterwards, the load current starts to transfer from MCB to the thyristor branch, as shown in Fig. 2(b). The interval between t_2 and t_3 (namely Δt_1) is defined as

$$\Delta t_1 = (L_{\rm LCS} + L_{\rm tr})\, I_{\rm tr}/U_{\rm MOV1.res} \tag{2}$$

where $L_{\rm LCS}$ is the stray inductances in the LCS branch, $L_{\rm tr}$ is the stray inductances in the thyristor branch, and $U_{\rm MOV1.res}$ is the clamping voltage of the used $\rm MOV_1$. The transfer time Δt_1 usually ranges from several hundreds of nanoseconds to several microseconds depending on the values of $L_{\rm LCS}$ and $L_{\rm tr}$; accordingly, it has almost no impact on the interruption speed of the HCB.

3) UFD starts to break (t_3–t_4): At t_3, LCS turns OFF completely and all the short circuit current flows through the main breaker, as shown in Fig. 2(c). As no current exists in the UFD at t_3, it can be broken without an arc. But due to the low-speed feature of a mechanical switch-based UFD, the required dielectric strength across it will be built slowly in the subsequent several milliseconds.

4) Submodule capacitors charging (t_4–t_5): At t_4, the dielectric strength across the UFD is partially built up but still not high enough to withstand the whole dc voltage. So, the main breaker cannot break yet. The half-bridge submodules will take the advantage of this period to charge their module capacitors (C_1–C_M). First, lower IGBT $Q_{{\rm L}M}$ is turned OFF, while $Q_{\rm L1}$ and $Q_{{\rm L}(M\text{-}1)}$ remain conducting, as shown in Fig. 2(d). The voltage across C_M and C will rise simultaneously. Then after a short period, as C_M is charged to the expected value, $Q_{{\rm L}M}$ is turned OFF and $Q_{{\rm L}(M\text{-}1)}$ is turned ON to charge $C_{(M\text{-}1)}$. Subsequently, the same charging process will be gone through by the rest of the submodule capacitors. After the charge process is completed, all submodule capacitors are charged to a same value, namely U_m. As only one module capacitor is connected into the circuit to be charged each time, the voltage across snubber capacitor C (namely u_C) will meet

$$u_{\rm C} \le U_{\rm m}\,(t_4 \le t \le t_5)\,. \tag{3}$$

Although it is possible to charge the module capacitors all at once, sequentially charging them would be a better solution since this way, it will maintain a relatively low dielectric strength between contactors of the UFD. In high-voltage application where the number of submodules is high, the submodules can be divided into three groups, and each time, one group can be charged together.

5) Commutation from thyristors to RCD (t_5–t_6): At t_5, UFD is separated completely and the main breaker is ready to interrupt the fault current. All lower IGBTs in half-bridges will be turned OFF, and then all upper IGBTs will be turned ON after a short dead time. As shown in Fig. 2(e), a reverse voltage will be applied across the thyristors to force them to turn OFF. The applied reverse voltage needs to last long enough to fully turn OFF the thyristors. At t_6, thyristors are completely turned OFF and ready to block a forward voltage. During the second commutation process, $L_{\rm tr}$ as well as the stray inductance in the D_1–$D_{N\text{-}C}$ path (namely L_C) will affect the commutation speed. Similar to

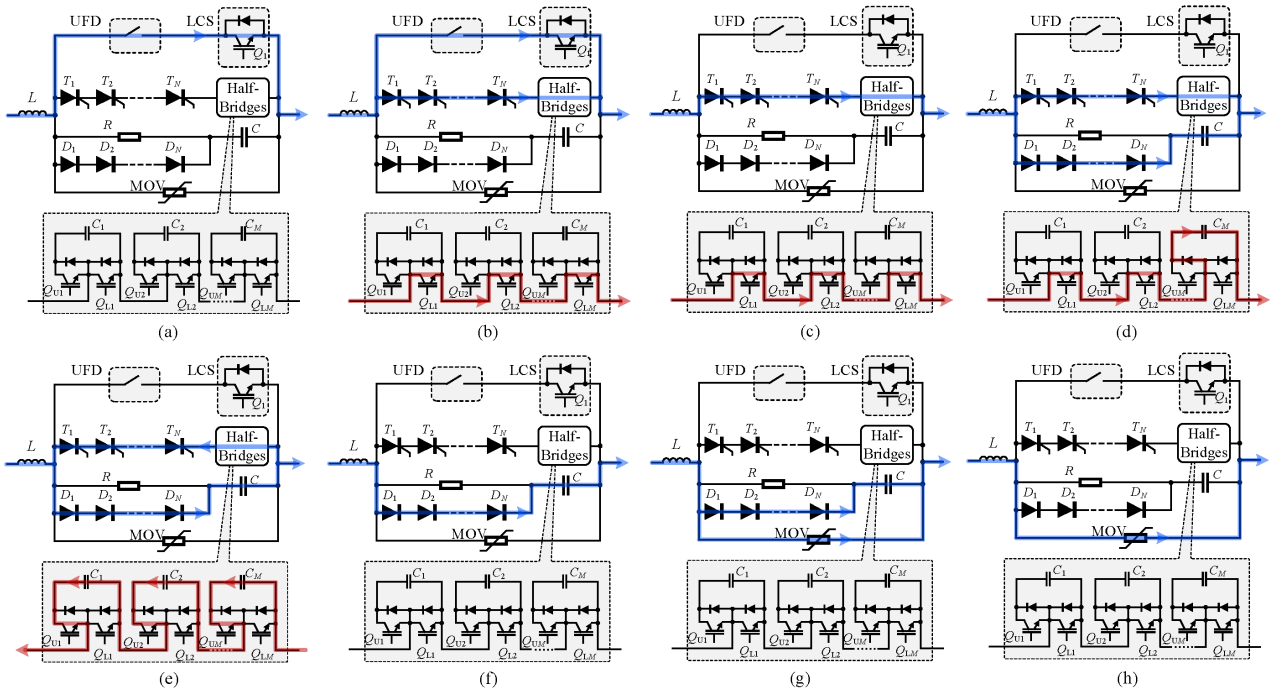

Fig. 2. Current path of the proposed HCB during normal break process.

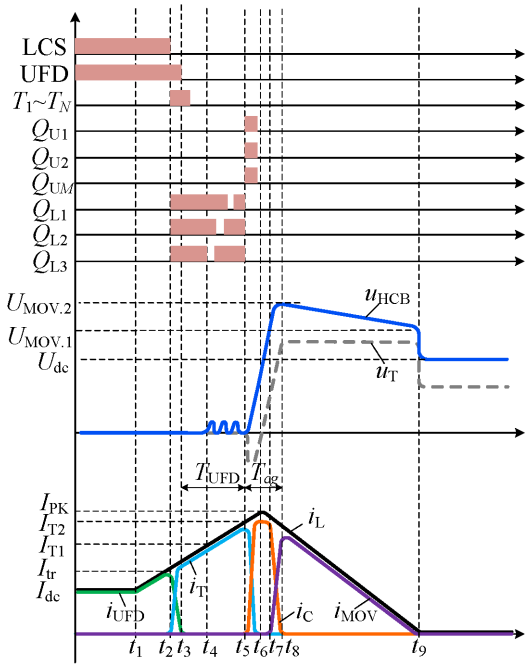

Fig. 3. Key waveforms of the proposed HCB during normal break process.

Δt_1, the second commutation time Δt_2 can be calculated with

$$\Delta t_2 = (L_{\rm tr} + L_{\rm C})\, I_{\rm T2}/MU_m \tag{4}$$

where MU_m is the total voltage of the submodule capacitors and $I_{\rm T2}$ is the load current amplitude during the second commutation process.

6) Snubber capacitor charging (t_6–t_7): As the thyristors are forced OFF at t_6, IGBTs in half-bridges are turned OFF, and the fault current will be carried by the RCD branch. The voltage across C then rises rapidly under the charging effect of short current, as shown in Fig. 2(f).

7) Commutation for RCD to MOV (t_7–t_8): At t_7, the voltage across the main breaker reaches the break voltage of the MOV ($U_{\rm MOV.1}$ shown in Fig. 3). The load current shifts again from the RCD branch to the MOV branch [refer to Fig. 2(g)].

8) Load current decreasing (t_8–t_9): At t_8, all current flows through MOV, and MOV voltage reaches a peak at $U_{\rm MOV.2}$. A counter voltage is built across L and force the load current to decrease. Finally, the load current reaches zero at t_9 [refer to Fig. 2(h)]. After the normal break process, thyristors and half-bridge submodules support the dc voltage together.

C. Reclose and Rebreak Process

A fast reclose process starts not long after the HCB is opened. Under this condition, the submodule capacitors are already charged. Therefore, a rebreak process does not need to charge the submodule capacitors again. Generally, a reclose and rebreak process of the proposed HCB includes five stages; corresponding load current paths and key waveforms are shown in Figs. 4 and 5, respectively.

1) Snubber capacitor discharge (t_{10}–t_{11}): The reclose process of the proposed HCB starts with discharging the snubber capacitor. First, thyristors and lower arm IGBTs in half-bridges are turned ON simultaneously, forming a discharge loop through $C - R - T_1$–T_{N-QL1}–$QLM - C$, as shown in Fig. 4(a). Then after 1–2 μs, capacitor voltage reaches almost zero, and the load current flows through the thyristor branch.

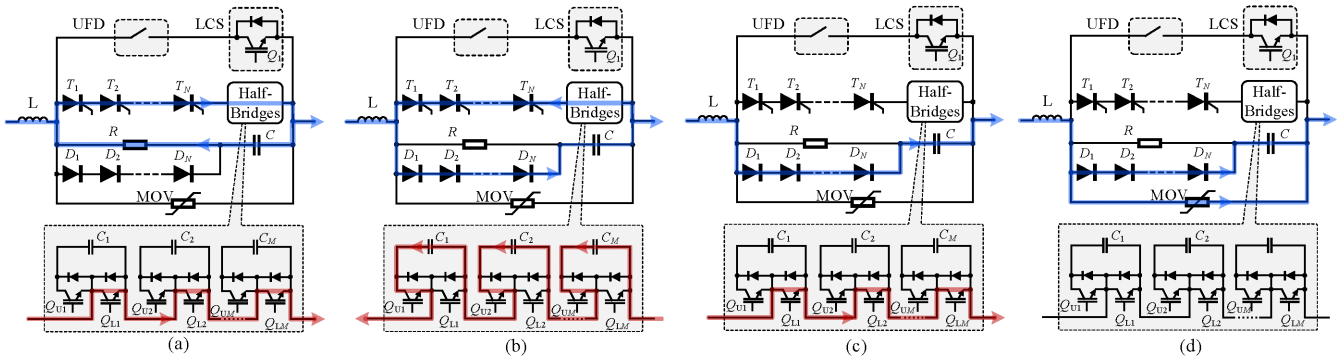

Fig. 4. Current path of the proposed HCB during reclose and rebreak process.

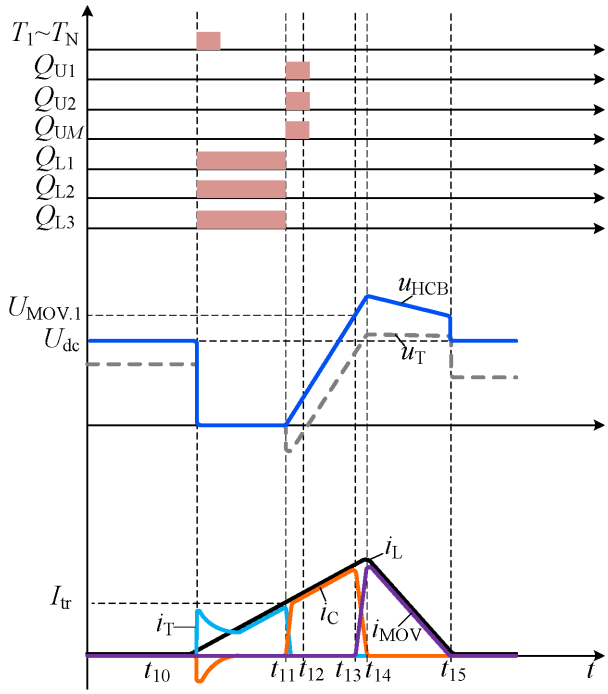

Fig. 5. Key waveforms of the proposed HCB during reclose and rebreak process.

2) Rebreak begins (t_{11}–t_{12}): If the fault is temporary, it will be cleared before the reclose process and the load current will not rise too much after the reclose process. Accordingly, a rebreak process is no longer required and the HCB is expected to conduct current. In this condition, the LCS and UFD are closed after the reclose process, and then all IGBTs in half-bridge submodules are blocked. Finally, the load current flows through the LCS and UFD branch.

However, if the fault is not temporary, the load current will rise continuously until a threshold current I_{tr} is reached, which will trigger the rebreak function. As the submodule capacitors are fully charged already during the last break process, they are ready to be used to turn OFF the thyristors by the time t_{11}. Lower IGBTs will be turned OFF first, and upper IGBTs will be turned ON subsequently. This will reversely bias the thyristors as shown in Fig. 4(b).

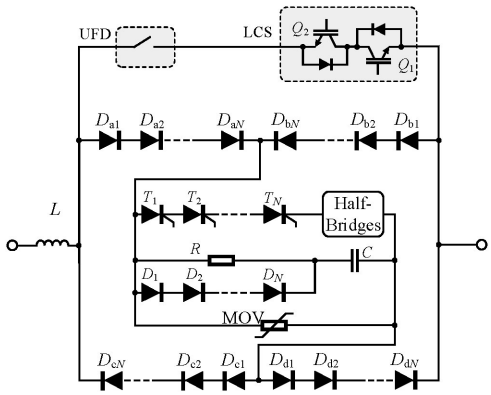

Fig. 6. Bidirectional configuration of the proposed HCB.

3) Snubber capacitor charging (t_{12}–t_{13}): It can be obtained from Fig. 4(c) that all load currents are carried by the RCD snubber at the time t_{12}; thus, the capacitor voltage rises rapidly after that. The load current amplitude, as well as the capacitor voltage rising slope, during a rebreak process is lower than those of a normal break; this is because the short circuit current amplitude is lower in a rebreak process than that in a normal break.

4) Commutation from RCD to MOV (t_{13}–t_{14}): Like the process between t_6 and t_7, after the breaker voltage exceeds $U_{MOV.1}$, MOV starts to conduct current, so the load current shifts from RCD branch to MOV, as shown in Fig. 4(d), resulting in a reverse voltage across the load inductor.

5) Load current decreasing (t_{14}–t_{15}): At t_{14}, all current flows through the MOV, a counter voltage is built across the HCB and force the load current to decrease. Finally, the load current reaches zero at t_{15}. The current path in this stage is the same as that shown in Fig. 2(h).

D. Bidirectional Configuration of the Proposed HCB

Bidirectional flow and interruption configuration of the proposed method is sketched in Fig. 6. The LCS is realized by two reversely series-connected IGBTs Q_1 and Q_2. Besides, in order to obtain bidirectional current capability of the main breaker, a diode H-bridge consisting of four diode stacks (D_{a1}–D_{an},

D_{b1}–D_{bn}, D_{c1}–D_{cn}, and D_{d1}–D_{dn}) is added to regulate the current flow.

A forward nominal current will flow through UFD-Q_2(freewheeling diode)-Q_1. When the current needs to be broken, it will flow through D_{a1}–D_{an}-main breaker-D_{d1}–D_{dn}. Similarly, a reverse nominal current will flow through Q_1(freewheeling diode)-Q_2-UFD. During the interruption of the reverse current, the current path is D_{b1}–D_{bn}-main breaker-D_{c1}–D_{cn} instead.

III. Design of the Proposed HCB

A. Design of RCD Snubber

The maximum voltage rising rate of thyristors can be obtained from the device datasheet as $(\mathrm{d}u_\mathrm{T}/\mathrm{d}t)_\mathrm{max}$; accordingly, the snubber capacitor value should be high enough to limit the critical voltage rising rate as

$$C \geq \frac{I_\mathrm{PK}}{N \cdot (\mathrm{d}u_\mathrm{T}/\mathrm{d}t)_\mathrm{max}} \tag{5}$$

where I_PK is the maximum current flowing through thyristors during HCB breaking.

After C is obtained, the snubber resistor value R needs to be designed. R is responsible to limit the current stress of the thyristors and the IGBT valves during reclose process. The maximum allowed current amplitude is determined by the device surge current capability

$$\frac{U_\mathrm{dc}}{R} \leq \min\left\{I_\mathrm{sr-IGBT},\ I_\mathrm{sr-thyristor}\right\} \tag{6}$$

where $I_\mathrm{sr\text{-}IGBT}$ is the maximum surge current value of the used IGBTs, and $I_\mathrm{sr\text{-}thyristor}$ is maximum surge current value of the used thyristors.

Also, R needs to be small enough to discharge the snubber capacitors quickly. Assume that the discharge time is T_dis, and the time constant of the $\tau = RC$ circuit should meet

$$3\tau \leq T_\mathrm{dis}. \tag{7}$$

Then, combining (6) and (7) yields

$$\frac{U_\mathrm{dc}}{\min\left\{I_\mathrm{sr-IGBT},\ I_\mathrm{sr-thyristor}\right\}} \leq R \leq \frac{3T_\mathrm{dis}}{C}. \tag{8}$$

R can be obtained through (8), while an optimized C value should be selected together with other parameters of the HCB.

It should be noted that although an RC snubber can be used instead of RCD for the sake of simplicity, the calculated R would be too small to limit the surge current amplitude during the reclose process. Therefore, RCD is a better choice in the proposed topology.

B. Design of the MOV

Rated voltage, clamping voltage, and energy absorption capability are three key parameters when choosing the MOV for an HCB. The rated voltage of the MOV is selected as the same as that of the nominal dc voltage U_dc. The clamping voltage $U_\mathrm{MOV.2}$ is commonly 1.2–2 times of U_dc according to the MOV characteristics. Although it is possible to choose a low value of $U_\mathrm{MOV.2}$ to suppress the voltage stress on power semiconductor devices during circuit breaking, in real application, that would be challenging since MOV with low clamping voltage value will require more columns to be paralleled. Besides, lower $U_\mathrm{MOV.2}$ prolongs the breaking process unwantedly according to Fig. 3. Therefore, $U_\mathrm{MOV.2} = 1.5\ U_\mathrm{dc}$ is chosen in this article to provide a relatively low breaking time and a moderate device voltage stress according to [8] and [29]. The required energy absorption capability can be obtained by integrating the power across the MOV as

$$E_\mathrm{MOV} = \int_{t_8}^{t_9} u_\mathrm{MOV} i_\mathrm{L} \mathrm{d}t \approx 1.5 {I_\mathrm{pk}}^2 L. \tag{9}$$

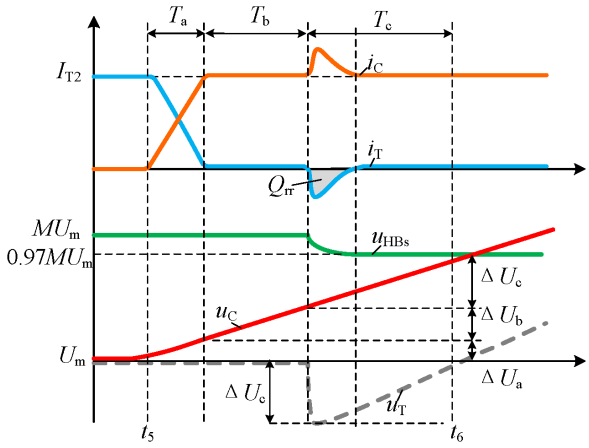

Fig. 7. Detailed waveforms during the thyristor turn-OFF.

C. Correlation Between M, N, C, and C_m

It is clear that a different M can lead to different thyristor number N, different snubber capacitor C, and different submodule capacitor $C_1 = C_2 = \cdots = C_M = C_\mathrm{m}$. Therefore, the correlation of these parameters should be expressed in detail, and through which an optimum set of parameters can be obtained.

Assume that each module capacitor voltage is U_m after being charged. Zooming in the time period between t_5 and t_6 yields Fig. 7. The thyristor current at t_5 is I_T2 according to Fig. 3. During a short period of time within t_5–t_6, the load current can be approximated as constant at I_T2. According to Fig. 7, the turn-OFF period of the thyristors can be divided into three stages: T_a—the time period for the lower IGBT (Q_L in Fig. 1) to turn OFF; T_b—the dead time required to prevent the half-bridges from short circuit; T_c—the time period when the thyristor is reversely biased.

As can be observed from Fig. 7, the lower arm IGBTs start to turn OFF at t_5, so their currents (equal to i_T) start to drop, and the snubber branch current i_C starts to rise accordingly. T_a is determined by the IGBT turn-OFF speed. The IGBT current turn-OFF rate can be approximated as constant during its turn-OFF transient. Accordingly, the capacitor voltage increase within T_a can be obtained as

$$\Delta U_a = 0.5 I_\mathrm{T2} T_a / C. \tag{10}$$

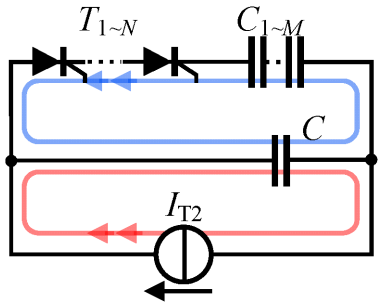

Fig. 8. Equivalent circuit during the thyristor turn-OFF.

During T_b, both upper and lower arm IGBTs are blocked. Therefore, all the load current flows through C, and the increase in u_C within T_b can be calculated as

$$\Delta U_b = I_{T2} T_b / C. \tag{11}$$

At the initial instant of T_c, the upper arm IGBTs in half-bridges are turned ON. A reverse voltage is applied across the thyristors; so the reverse recovery process is initiated. The equivalent circuit during the reverse recovery process is shown in Fig. 8. During T_c, the snubber capacitor is charged by both the reverse recovery current and the load current. Assuming the thyristor has a reverse recovery charge of Q_{rr}, the snubber capacitor voltage increase within T_c is

$$\Delta U_c = \left(I_{T2} T_c + N Q_{rr}\right) / C. \tag{12}$$

By the end of T_c, the snubber capacitor voltage u_C exceeds the total voltage of the submodule capacitors, and the thyristors are ready to withstand a forward voltage afterwards.

The reverse recovery charge NQ_{rr} during T_c are fed by the module capacitors C_1–C_M. To maintain a relatively stable voltage across C_1–C_M, the voltage drop of C_1–C_M during the reverse recovery period should be limited within 3%. Accordingly

$$0.03 M C_m U_m = N Q_{rr}. \tag{13}$$

The total voltage rise of u_C through t_5 to t_6 meets

$$0.97 M U_m = \Delta U_a + \Delta U_b + \Delta U_c \tag{14}$$

where M represents the total number of half-bridges.

In order to successfully turn OFF the thyristors, the reverse voltage period must exceed the thyristors' turn-OFF storage time t_q. Leaving a margin, we have

$$T_c = 2 t_q. \tag{15}$$

With combination of (11)–(15), the reverse voltage provided by the half-bridge submodules can be calculated as

$$M U_m = \frac{0.5 I_{T2} T_a + I_{T2} T_b + 2 I_{T2} t_q + N Q_{rr}}{0.97 C}. \tag{16}$$

During short current interrupting, the thyristor and the module capacitors will support the maximum break voltage ($U_{MOV.2}$ in Fig. 3) together. As the module number is M and module voltage is $0.97 U_m$, assume the used thyristor has a peak voltage of U_T during break, the required thyristors number N can be derived as

$$U_{MOV.2} = 0.97 M U_m + N U_T. \tag{17}$$

According to (13), (16), and (17), correlation of M, N, C, and C_m can be obtained. It can be seen from these equations that M, N, C, and C_m interact with each other. Therefore, an optimized parameter selection method should be proposed.

TABLE I
PARAMETERS OF A 10-kV/9-kA HCB

Name	Value	Name	Value
U_{dc}	100 kV	I_{pk}	9 kA
L	43 mH	T_{UFD}	2.5 ms
T_{de}	0.5 ms	I_{T1}	5 kA
I_{T2}	8.5 kA	U_m	3.3 kV
U_T	3.3 kV	T_a	2 μs
T_b	2 μs	$U_{MOV.2}$	150 kV
t_q	50 μs	Q_{rr}	600 uC

D. Parameters Optimization

Aiming at establishing a 100 kV/9 kA (rated voltage/peak current) HCB, the design guideline is given as follows. For a 9-kA peak current interruption, 4.5 kV/2 kA IGBT modules with rated current are generally used [8]. According to (16), a smaller t_q may reduce the required half-bridge modules, and thus decrease the number of expensive IGBTs and module capacitors. Therefore, pulse-power thyristors (PPTs) are preferred over phase control thyristors in the proposed CB. Finally, 4.5 kV/2 kA PPTs with $t_q = 50$ μs are selected. Table I lists some parameters which can be determined independently from M, N, C, and C_m.

As Q_{rr}, t_q, and $U_{MOV.2}$ can be read from Table I, the rest of the unknown parameters are M, N, C, and C_m.

In our design, three major concerns are total cost, breaking time, and system volume of the HCB. According to Fig. 3, T_{cg} is the charging time for the snubber capacitor. A small T_{cg} is preferred since it will reduce the total breaking time of the HCB

$$T_{cg} \approx U_{MOV.2} C / I_{T2} \tag{18}$$

Besides, as T_{cg} is in direct proportion with the snubber capacitance value C, shortening T_{cg} also implies suppressing the snubber capacitor volume. Therefore, reducing cost and shortening T_{cg} are two targets of the parameter optimization process. Fig. 9 shows the parameter optimization flowchart of the proposed method.

While M changes from 3 to 21 with a step of 3, Fig. 10 shows the varying tendency of N, C, C_m, Cost, and T_{cg}. It is clearly seen from Fig. 10 that N, C, and C_m decreases as M rises. From the cost point of view, the optimized M is 9 since the total cost touches a bottom at this point. Besides, the induced T_{cg} is around 450 μs, and the snubber capacitor C is 30 μF, preserving a relatively short breaking time and low capacitor volume. Accordingly, $M = 9$ is finally chosen as the optimized value. As M increases further, the induced T_{cg} is smaller, but the

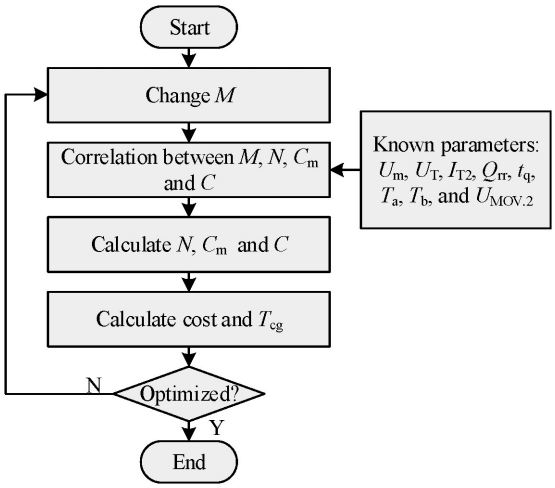

Fig. 9. Parameter optimization flowchart of the proposed HCB.

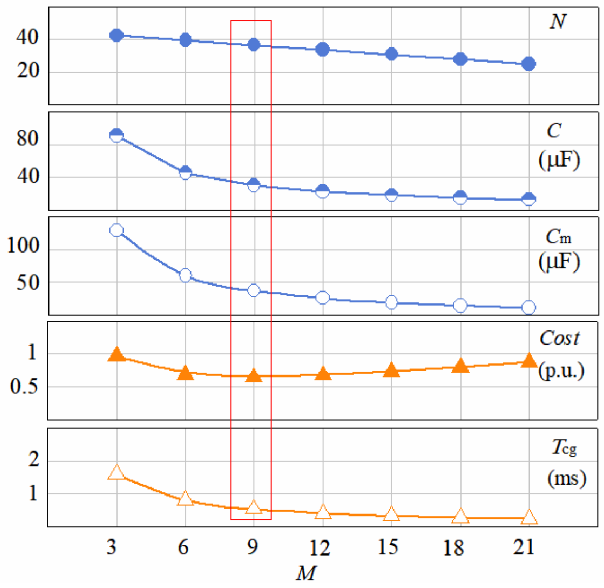

Fig. 10. Varying tendency of N, C, C_m, Cost, and T_{cg} while M is changing.

cost increases unwantedly since a larger number of expensive IGBT modules are required in the HCB. For a unidirectional 100-kV HCB, the required IGBT of the proposed topology is $9 \times 2 = 18$, while for an ABB HCB, the actual required number of IGBTs can be calculated as $1.5U_{dc}/U_m = 150$ kV/3.3 kV ≈ 46. Clearly, the required number of full-controlled semiconductors can be suppressed greatly with the proposed topology.

E. Simulation Verification

In order to verify the parameter selection method, a 100 kV/9 kA HCB is established in Matlab/Simulink software based on the parameters obtained from Table I and Fig. 10.

Fig. 11 shows the simulation waveforms during the circuit breaking. At the initial state, the load current i_L is 2 kA. A short circuit fault begins at $t = 10$ ms, and the load current rises

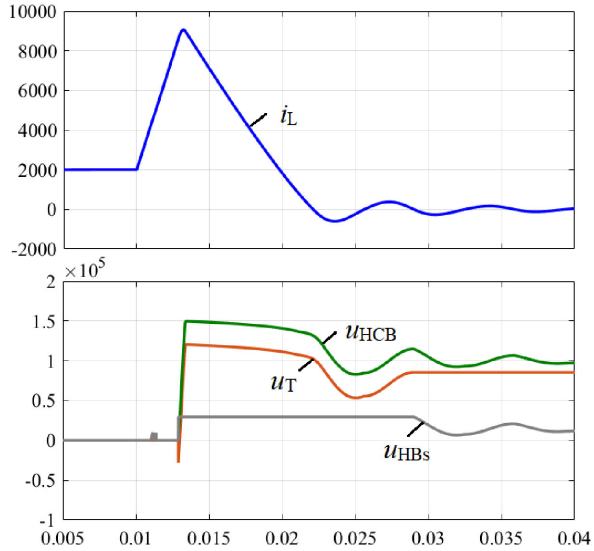

Fig. 11. Simulated waveforms of a 100-kV/9-kA HCB.

linearly to about 9 kA in the following 3 ms. At $t = 13$ ms, the current interruption is initiated. Voltage across the HCB rises fast to the clamping level of MOV. After that, the load current decreases very fast. After the short circuit current reaches zero, the snubber capacitor C still has a higher voltage than U_{dc}. Accordingly, C will discharge to U_{dc}, resulting in a resonance in the path of $C - R - L - U_{dc}(U_{dc} - L - D_1$–$D_N - C)$ as shown in Fig. 1. The load current drops down below zero and then bounces back. Since R acts as a damping resistor in the resonant path, the load current decays very fast in the following several milliseconds. In the figure, u_T is negative when the current interruption starts at $t = 13$ ms, this negative voltage helps turning OFF the thyristors completely. Soon after that, the thyristors are forward blocked and withstand up to 4/5 of the transient overvoltage during the current interruption. The induced charging time T_{cg} is measured as 430 μs from Fig. 11, which is in good match with the calculated value from Fig. 10.

IV. Experimental Verification

A. Experimental Setup

More solid verification of the proposed method is done in this section by means of downscaled experimental results. Fig. 12 shows the circuit configuration of the experimental setup. The dc power source consists of a power supply U_{dc} and a capacitor bank C_{dc}, and an inductor L serves as the current-limiting device. In the CB part, a downscaled and simplified CB is established. Since the effectiveness of the LCS and UFD has already been studied extensively and verified thoroughly in existing work, this article will focus on the solid-state part of the proposed HCB. In the main branch, eight thyristors T_1–T_8 and three half-bridge submodules HB_1–HB_3 are connected in series. The diode in the RCD snubber part is formed by two series-connected diodes D_1 and D_2.

In the load part, a load resistor R_L and a high-voltage IGBT S_L are connected in parallel. During normal operation, S_L is

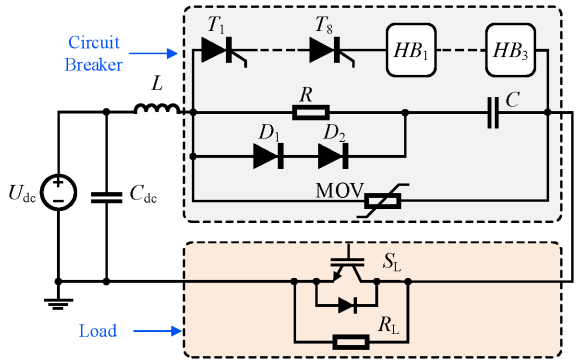

Fig. 12. Circuit diagram of the experimental setup.

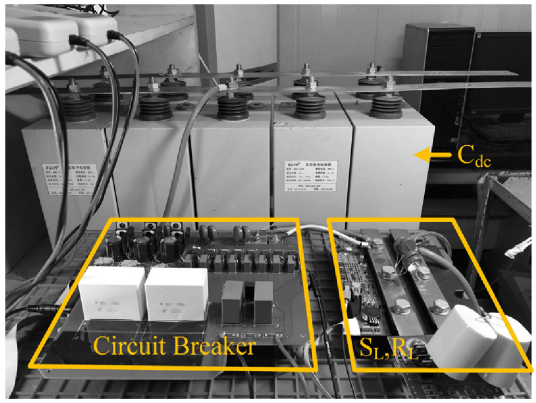

Fig. 13. Photograph of the experimental setup.

turned OFF and the load current flows through the CB and R_L. S_L is turned ON to simulate a short circuit fault on the load. Then the current breaking capability of the proposed CB can be tested. The voltage balancing circuits and snubber devices for the semiconductors are omitted in Fig. 12 for simplicity.

Fig. 13 shows the photograph of the established experimental setup, and Table II lists key parameters of the experimental setup.

B. Control Algorithms

In the prototype, the protection flowcharts during a normal break and reclose process are drawn in Fig. 14(a) and (b), respectively.

During a normal break process as shown in Fig. 14(a), the controller will sample the load current in real time. As soon as the load current exceeds the preset threshold value I_{tr}, the HCB starts to break. First, LCS is turned OFF, and UFD is triggered to open. Then after a short delay of 1.3 ms, UFD is expected to withstand a small portion of voltage; so the half-bridge module capacitors start to be sequentially charged. When the delay time reaches 2.5 ms, UFD is fully opened and the thyristors can be forced to turn OFF. After that the voltage across the HCB rises and the load current decays gradually to zero, which concludes the normal break process. During the submodule capacitor charging process, the submodules are divides into three groups, and each

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

Name	Parameters
Power supply (U_{dc})	0-1.2 kV
Bus capacitor (C_{dc})	film capacitor (2 mF/5 kV)
Load inductor (L_{load})	air cored inductor (20 mH)
Thyristors (T_1~T_8)	S4040xQ3 (400 V/40 A)
IGBT (Q_{U1}~$_{U3}$; Q_{L1}~$_{L3}$)	FGH40N60SMDF (600V/40 A)
Capacitor (C_1~C_3)	A759SZ826M2EAAE150×2 (500 V/41 μF)
Capacitor (C)	C4AQUBW5200A3MJ×2 (2600 V/10μF)
Resistor (R)	18 Ω/50 W
Diode (D_1, D_2)	DHH55-36N1F (1.8 kV/60 A)
Load Resistor (R_L)	200 Ω/500 W
IGBT (S_L)	FZ1500R33HE3 (3.3 kV/ 1.5kA)
MOV	20D152K × 6 (1.8 kV@1 mA)

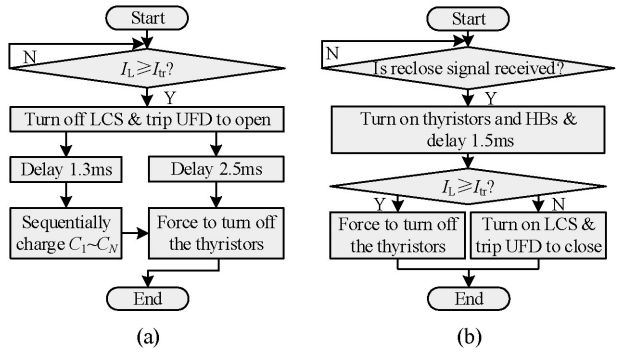

Fig. 14. Control flowcharts of the proposed HCB. (a) Normal break process. (b) Reclose process.

time, one group is charged. The required charging time for each group can be expressed as

$$\Delta t_y = \frac{1}{3}\frac{MU_{\mathrm{m}}C_{\mathrm{m}}}{i_{\mathrm{L}}(t)|_{t=T_y}} \quad (y = 1, 2, 3) \tag{19}$$

where Δt_y is the charging time required for the yth submodules group and T_y is the starting time instant when the yth group is being charged. As the load current is sampled in real time by the controller, the submodules' charging time can be determined by (19) without the need of sampling each submodule capacitor voltage. It should be noted that 1.3 and 2.5 ms shown in Fig. 14(a) are fixed values to simulate the breaking characteristics of an UFD. These values would guarantee a sufficient margin for a UFD [4]. Whereas in a real HCB, where the status of the UFD can be sampled by position sensors or other means, these two delay times may change depending on the actual opening speed of the UFD.

During a reclose process shown in Fig. 14(b), the thyristors and half-bridge submodules are turned ON to discharge the snubber capacitor C whilst the reclose command is received. After delay of 1.5 ms, C is completely discharged. The delay

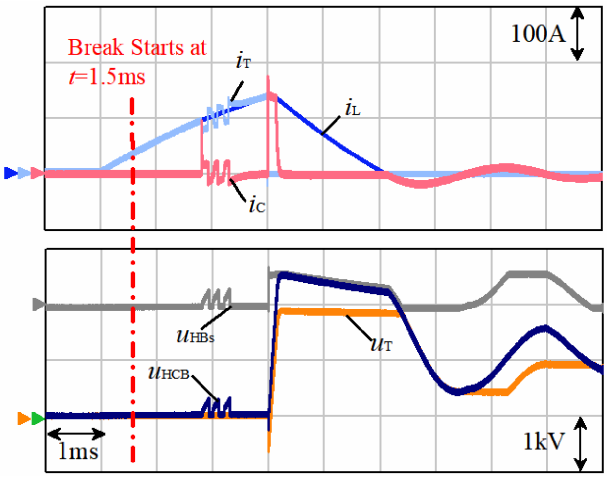

Fig. 15. Breaking waveforms of the proposed circuit breaker.

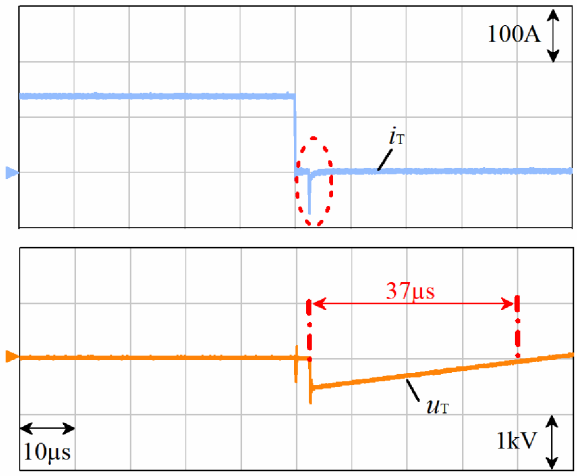

Fig. 16. Detailed turn-OFF waveforms of the thyristors.

time needs to be selected at least three times larger than the *RC* time constant of the snubber circuit, and thus ensures a zero voltage across *C* before the rebreak process is initiated. The controller samples the load current amplitude to determine the next step. If the load current $I_L \geq I_{tr}$, which means the load is still shorted, the thyristors will be forced to turn OFF again. Otherwise, the controller will turn ON LCS and UFD to conduct the normal load current.

C. Verification of Normal Break Function

Fig. 15 shows the breaking waveforms of the proposed CB. At the initial state, S_L is turned OFF, and the main breaker is in the ON-state. As the U_{dc} is 1.2 kV and R_L is 200 Ω, the load current i_L is 6 A. At $t = 1$ ms, S_L is turned ON, and the load current starts to rise. The controller detected the fault at around $t = 1.5$ ms; accordingly, at $t = 1.5$ ms, the CB starts to break. In real applications, the LCS and UFD will be triggered to break at $t = 1.5$ ms as described in Fig. 3, while in the simplified structure, no action is made since the load current is already flowing through the thyristor branch. At $t = 2.8$ ms, although UFD is not fully opened, it is able to withstand a certain value of voltage. Therefore, the half-bridge submodules start to charge their capacitors sequentially. The maximum voltage during the capacitor charging period is just 200 V, which is far lower than the peak value of u_{HCB} during the circuit breaking; therefore, charging the module capacitors will not cause arcing of the UFD. At $t = 4$ ms, the UFDs are opened completely and the HCB starts to break current. It is clearly seen that a reverse voltage is applied across the thyristors and turns them OFF, so the thyristor branch current i_T drops, and RCD branch current rises simultaneously. The breaker voltage u_{HCB} increases afterwards until a peak voltage of 2.5 kV is reached. The peak load current reaches 135 A during the break, which is two times higher than the rated current of the used IGBTs and Thyristors.

There is some time needed to charge the snubber capacitor *C* during circuit breaking. Therefore, the breaking time of the proposed HCB is higher than an ABB HCB with series-connected IGBTs. However, the increased breaking delay is quite minimum (around 100 μs in Fig. 15).

During the voltage rising period of the u_{HCB}, u_{HBs} rises first since the equivalent output capacitances of the HBs are much smaller than the dynamic balancing capacitors of the thyristors. As soon as u_{HBs} reach the module capacitor voltage, u_{HB} is clamped at around 600 V. Afterwards, the thyristors' voltage u_T rises until a peak voltage of u_{HCB} is reached. Since the dynamic balancing capacitor value is much smaller than the module capacitor C_1–C_3, u_{HBs} remains almost constant during u_T rising. Similarly, u_{HBs} drops first while u_{HCB} is decreasing. Then u_{HBs} is clamped at zero and u_T begins to drop. In conclusion, the voltage distribution between u_T and u_{HBs} does not obey a fixed portion during the voltage transients. However, the peak voltages of u_T and u_{HBs} are predictable with the above analysis. Quantitatively, the peak u_{HBs} is MU_m, and the peak u_T is defined by $U_{MOV.2} - MU_m$, where $U_{MOV.2}$ is defined by the residual voltage of MOV. In the waveforms shown in Fig. 15, the maximum u_{HBs} is 650 V, which is just around a quarter of the peak breaker voltage (2.5 kV).

Fig. 16 shows detailed voltage and current waveforms of the thyristor stack during the turn-OFF transient. At $t = 50$ μs, the thyristor current drops to zero due to the turn-OFF of the lower arm IGBTs Q_{L1}–Q_{L3}. No reverse recovery is observed at this time since no reverse voltage is applied across the thyristors yet. Then after a short dead time of 2 μs, the upper arm IGBTs Q_{U1}–Q_{U3} are turned ON at $t = 52$ μs; therefore, a reverse voltage is applied across the thyristors. The peak reverse voltage amplitude is around 600 V, which equals the sum of three module capacitor voltages. Besides, the reverse recovery process is observed in i_T waveform. The reverse recovery time is quite short, thanks to the use of fast-switching thyristors. After the reverse current drops to zero, reverse voltage of u_T lasts for around 37 μs to fully turn OFF the thyristors. After this, the thyristors will be ready to withstand a positive voltage.

Fig. 17 shows the current decreasing period of the thyristors during the forced turn-OFF period. As can be observed, the current decreasing period is $\Delta t_2 = 160$ ns. As $MU_m = 600$ V,

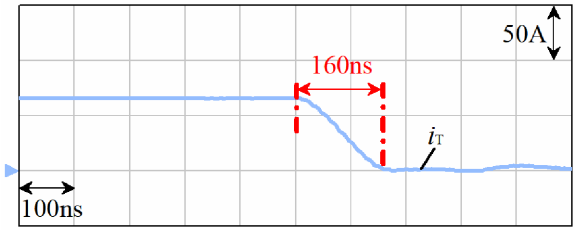

Fig. 17. Current decreasing period of the thyristors.

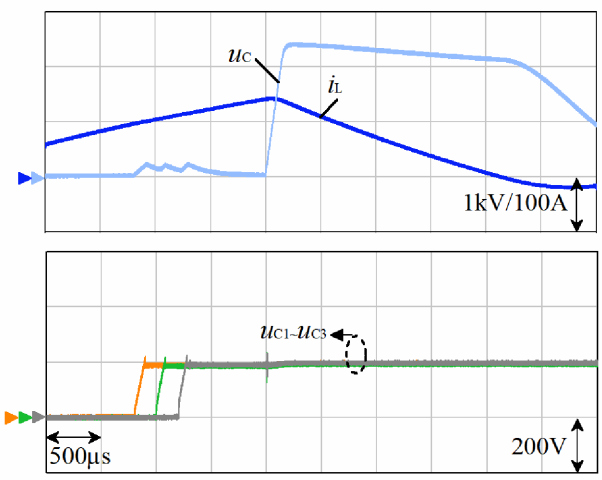

Fig. 18. Detailed waveforms during charging of half-bridge capacitors.

and $I_{T2} = 130$ A, the calculated $L_{tr} + L_c$ is 740 nH according to (4). This implies that a moderate stray inductance in the current commutation loop will have no significant impact on the current transfer speed.

Detailed waveforms during the charging process of the half-bridge submodules are shown in Fig. 18. As can be observed, the module capacitor voltages u_{C1}–u_{C3} rise sequentially from zero to the expected value. The final steady-state value of each capacitor is 200 V; therefore, a total voltage of 600 V can be reversely applied to the thyristors. Although electrolytic capacitors with very low equivalent series resistance are adopted in HBs, voltage overshoots on u_{C1}–u_{C3} are still noticeable, leading to a derating of the IGBTs. To further suppress these overshoots, film capacitors are preferable in real applications. During the capacitor charging, the RCD branch is paralleled with the half-bridges; therefore, the snubber capacitor voltage u_C envelops the module capacitor voltages, as shown in Fig. 18. After u_{C1}–u_{C3} are fully charged, u_C drops gradually to zero.

D. Verification of Reclose and Rebreak Function

Generally, the time interval between the first breaking and reclosing ranges from tens to hundreds of milliseconds according to [30] and [31]. In our test, the time interval is set as 40 ms, which is more severe than the actual working condition.

There are two conditions after a reclose process of the HCB: Reclose without fault and reclose with short circuit fault. In the first condition, HCB does not need to rebreak as the load is already normal. Fig. 19 shows the waveforms during a reclose process without fault. At $t = 3$ ms, thyristors and lower arm IGBTs are turned ON simultaneously; so the voltage across the HCB drops rapidly to zero. Then, snubber capacitor C discharges through the snubber resistor R and the semiconductors' branch. It takes about 1.5 ms until u_C drops to zero. After that, the LCS and UFD can be closed to conduct the load current. In the second condition, the load remains shorted after the reclose process; so the HCB needs to break again. Fig. 20 shows detailed waveforms of a reclose and rebreak process. Similar to Fig. 19, u_C discharges fast after the thyristors and IGBTs are turned ON. Since the load is still shorted, i_L rises linearly. The HCB can break as soon as u_C drops to zero since it does not need to wait until the UFD is opened. In this case, HCB starts to break 1.5 ms after the reclose function. As the submodule capacitors are already charged during last break process, the HCB can break directly. Since the delay time of UFD (T_{UFD} in Fig. 3) is no longer required in a rebreak process, the load current does not rise too high, yielding a peak value of 80 A.

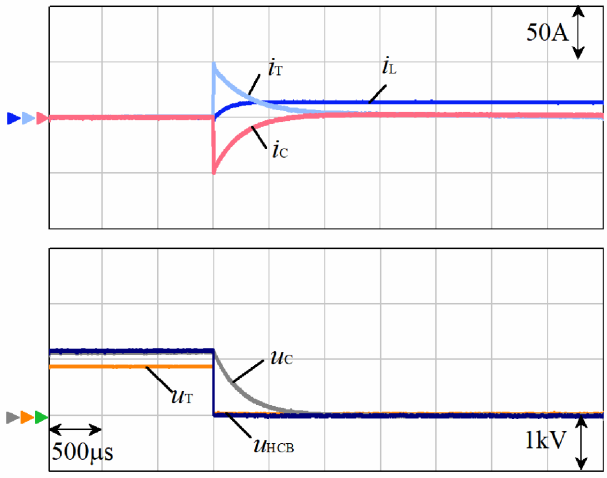

Fig. 19. Detailed waveforms during the reclose process without fault.

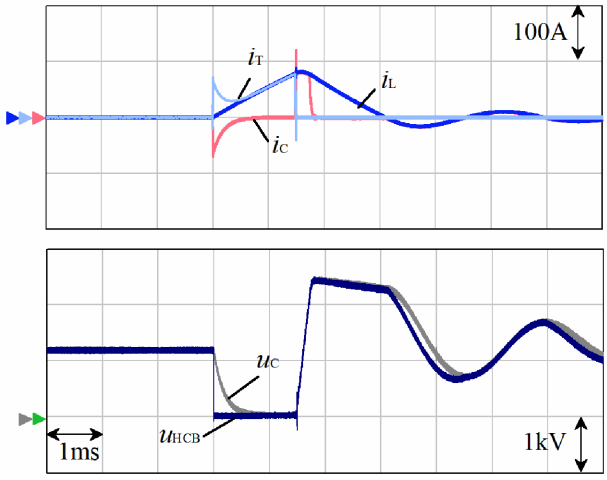

Fig. 20. Detailed waveforms during the reclose and rebreak process.

V. Conclusion

In this article, a novel HCB topology is proposed. The proposed HCB is characterized by hybrid connecting PPTs and IGBT half-bridge submodules in its main breaker part. Since thyristors can withstand a major part of the surge voltage during circuit breaking, the required number full-controlled power semiconductors are reduced significantly. This has led to a significant decrease in the total cost of the HCB. The proposed method has not increased the total breaking time by a considerable value (less than 0.5 ms) in comparison with a full-controlled semiconductor-based HCB. Besides, fast reclose and rebreak function is provided by the proposed method.

The operation principle and parameter selection method have been verified by both circuit simulation of a 100-kV/9-kA HCB and experimental results of a downscaled prototype under 1.2-kV/135-A condition.

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