Multi-objective Design and Optimization of Power Electronics Converters With Uncertainty Quantification—Part II: Model-Form Uncertainty

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***Abstract*—The second part of the multi-objective design and optimization with parametric and model-form uncertainty quantification (MDO with P&MF-UQ) is dedicated to incorporating MF-UQ into the MDO framework. MF-UQ is used to estimate the error due to modeling inaccuracies and to validate the mathematical models used in the MDO framework. In this approach, the sensitivity index introduced in the first part of the article is modified too so that it is a quantitative measure of system design robustness with regards to modeling inaccuracies as well as the manufacturing variability in the design of systems with multiple performance functions. The optimum design solution is finally realized by exploring the Pareto Front of the enhanced performance space, where the model-form error associated with each design is used to modify the estimated performance measures and the parametric sensitivity of each design point is considered to discern between cases and help identify the most parametrically robust of the Pareto-optimal design solutions. To demonstrate the benefits of incorporating uncertainty quantification analysis into the design optimization from a more practical standpoint, design of a robust high-efficiency high-power-density 1.25 kW Vienna-type rectifier is used as a case study to compare the theoretical analysis with a comprehensive experimental validation. It is shown that the final design selected using the MDO with P&MF-UQ reduces the design sensitivity and system loss by 33% and 5%, respectively, compared to the optimal design selected using the conventional MDO.**

***Index Terms*—Model-form uncertainty, multi-objective design optimization, parametric uncertainty, robustness, sensitivity, tolerances, Vienna-type rectifier.**

I. Introduction

THE MULTI-OBJECTIVE design and optimization (MDO) of power converters based on multidimensional performance space and the resultant Pareto Front was proposed in [2]. This approach in the field of power electronics has been applied to realize the performance limit relationship as well as to determine the final optimum design point, e.g., realization of ultracompact ultraefficient power converters [3]–[7].

In all previous works discussing MDO in power electronics, it is assumed that the mathematical models available for design optimization adequately model the system performance and make tradeoffs in interest for the problem. However, this assumption is, in principle, not valid because no model is perfect. Modeling inaccuracy introduces an additional source of uncertainty in the design of power converters and systems [8]. Therefore, depending on the accuracy of the model for the selected design, actual performance of the final converter could vary from the predicted performance ascertained using MDO approach.

In this article, a new method for MDO with parametric and model-form uncertainty quantification (MDO with P&MF-UQ) is proposed that includes robustness considerations with regards to modeling inaccuracies as well as the other sources of uncertainty in the design of power converters with multiple performance functions. In particular, in this approach, MF-UQ analysis enables validating models and accounting for the modeling inaccuracy in the MDO of power converters [9]. The first part of this article described how MDO with P-UQ could be accomplished by adding P-UQ loop in the system design flow and modifying the performance vector accordingly [1]. The second part of the article is dedicated to incorporating MF-UQ into the MDO framework and it is organized as follows.

In Section II, the system design flow is modified to incorporate an MF-UQ analysis into the optimization framework, where the mathematical description of the MDO and the modified performance vector are provided. Section III demonstrates the benefits of incorporating MF-UQ analysis in MDO from a more practical standpoint, where the Vienna-type rectifier is used as a case study to compare the theoretical analysis with a comprehensive experimental validation; the modified system design flow is utilized to optimize the design of a robust high-efficiency high-power-density 1.25 kW Vienna-type rectifier. Hardware demonstrations of a limited number of design points are presented to validate the analytical and numerical models used in the MDO framework, and to estimate the error due to model-form uncertainty (MFU). A regression model is then developed to predict the model-form (MF) error for the rest of design cases in the performance space; the final performance space and the resultant Pareto Front are modified accordingly. The final optimum design is ultimately realized by exploring the

Manuscript received January 26, 2020; revised April 28, 2020; accepted June 12, 2020. Date of publication July 8, 2020; date of current version September 22, 2020. Recommended for publication by Associate Editor D. Xu. *(Corresponding author: Niloofar Rashidi.)*

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Digital Object Identifier 10.1109/TPEL.2020.3007227

Pareto Front of the enhanced performance space of the system, where the MF error associated with each design is used to modify the estimated performance measures, and parametric sensitivity of each design point is used to discern between cases and to help identify the most parametrically robust of the Pareto-optimal solutions. Section IV discusses how incorporating UQ analyses into the MDO results in realizing different sets of design variable values in the final optimum design solution. Finally, Section V concludes the article.

II. Multi-objective Design Optimization With P&MF-UQ

Although adding P-UQ to the system design flow in MDO helps identifying the most robust design [1], [10], the credibility of the selected design point, in the end, relies entirely on the accuracy of the simulation models used in the process, which has not been addressed in the MDO formulation thus far. In the next step, MF-UQ should be incorporated in the MDO to estimate the error due to modeling inaccuracy, known as MF error, for all the points in the performance space.

For practical purposes, a reduced number of points in the performance space are selected based on a design of experiments (DOE) [11]. A validation metric is then used to calculate the MF error associated with performance indices for the selected design points [8].

These measured MF errors are used as training data points. Next, an interpolation procedure must be used for the estimation of MF error for the entire performance space. Thereby, MF error is based directly on what has been observed in the prediction performance of the training dataset. A regression-based model is hence developed to determine the MF error associated with performance indices of all design cases in the performance space based on validation results of the selected design points.

Primary MDO objectives as well as the sensitivity indices are then modified based on the calculated MF errors as below

$$S_i' = \frac{3\sigma_{j_i}\left(\mathbf{s}_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d\right)}{\mu_{j_i}\left(\mathbf{s}_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d\right) - \epsilon_{MF_{j_i}}\left(\mathbf{s}_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d\right)} \tag{1}$$

where S_i' is the modified sensitivity index of the ith performance measure, σ_{j_i} and μ_{j_i} are, respectively, the standard deviation and mean value of the ith performance index; $\mathbf{s}_{\mathrm{nom}}$ is the vector of variables defining nominal operating conditions; $\mathbf{x}$ and $\mathbf{x}_d$ are, respectively, the vector of nondeterministic and deterministic design variables; $\mathbf{p}$ and $\mathbf{p}_d$ are, respectively, the vector of nondeterministic and deterministic nondesign system parameters.

The modified total sensitivity index (S_T') is also calculated as follows:

$$S_T' = \sum_{i=1}^{k} w_i S_i'; \qquad \sum_{i=1}^{k} w_i = 1. \tag{2}$$

Finally, the mathematical description of MDO with P&MF-UQ is formulated as below

$$\begin{aligned} &\max\left(\mu_{\mathbf{J}}(\mathbf{s}_{\mathrm{nom}}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d) - \epsilon_{\mathrm{MF}}\left(\mathbf{s}_{\mathrm{nom}}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d\right)\right) \\ &\min S_T' \end{aligned} \tag{3}$$

such that (s.t.)

$$\begin{aligned} &\mathrm{Prob}(\mathbf{g}(\mathbf{s}_{wc}, \mathbf{x}, \mathbf{x_d}, \mathbf{p}, \mathbf{p_d}) \le 0) \ge P_{\mathrm{target}} \\ &\mathrm{Prob}(\mathbf{h}(\mathbf{s}_{wc}, \mathbf{x}, \mathbf{x_d}, \mathbf{p}, \mathbf{p_d}) = 0) \ge P_{\mathrm{target}} \end{aligned} \tag{4}$$

$$\begin{aligned} &\mathbf{x_{dLB}} \le \mathbf{x_d} \le \mathbf{x_{dUB}} \\ &\mathbf{p_{dLB}} \le \mathbf{p_d} \le \mathbf{p_{dUB}} \\ &\mathbf{x_{LB}} + 3\sigma_{\mathbf{x}}^2 \le \mu_{\mathbf{x}} \le \mathbf{x_{UB}} - 3\sigma_{\mathbf{x}}^2 \\ &\mathbf{p_{LB}} + 3\sigma_{\mathbf{p}}^2 \le \mu_{\mathbf{p}} \le \mathbf{p_{UB}} - 3\sigma_{\mathbf{p}}^2 \end{aligned} \tag{5}$$

where functions $\mathbf{g}(.)$ and $\mathbf{h}(.)$ are side conditions describing the inner converter function, the system requirements or specifications, and minimum required values of other performance indices to ensure feasibility of the designs; $\mu_{\mathbf{J}}$ is the mean vector of performance functions; ϵ_{MF} is the vector of MF errors associated with performance functions; $\mathbf{s}_{wc}$ is the vector of variables defining the worst-case operating conditions; $\mathbf{x}_{dUB}$, $\mathbf{x}_{dLB}$, $\mathbf{x}_{UB}$, and $\mathbf{x}_{LB}$ are, respectively, the vectors of upper and lower bounds on the deterministic and nondeterministic design parameters; $\mathbf{p}_{dUB}$, $\mathbf{p}_{dLB}$, $\mathbf{p}_{UB}$, and $\mathbf{p}_{LB}$ are, respectively, the vectors of upper and lower bounds on the deterministic and nondeterministic nondesign system parameters; and $\mu_{\mathbf{x}}$, $\sigma_{\mathbf{x}}^2$, $\mu_{\mathbf{p}}$, and $\sigma_{\mathbf{p}}^2$ are, respectively, the mean and variance vectors of uncertain design and nondesign system parameters.

It should be noted that, as discussed in [8], there are in fact three types of uncertainty sources that need to be considered in the design optimization under uncertainty: parametric uncertainty, uncertainty due to numerical approximations, and MFU. Uncertainty due to numerical approximations, which is mainly due to the discretization error, however, can be minimized and is often ignored when ordinary differential equation-based models are used. Thus, the proposed design optimization approach in this article quantifies and formulates design robustness with regards to PU and MFU only. Nevertheless, in the case of partial differential equation-based models, the proposed framework can be easily modified to include this source of uncertainty in the framework by adding another computation loop in the system design flow.

III. Case Study: Design Optimization of a Vienna-Type Rectifier

The first part of the article demonstrated the benefits of incorporating the P-UQ analysis into the MDO where the Vienna-type rectifier, i.e., a popular topology for implementing ac–dc mains interface in MEA, was used as a case study. A thorough mathematical modeling and design optimization of the converter system and its components concerning efficiency and power density within given size limitations and operational requirements (electromagnetic interference (EMI), power quality, and temperature) were provided. Key specifications, design variables, procedures, and models involved in the design and optimization were also presented. The MDO with built-in P-UQ was then used to design a robust free-convection-cooled Vienna-type rectifier with an input EMI filter [1].

In the following, the same converter is used as a case study to present the benefits of incorporating MF-UQ into the MDO from a more practical standpoint.

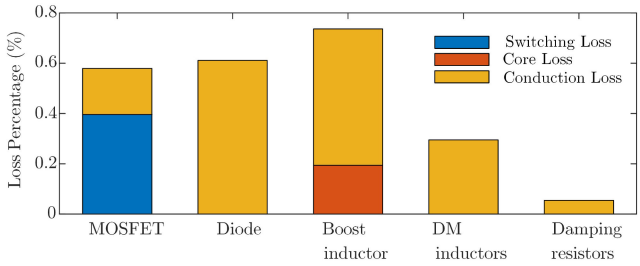

Fig. 1. Maximum contribution of each component to the total converter loss with loss breakdown for each component

A. System Design Flow With P&MF-UQ

To validate the analytical and numerical models used in the MDO framework, and to estimate the MF error for all the points in the performance space, hardware demonstrations of a limited number of design points are presented with measurement results indicating the actual loss and size of the selected design points. Given the acceptable accuracy of the size models used in the design process and their low weighting factor in the optimization problem defined in this article, MF error is only calculated for loss models.

In this section, to begin, DOE is conducted to determine different value combinations of design variables that should be studied for accuracy assessment of loss models. In this work, two hardware prototypes are built and tested for each design to evaluate the accuracy of the models used in the MDO framework. These tests are specifically in regard to the accuracy assessment of models in the prediction of primary performance measures and to ensure that the design meets qualification testing standard constraints. A Gaussian process (GP) regression model is then developed to predict the MF error of the rest of design cases in the performance space based on validation results of the selected design points.

1) Design of Experiments: MOSFET, diode, boost inductor, DM inductor, and damping resistors are the components considered in the total loss calculation of the Vienna-type rectifier. There are several design variables associated with these five components that are loss-model input parameters as well; i.e., switching frequency, boost-inductance value, boost-core size, boost-core type, DM-core type, DM-core size, MOSFET ON-resistance, and diode current rating. In this section, a DOE is conducted to study the effect of these design variables on the MF error.

To minimize the number of variables in the DOE, the components are first ranked based on their contribution to the total converter loss. Those with an insignificant contribution to the total loss can be ignored in the DOE, as their effect on the changes in the MF error over the entire performance space is perhaps insignificant. It should be noted that the contribution of each component to the total loss is not the same for all points in the performance space. To evaluate the importance of a component regarding loss calculation, its maximum contribution over the whole performance space is used for the comparison. Fig. 1 shows the maximum contribution of each component to the total converter loss, indicating loss breakdown for each component.

The analysis of loss distribution shows that the boost inductor is the most important component to be considered in the DOE as it contributes up to 70% to the total loss in the Vienna-type rectifier. MOSFETS and diodes each contribute more than half, about 60%, to the total loss individually. DM inductors and damping resistors, however, are excluded from DOE due to their low contribution to the converter loss. Finally, those design variables associated with boost inductor, MOSFET, and diode are considered as variables in the conducted DOE.

To further minimize the number of design variables and their range in the DOE, the values of each design variable for the feasible design points in the performance space, especially for the Pareto-optimal solutions and their nearby design points, hereinafter referred to as the critical region, need to be studied. In fact, for a better decision-making, design solutions in the critical region require a precise estimate of their associated MF error as they are more likely to be selected as the final design. Therefore, the selected values of each design variable in the DOE must focus on its value in this region. Fig. 2 shows the color-coded resultant Pareto Front of performance space with P-UQ; the color of each design point in the performance space indicates the value of the selected design variable for the design corresponding to that specific point.

The switching frequency of feasible design points ranges from 60 to 86 kHz. As shown in Fig. 2(a), the frequency range of the critical design points, however, is more focused on lower values. As seen in Fig. 2(b), both diode candidates are used in the design points of the critical region. With regards to the MOSFET, as illustrated in Fig. 2(c), although the 200N25N3 device is dominant in the critical region, due to the critical role of MOSFET in determining the total loss of the converter, the MOSFET selection option will remain as a variable in the DOE.

According to Fig. 2(d), boost-inductance value of the design points in the critical region is more focused on higher values. In addition, in the critical region, very few design points have been implemented using a powder core. Over 85% of the points on the Pareto front are, in fact, based on the use of a ferrite core [see Fig. 2(e)]. The conducted DOE is thus limited to designs with ferrite cores. Also, as shown in Fig. 2(f), the design points using cores with an effective volume of 5470 and 52600 mm^3 will result in points toward extreme loss or size values in the performance space, which are not desired among Pareto-optimal design solutions. Therefore, the conducted DOE will be limited to those core sizes with an effective volume of 9440 and 25800 mm^3.

In summary, the following design variables and their respective values have been selected for the DOE:

1) diode: 16G65C5 (Diode 1) and 20G65C5 (Diode 2);
2) MOSFET: 200N25N3 (MOSFET 1) and 600N25N3 (MOSFET 2);
3) switching frequency: 64 and 76 kHz;
4) boost-inductance value: 410 and 450 μH;
5) boost-core type and size: ferrite cores with 25800 and 9440 mm^3 effective volume.

It is assumed that for the same operating condition, the losses generated by different components in the Vienna-type rectifier are independent of one another, i.e., the parameters used in estimating the loss of a component are not affected by the design

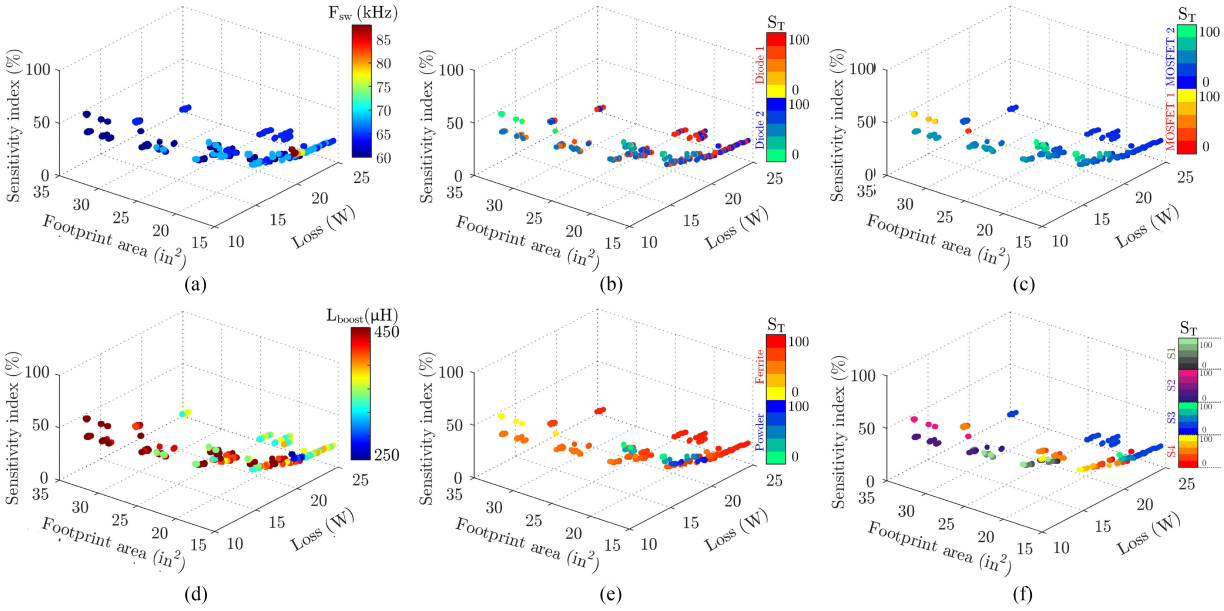

Fig. 2. Enhanced Pareto Front of the Vienna-type rectifier; the color of each design point indicates the (a) switching frequency, (b) diode number (diode 1: IDH20G65C5 and diode 2: IDH16G65C5), (c) MOSFET number (MOSFET 1: IPB200N25N G3 and MOSFET 2: IPB600N25N G3), (d) boost-inductance value, (e) boost-core type, and (f) boost-core size (s_1: 9440 mm^3, s_2: 5470 mm^3, s_3: 52600 mm^3 s_4: 25800 mm^3); the spectrum identifies the total sensitivity value of the design for discrete design variables.

TABLE I
FINAL SELECTED DESIGN POINTS FOR THE CONDUCTED VALIDATION EXPERIMENTS BASED ON A DOE

Design		1		2		3		4		5		6	
		a	b	a	b	a	b	a	b	a	b	a	b
Diode		2		1		2		1		2		2	
MOSFET		2		2		1		1		2		2	
Boost inductor	Inductance value (μH)	410		410		410		410		410		450	
	Core size (mm^3)	25800		25800		25800		25800		9440		25800	
Switching frequency (kHz)		64	76	64	76	64	76	64	76	64	76	64	76

variables associated with other components. In other words, the dissipated loss of a component will not affect the loss generated by the rest of the components. As a result, it is assumed that there is no interaction between design variables regarding the accuracy of the total loss of the converter. Four one-factor DOEs are thus conducted to study the main effects of MOSFET ON-state resistance, diode current rating, core size, and inductance value on the accuracy of the estimated loss (see Design 1a–3a, 5a, and 6a in Table I).

It should be noted that in the PCB layout of the final converter, semiconductor devices are placed close to one another. The temperature rise for diodes (MOSFETs) might be affected by the dissipated heat by MOSFETs (diodes); as a result, the temperature-dependent parameters of the diodes (MOSFETs) and their generated losses might get affected. This may violate the assumption made earlier regarding independence of estimated loss for components from one another. To verify the assumption, another case is also tested, in which both diode and MOSFET devices are changed compared to any of the first three designs conducted above (see Design 4a in Table I).

Furthermore, switching frequency affects the estimated loss of all critical components. As a result, for each of the selected designs, the switching frequency is varied and the results are obtained to investigate the effects of switching-frequency value on the accuracy of estimated loss for each component (see Design 1b - 6b in Table I).

In summary, 12 different validation experiments need to be conducted, each of which correspond to a unique design point in the performance space. Table I summarizes the selected design points. It is worth noting that the primary design points (Designs 1a–6a) are selected from feasible designs in the performance space. Also, to have a fair comparison, these primary designs have been selected in such a way that, except for the DOE variables, the remaining design and nondesign system parameters of the converter are quite similar in all six designs.

2) Validation Experiment: For the sake of brevity, this section presents testing results and the performance evaluation of one of the hardware prototypes built based on Design 1 only. Similar experimental results were achieved for the remaining designs.

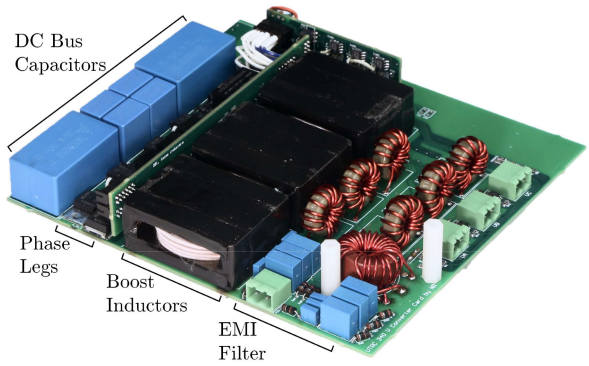

Fig. 3. Converter card hardware prototype based on Design 1.

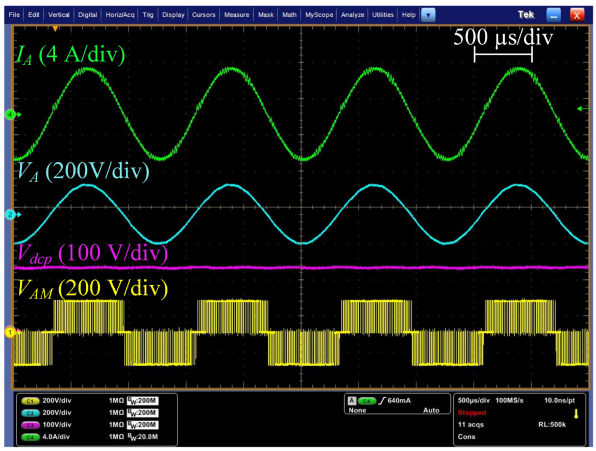

Fig. 4. Vienna-type rectifier operation waveforms for Design 1a with 800 Hz line frequency. I_a is the input current of phase A, V_a is the input phase to neutral voltage of phase A, V_{am} is the phase-leg output voltage (voltage at point *A* referred to neutral point *M*), V_{dcp} is the voltage across upper capacitor of the dc bus.

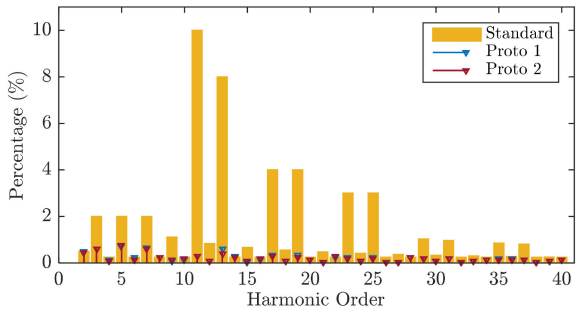

Fig. 5. Input-current harmonics of Design 1a with 800 Hz input frequency.

Fig. 3 shows one of the hardware prototypes built based on Design 1. Experimental waveforms at nominal output power at 800 Hz input-line frequency are shown in Fig. 4.

The input current is measured and analyzed to evaluate an input power quality. Phase currents in the tests are measured by a Tektronics TCP0030 current probe, and the spectrum is calculated by MATLAB. The input-current spectrums within the power-quality standard range (from the second-order harmonic up to the 40th-order harmonic), with 800 Hz input frequency, are shown in Fig. 5. As shown, there is no violation with regards to

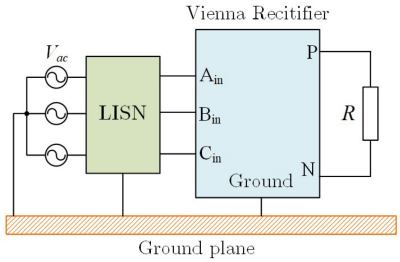

Fig. 6. Grounding arrangement for EMI measurement setup.

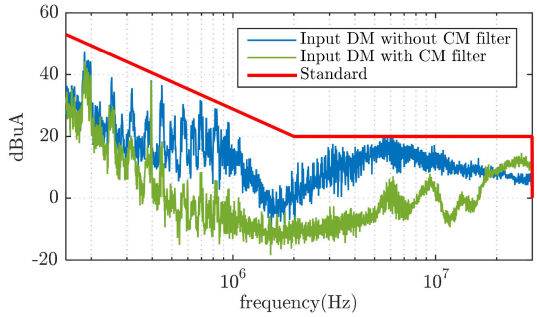

Fig. 7. Input current spectrum for Design 1a and EMI standard.

TABLE II
SUMMARY OF THE CM FILTER DESIGN FOR THE VIENNA-TYPE RECTIFIER

Design		Design parameters
CM choke	Inductance value (μH)	230
	Core part number	Vac T60006-L2015-W865
	Windings	9 turns of AWG 19
CM capacitors	Capacitance value (nF)	10
	Part number	EPCOS 32911
R_{CMdamp} (Ω)		1

power quality in the 800 Hz line-frequency case. Similar result was derived at 360 Hz line frequency.

Tests have also been conducted to evaluate the EMI performance of the converters. The converter-grounding arrangement for EMI measurement is shown in Fig. 6. The input currents are measured by an ETS-Lindgren 95510-1 current probe and are captured by an Agilent E7402A EMC analyzer. All measurements are taken under full-load operation, 400 Hz input frequency and 115 V ac input voltage. The measured input DM current spectrum and EMI standards are shown in Fig. 7. As shown, by adding a common mode (CM) filter, the DM noise is effectively attenuated due to the cross-coupling between CM and DM noise, which is identified as mixed-mode noise [12]. The mixed-mode noise occurs due to the circuit asymmetry caused by the tolerance of components and can be attenuated by adding a CM filter. The design of the CM filter is summarized in Table II. In all six designs, however, with and without CM filters, line-current noise complies with the standard within the conducted EMI frequency range (150 kHz–30 MHz); this validates the design of the input EMI filter.

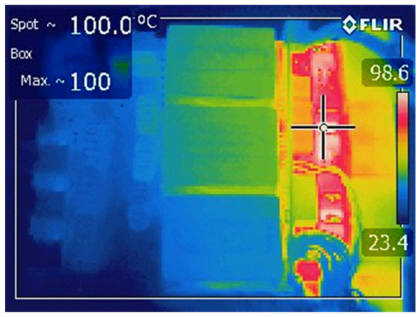

Fig. 8. Temperature distribution of the converter based on Design 1a.

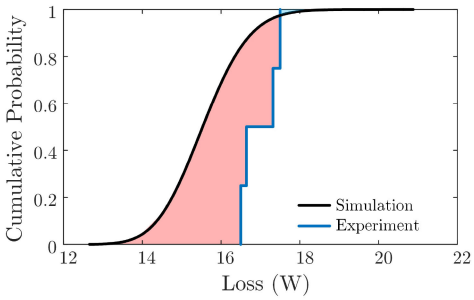

Fig. 9. CDFs of the total loss from simulation and experiment for Design 1a (d^+, red shaded region, and d^-, blue shaded region).

To evaluate the thermal performance of the converter prototype, the temperature is measured by an FLIR E40 thermal camera. The thermal graphic of the converter prototype under full-load operation, when the temperature of all devices has reached in a steady state, is shown in Fig. 8. According to the recorded temperature for all designs at nominal output power and at lab ambient temperature without active cooling, the hottest spot appears on the diode. In all scenarios, the case temperatures of the diodes and MOSFETs remain below their maximum temperature limit (175 °C), and thus, safe operation of the devices is verified. If the ambient temperature is higher, e.g., 70 °C, assuming the loss of the device is kept the same, a 45 °C increase in junction temperature is expected. This results in over 150 °C junction temperature, which is marginal for the safe operation. However, the surface temperatures of other components such as boost inductors, DM inductors, and filter capacitors are far below their limits.

Finally, for efficiency measurements, input and output power are measured by a Yokogawa PZ4000 power analyzer. All tests are conducted with about 1.25 kW input power, 115 V_{ac} input voltage, and 400 Hz input-line frequency. The efficiency data were recorded over 15 cycles at steady state operating condition (after 30 min of full-load operation) for a period of 90 s. The mean value of those measurements was then used as the recorded efficiency. This measurement was repeated in another run for each prototype. Fig. 9 shows the cumulative distribution function (CDF) from the measured efficiency for Design 1(a) at nominal output power.

3) Validation Metric: In this section, the CDF from experimental measurements together with the CDF from simulation results (discussed in [1]) are used to estimate the MF error associated with each design point for which a validation metric is used.

The modified area validation metric, that is the validation metric used in this article, separately tracks the regions between CDFs of simulation and experimental results for each design point (see Fig. 9) [8]. Specifically, the region where the experimental values are larger than the simulation values is referred to as "d^+," and the region where the experimental values are smaller than the simulation values, is referred to as "d^-." The MF error (ϵ_{MF}) is then calculated using

$$\epsilon_{\mathrm{MF}} = d^+ - d^-. \tag{6}$$

The calculated MF error is finally normalized with respect to the mean value of the loss distribution (μ_{Loss}) obtained from simulation results

$$\epsilon_{\mathrm{MFnorm}} = \frac{\epsilon_{\mathrm{MF}}}{\mu_{\mathrm{Loss}}} \times 100. \tag{7}$$

This value indicates the percentage of MF error at each design point. The normalized MF error for all 12 design points is summarized in Table III.

It should be noted that to use one factor DOE, it was assumed that the estimated losses of components are independent of one another. If the assumption is valid, then the MF error for Design 4 can be calculated based on Designs 1, 2, and 3, as follows:

$$\begin{aligned}\epsilon_{\mathrm{MFnorm4}} &= \epsilon_{\mathrm{MFnorm1}} + \Delta\epsilon_{\mathrm{MFnorm21}} + \Delta\epsilon_{\mathrm{MFnorm31}} \\ &= \epsilon_{\mathrm{MFnorm1}} + (\epsilon_{\mathrm{MFnorm2}} - \epsilon_{\mathrm{MFnorm1}}) \\ &\quad + (\epsilon_{\mathrm{MFnorm3}} - \epsilon_{\mathrm{MFnorm1}}).\end{aligned} \tag{8}$$

According to MF error of Designs 1, 2, and 3, the MF error for Designs 4a and 4b is estimated to be 1.5488 W (8.85%) and 1.4749 W (7.89%), respectively, which is very close to the measured values directly from Design 4. This verifies the assumption made in the DOE.

As seen, overall, the MF error is significant, and for most of the cases the model is underestimating the total converter loss. However, its percentage varies depending on the value combinations of design parameters. The observed trend in the measured MF errors reveals that the MF error is perhaps due to the poor thermal model used in the MDO framework. In other words, as the expected temperature-rise for a design increases/decreases, the thermal model fails to provide an accurate estimate of the expected change in parameter values.

Besides, the contribution of auxiliary circuit components to the total losses and the traces in the PCB board were not considered in the design, which also results in underestimating the loss.

4) GP Regression

The calculated MF errors of the designs selected based on the DOE are used as training dataset. The training dataset in this case contains five variables, of which the diode and MOSFET are categorical variables, and switching frequency, boost-inductance value, and boost inductor-core size are numerical variables.

Many linear and nonlinear parametric regression tools are available for the predictive modeling, which try to find the best fit for the training dataset [13]. The best fit is ultimately used to

TABLE III
CALCULATED MF ERRORS FOR THE TRAINING DATASET

Design	1		2		3		4		5		6	
	a	b	a	b	a	b	a	b	a	b	a	b
ϵ_{MF} (W)	1.59	1.41	1.19	1.06	1.94	1.82	1.49	1.36	4.90	4.92	2.22	2.12
ϵ_{MFnorm} (%)	10.03	8.46	7.48	6.38	11.40	9.91	8.71	7.37	24.56	23.66	13.93	12.64

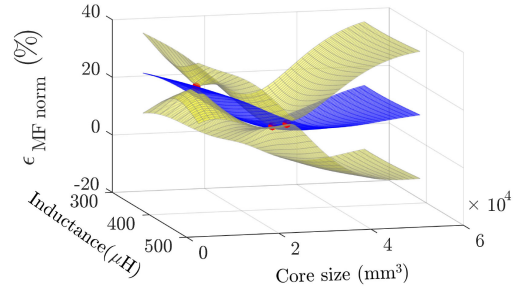

Fig. 10. Mean of the estimated MF error (blue plane) and its 95% PI (yellow planes) versus boost inductor-core size and boost-inductance value for MOSFET 600N25N3, diode 20G65C5, at 64 kHz switching frequency; red points indicate the training data points.

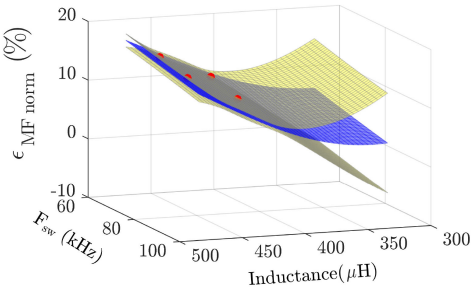

Fig. 11. Mean of the estimated MF error (blue plane) and its 95% PI (yellow planes) versus switching frequency and inductance value for MOSFET 600N25N3, diode 20G65C5, and 9440 mm^3 boost inductor-core size; red points indicate the training data points.

make predictions. In this article, however, the GP regression is used for developing a regression-based predictive model. GP regression is a simple nonlinear nonparametric regression tool, which is widely used in various application areas; it is an alternative for parametric regression tools [14], [15]. This method gives a prior probability to every possible function. This prior distribution is then conditioned on the training dataset, and a posterior distribution is finally derived over all possible functions.

A complete discussion on GP regression tools is provided in [14]; following the same procedure, a GP regression is developed for MF error using the 12 training data points, i.e., 12 estimated MF errors. Equation (9) denotes the GP regression model specified by its mean and covariance functions that are $m(\mathbf{X})$ and $k(\mathbf{X}, \mathbf{X}_0)$, respectively,

$$\epsilon_{\mathrm{MFnorm}}(\mathbf{X}) \sim GP(m(\mathbf{X}), k(\mathbf{X}, \mathbf{X}_0)) \tag{9}$$

where $\epsilon_{\mathrm{MFnorm}}(\mathbf{X})$ is the vector of MF errors for all feasible designs in the performance space, $\mathbf{X}$ is the vector of design variables corresponding to feasible designs in the performance space, and $\mathbf{X_0}$ is the vector of training dataset that are the

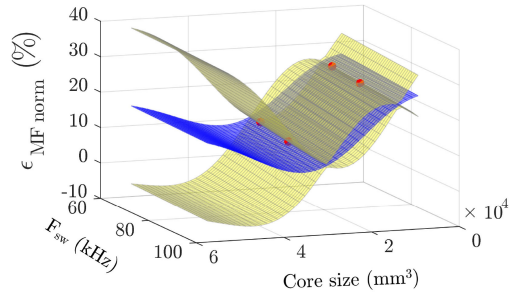

Fig. 12. Mean of the estimated MF error (blue plane) and its 95% PI (yellow planes) versus switching frequency and boost-core size for MOSFET 600N25N3, diode 20G65C5, and 410 μH boost-inductance value; red points indicate the training data points.

combinations of design variables for which MF error is available (see Table III).

Among possible options for the covariance function, squared exponential covariance function is selected due to the smooth function behavior that is expected for the MF error over different design points. The associated hyper parameters with the covariance function are then calculated using maximum likelihood [14]. The mean function is first assumed to be zero; however, this can be later modified, and it is not a drastic limitation, as the mean of the posterior process is not confined to zero. Furthermore, in this case, the training dataset is considered to be noisy due to inevitable measurement errors. As a result, the error bound would not be zero at the training data points but has a minimum value. Moving away from the training data points, the error bound increases. More training data points are thus required to reduce the error bound associated with the estimated MF errors. GP finally defines a posterior distribution over all possible functions conditioned on the training dataset. A 95% prediction interval is selected to calculate an error bound for the predicted MF errors.

To provide an insight into the relationship between the estimated MF error using GP and design variables, for a given diode and MOSFET, predicted MF error versus the boost-inductance value and boost-core size for 64 kHz switching frequency, predicted MF error versus the switching frequency and boost-inductance value for designs with 9440 mm^3 core size; the predicted MF error versus the switching frequency and boost-core size for designs with 410 μH boost-inductance value are shown in Figs. 10, 11, and 12, respectively.

B. Final Performance Space With P&MF-UQ

The estimated loss and total sensitivity of each point in the performance space is finally modified using (1)–(5). Fig. 13 illustrates the performance and the resultant Pareto Front using MDO with P-UQ and MDO with P&MF-UQ.

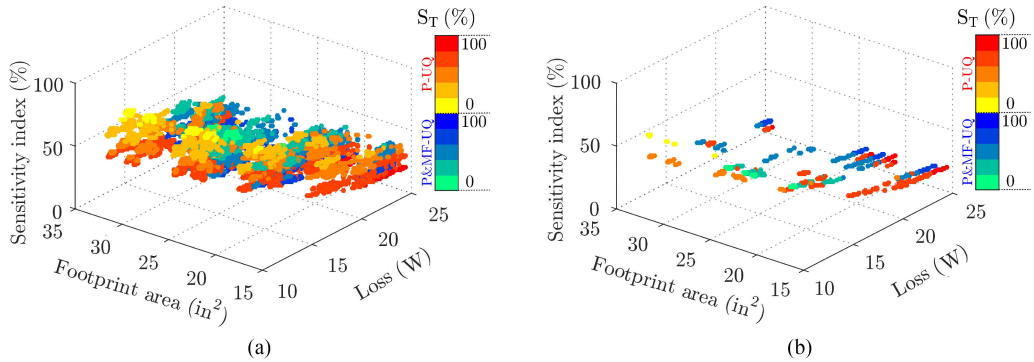

Fig. 13. Enhanced performance space and the resultant Pareto Front for the Vienna-type rectifier, where the red colormap corresponds to MDO with P-UQ and the blue colormap corresponds to MDO with P&MF-UQ.

TABLE IV
PERFORMANCE MEASURES OF THE SELECTED OPTIMUM DESIGNS BASED ON THE CONVENTIONAL MDO, MDO WITH P-UQ, AND MDO WITH P&MF-UQ

MDO Approach / Performance Index	Without UQ	With P-UQ	With P&MF-UQ
Size (in^2)	21.58	21.58	21.58
Loss (W)	14.02	14.10	14.14
Total sensitivity (%)	49.70	30.6	31.18
Compensated loss (W)	15.94	15.65	15.17
Compensated total sensitivity (%)	43.71	27.84	29.10

TABLE V
KEY DESIGN VARIABLES OF THE SELECTED OPTIMUM DESIGNS BASED ON THE CONVENTIONAL MDO, MDO WITH P-UQ, AND MDO WITH P&MF-UQ

MDO Approach / Design Variable		Without UQ	With P-UQ	With P&MF-UQ
Diode		2	2	1
MOSFET		1	2	2
Boost inductor	Inductance (μH)	330	410	390
	Core size (mm)	25800	25800	25800
	Airgap length (mm)	0.54	0.64	0.62
	Number of turns	21	25	24
DM inductor	Inductance (μH)	24.4	25.5	26.1
	Core size (mm)	19	22	22
	Airgap length (mm)	0	0	0
	Number of turns	16	16	16
Damping resistance (Ω)		1	0.5	2
Switching frequency (kHz)		68	64	64

As seen, by adding the MF error, the final performance space and the resultant Pareto Front are changed compared to those obtained by the MDO with P-UQ. According to the results from validation experiments, the estimated loss for the selected optimum design solution based on MDO with P-UQ was actually inaccurate by around 2 W. After correcting the loss models by adding the error term to them, so that the models now match the experiments, the preselected optimum design point based on MDO with P-UQ is outperformed by another design, which was not previously realized as a Pareto-optimal solution. A new design is hence selected that features 15.17 W loss and a footprint area of 21.58 in^2. This design is found to have better performance overall as compared to the optimum designs that were selected based on the conventional MDO and MDO with P-UQ. Table IV summarizes the actual performance measure of the selected optimum design based on the conventional MDO, MDO with P-UQ, and MDO with P&MF-UQ.

As mentioned, the MF error affects constraint conditions as well; as a result, in the new performance space the number of feasible designs is reduced by 20%. The number of Pareto-optimal designs is also increased by 15%. It should be noted that not all the Pareto-optimal designs from the MDO with P-UQ approach are among the new Pareto-optimal design solutions. This further emphasizes the necessity of including P&MF-UQ analysis in the MDO, as without considering these sources of uncertainty, an incorrect nonoptimum design solution might get selected.

Despite all the long-term benefits of incorporating UQ into the MDO, the main drawback of this approach is its initial high cost regarding both computation and hardware prototyping. In this article, the computational cost for the MDO with UQ is 442 core hours, whereas this value for the MDO without UQ is 0.63 core hour.

IV. DISCUSSION

Table V summarizes the key design variables of the selected optimum designs based on the conventional MDO, MDO with PU-Q, and MDO with P&MF-UQ. This section discusses how

incorporating P-UQ and MF-UQ analyses into the MDO results in realizing a different set of design variable values in the final optimum design solution.

According to simulation results, the estimated loss for Diode 1 is slightly higher than that of Diode 2, and MOSFET 2 is expected to have significantly higher loss compared to MOSFET 1. Therefore, in the MDO without UQ, Diode 2 and MOSFET 1 are selected as the semiconductor devices to minimize the total converter loss. It should be noted that, since the MOSFET and diode selection in this case does not affect the size of the converter, no compromise between loss and size needs to be made in the selection of semiconductor devices. The switching frequency, boost inductor core size, and boost-inductance values are, however, selected based on a compromise between loss and size.

In the design with P-UQ, it is found that the design becomes less sensitive to tolerances by simultaneously decreasing the switching frequency and increasing the boost-inductance value. Therefore, in the selected optimum design solution based on MDO with P-UQ the switching frequency is reduced to 64 kHz and the inductance value is increased to 410 μH. In this case, MOSFET 2 is selected, which slightly increases the nominal loss of the converter, resulting in a decrease in the sensitivity of the design. The effective loss of this design, i.e., the product of sensitivity index and nominal loss, however, is lower than what occurs in the design that was selected based on the conventional MDO. In other words, the selected design based on P-UQ has a better performance overall as compared to the design that was selected based on the conventional MDO.

Finally, according to validation experiments and estimated MF errors, it is found that the developed converter loss model is not accurate; it is, in fact, on average around 2 W inaccurate over the performance space. Specifically, it is found that the actual loss of Diode 1 is significantly lower than Diode 2. Therefore, in the new optimum design, Diode 1 is selected. In addition, according to validation experiments, the actual loss difference between MOSFETs 1 and 2 is less than the predicted values from simulation results; in reality, MOSFET 2 will not cause any significant increase in the nominal loss of the converter. Therefore, in the final design, MOSFET 2 remains as the selected device to maintain low sensitivity index without a significant increase in the nominal loss. According to validation experiments, it is also shown that for the same core size, increasing the inductance value will, in fact, significantly increase core and conduction losses. Therefore, there is a compromise between design sensitivity and the converter loss, which should be considered when increasing the inductance value. As a result, in the final design selection, the inductance value is reduced to 390 μH, which allows the nominal loss to be reduced with a slight increase in the sensitivity index, as compared to the design selected based on MDO with P-UQ.

Notably, from the MF error estimated for six design cases, it can be concluded that the thermal model needs to be improved, as there is a relationship between the expected temperature rise and the calculated error. For the boost inductor, in particular, it can be concluded that the thermal model performs poorly. Although it has been assumed that all cores are large enough to dissipate the thermal loss, when comparing the MF error for Designs 5 and 1, it can be seen that once a smaller core is selected, the temperature rise is, in fact, significant and has affected the temperature-dependent parameters and total loss accordingly.

V. Conclusion

In this article, MDO with P&MF-UQ was developed and applied to the design optimization of a Vienna-type rectifier, with regards to its primary performance measures, i.e., loss and size, and the total sensitivity, while considering specific design constraints, operation requirements, and modeling inaccuracies.

The final optimum design was realized by exploring the system loss-size-sensitivity Pareto Front of the enhanced performance space, where the MF error associated with each design was used to modify the estimated performance measures based on the estimated modeling error; the parametric sensitivity of each design point was used to discern between cases and to help identify the most parametrically robust of the Pareto-optimal solutions. For comparison purposes, the results of the traditional formulation and MDO with P-UQ were also illustrated. The final design selected using the MDO with P&MF-UQ was shown to reduce the design sensitivity and system loss by 33% and 5%, respectively.

Another advantage of including P&MF-UQ in the design is that even when the model used in the MDO is not accurate, this approach quantifies the inaccuracy of the model and modifies the performance space accordingly to select the actual optimal design solution. MF estimation will also provide insights into any fidelity improvements needed in the model to reduce the uncertainty for future design iterations.

The main conclusion drawn from the results provided in this article is that the MF error and sensitivity of each design point could potentially change the performance space and its resultant Pareto Front. Thus, ignoring these main sources of uncertainty in the design will result in wrong decision-making and could potentially lead to choosing a design that is not optimum in practice.

Acknowledgment

The authors would like to thank Dr. Vladimir Blasko, Senior Fellow, Power Electronics, at United Technologies Research Center, for the generous support granted through a power electronics fellowship at Virginia Tech.

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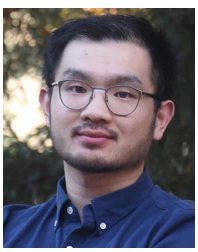

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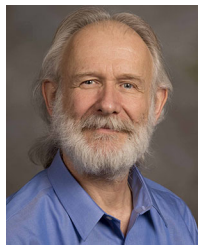

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