Letters

Modular Multilevel Converter (MMC) Modeling Considering Submodule Voltage Sensor Noise

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***Abstract*—The modular multilevel converter (MMC) is a popular topology in medium- and high-voltage applications, and many efforts have been spent on MMC modeling. However, the impact of submodule voltage sensor noise (SVSN), which becomes more severe due to increasing switching speed of power semiconductors and compact submodule design, has not been considered in conventional models. In this letter, the SVSN is introduced by coupling capacitances between the sensor and power stage in an MMC switching model. Furthermore, the SVSN impact is considered in an MMC average model based on derivation of the relationship between the SVSN and the duty cycle. The proposed MMC switching model and average model considering the SVSN are validated by comparing simulations with experimental results in an MMC prototype using 10-kV SiC MOSFETS.**

***Index Terms*—Average model, modular multilevel converter (MMC), submodule voltage sensor noise (SVSN), switching model.**

I. Introduction

THE modular multilevel converter (MMC) has been very popular and widely applied in medium-voltage and high-voltage applications [1]–[3], e.g., large motor drives and HVdc transmission grids. It can achieve high-voltage rating by using low-voltage submodules (SMs) in series connection, bringing many benefits compared to other power converters, such as easy scalability, high-voltage quality, less filter size, etc. [4].

Modeling and simulation are essential in the design and testing of the MMC. There are two major types of MMC models including the switching model [5], [6] and the average model [7]–[9]. In the switching model, the SM is described in detail with power semiconductors built in. Considering there is no simplification in the model, the switching model has a good accuracy and can also describe switching-related issues (e.g., electromagnetic interference). However, the penalty is the model complexity, resulting in a long simulation time [6]. In order to save computation resources and improve simulation speed, the average model [7]–[9] is proposed by neglecting switching details. The SM is described by controlled voltage and current sources with states calculated only once in each switching cycle. The average model has been validated in the MMC with a large number of SMs (e.g., hundreds of SMs [8]).

Novel power semiconductors with improved switching performance (e.g., fast switching wide bandgap devices) have been rapidly developed in recent years [10], [11]. Meanwhile, the compact SM design is attractive in order to increase the power density. However, noise issues become more severe because of stronger noise sources under higher *dv/dt* and *di/dt* and closer coupling due to the compact SM design [12]. This letter focuses on the impact of the submodule voltage sensor noise (SVSN) on the MMC modeling, which has not been considered in previous MMC models. Based on the study in this article, the SVSN can result in significant unbalanced SM voltage sharing and arm current harmonics. But this phenomenon cannot be described by conventional models without consideration of the SVSN. The MMC model considering the SVSN, which can describe the SM voltage unbalance and arm current harmonics, is proposed here.

The mathematical derivation of SVSN is presented in Section II. The improved switching model and average model considering SVSN are introduced in Section III. The simulation results with two improved models are compared to experimental results as validation in Section IV.

II. SVSN Impact Derivation

The MMC, which can achieve a high-voltage rating by using many SMs in series connection, is shown in Fig. 1. An SM voltage sensor is necessary for voltage balancing control.

The equivalent circuit of an SM voltage sensor based on Σ-Δ method [13] is given in Fig. 2. In this way, the average voltage can be obtained by counting pulses in a sampling period. The noise coupling can be modeled by parasitic capacitances C_{Hi} ($i = 1, 2, \ldots, N$) between PCB traces of the voltage divider and SM's midpoint (i.e., v_{PWM}). In a compact SM design, the voltage sensor is very close to the power stage, resulting in a

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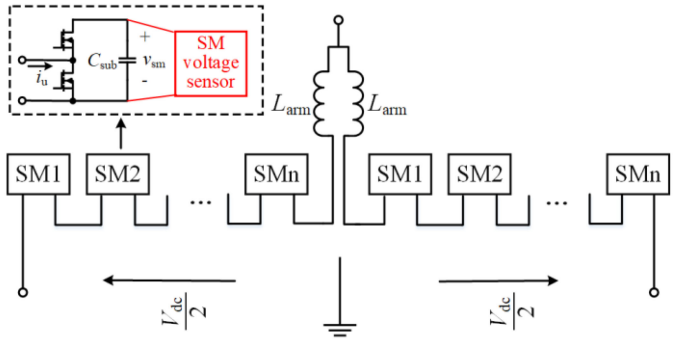

Fig. 1. MMC topology.

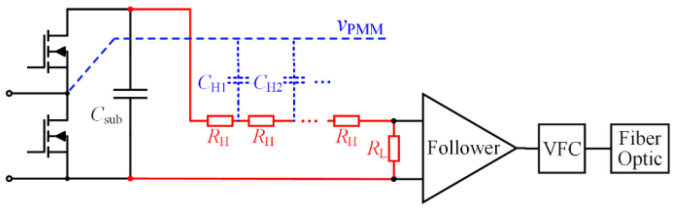

Fig. 2. Schematic of SM voltage sensor with SVSN.

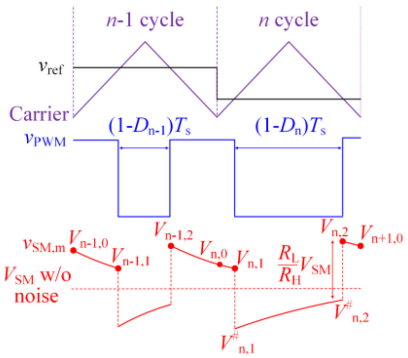

Fig. 3. Schematic of sampled noise waveforms.

0.1 $\sim$ 1 pF parasitic capacitance which cannot be neglected. Under high *dv/dt* environment, the SVSN is coupled through C_{Hi} and impacts the MMC operation. In an MMC switching model, the SVSN impact can be described by adding C_{Hi} in the equivalent circuit. However, it is not clear how to model the SVSN impact in an average model, which is more applicable in an MMC with a large number of SMs.

A simple case is used with only two resistors and one coupling capacitor (i.e., $N=1$) to derive the SVSN impact. The schematic SM sampling waveforms are shown in Fig. 3. Under high *dv/dt* environment, v_{PWM} can be seen as an ideal square waveform. V_{SM} is the real SM voltage without the sampling noise, while $v_{\mathrm{SM,m}}$ is the sampled SM voltage with the sampling noise. The noise can be divided into three sections in a cycle (i.e., section I from $V_{n,0}$ to $V_{n,1}$, section II from $V^{\#}_{n,1}$ to $V^{\#}_{n,2}$, and section III from $V_{n,2}$ to $V_{n+1,0}$). The sudden change from $V_{n,1}$ to $V^{\#}_{n,1}$ and from $V^{\#}_{n,2}$ to $V_{n,2}$ is induced by coupling of v_{PWM} through C_{H}, and the step is $R_{\mathrm{L}}V_{\mathrm{SM}}/R_{\mathrm{H}}$. In each section, the sampled noise can be seen as exponential. Using Section I (S1) as an example, the time-voltage integration of the noise can be described by

$$\int_{S1} v_{\mathrm{noise}}(t)\,dt = \int_{S1} V_{n,0}\exp\left(-\frac{t}{\tau}\right)dt = (V_{n,0}-V_{n,1})\,\tau \tag{1}$$

where τ is the time constant of the *RC* circuit shown in Fig. 2 and can be described by

$$\tau = \frac{R_H C_H}{2}. \tag{2}$$

Therefore, the sampled noise in a cycle can be represented as

$$\begin{aligned} v_{\mathrm{noise},n} &= \int_{(n-1)T_s}^{nT_s} v_{\mathrm{noise}}(t)dt/T_s = [(V_{n,0}-V_{n,1})\,\tau \\ &\quad + (V_{n,1}-V_{n,2})\,\tau + (V_{n,2}-V_{n+1,0})\,\tau]/T_s \\ &= (V_{n,0}-V_{n+1,0})\,\tau/T_s \end{aligned} \tag{3}$$

where $v_{\mathrm{noise},n}$ is the sampled noise in *n*th cycle and T_{s} is switching period. It can be seen that the noise is determined by $V_{n,0}$ and $V_{n+1,0}$, which are sampled SM voltages at initial and end points in a switching cycle. $V_{n,0}$ and $V_{n+1,0}$ can be represented as

$$V_{n+1,0} = aV_{n,0} + \frac{(1-a)\,R_L V_{SM}}{2R_H} + b(D_n)\,V_{SM} \tag{4}$$

where

$$\begin{aligned} a &= \exp(-T_s/\tau) \\ b(D_n) &= \{\exp(-D_n T_s/2\tau) \\ &\quad - \exp[-(2-D_n)\,T_s/2\tau]\}\,R_L/R_H \end{aligned} \tag{5}$$

where D_n is the duty cycle in *n*th cycle. Use linear approximation for (5) with Taylor's theorem in the case of a large τ compared to T_{s}, $b(D_n)$ can be represented as

$$b(D_n) = \frac{(1-D_n)\,T_s R_L}{\tau R_H}. \tag{6}$$

Considering a is smaller than 1, the third item in (4) (i.e., $b(D_n)$) plays a major role in $V_{n+1,0}$, and the first item can be ignored. $v_{\mathrm{noise},n}$ in (3) can be described by the variation of the duty cycle

$$v_{\mathrm{noise,n}} = \alpha\,(D_n - D_{n-1}) \tag{7}$$

where α is noise impact coefficient and can be represented as

$$\alpha = \frac{R_L V_{SM}}{R_H}. \tag{8}$$

It should be noted that with decreasing switching frequency, a and b are nearly zero considering T_{s} is much larger than τ. According to (3) and (4), the SVSN can be neglected because $V_{n+1,0}$ is equal to $V_{n,0}$. Therefore, (7) and (8) are only suitable in the case that T_{s} is close to τ. In some cases, a small filter capacitor will be placed in parallel with R_{L} in order to suppress high frequency interference (e.g., pF level capacitance with 100 kHz bandwidth). However, its suppression on the SVSN discussed here is limited considering the time constant of the SVSN in (2) could be even larger than the switching cycle (e.g., 100 μs). Even

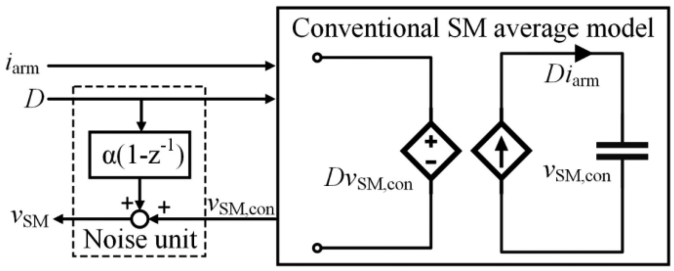

Fig. 4. MMC SM average model considering the SVSN.

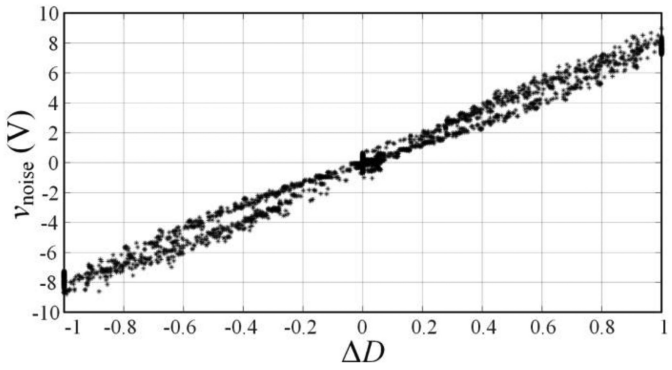

Fig. 5. Simulation results of sampled noise and change of duty cycle.

though with the filter capacitor, the SVSN can also be described using (7).

III. MMC Model Considering SVSN

In the MMC switching model, the SVSN can be introduced by adding $C_{\rm H}$ in the SM equivalent circuit. In the MMC average model, the SVSN can be considered, as shown in Fig. 4. Compared to conventional MMC models, a noise unit is integrated into the SM voltage sampling circuit (i.e., $v_{\rm SM}$ considering SVSN impact versus $v_{\rm SM,con}$ in conventional models shown in Fig. 4) based on the derivation in Section II. If the noise is low, α can be set to be 0, while under high noise environment, α is determined by (8). The way considering the SVSN in the SM Thevenin equivalent model [14], which is also widely applied in MMC simulations, is similar with the average model by adding the noise unit according to (7). Here, only the average model is selected as a representative.

The simulation results of duty cycle and sampled noise in an MMC switching model with nearest level PWM (NL-PWM) modulation are shown in Fig. 5. The voltage sensor parameters are given in Table I. $C_{\rm H}$, which is parasitic capacitance, is obtained using Ansys Q3D based on a practical SM prototype using 10-kV SiC MOSFETs. The simulation with the MMC switching model is done for 1 s. The simulated $v_{\rm noise}$ and the change of the duty cycle ΔD (i.e., $D_n - D_{n-1}$) for overall SMs are collected in an array and presented as a scatterplot in Fig. 5. Because $v_{\rm noise}$ is also slightly impacted by the duty cycle in previous switching cycles (i.e., $D_{n-2}\ldots$), there is minor difference on $v_{\rm noise}$ under same ΔD. However, the difference can be ignored, indicating that $v_{\rm noise}$ linearly changes with ΔD and can be described using (7).

TABLE I
Voltage Sensor Parameters

Parameter	Value	Parameter	Value
$R_{\rm L}/R_{\rm H}$	200 kΩ/100 MΩ	$C_{\rm H}$	1 pF
$T_{\rm s}$	100 μs	$V_{\rm SM}$	6.25 kV

TABLE II
Simulation Platform and Prototype Parameters

Parameter	Value	Parameter	Value
Dc link voltage	6 kV	SM number per arm	4
Rated SM voltage	1.5 kV	SM capacitance	8.75 μF
Arm inductance	90 mH	*RC* Load	2 kΩ/1.25 μF

IV. Model Validation

The simulation results of the improved MMC switching and average model considering the SVSN (i.e., $C_{\rm H}$ in the switching model and noise unit in the average model) are compared with experimental results, shown in Fig. 6. The simulation platforms are built in MATLAB Simulink. The prototype for experimental validation is developed using 10 kV/20 A SiC MOSFETs [15]. The simulation platforms and prototype have the same parameters (i.e., passives and control parameters) as given in Table II.

The SVSN-related parameters in the switching model is given in Table I, and α is set to be 3 in the average model. The FFT analysis of simulated arm current $i_{\rm arm}$ and SM voltage $v_{\rm SM}$ in both average and switching models with SVSN impact and without the impact (i.e., $C_{\rm H} = 0$ in the switching model and $\alpha = 0$ in the average model) are compared both in Fig. 6(a) and (b). It can be seen that the simulation results of the average model and the switching model are similar.

Compared to simulations without the SVSN, there is significant SM voltage unbalance and low-frequency $v_{\rm SM}$ disturbance (e.g., 400 V peak–peak SM voltage with the SVSN versus 220 V without the SVSN based on theoretical calculation [16], and $<$60 Hz components in FFT of $v_{\rm SM}$), and harmonics in $i_{\rm arm}$ (e.g., nearly 80% harmonics from 200 to 300 Hz in FFT of $i_{\rm arm}$). This phenomenon is also observed in the experimental results given in Fig. 6(c). The noise immunity improvement in the prototype is achieved by reducing the coupling capacitance $C_{\rm H}$ using some methods such as applying a shield layer in the voltage sensor circuit [17]. It can be concluded that both the improved switching and average models match the experimental results, and can be used to investigate the SVSN impact on the MMC design, e.g., arm inductor, SM capacitor, and thermal effects, due to increased SM voltage unbalance and arm current harmonics.

The simulation results of the proposed average model for an MMC with 32 SMs per arm for $\pm$100 kV HVdc application are shown in Fig. 7, including with and without the SVSN. The nearest level modulation is applied with 10 kHz switching frequency for the SM. Due to voltage balancing control, an SM needs to switch between inserted mode ($D = 1$) and bypassed mode ($D = 0$), resulting in the duty cycle change. Therefore, the SM voltage unbalance can still be observed with the SVSN (e.g., 410 V peak–peak SM voltage versus 170 V without the SVSN). The arm current harmonics are lower compared to less

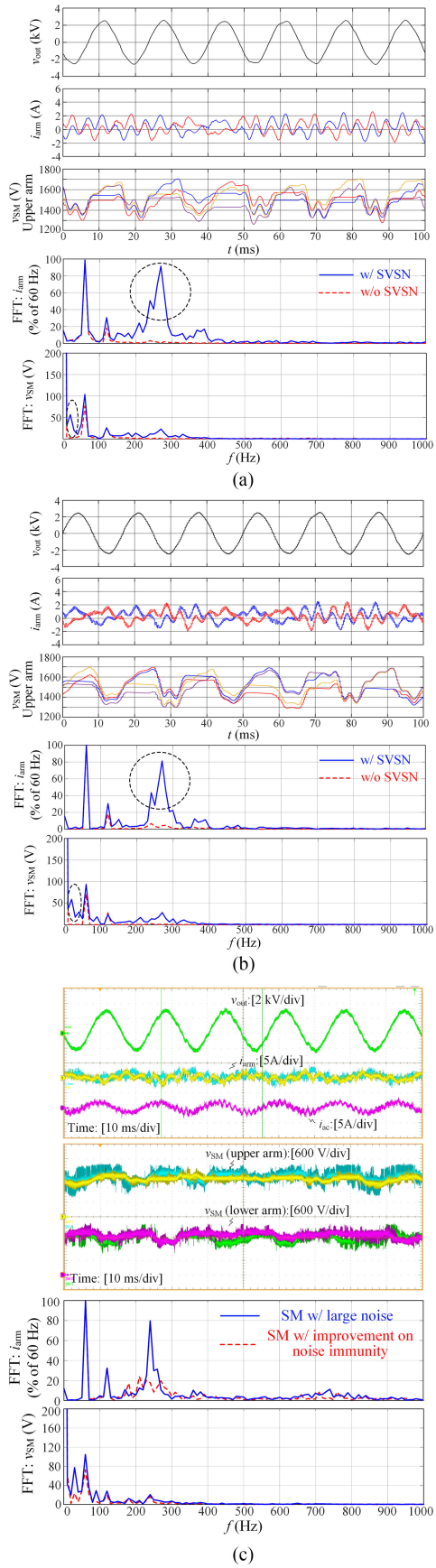

Fig. 6. Simulation and experimental results considering the SVSN. (a) Average model. (b) Switching model. (c) Experimental results.

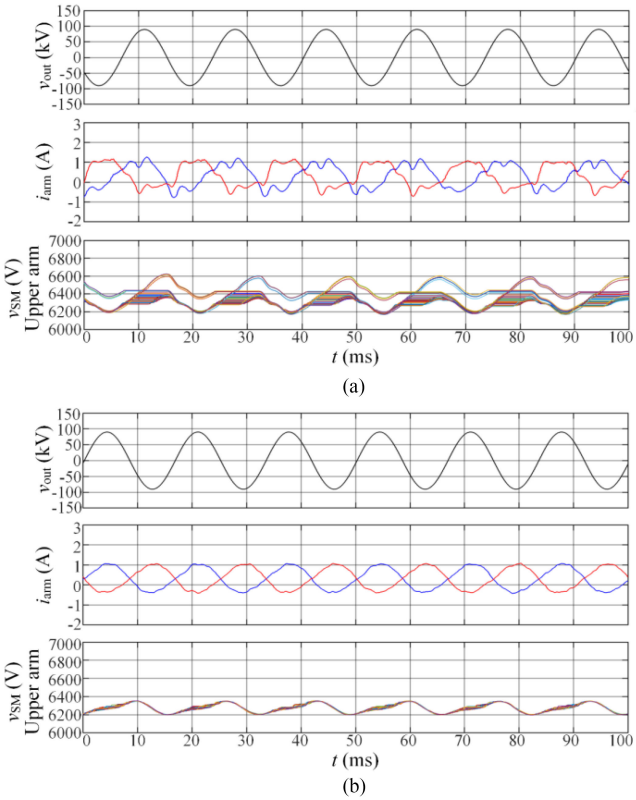

Fig. 7. Simulation results with the proposed average model for an MMC with 32 SMs per arm. (a) w/ SVSN. (b) w/o SVSN ($\alpha = 0$).

SMs (e.g., 25% with 32 SMs compared to 80% with 4 SMs). However, in practical HVdc systems, with high number of SMs, the switching frequency of the SM is strictly limited in order to save the power semiconductor loss (e.g., 100 Hz for high-voltage Si devices). In this case, the SVSN impact can be ignored, as discussed in Section II.

V. Conclusion

In the SM of MMC, the SVSN is coupled through parasitic capacitances between the voltage divider and SM's midpoint. The noise magnitude is determined by the change of the duty cycle. Both switching and average models are improved considering the SVSN by adding parasitic coupling capacitors in the switching model and a noise unit in the average model. The proposed switching model and average model match experimental results. The SM voltage unbalance and arm current harmonics can be described by the proposed models.

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