Integrated High- and Low-Frequency Current Ripple Suppressions in a Single-Phase Onboard Charger for EVs

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***Abstract*—Current ripples produced in single-phase onboard charging systems of electric vehicles (EVs) impact the lifetime of their batteries. In this article, an isolated multifunctional charger topology is proposed. The charging system can be used to charge the auxiliary batteries or serve as an active filter (AF) for the power battery charger. By time-sharing multiplexing it, the high-frequency (HF) and low-frequency (LF/second harmonic) current ripple can be suppressed in driving and parking charging modes, respectively. The proposed topology can also achieve zero voltage switching for all power switches under a full-load range in the driving charging mode. In addition, the integration and the power density of the charging system can be improved due to the reconstruction of the capacitive energy storage AF in the parking charging mode. Finally, a 400-W experimental prototype is developed and the experimental results are presented to validate the performance and feasibility of the proposed topology.**

***Index Terms*—Auxiliary battery, integrated high-frequency (HF) and low-frequency (LF) current ripple suppressions, isolated charger topology, onboard charging system, single-phase PWM rectifier charging.**

NOMENCLATURE

$u_{\rm s}$	Grid side input voltage.
$i_{\rm s}$	Grid side input current.
$i_{\rm out}$	Output current in driving charging mode.
$L_{\rm s}$	Grid side input filtering inductor.
$C_{\rm bus}$	DC side capacitor.
$U_{\rm low}$	Auxiliary battery voltage.
$U_{\rm high}$	Power battery voltage.
$L_1(L_2)$	DC input filtering inductor.
$i_{L1}(i_{L2})$	DC input filtering inductor current.
T	High-frequency transformer.
L_{ks}	External energy transmission inductor.
L_k	Sum of L_{ks} and L_{keq}.
i_{Lks}	External energy transmission inductor current.
$L_{\rm EST}$	Equivalent inductance of high-frequency transformer's high-voltage side winding.
C_i	Low-voltage side energy storage capacitor.
U_{Ci}	Low-voltage side energy storage capacitor voltage.
C_c	High-voltage side energy storage capacitor.
U_{Cc}	High-voltage side energy storage capacitor voltage.
i_{Cc}	High-voltage side energy storage capacitor current.
V_{h1}	Midpoint voltage of low-voltage side H-bridge.
V_{h2}	Primary side voltage of a high-frequency transformer.
N	Turns ratio of transformer.
T_{s1}	Half switching period of the proposed topology in driving charging mode.
D	Phase shift duty cycle.
f_s	Switching frequency of a single-phase rectifier.
f_{s1}	Switching frequency of the proposed topology in driving charging mode.
f_{s2}	Switching frequency of the proposed topology in parking charging mode.

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I. INTRODUCTION

FOLLOWING the trend of developing clean energy and achieving sustainable development [1], [2], electric vehicles (EVs) powered by renewable energies achieve clean and carbon-neutral operation and can help alleviate the pressure of energy shortage and environmental pollution [3]–[5]. As an important part of EVs, batteries are a key factor in their development, and the charging time and service life of batteries are closely related to charging technology [6].

In many charging technologies of EVs, onboard charging has become a research hotspot [7]–[9]. Fig. 1 shows the block diagram of onboard charging system for EVs. Among various charging technologies, the single-phase slow charging is widely adopted in household parking charging because it can protect the batteries effectively and prolong its lifetime [10]. In addition, there are two kinds of charging modes: parking and driving charging modes. The power batteries would be charged by grid in parking charging mode and the auxiliary batteries would be charged by power batteries in driving charging mode. Actually, there are many single-phase charging methods, among which single-phase PWM rectifier charging has attracted more

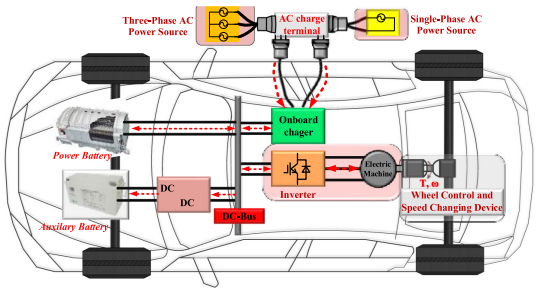

Fig. 1. Block diagram of onboard charging system for EVs.

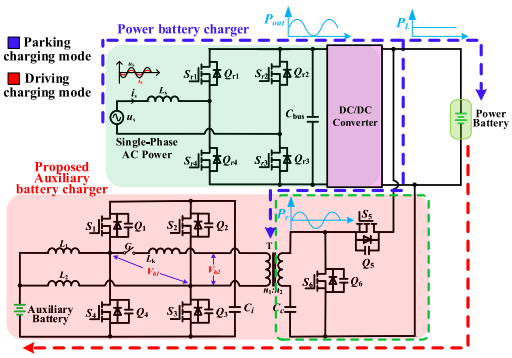

Fig. 2. Proposed topology of the charging system integrated with auxiliary and power batteries.

attention due to its controllability of charging voltage, current, and power factor, as well the requirement of vehicle to grid (V2G) application. However, a pulsating power at twice the frequency ($P_{\rm out}$ in Fig. 2) of the grid voltage is generated from the combined action of sinusoidal alternating current and grid voltage during single-phase PWM rectifier charging [11]. For EV charging systems, the second-harmonic pulsating current is potentially harmful to the batteries, as it can produce additional electrochemical overpotential at high state of charge, as well as causing overheat due to higher rms current, resulting in shorter battery life [12], [13]. Generally, the current ripple of battery should be less than 10% of its rated value [14]. Therefore, to suppress the second-harmonic ripple voltage on the dc side of single-phase PWM rectifier in the onboard charging system is of great importance, as well as the ripple of the charging current/voltage for batteries [15]–[17]. So far, there are two dominant methods to suppress the second-harmonic ripple voltage: passive filtering and active filtering.

To suppress the second-harmonic ripple voltage, there exist two dominant passive filtering methods: to install large dc capacitors or *LC* resonant circuits in parallel with the dc bus. Although both methods are simple and effective, they suffer from the drawbacks of unreliability and low power density. In order to overcome the abovementioned disadvantages, various active filtering methods have been proposed. Depending on the location, an active filter (AF) can be on the dc link or on the ac link [18]–[20]. A dc-link AF is usually connected to the dc bus by a bidirectional dc–dc converter, through which the pulsating power in the dc bus can be transferred to the energy storage elements to achieve "peak shaving and valley filling." Another categorization of an AF can be made based on whether the AF uses capacitive or inductive energy storage [21]–[23]. Compared with inductors, capacitors typically provide much higher energy storage density and hence are often favored by an AF when a separate energy component is needed [24]. However, these AFs require additional power switches and passive devices in the charging system, and the power density has been sacrificed.

In order to further improve the power density of onboard charging systems, some researchers have been working on suppressing the dc side second-harmonic ripple voltage via the existing hardware circuit in the single-phase onboard charging system of EVs with very few additional components or circuits (if necessary, the hardware circuit needs to be reconfigured through relays). In [25], a method with second-harmonic ripple voltage suppression based on the two-stage onboard charging system has been proposed, in which the ripple voltage can be suppressed to a certain extent with an additional rotating-frame-based control scheme, but the effect is overdependent on the wide bandgap power device and the corresponding efficiency is relatively low. In [26] and [27], capacitive storage AFs based on an auxiliary battery charging module have been proposed. Although these methods improve the power density to a certain extent, they both require additional passive energy storage devices and relays, and the integration is not high. Whereas, auxiliary power modular (APM)-based capacitive energy storage AFs have been proposed in [28] and [29], where the high-frequency (HF) transformer adopted in the converter is with central-tapped windings and the flux generated in the two split parts cancel each other out when AF operates. Therefore, it obviates the need of relays to cutoff the low-voltage side circuit. However, these methods still require additional passive energy storage devices, and the flux produced in the two split parts cannot be completely offset due to the slight asymmetry in the windings, which can cause additional losses in the low-voltage side circuit.

Obviously, the charging topology of the APM plays a key role in the abovementioned AF, but the HF charging current ripple which would affect the life-span of auxiliary battery has not been considered yet [30]. Therefore, an interleaved switched-capacitor dc–dc converter with low output current ripple has been proposed in [31]. However, there would be safety issues without isolation, and all power switches operate in hard switching so that the switching frequency is limited and suffer from low power density. To solve the problem, an isolated dc–dc converter has been proposed in [32]. Although it realizes electrical isolation, it can only reduce the HF output current ripple to a certain extent. In order to further reduce the HF current ripple, a dc–dc converter with interleaved modules has been proposed in [33], which can reduce the output current ripple on the low-voltage side effectively. However, the topology is complex and it involves current sharing issue among modules. In addition, the cost is high due to a quite large number of power devices.

To fill the gap, an isolated charging topology for an APM has been proposed in Fig. 2 to suppress the HF and LF charging current ripples of batteries by a time-sharing multiplexing technique. Moreover, all power switches can achieve zero voltage switching (ZVS) under a full-load range in driving charging mode, and the suppression of LF current ripple in parking charging mode can be realized by utilizing the high-voltage side hardware circuit of the topology without additional power switches and passive devices, which has the advantages of high integration and low cost.

The structure of this article is organized as follows. Section II introduces the proposed charging topology with HF and LF current ripple suppressions, and then analyzes its operating principle in two modes. The control strategies of the proposed topology operated in two modes are given in Section III. Section IV performs the characteristic analysis and parameter design of the converter. Experimental results are shown in Section V. Finally, Section VI draws the conclusion.

II. Operating Principle of the Proposed Topology With HF and LF Current Ripple Suppressions

As shown in Fig. 2, a proposed structure of the charging system integrated with auxiliary and power batteries can realize the suppression of both the HF current ripple in driving charging mode and the LF current ripple is produced in a single-phase PWM rectifier in parking charging mode by designing the auxiliary battery charger reasonably in a single-phase onboard charging system for EVs.

In Fig. 2, the high-voltage power battery charger consists of a single-phase rectifier and a dc–dc converter (the topology is same as the auxiliary battery charger). There are four power switches Q_{r1}–Q_{r4} and an filter inductor L_s in the rectifier, and $C_{\rm bus}$ is the dc bus capacitor. Then, the auxiliary battery charger consists of six power switches Q_1–Q_6, HF transformer T (turns ratio $N = n_1{:}n_2$), dc filter inductors L_1 and L_2, an external series inductor L_k, and energy storage capacitors C_i and C_c. As shown in Fig. 2, the auxiliary battery charger operates in two modes: parking and driving charging modes. Parking charging mode is that the power battery is charged by grid when the vehicle is statically parked while driving charging mode is that the auxiliary battery is charged by power battery when the vehicle is dynamically running. In order to suppress the LF current ripple caused by the single-phase PWM rectifier in parking charging mode, the high-voltage side hardware circuit of the auxiliary battery charger (see the dotted line frame in Fig. 2) is utilized and the low-voltage side circuit is cutoff by relay G to avoid producing circulating current when the AF is operated (circulation path: low-voltage side winding of the HF transformer—the external series inductance L_k—dc filter inductance L_1—dc filter inductance L_2—low-voltage side winding of HF transformer), which can reduce the additional losses of the charging system.

A. HF Current Ripple Suppression for Auxiliary Battery in Driving Charging Mode

In order to suppress the HF charging current ripple for the auxiliary battery, a low-voltage ($U_{\rm low}$) side topology with two-phase interleaving based on the basic buck–boost converter has been deduced in this article. Hence, zero output current ripple can be achieved theoretically by shifting the phase 180 ° between the basic units, and the derived H-bridge can also operate in HF rectification. Similarly, the high-voltage ($U_{\rm high}$) side (dc link) topology can be derived by the basic buck–boost converter and the HF inverter can be obtained by the combination of power switches and energy storage capacitor C_c. Thus, the isolated charging converter can be synthetized by the two basic units mentioned above and HF transformer, and the equivalent circuit is shown in Fig. 3.

To simplify the analysis, all components are assumed to be ideal; for example, by neglecting the ON-state resistance $R_{\rm DS}({\rm on})$ of the power switches and equivalent series resistance

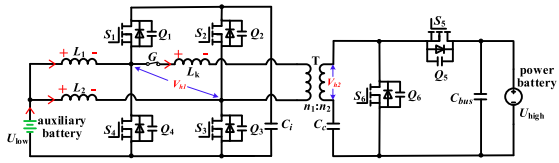

Fig. 3. Equivalent circuit of the proposed topology.

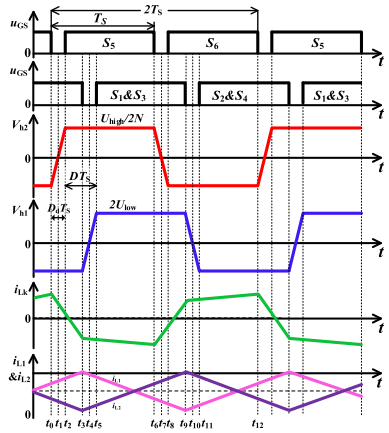

Fig. 4. Typical waveforms of the proposed topology in driving charging mode.

of the inductors and capacitors. In addition, the current and voltage of inductors and capacitors are assumed to behave linearly. The reference directions of the current and voltage are shown in Fig. 3. Finally, the voltage matching ratio $k = U_{\rm high}/(4NU_{\rm low}) > 1$.

The duty cycles of gate signals S_1–S_6 of power swiches Q_1–Q_6 are fixed at 0.5. The gate signal S_6 (S_3, S_4) is 180° shifted on the basis of S_5 (S_2, S_1), and S_5 is leading S_1 by a certain angle. The magnitude and direction of the power transferred by the converter are determined by the phase shift angle (corresponding phase shift ratio is D). It can be seen from Fig. 4 that there are six operating states for the converter during half switching period (T_s) when the auxiliary battery is charged by the power battery. The corresponding current-flow paths are illustrated in Fig. 5 and can be described as follows.

State 1 [t_0–t_1]: Switch Q_6 is turned ON before t_0, and the currents passing through primary winding of transformer and equivalent leakage inductor are positive. Fig. 5(a) shows the current-flow paths. At t_0, the power switch Q_6 is turned OFF and its parasitic capacitor is charged. Meanwhile, the parasitic capacitor of power switch Q_5 is discharged. Then, the power switches Q_2 and Q_4 are turned ON, and the energy storage capacitor C_i on the low-voltage side is discharged. At t_1, the parasitic capacitor of power switch Q_6 is fully charged.

State 2 [t_1–t_2]: The power switch Q_6 is turned OFF at t_1, and the current flowing through the equivalent leakage inductor remains positive. As shown in Fig. 5(b), the current is passing through the antiparallel diode of Q_5 according to Kirchhoff's current law (KCL). Meanwhile, Q_2 and Q_4 are still ON and the capacitor C_i is still discharging.

State 3 [t_2–t_3]: The power switch Q_5 is turned ON at t_2, and the current paths are shown in Fig. 5(c). During this interval, the capacitor C_i is still discharging, but the current through

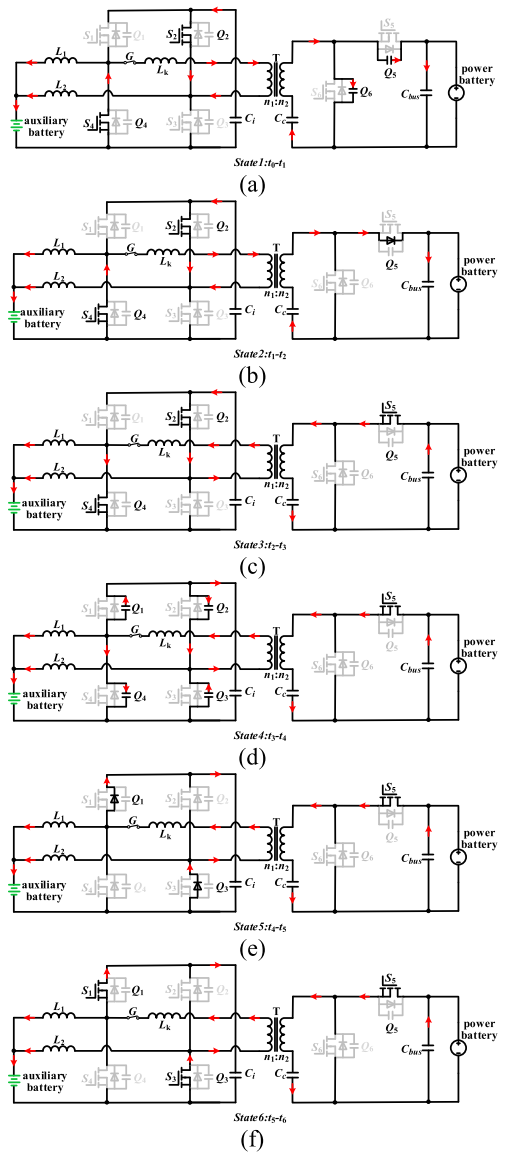

Fig. 5. Current-flow paths of the proposed topology in driving charging mode. (a) State 1: [t_0–t_1]. (b) State 2: [t_1–t_2]. (c) State 3: [t_2–t_3]. (d) State 4: [t_3–t_4]. (e) State 5: [t_4–t_5]. (f) State 6: [t_5–t_6].

leakage inductance is changed from positive to negative. That is, the state of energy storage capacitor C_c on the high-voltage side is changed from releasing to storing energy. Then, Q_2 and Q_4 are turned OFF at t_3.

State 4 [t_3–t_4]: The power switches Q_2 and Q_4 are turned OFF at t_3, and the current path through equivalent leakage inductance is negative. The capacitors C_c and C_i are charging during this time. Meanwhile, the parasitic capacitors of Q_2 and Q_4 are charged by the current passing through primary winding of transformer and that of Q_1 and Q_3 are discharged. The current is flowing through the antiparallel diode of Q_5 according to KCL. Meanwhile, Q_2 and Q_4 are still ON and the capacitor C_i is still discharging. The current-flow paths are shown in Fig. 5(d).

State 5 [t_4–t_5]: At t_4, the parasitic capacitor of Q_2 and Q_4 are fully charged, and that of Q_1 and Q_3 are discharged absolutely. Then, the current passes through the antiparallel diodes of Q_1 and Q_3 for the ZVS turning ON. The current-flow paths are shown in Fig. 5(e).

State 6 [t_5–t_6]: During this interval, the power switches Q_1 and Q_3 are ZVS turned ON at t_5, and the capacitor C_i is charging. Meanwhile, the energy is transferred from the primary winding of the transformer to the capacitor C_i and auxiliary battery. The current-flow paths are shown in Fig. 5(f). The power switch Q_1 is turned OFF at t_6.

The operating principle of the converter during the other half switching period is repetitive and thus it will not be illustrated here.

Assuming that $t_0 = 0$, $t_3 = DT_S$, $t_6 = T_S$, and, if the effect of dead time is neglected, i.e., $D_d = 0$, then the following equation can be obtained:

$$\begin{cases} i_{Lk}(t) = i_{Lk}(t_0) + \frac{V_{h1}-V_{h2}}{L_k} \cdot t \\ \qquad = i_{Lk}(t_0) - \frac{4NU_{\text{low}}+U_{\text{high}}}{2NL_k} \cdot t,\ t_0 < t \le t_3 \\ i_{Lk}(t) = i_{Lk}(t_3) + \frac{V_{h1}-V_{h2}}{L_k} \cdot t \\ \qquad = i_{Lk}(t_3) + \frac{4NU_{\text{low}}-U_{\text{high}}}{2NL_k} \cdot t,\ t_3 < t \le t_6. \end{cases} \tag{1}$$

The current of each node can be obtained as

$$\begin{cases} i_{Lk}(t_3) = i_{Lk}(t_0) - \frac{2U_{\text{low}}(1+k)}{L_k} \cdot DT_S \\ i_{Lk}(t_6) = i_{Lk}(t_3) + \frac{2U_{\text{low}}(1-k)}{L_k} \cdot (1-D)T_S. \end{cases} \tag{2}$$

It can be seen from Fig. 4 that the converter operates symmetrically during one switching period, so it can be obtained as

$$\begin{cases} i_{Lk}(t_0) = \frac{U_{\text{low}}(k+2D-1)}{2f_sL_k} \\ i_{Lk}(t_3) = \frac{U_{\text{low}}[k(1-2D)-1]}{2f_sL_k} \\ i_{Lk}(t_6) = -\frac{U_{\text{low}}(k+2D-1)}{2f_sL_k}. \end{cases} \tag{3}$$

So, the transmitted power can be derived as

$$\begin{aligned} P &= \frac{1}{T_S}\int_0^{T_S} V_{h2} \cdot [-i_{Lk}(t)]dt \\ &= \frac{kU_{\text{high}}U_{\text{low}}}{2Nf_sL_k}D(1-D), \quad 0 < D < 1. \end{aligned} \tag{4}$$

In addition, since the duty cycles of buck–boost converter's gate signals are fixed at 0.5, the average voltage of energy storage capacitor C_i is

$$U_{Ci} = 2U_{\text{low}}. \tag{5}$$

The voltage across L_1 is U_{low} and that of L_2 is U_{low}–U_{Cc} during the interval [t_0–t_3]; while during [t_3–t_6], the voltage across L_1 is U_{low}–U_{Cc} and that of L_2 is U_{low}. Given the assumption that $L_1 = L_2 = L$, then the following equation can be obtained:

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \frac{U_{\text{low}}}{L} \cdot t, & t_0 \le t \le t_3 \\ i_{L1}(t) = i_{L1}(t_3) - \frac{U_{\text{low}}}{L} \cdot t, & t_3 \le t \le t_6 \end{cases} \tag{6}$$

$$\begin{cases} i_{L2}(t) = i_{L2}(t_0) - \frac{U_{\text{low}}}{L} \cdot t, & t_0 \le t \le t_3 \\ i_{L2}(t) = i_{L2}(t_3) + \frac{U_{\text{low}}}{L} \cdot t, & t_3 \le t \le t_6 \end{cases} \tag{7}$$

where $i_{L1}(t)$ and $i_{L2}(t)$ are the instantaneous currents of the dc filter inductors L_1 and L_2, respectively. Assuming that the initial currents $i_{L1}(t_0)$ and $i_{L2}(t_0)$ are I_1 and I_2 respectively, according

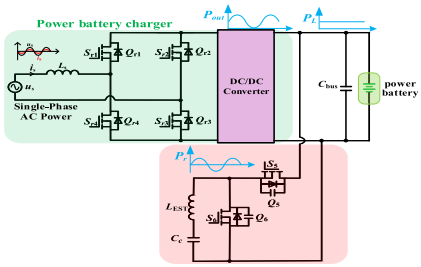

Fig. 6. Equivalen circuit of the proposed AF.

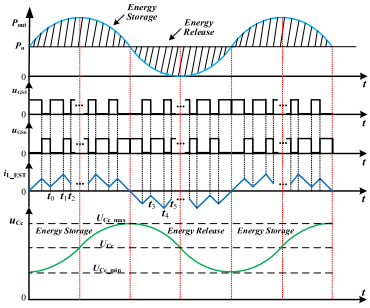

Fig. 7. Typical waveforms of the proposed AF.

to KCL, the charging current i_{out} is

$$\begin{aligned} i_{\text{out}} &= i_{L1}(t) + i_{L2}(t) \\ &= I_1 + I_2, \quad t_0 \le t \le t_6. \end{aligned} \tag{8}$$

It can be seen from (8) that the charging current is constant. Thus, the HF ripple of the charging current is zero theoretically if the inductance of L_1 and L_2 are identical. That is, the proposed topology can suppress the HF charging current ripple for auxiliary battery effectively.

B. LF Current Ripple Suppression for Power Battery in Parking Charging Mode

In order to provide controllable charging voltage and current for high-voltage battery and assure controllable power factor and bidirectional power flow, single-phase PWM converters have been widely applied. Assuming a unity power factor and input ac current is not distorted, the sinusoidal input ac voltage u_s and ac current i_s can be obtained as

$$\begin{cases} u_s(t) = V_S \cdot \sin(\omega t) \\ i_s(t) = I_S \cdot \sin(\omega t) \end{cases} \tag{9}$$

where V_S and I_S are the magnitudes of grid voltage and input current, respectively, and ω is the angular frequency.

Considering the instantaneous power of the input filter inductor L_s, the pulsating power can be obtained as

$$\begin{aligned} p_r(t) &= -\frac{V_S I_S}{2}\cos(2\omega t) - \frac{\omega L I_S^2}{2}\sin(2\omega t) \\ &= -p_{r\_\text{peak}}\sin(2\omega t + \psi). \end{aligned} \tag{10}$$

In (10), the amplitude p_{r_peak} of the second-harmonic pulsating power with its phase angle ψ can be obtained as

$$\begin{cases} p_{r\_\text{peak}} = \sqrt{V_S^2 I_S^2 + \omega^2 L^2 I_S^4}/2 \\ \psi = \tan^{-1}(V_S/\omega L I_S). \end{cases} \tag{11}$$

The pulsating power, which is unfriendly to the batteries, would be produced in the dc link of the single-phase PWM rectifier charging according to the abovementioned quantitative analysis. To tackle this, an AF is proposed and the equivalent circuit is shown in Fig. 6, where L_{EST} is the equivalent inductance of transformer's high-voltage side winding. In addition, there are no additional power switches and passive devices of the proposed method to suppress the LF current ripple.

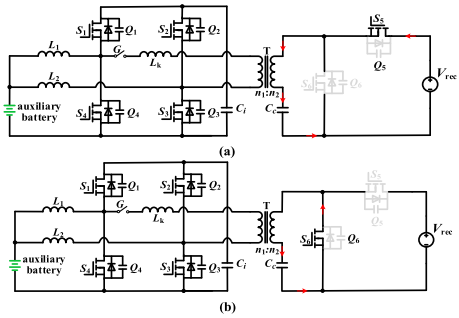

Fig. 8. Current-flow paths in buck mode. (a) State1 [t_0–t_1]. (b) State2 [t_1–t_2].

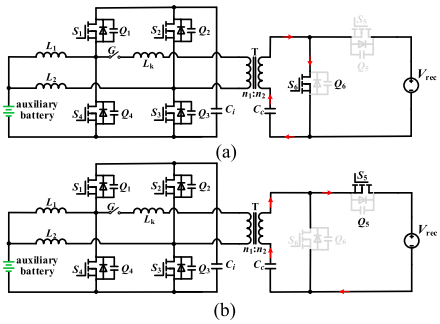

Fig. 9. Current-flow paths in boost mode. (a) State 1 [t_3–t_4]. (b) State 2 [t_4–t_5].

Generally, the auxiliary battery charger (proposed topology) is in standby mode during parking charging. Therefore, a capacitive energy storage AF can be constructed by the high-voltage side circuit of the isolated charger in APM, where the high-voltage side winding of transformer is utilized as energy transmittion and the capacitor C_c is used as energy storage. Fig. 7 shows the typical waveforms of the proposed AF.

It can be seen from Fig. 7 that the high-voltage side bidirectional converter used as AF would operate in buck and boost mode to achieve the charging and discharging for the energy storage capacitor. The current-flow paths in buck and boost mode of the converter are shown in Figs. 8 and 9 respectively, where V_{rec} is the output voltage of the single-phase PWM rectifier and the relay G is turned OFF.

1) Buck Mode (Energy Storage). State 1 [t_0–t_1]: The power switch Q_5 is turned ON at $t = t_0$, and Fig. 8(a) shows the current-flow path. The instantaneous output power of the single-phase PWM rectifier is larger than its average output power during this

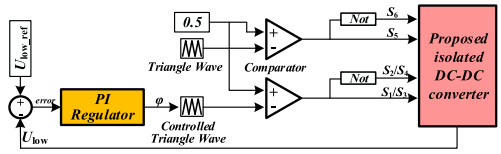

Fig. 10. Control block diagram of the proposed topology in driving charging mode.

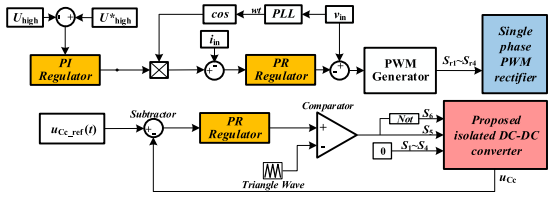

Fig. 11. Control block diagram of the proposed topology in parking charging mode.

interval. The excess part of the pulsating power is transferred to the high-voltage side winding of the transformer through Q_5.

State 2 [t_1–t_2]: As shown in Fig. 8(b), the power switch Q_5 is turned OFF and Q_6 is turned ON at $t = t_1$, and the energy stored in high-voltage side winding of the transformer is transferred to the capacitor C_c, that is, the capacitor C_c is charging during this time.

The converter operated in buck mode would realize "peak shaving" for pulsating power during this period, and the redundant energy would be stored in capacitor C_c temporarily.

2) Boost Mode (Energy Release). State 1 [t_3–t_4]: The power switch Q_6 is turned ON at $t = t_3$, and the instantaneous output power of the single-phase PWM rectifier is less than its average output power during this interval. The energy stored in capacitor C_c is transferred to the high-voltage side winding of the HF transformer through the power switch Q_6. Therefore, the current passing through the high-voltage side winding is increasing reversely, and the current-flow path of the topology is shown in Fig. 9(a).

State 2 [t_4–t_5]: Fig. 9(b) shows the current-flow path in this interval. The power switch Q_6 is turned OFF and Q_5 is turned ON at t_4. The energy stored in high-voltage side winding of the transformer and capacitor C_c are transferred to the dc bus, that is, the capacitor C_c is discharged at this time.

The converter operated in boost mode would achieve "valley filling" for pulsating power during this period, and the energy stored in the capacitor was transferred to the dc bus to compensate its power shortage.

To sum up, the second harmonic current ripple can be suppressed with the "peak shaving and valley filling" for the pulsating power in dc link by charging and discharging the capacitor C_c.

III. Control Strategies

A. Driving Charging Mode

When the duty cycle of gate signals of all power switches are 0.5, the transmission power of the converter is only determined by the phase shift raio *D*. Fig. 10 shows the control block diagram and the output voltage can be adjusted by a proportional integral (PI) regulator of whose output is phase shift angle φ. Thus, the voltage closed-loop control can be realized by adjusting the angle.

B. Parking Charging Mode

It can be assumed that the capacitor C_c can absorb/release the pulsating energy absolutely when the pulsating power $p_r(t)$ is determined, then the reference voltage $u_{Cc\_ref}(t)$ of the capacitor can be derived consequently. Therefore, the second-harmonic ripple voltage can be reduced dramatically when the real voltage across the capacitor is equal to the reference. Among them, the pulsating power can be transferred by the equivalent inductance $L_{\rm EST}$ of the transformer's high-voltage side winding, and the instantaneous power $p_{L\_\rm EST}(t)$ produced in the inductance accounts for a small proportion of the pulsating power, so the inductor and other parasitic losses can be ignored.

The instantaneous power transfer from dc bus to capacitor C_c can be obtained as

$$p_r(t) = u_{Cc}(t) \cdot i_{Cc}(t) = C_c \cdot \frac{du_{Cc}(t)}{dt} \cdot i_{Cc}(t) \tag{12}$$

where $u_{Cc}(t)$ and $i_{Cc}(t)$ are the instantaneous voltage and current of capacitor C_c, respectively. According to (10) and (12), the reference voltage across the capacitor C_c can be derived as

$$u_{Cc\_\rm ref}(t) = \sqrt{\frac{1}{\omega C_{Cc}} P_{r\_\rm peak} \left[K - \cos\left(2\omega t + \psi\right)\right]} \tag{13}$$

where *K* is a constant in the integration calculation, whose physical meaning is related to the peak value of the capacitor voltage $U_{Cc\_\max}$

$$K = \frac{\omega C_c U_{Cc\_\max}^2}{p_{r\_\rm peak}} + \cos\psi - 1. \tag{14}$$

The energy stored in the capacitor at each time can be written as

$$\begin{cases} \frac{1}{2} C_c U_{Cc\_\max}^2 - \frac{1}{2} C_c U_{Cc\_\min}^2 = W_{Cc} \\ W_{Cc} = \frac{p_{r\_\rm peak}}{\omega} \end{cases} \tag{15}$$

where $U_{Cc\_\min}$ is the minimum value of the capacitor voltage that satisfies $U_{Cc\_\max} > U_{Cc\_\min} \geq 0$, and W_{Cc} is the stored energy of the capacitor. Therefore, the maximum value of the capacitor voltage can be derived as

$$U_{Cc\_\max} = \sqrt{\frac{2p_{r\_\rm peak}}{\omega C_c} + U_{Cc\_\min}^2}. \tag{16}$$

The peak value of the capacitor voltage can reach its minimum value when $U_{Cc\_\min}$ is equal to 0, and at this point $K = 1 + \cos\psi$. Thus, the range of *K* can be obtained as

$$K \geq 1 + \cos\psi. \tag{17}$$

According to the theoretical analysis above, Fig. 11 shows the control block diagram. It can be seen that the control strategy in the single-phase PWM rectifier adopts an internal current loop based on a proportional-resonant (PR) regulator and an external voltage loop based on a PI regulator, and the PR regulator has a better performance than that of a PI regulator in tracking an alternating value. Similarly, the control strategy in AF adopts a single voltage loop based on a PR regulator.

IV. Characteristic Analysis and Parameters Design

A. Driving Charging Mode

1) Capacitor C_c: For capacitor C_c, the ripple voltage can be controlled within 5% of its rated value, namely $\Delta U_{Cc} \leq 5\% \cdot U_{\text{high}}$, then

$$C_c \geq \frac{10U_{\text{low}}[k+(2D-1)]}{Nf_s^2 L_k U_{\text{high}}}. \tag{18}$$

2) External Series Inductor L_{ks}: It can be seen that the sum of equivalent leakage inductance and external series inductance L_k is related to the transmission power of the converter according to previous analysis, that is

$$P_b = \frac{U_{\text{high}}U_{\text{low}}}{8Nf_s L_k} \tag{19}$$

where P_b is the basic value of transmittion power, and the value of external series inductor L_{ks} can be decided by the base power, switching frequency, and input and output voltage of the converter as

$$L_{ks} < L_k = \frac{U_{\text{high}}U_{\text{low}}}{8Nf_s P_b}. \tag{20}$$

3) DC Filter Inductor L_1 (L_2) Design and Soft-Switching Analysis: Before analyzing the constraints of the design of output dc filter inductance, the soft switching range of the power switches of the proposed topology should be analyzed.

Obviously, the relationship between the currents passing through inductor L_1 (L_2) at t_0 and t_6 is

$$i_{L1}(t_0) + i_{L1}(t_6) = -\frac{P_o}{U_{\text{low}}}. \tag{21}$$

According to (6) and (21)

$$\begin{cases} i_{L1}(t_0) = \frac{U_{\text{low}}}{2L}(1-2D)T_S - \frac{P_o}{2U_{\text{low}}} \\ i_{L1}(t_3) = \frac{U_{\text{low}}}{2L}T_S - \frac{P_o}{2U_{\text{low}}} \\ i_{L1}(t_6) = \frac{U_{\text{low}}}{2L}(2D-1)T_S - \frac{P_o}{2U_{\text{low}}} \end{cases} \tag{22}$$

where L is the value of inductors L_1 and L_2, and the constrains with soft switching of power switches Q_1 and Q_3 can be obtained as

$$\begin{cases} i_{L1}(t_3) = \frac{U_{\text{low}}}{2L}T_S - \frac{P_o}{2U_{\text{low}}} = \frac{U_{\text{low}}}{4f_s L} - \frac{kU_{\text{high}}D(1-D)}{4Nf_s L_k} \\ i_{Lk}(t_3) = \frac{U_{\text{low}}[k(1-2D)-1]}{2f_s L_k} \\ i_{L1}(t_3) - i_{Lk}(t_3) > 0. \end{cases} \tag{23}$$

Then, the constraint condition is

$$L < \frac{L_k}{k^2-1}, \quad k > 1. \tag{24}$$

Thus, soft switching can be achieved theoretically for low-votage side power switches in full-load range when (24) is satisfied.

For power switch Q_5, the initial inductor current should satisfy

$$\begin{cases} i_{Lk}(t_0) = \frac{U_{\text{low}}(k-1+2D)}{2f_s L_k} \\ i_{Lk}(t_0) > 0. \end{cases} \tag{25}$$

Actually, (25) can be always satisfied due to $k > 1$ and $D > 0$. Thus, the ZVS for power switch Q_5 can be achieved in full-load range. Similarly, the power switches Q_2, Q_4, and Q_6 can also achieve ZVS in full-load range during the other half period. Fig. 12 shows the range of soft switching and it can be seen that all power switches can achieve ZVS in full-load range when $k > 1$.

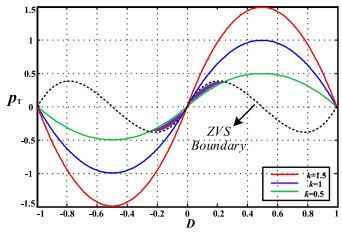

Fig. 12. ZVS region across the full operation range.

Therefore, it should be satisfied for dc filter inductance in (24). Then, in order to ensure that $k > 1$, turns ratio N can be designed as

$$N = \frac{U_{\text{high\_min}}}{4U_{\text{low\_max}}} \tag{26}$$

where $U_{\text{high\_min}}$ is the discharging cutoff voltage of power battery and $U_{\text{low\_max}}$ is the charging cutoff voltage of an auxiliary battery. Therefore, $k > 1$ is always satisfied when the input and output voltages change.

B. Parking Charging Mode

On the premise of meeting the requirements of ripple voltage of dc bus and switching harmonic of power switches caused by switching, it is necessary to improve the resonance frequency of $L_{\text{EST}}C_c$ on the high-voltage side of the auxiliary battery charger, which can eliminate the effects caused by the equivalent inductor L_{EST}. Meanwhile, the resonance frequency should be 1/10–1/5 of the switching frequency to aviod resonance between switching hamonic and the circuit with $L_{\text{EST}}C_c$.

Applying the principle of conservation of energy and the integral of (12), the energy $E_{Cc}(t)$ stored in capacitor C_c can be obtained as

$$\begin{aligned} E_{Cc}(t) &= \int P_{r\_\text{peak}} \sin(2\omega t + \psi)\, dt \\ &= \int C_c \frac{du_{Cc}(t)}{dt} u_{Cc}(t) dt = \int C_c u_{Cc}(t) du_{Cc}(t). \end{aligned} \tag{27}$$

Then, the capacitance of C_c can be obtained according to the following equation:

$$\begin{aligned} C_c &= \frac{P_{r\_\text{peak}}[K - \cos(2\omega t + \psi)]}{\omega u_{Cc}^2} \\ &\geq \frac{(K - \cos(2\omega t + \psi))P_{r\_\text{peak}}}{\omega U_{Cc\_\max}^2} \geq \frac{2P_{r\_\text{peak}}}{\omega U_{Cc\_\max}^2} \end{aligned} \tag{28}$$

where $U_{Cc\_\max}$ is the peak value of voltage across the capacitor C_c. Meanwhile, in order to ensure that the resonance frequency satisfies the requirement metioned above, the equivalent inductance can be obtained as

$$L_{\text{EST}} \geq \frac{1}{(2\pi f_{SC})^2 C_c}. \tag{29}$$

TABLE I
CHARACTERISTIC COMPARISON OF THE PROPOSED CONVERTER WITH THE COUNTERPARTS

Modular	method	Number of power switch	Number of diode	Number of inductor	Number of capacitor	Number of relay	Current stress in rectifier	Efficiency (%)
Low frequency current ripple suppression	[21]	1	1	1	0	0	high	-
	[22]	0	0	1	2	0	high	90.0-93.8
	[23]	2	0	1	1	0	normal	-
	[26]	0	0	1	1	1	normal	-
	[28]	0	0	1	1	0	normal	-
	proposed	0	0	0	0	1	normal	90.4-94.4
High frequency current ripple suppression	method	Number of power switch	Number of inductor	Number of capacitor	Current ripple rate(%)	Isolated converter	Full load ZVS rage	Efficiency (%)
	[31]	5	2	3	17.86	No	No	92.6-95.3
	[32]	6	1	4	200	Yes	No	87.4-91.8
	[33]	8	1	2	1.3	Yes	No	92.3-93.0
	proposed	6	2	3	0.9	Yes	Yes	87.6-95.2

On the other hand, in order to ensure that the converter operates in CCM mode, the equivalent inductance can also be obtained as

$$L_{\mathrm{EST}} \geq \frac{(u_{C\mathrm{Bus}}u_{Cc} - u_{Cc}^2)}{2u_{C\mathrm{Bus}}f_{s2}\bar{i}_{Cc}} \tag{30}$$

where $\bar{i}_{Cc}$ is the average current of capacitor during one switching period and f_{s2} is the switching frequency of the proposed topology.

C. Parameter Characterization

Obviously, the capacitance of C_c and the inductance of transformer's high-voltage side winding should be considered comprehensively. Taking both driving and parking charging modes into consideration, the capacitance of C_c can be finally obtained as

$$C_c \geq \mathrm{MAX}\left\{\frac{10U_{\mathrm{low}}[k+(2D-1)]}{Nf_s^2L_kU_{\mathrm{high}}}, \frac{2P_{r\_\mathrm{peak}}}{\omega U_{Cc\_\max}^2}\right\}. \tag{31}$$

Similarly, the inductance of transformer's high-voltage side winding should satisfy

$$L_{\mathrm{EST}} \geq \mathrm{MAX}\left\{\frac{1}{(2\pi f_{S2})^2C_c}, \frac{(u_{C\mathrm{Bus}}u_{Cc} - u_{Cc}^2)}{2u_{C\mathrm{Bus}}f_{s2}\bar{i}_{Cc}}\right\}. \tag{32}$$

D. Comparison Analysis of the Proposed Converter

The characteristic comparison of the proposed converter with the counterparts is shown in Table I. On the one hand, in order to suppress the LF current ripple in the single-phase PWM rectifier, an AF with capacitive energy storage has been proposed in [23], it not only required one inductor and capacitor, respectively, but also needed two power switches. So, the power density and integration are too low. To solve its problem, the ripple power-decoupling circuit shares one bridge arm with the H-bridge circuit has been proposed in [21], in which one IGBT, one diode, and an energy storage inductor were required and the power density and integration would be increased to some extent. However, the current stresses of power switches in the rectifier were relatively high. Similarly, an AF with capacitive energy storage has been proposed in [22], where one inductor and two capacitors were needed only without additional power switches. However, the current stresses of power switches in the rectifier were still relatively high and the system efficiency was relatively low. In order to achieve higher power density and integration of the charging system, an active filtering method by time-sharing multiplexing APM has been proposed in [26] and [28]. In [26], it required one inductor, one capacitor, and one relay to suppress the LF current ripple with the primary circuit of APM. In [28], it can achieve current ripple suppression without the aid of relay, and it just needed one capacitor and a three-winding transformer. Although the relay was avoided to applying, the current would flow into the secondary circuit of the APM with the slight asymmetry in the transformer windings and cause additional losses. On the other hand, in order to suppress HF current ripple, a dc–dc converter with low output current ripple has been proposed in [31]. However, there would be safety issues without isolation, and all power switches operate in hard switching so that the switching frequency is limited and suffer from low power density. To solve the problem, an isolated dc–dc converter has been proposed in [32]. Although it realizes electrical isolation, it can only reduce the HF output current ripple to a certain extent. In order to further reduce the HF current ripple, a dc–dc converter with interleaved modules has been proposed in [33], which can reduce the output current ripple on the low-voltage side effectively. However, the topology is complex and it involves current sharing issue among modules. In addition, the cost is high due to a quite large number of power devices. It can be seen that the proposed topology can achieve HF and LF current ripple suppressions without additional power switches and passive devices, which has the advantages of high integration and low cost.

V. EXPERIMENTAL AND SIMULATION RESULTS

In order to validate the effectiveness of the proposed charging topology, a scaled-down experimental prototype was developed. Based on the single-phase charging experimental platform with the proposed topology, a 400-W prototype with 36–48 V output voltage and 200 V dc bus voltage was developed, as shown in Fig. 13. The specific parameters of the experimental prototype are listed in Table II. Texas Instruments microcontroller TMS320F28335 (DSP) and ALTERA microcontroller EP4CE622C8N (FPGA) are used to implement the current and

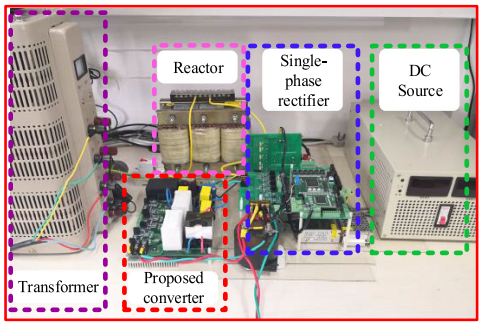

Fig. 13. Experimental prototype.

TABLE II
EXPERIMENTAL PARAMETERS OF INTEGRATED CHARGING SYSTEM

Modular	*Parameter*	*Values*
Single-Phase PWM Rectifier	Amplitude of grid voltage: U_S	141 V
	Angular frequency of grid: ω	100π rad/s
	DC bus voltage: U_{bus}	200 V
	Filtering capacitor in DC-link: C	200 μF
	Filtering inductor in AC-link: L_S	10 mH
	Switching frequency: f_s	10 kHz
Auxiliary battery charger	Input voltage: U_{high}	200 V
	Output voltage: U_{low}	36-48 V
	DC filter inductance: L	25 μH
	External series inductance: L_{ks}	24 μH
	Turns ratio: N	1
	Capacitor: C_i	50 μF
	Capacitor: C_c	200 μF
	Switching frequency: f_{s1}	100 kHz

voltage loop controllers. The dc electronic load ITECH8904E is employed to simulate batteries.

A. Driving Charging Mode

Fig. 14 shows the experimental results of the proposed topology operating in driving charging mode. The output voltage is 48 V and the power is 400 W while the dc electronic load is set to common resistance mode. The charging voltage/current and the voltage across the external series inductor are shown in Fig. 14(a). It can be seen that the charging current is 8.4 A and the HF current ripple is 0.08 A, i.e., its ripple rate is 0.95%, which shows a better effect on the HF current ripple suppression. Then, the current passing through the external series and dc filter inductors are shown in Fig. 14(b). The phase difference of the current passing through the two filter inductors is 180° and the amplitudes of its ac components are close. Thus, the HF output current ripple can be reduced. Moreover, the ZVS can be realized for all power switches, and the soft switching waveforms for Q_2 (primary side) and Q_6 (secondary side) are shown in Fig. 14(c).

Similarly, the proposed topology operating in driving charging mode at light load is tested. Fig. 15 shows the experimental result of the converter at 100 W (light load). The charging voltage/current and the voltage across the external series inductor are shown in Fig. 15(a). It can be seen that the charging current is 2.1 A and the HF current ripple is 0.03 A, i.e., its ripple rate is 1.43%, which also shows a better effect on suppressing the HF current ripple. Then, in order to compare with the results in Fig. 14(c), the soft switching waveforms for Q_2 and Q_6 are shown in Fig. 15(b).

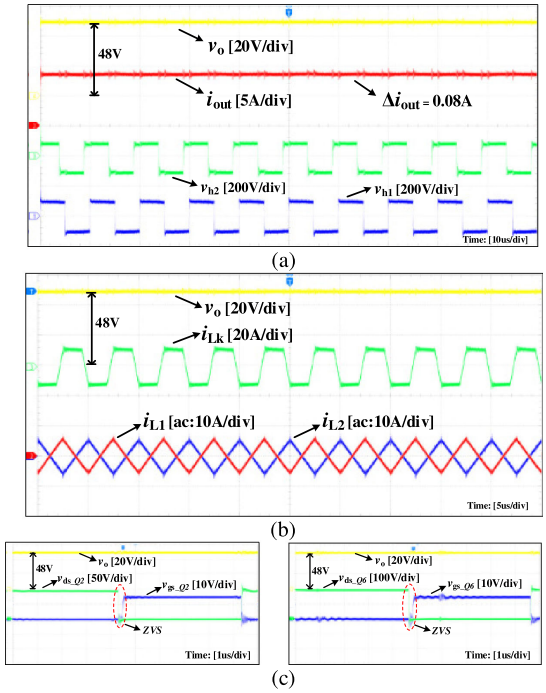

Fig. 14. Experimental results of the proposed topology in driving charging mode ($U_{low} = 48$ V, $P_o = 400$ W). (a) Output voltage and current. (b) Inductance currents. (c) ZVS for Q_2 and Q_6.

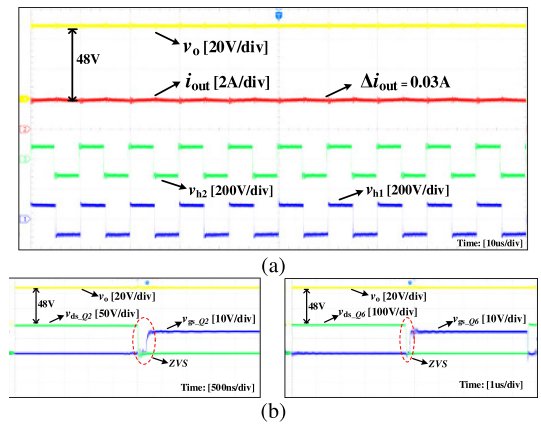

Fig. 15. Experimental results of the proposed topology in driving charging mode ($U_{low} = 48$ V, $P_o = 100$ W). (a) Output voltage and current. (b) ZVS for Q_2 and Q_6.

For the purpose of verifing the characteristic of the proposed topology with wide operation range, the experimental results with 36 V output voltage of the converter in driving charging mode under full-load and light-load conditions are given in Figs. 16 and 17, respectively.

First, the output power is 400 W. The charging voltage/current and the voltage across the external series inductor are shown in Fig. 16(a). As can be seen, the charging current is 11.2 A and the HF current ripple is 0.1 A, i.e., its ripple rate is 0.9%. Then, the current passing through the external series and dc filter inductors are shown in Fig. 16(b). As can be seen, the phase difference of the current passing through the two filter inductors is also 180° and the amplitude of its ac component is closely, too. Thus, the

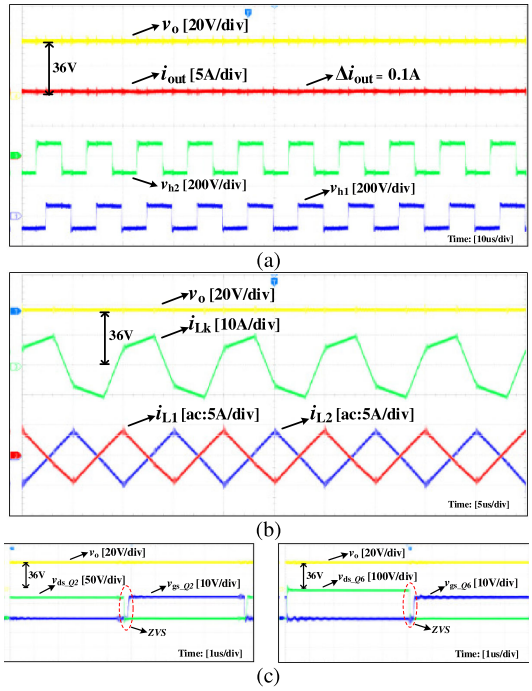

Fig. 16. Experimental results of the proposed topology in driving charging mode ($U_{\text{low}} = 36$ V, $P_o = 400$ W). (a) Output voltage and current. (b) Inductance currents. (c) ZVS for Q_2 and Q_6.

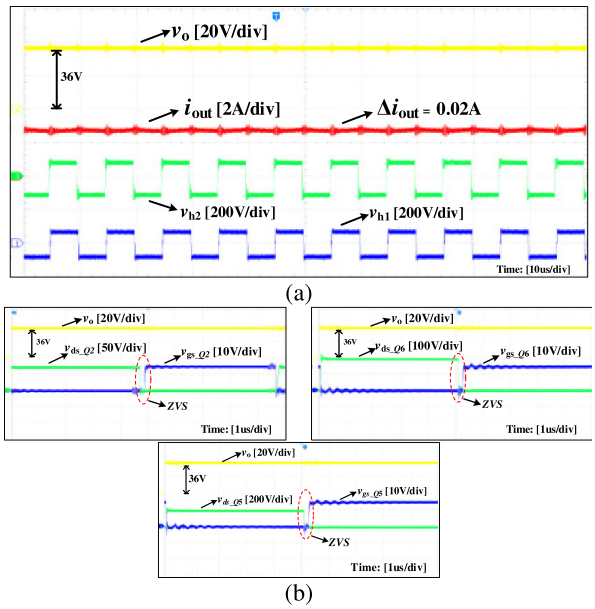

Fig. 17. Experimental results of the proposed topology in driving charging mode ($U_{\text{low}} = 36$ V, $P_o = 100$ W). (a) Output voltage and current. (b) ZVS for Q_2, Q_5, and Q_6.

HF output current ripple can be reduced. Meanwhile, the ZVS operation of Q_2 and Q_6 can be seen in Fig. 16(c).

Second, the experimental results with 100-W output power of the proposed topology operating in driving charging mode are shown in Fig. 17. Similarly, the charging voltage/current and the voltage across the external series inductor are shown in Fig. 17(a). The charging current is 2.79 A and the HF current ripple is 0.02 A, i.e., its ripple rate is 0.7% from Fig. 17(a). Also, the soft switching waveforms for Q_2, Q_5, and Q_6 can be observed in Fig. 17(b).

As a short summary, the experimental results verify the HF current ripple suppression in driving charging mode effectively and it agrees with theoretical analysis.

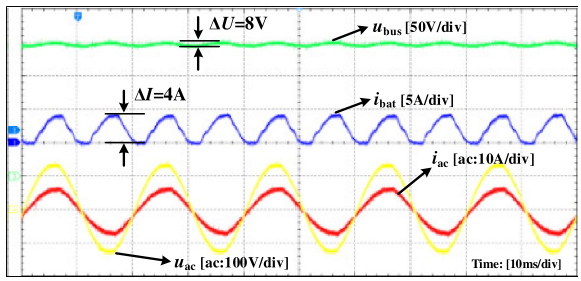

Fig. 18. Experimental results of the single-phase PWM rectifier without AF in parking charging mode.

B. Parking Charging Mode

In order to verify the effect of suppressing LF ripple voltage in parking charging mode (the dc electronic load is set to a constant voltage (CV) mode), the corresponding experimental results are given as below and the charging power is also 400 W.

For the sake of the comparison with the effect of the proposed capacitive energy storage AF, the experimental results from a 400-W single-phase PWM rectifier with the dc-link capacitance 200 μF are shown in Fig. 18 as a benchmark. The input ac current tracks in phase with the input voltage approximately. However, the peak-to-peak value of the second-harmonic ripple voltage on the dc bus is 8 V, i.e., its voltage ripple rate is 4%. The peak-to-peak value of the second-harmonic ripple current into the battery is 4 A, i.e., its current ripple rate is 200%. Also, the quality of the input ac current is shown in Fig. 20(a), in which the THD is 2.8%.

Fig. 19 shows the experimental results of the single-phase rectifier in parking charging mode with the AF operation. It can be seen from Fig. 19(a) that the second-harmonic ripple voltage can be reduced to 2 V, i.e., its voltage ripple rate is reduced from 4% to 1%, and the peak-to-peak value of the second-harmonic ripple current into the battery is 1.8 A, i.e., its current ripple rate is reduced from 200% to 90%, demonstrating the effects on the second-harmonic ripple voltage and current suppressions. Meanwhile, the quality of the input ac current is improved as shown in Fig. 20(b), in which the THD is 2.5%.

Fig. 19(b) shows the voltage and current waveforms of the capacitor and the inductor in the AF. As it can be seen, the frequency of the capacitor voltage is 100 Hz, i.e., twice of the grid voltage frequency. The capacitor is storing energy and its voltage is increasing when the inductor current is positive. The capacitor is releasing energy and the voltage is decreasing when the inductor current is negative. Therefore, the LF ripple voltage can be suppressed in the process of charging and discharging the capacitor.

In order to see the dc bus voltage clearly, the simulation results of the zoomed dc-link voltage oscillation are given in Fig. 21. It can be seen from Fig. 21 that the ripple voltage of the dc

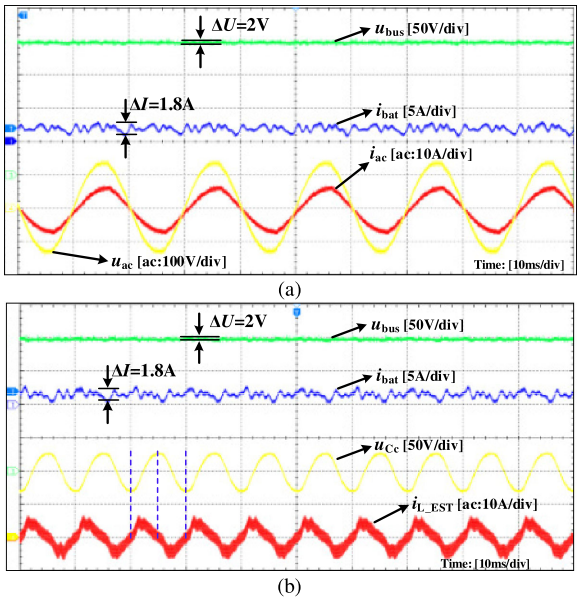

Fig. 19. Experimental results of a single-phase PWM rectifier with AF in parking charging mode. (a) Grid-side voltage, battery current, and dc bus voltage. (b) Capacitor voltage and inductance current, battery current, and dc bus voltage.

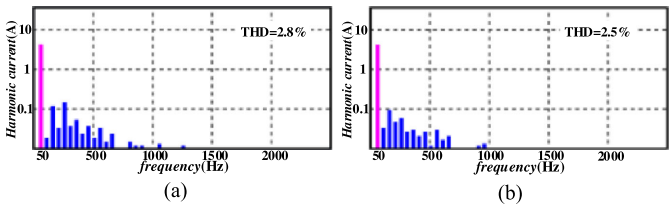

Fig. 20. Fourier analysis of the input current. (a) Without AF. (b) With AF.

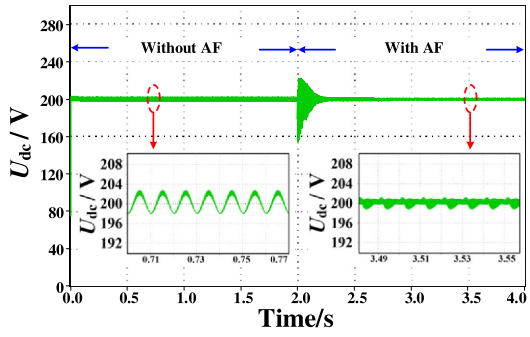

Fig. 21. Simulation results of the zoomed dc-link voltage oscillation.

bus without an AF is about 4 V, and it can be decreased to 1 V approximately with an AF.

In order to validate the dynamic performance of the proposed integrated charging system with the second-harmonic ripple current suppression, the simulation results of the load step change from 200 to 400 W are shown in Fig. 22. It can be seen that the dc bus voltage and charging current quickly reach steady state in less than 10 ms.

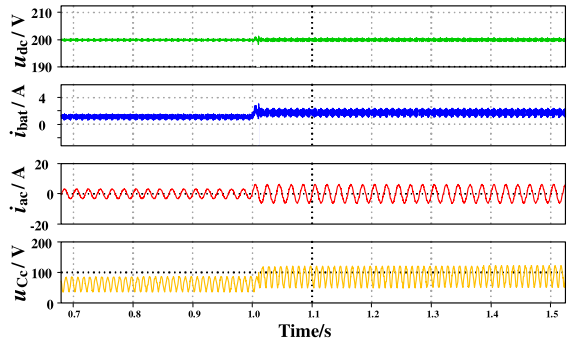

Fig. 22. Simulation results of load step change from 200 to 400 W.

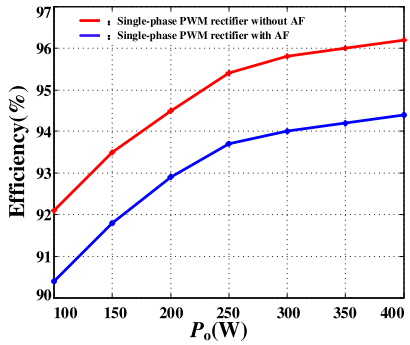

Fig. 23. Efficiency of the single-phase PWM rectifier with and without AF.

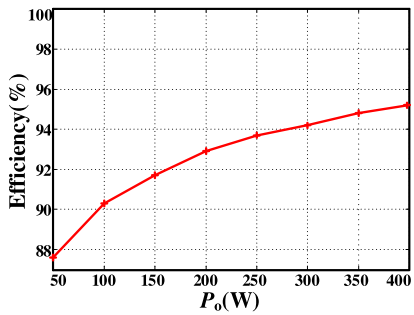

Fig. 24. Efficiency of the proposed topology operating in driving charging mode.

C. *Efficiency Analysis*

The efficiencies of the single-phasePWMPWM rectifier without and with the AF are shown in Fig. 23. The experimental efficiency is measured by the power analyzer YOKOGAWA/WT3000. From Fig. 23, the maximum and minimum efficiencies of the single-phase PWM rectifier without the AF are 96.2% (the output power is 400 W) and 92.1% (the output power is 100 W), respectively. The maximum and minimum efficiencies of the single-phase PWM rectifier with the AF are 94.4% (the output power is 400 W) and 90.4% (the output power is 100 W), respectively. It can be seen from the experimental results that the efficiency of the single-phase PWM rectifier with the AF has been reduced by about 1.8% on average compared to

that without the AF, due to the existence of the additional power losses of the power switches and passive devices.

Moreover, the efficiency of the proposed topology that operated in driving charging mode is shown in Fig. 24. The experimental efficiency is measured by the power analyzer YOKOGAWA/WT3000. From Fig. 24, the maximum and minimum efficiencies of the single-phase PWM rectifier without the AF are 95.20% (the output power is 400 W) and 87.60% (the output power is 50 W), respectively.

VI. Conclusion

In the context of single-phase onboard EV charging systems, this article proposes a multifunctional and isolated charger topology with time-sharing multiplexing. Without additional power switches and passive devices, it can suppress not only the HF current ripple in driving charging mode, but also the low-frequency voltage ripple in parking charging mode. Moreover, the ZVS can be achieved for all power switches under full-load range in driving charging mode. Therefore, the proposed topology is friendly to the auxiliary and power batteries in charging modes, so as to prolong their service lifetimes. In addition, the integration and power densities of the charging system can be improved while significant cost and space savings could be achieved in the charger circuit when this concept is applied to practical EV charging systems.

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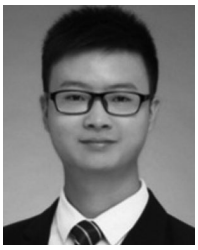

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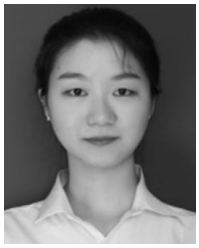

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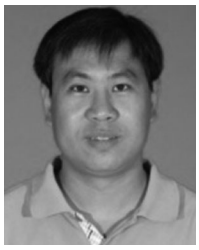

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